

## AUTOSWITCHING POWER MULTIPLEXER

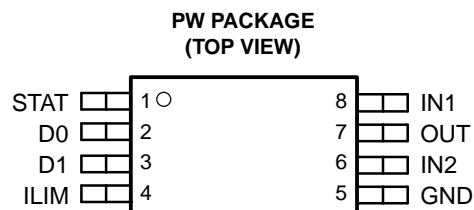
### FEATURES

- Two-Input, One-Output Power Multiplexer With Low  $r_{DS(on)}$  Switches:
  - 84 m $\Omega$  Typ (TPS2115)
  - 120 m $\Omega$  Typ (TPS2114)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range: 2.8 V to 5.5 V
- Low Standby Current: 0.5  $\mu$ A Typical
- Low Operating Current: 55  $\mu$ A Typical
- Adjustable Current Limit
- Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance
- CMOS and TTL Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown

- Available in a TSSOP-8 Package

### APPLICATIONS

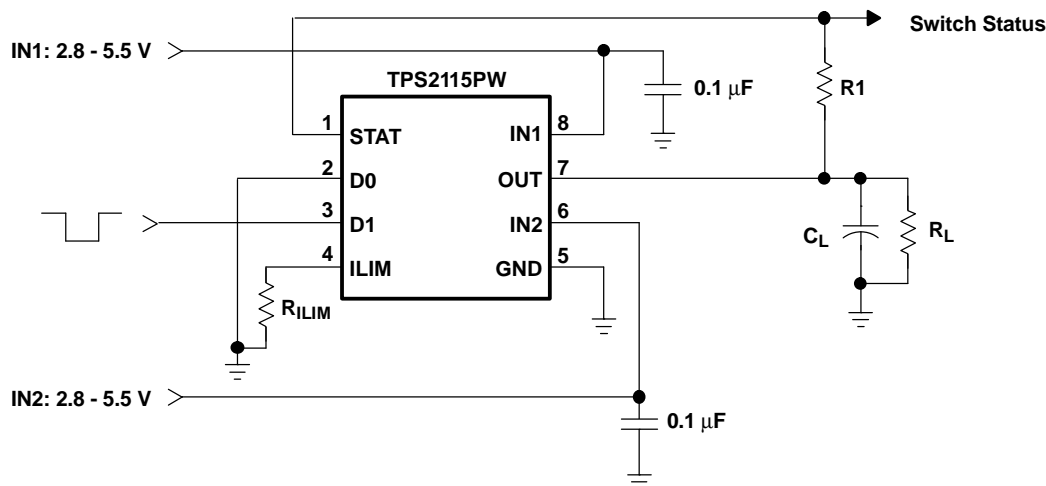
- PCs
- PDAs
- Digital Cameras
- Modems
- Cell phones
- Digital Radios
- MP3 Players



### DESCRIPTION

The TPS211x family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8-5.5 V and delivering up to 1 A. The TPS211x family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

### TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### AVAILABLE OPTIONS

FEATURE		TPS2110	TPS2111	TPS2112	TPS2113	TPS2114	TPS2115
Current limit adjustment range		0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A	0.31-0.75A	0.63-1.25A
Switching modes	Manual	Yes	Yes	No	No	Yes	Yes
	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch status output		No	No	Yes	Yes	Yes	Yes
Package		TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8	TSSOP-8

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	ORDERING NUMBER <sup>(1)</sup>	MARKINGS
-40°C to 85°C	TSSOP-8 (PW)	TPS2114PW	2114
		TPS2115PW	2115

(1) The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2114PWR) to indicate tape and reel.

### PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
TSSOP-8 (PW)	3.87 mW/°C	386.84 mW	212.76 mW	154.73 mW

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

			TPS2114, TPS2115
V <sub>I</sub>	Input voltage range	IN1, IN2, D0, D1, ILIM <sup>(2)</sup>	-0.3 V to 6 V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	OUT, STAT	-0.3 V to 6 V
I <sub>O</sub>	Output sink current	STAT	5 mA
I <sub>O</sub>	Continuous output current	TPS2114	0.9 A
		TPS2115	1.5 A
Continuous total power dissipation			See Dissipation Rating Table
T <sub>J</sub>	Operating virtual junction temperature range		-40°C to 125°C
T <sub>stg</sub>	Storage temperature range		-65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage at IN1	V <sub>I(IN2)</sub> ≥ 2.8 V	1.5	5.5	V
		V <sub>I(IN2)</sub> < 2.8 V	2.8	5.5	
V <sub>I</sub>	Input voltage at IN2	V <sub>I(IN1)</sub> ≥ 2.8 V	1.5	5.5	V
		V <sub>I(IN1)</sub> < 2.8 V	2.8	5.5	
V <sub>I</sub>	Input voltage at D0, D1	0	5.5	V	
I <sub>O(OUT)</sub>	Current limit adjustment range	TPS2114	0.31	0.75	A
		TPS2115	0.63	1.25	
T <sub>J</sub>	Operating virtual junction temperature	-40	125	°C	

## ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2	kV
CDM		500	V

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, V<sub>I(IN1)</sub> = V<sub>I(IN2)</sub> = 5.5 V, R<sub>(LIM)</sub> = 400 Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPS2114			TPS2115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>POWER SWITCH</b>								
r <sub>DS(on)</sub> <sup>(1)</sup> Drain-source on-state resistance (INx-OUT)	T <sub>J</sub> = 25°C, I <sub>L</sub> = 500 mA	V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 5.0 V	120	140	84	110	mΩ	
		V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 3.3 V	120	140	84	110		
		V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 2.8 V	120	140	84	110		
	T <sub>J</sub> = 125°C, I <sub>L</sub> = 500 mA	V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 5.0 V		220		150	mΩ	
		V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 3.3 V		220		150		
		V <sub>I(IN1)</sub> = V <sub>I(IN2)</sub> = 2.8 V		220		150		

(1) The TPS211x can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS2115			UNIT	
			MIN	TYP	MAX		
<b>LOGIC INPUTS (D0 AND D1)</b>							
$V_{IH}$	High-level input voltage		2			V	
$V_{IL}$	Low-level input voltage				0.7	V	
Input current at D0 or D1		D0 or D1 = High, sink current			1	$\mu$ A	
		D0 or D1 = Low, source current	0.5	1.4	5		
<b>SUPPLY AND LEAKAGE CURRENTS</b>							
Supply current from IN1 (operating)		D1 = High, D0 = Low (IN1 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		55	90	$\mu$ A	
		D1 = High, D0 = Low (IN1 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		1	12		
		D0 = D1 = Low (IN2 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			75		
		D0 = D1 = Low (IN2 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			1		
Supply current from IN2 (operating)		D1 = High, D0 = Low (IN1 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			1	$\mu$ A	
		D1 = High, D0 = Low (IN1 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			75		
		D0 = D1 = Low (IN2 active), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		1	12		
		D0 = D1 = Low (IN2 active), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		55	90		
Quiescent current from IN1 (STANDBY)		D0 = D1 = High (inactive), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A		0.5	2	$\mu$ A	
		D0 = D1 = High (inactive), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A			1		
Quiescent current from IN2 (STANDBY)		D0 = D1 = High (inactive), $V_{I(IN1)} = 5.5$ V, $V_{I(IN2)} = 3.3$ V, $I_{O(OUT)} = 0$ A			1	$\mu$ A	
		D0 = D1 = High (inactive), $V_{I(IN1)} = 3.3$ V, $V_{I(IN2)} = 5.5$ V, $I_{O(OUT)} = 0$ A		0.5	2		
Forward leakage current from IN1 (measured from OUT to GND)		D0 = D1 = High (inactive), $V_{I(IN1)} = 5.5$ V, IN2 open, $V_{O(OUT)} = 0$ V (shorted), $T_J = 25^\circ\text{C}$		0.1	5	$\mu$ A	
Forward leakage current from IN2 (measured from OUT to GND)		D0 = D1 = High (inactive), $V_{I(IN2)} = 5.5$ V, IN1 open, $V_{O(OUT)} = 0$ V (shorted), $T_J = 25^\circ\text{C}$		0.1	5	$\mu$ A	
Reverse leakage current to INx (measured from INx to GND)		D0 = D1 = High (inactive), $V_{I(INx)} = 0$ V, $V_{O(OUT)} = 5.5$ V, $T_J = 25^\circ\text{C}$		0.3	5	$\mu$ A	
<b>CURRENT LIMIT CIRCUIT</b>							
Current limit accuracy		TPS2114	$R_{(ILIM)} = 400 \Omega$	0.51	0.63	0.80	A
			$R_{(ILIM)} = 700 \Omega$	0.30	0.36	0.50	
		TPS2115	$R_{(ILIM)} = 400 \Omega$	0.95	1.25	1.56	
			$R_{(ILIM)} = 700 \Omega$	0.47	0.71	0.99	
$t_d$	Current limit settling time <sup>(1)</sup>	Time for short-circuit output current to settle within 10% of its steady state value.		1		ms	
Input current at ILIM		$V_{I(ILIM)} = 0$ V, $I_{O(OUT)} = 0$ A		-15	0	$\mu$ A	

(1) Not tested in production.

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPS2115			UNIT
		MIN	TYP	MAX	
<b>UNDERVOLTAGE LOCKOUT</b>					
IN1 and IN2 UVLO	Falling edge	1.15	1.25		V
	Rising edge		1.30	1.35	
IN1 and IN2 UVLO hysteresis <sup>(2)</sup>		30	57	65	mV
Internal V <sub>DD</sub> UVLO (the higher of IN1 and IN2)	Falling edge	24	2.53		V
	Rising edge		2.58	2.8	
Internal V <sub>DD</sub> UVLO hysteresis <sup>(2)</sup>		30	50	75	mV
UVLO deglitch for IN1, IN2 <sup>(2)</sup>	Falling edge		110		μs
<b>REVERSE CONDUCTION BLOCKING</b>					
ΔV <sub>O(I_block)</sub> Minimum output-to-input voltage difference to block switching	D0 = D1 = high, V <sub>I(INx)</sub> = 3.3 V. Connect OUT to a 5 V supply through a series 1-kΩ resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV
<b>THERMAL SHUTDOWN</b>					
Thermal shutdown threshold <sup>(2)</sup>	TPS211x is in current limit.	135			°C
Recovery from thermal shutdown <sup>(2)</sup>	TPS211x is in current limit.	125			
Hysteresis <sup>(2)</sup>			10		
<b>IN2-IN1 COMPARATORS</b>					
Hysteresis of IN2-IN1 comparator		0.1		0.2	V
Deglitch of IN2-IN1 comparator, (both↑↓) <sup>(2)</sup>		90	150	220	μs
<b>STAT OUTPUT</b>					
Leakage current	V <sub>O(STAT)</sub> = 5.5 V	0.01	1		μA
Saturation voltage	I <sub>I(STAT)</sub> = 2 mA, IN1 switch is on	0.13	0.4		V
Deglitch time (falling edge only)			150		μs

(2) Not tested in production.

### SWITCHING CHARACTERISTICS

over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$ ,  $R_{(LIM)} = 400\ \Omega$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPS2114			TPS2115			UNIT					
		MIN	TYP	MAX	MIN	TYP	MAX						
<b>POWER SWITCH</b>													
$t_r$	Output rise time from an enable <sup>(1)</sup>	$V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$	$T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(a)			0.5	1.0	1.5	1	1.8	3	ms	
$t_f$	Output fall time from a disable <sup>(1)</sup>	$V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$	$T_J = 25^\circ\text{C}$ , $C_L = 1\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(a)			0.35	0.5	0.7	0.5	1	2	ms	
$t_t$	Transition time <sup>(1)</sup>	IN1 to IN2 transition, $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$	$T_J = 125^\circ\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ [Measure transition time as 10-90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$ ], See Figure 1(b)			40	60		40	60		$\mu\text{s}$	
		IN2 to IN1 transition, $V_{I(IN1)} = 5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$				40	60		40	60			
$t_{PLH1}$	Turnon propagation delay from enable <sup>(1)</sup>	$V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , Measured from enable to 10% of $V_{O(OUT)}$	$T_J = 25^\circ\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(a)			0.5			1			ms	
$t_{PHL1}$	Turnoff propagation delay from a disable <sup>(1)</sup>	$V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , Measured from disable to 90% of $V_{O(OUT)}$	$T_J = 25^\circ\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(a)			3			5			ms	
$t_{PLH2}$	Switch-over rising propagation delay <sup>(1)</sup>	Logic 1 to Logic 0 transition on D1, $V_{I(IN1)} = 1.5\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$ , $V_{I(D0)} = 0\text{ V}$ , Measured from D1 to 10% of $V_{O(OUT)}$	$T_J = 25^\circ\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(c)			0.17			1			ms	
$t_{PHL2}$	Switch-over falling propagation delay <sup>(1)</sup>	Logic 0 to Logic 1 transition on D1, $V_{I(IN1)} = 1.5\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$ , $V_{I(D0)} = 0\text{ V}$ , Measured from D1 to 90% of $V_{O(OUT)}$	$T_J = 25^\circ\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ , See Figure 1(c)			2			3			10	ms

(1) Not tested in production.

### TRUTH TABLE

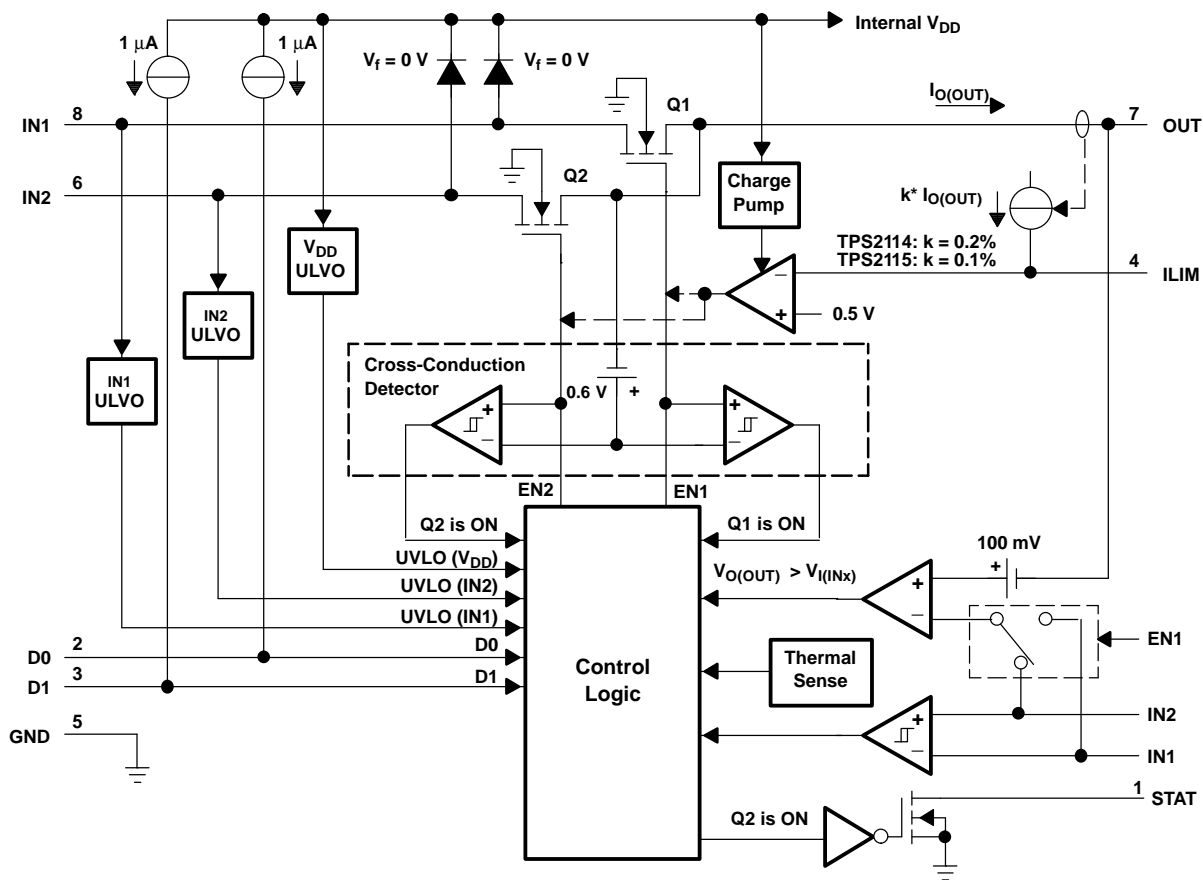
D1	D0	$V_{I(IN2)} > V_{I(IN1)}$	STAT	OUT <sup>(1)</sup>
0	0	X	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

(1) The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal  $V_{DD}$  UVLO.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
D0	2	I	TTL and CMOS compatible input pins. Each pin has a 1- $\mu$ A pullup resistor. The truth table shown above illustrates the functionality of D0 and D1.
D1	3	I	
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal $V_{DD}$ UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal $V_{DD}$ UVLO.
ILIM	4	I	A resistor $R_{(ILIM)}$ from ILIM to GND sets the current limit $I_L$ to $250/R_{(ILIM)}$ and $500/R_{(ILIM)}$ for the TPS2114 and TPS2115, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., EN is equal to logic 0).

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

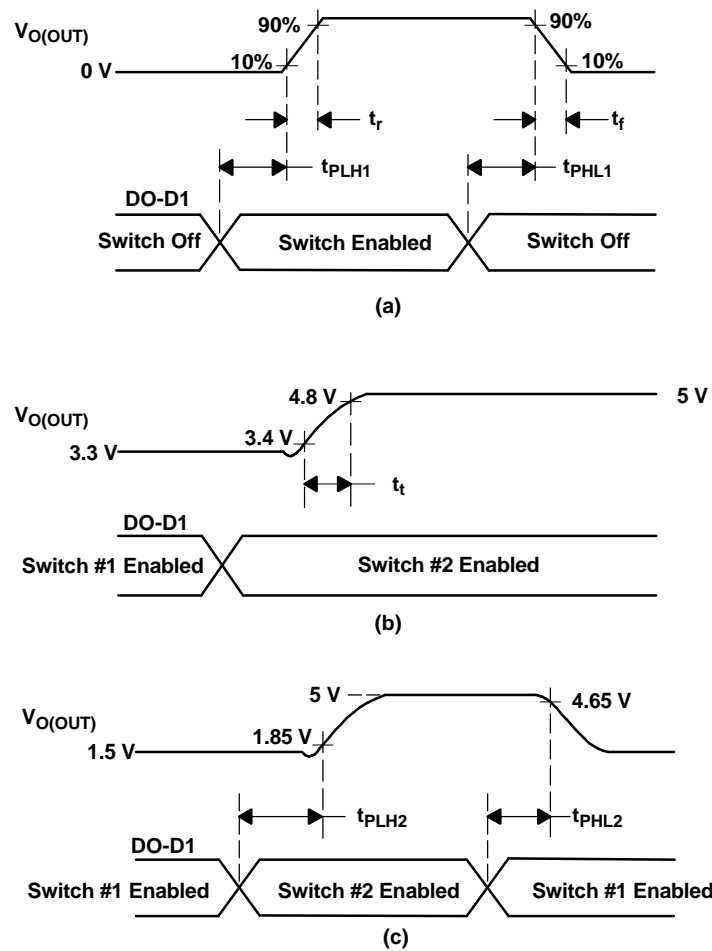
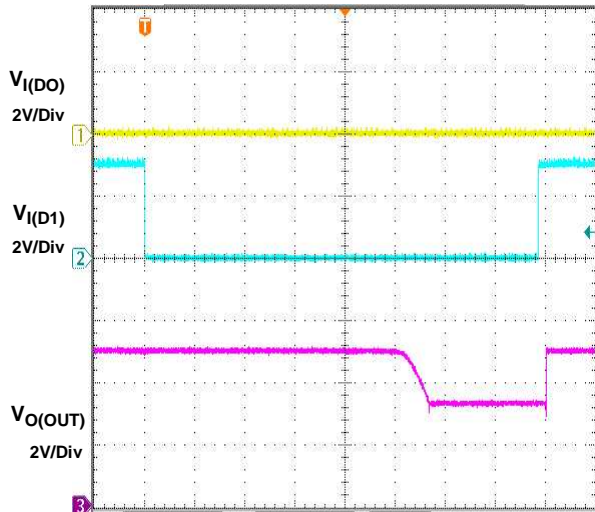


Figure 1. Propagation Delays and Transition Timing Waveforms

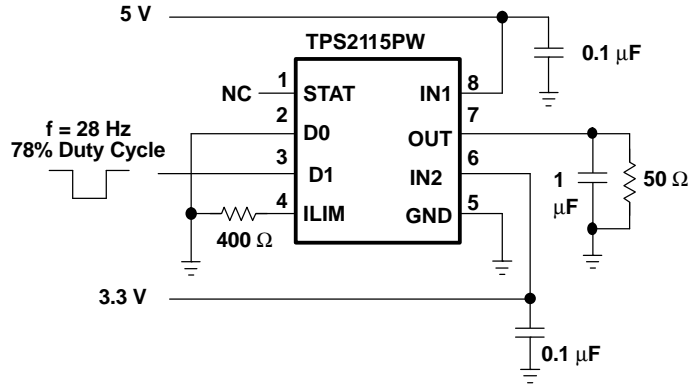


**TYPICAL CHARACTERISTICS**

**OUTPUT SWITCHOVER RESPONSE**



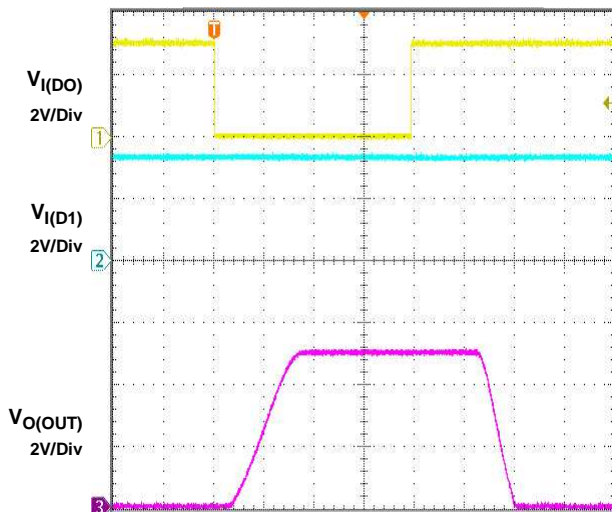
t - Time - 1 ms/div



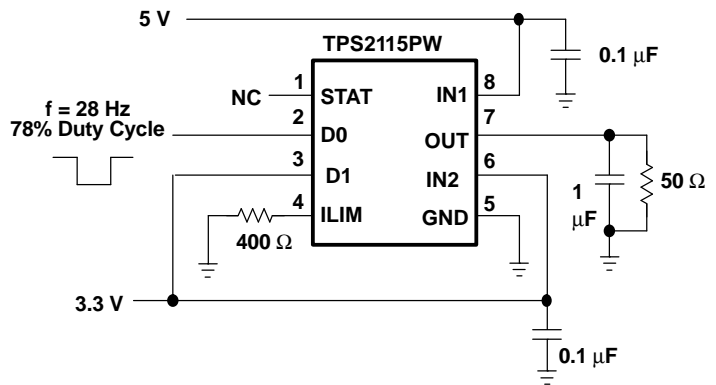
**Output Switchover Response Test Circuit**

Figure 2.

**OUTPUT TURNON RESPONSE**



t - Time - 2 ms/div

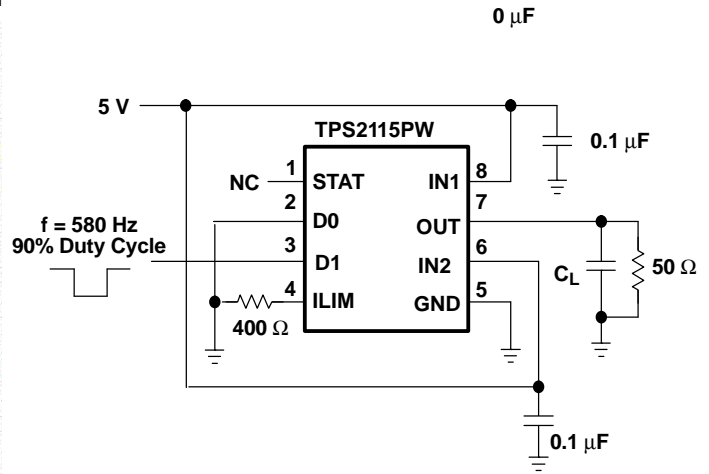
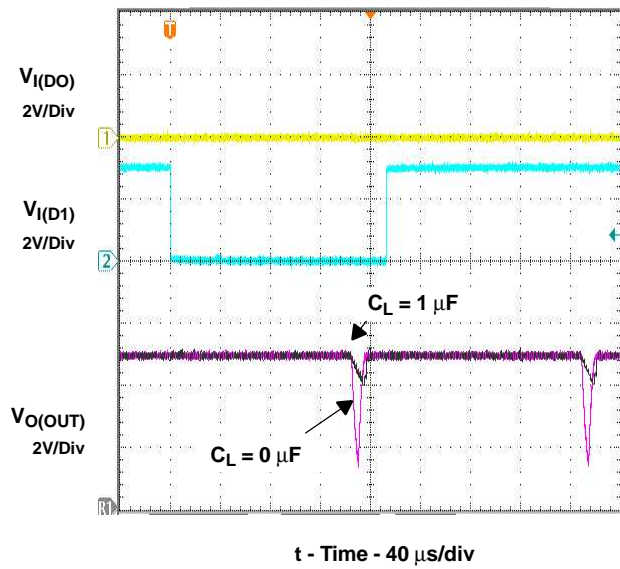


**Output Turnon Response Test Circuit**

Figure 3.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP

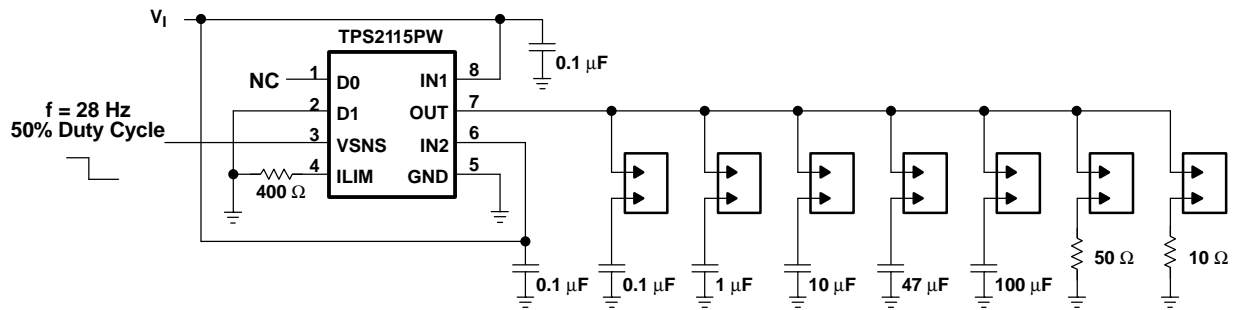
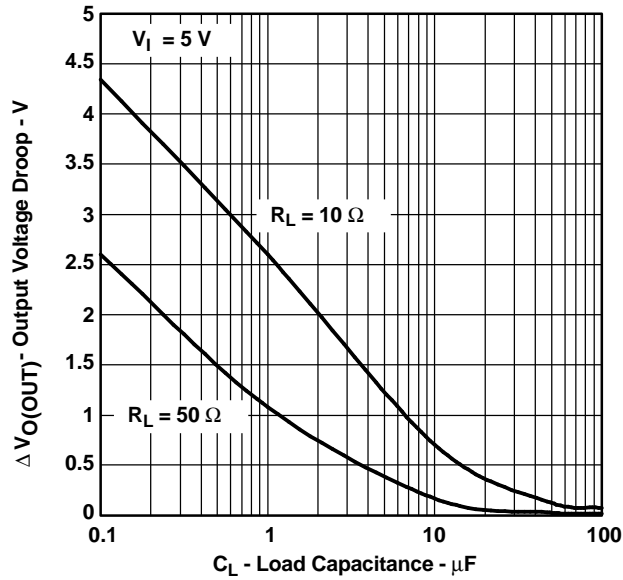


Output Switchover Voltage Droop Test Circuit

Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP  
VS  
LOAD CAPACITANCE

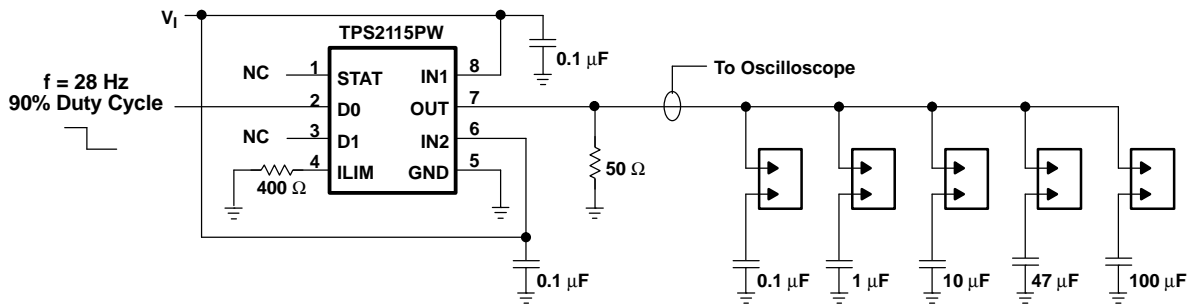
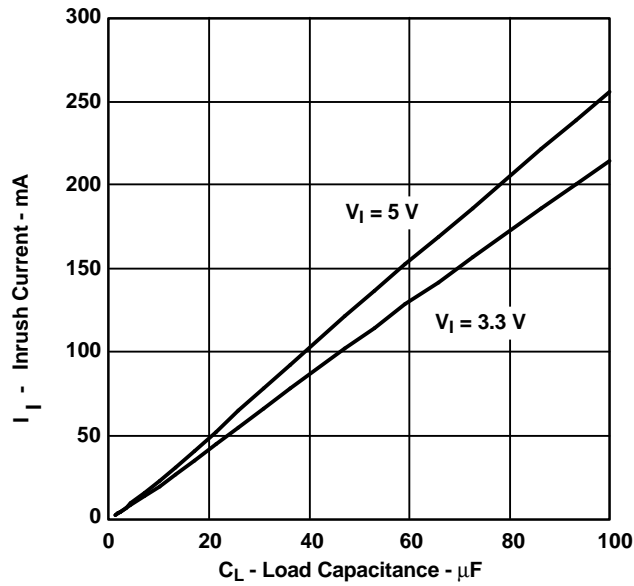


Output Swiclover Voltage Droop Test Circuit

Figure 5.

TYPICAL CHARACTERISTICS (continued)

INRUSH CURRENT  
VS  
LOAD CAPACITANCE



Output Capacitor Inrush Current Test Circuit

Figure 6.

TYPICAL CHARACTERISTICS (continued)

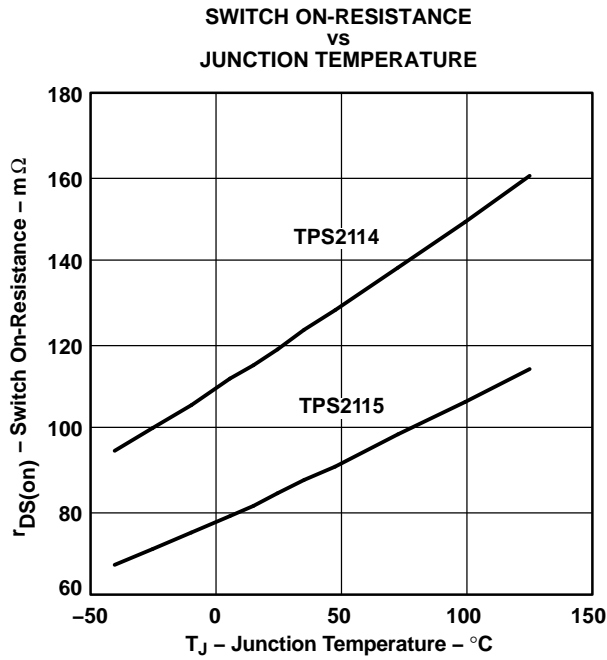


Figure 7.

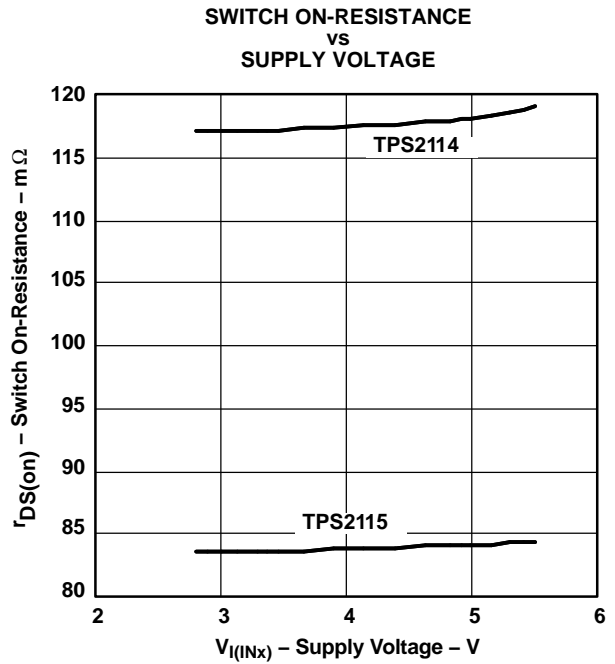


Figure 8.

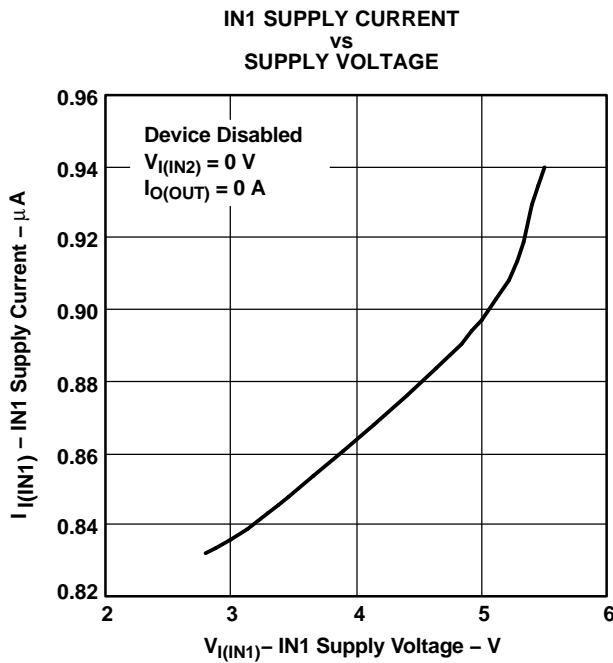


Figure 9.

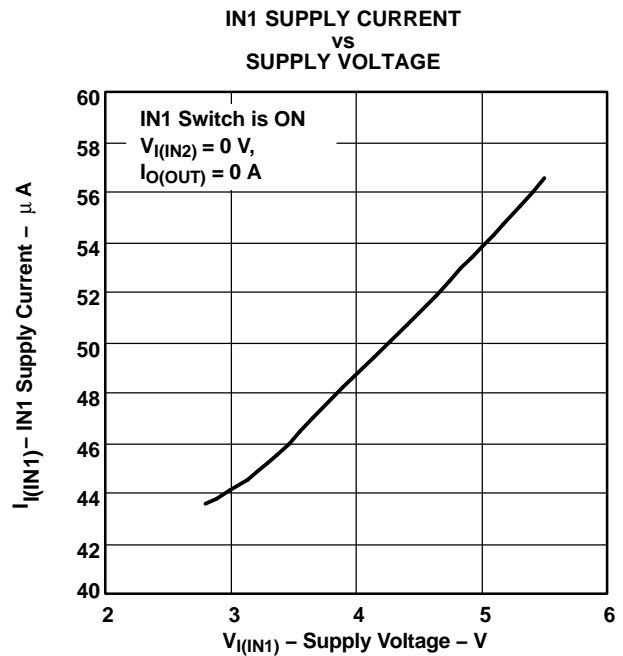


Figure 10.

TYPICAL CHARACTERISTICS (continued)

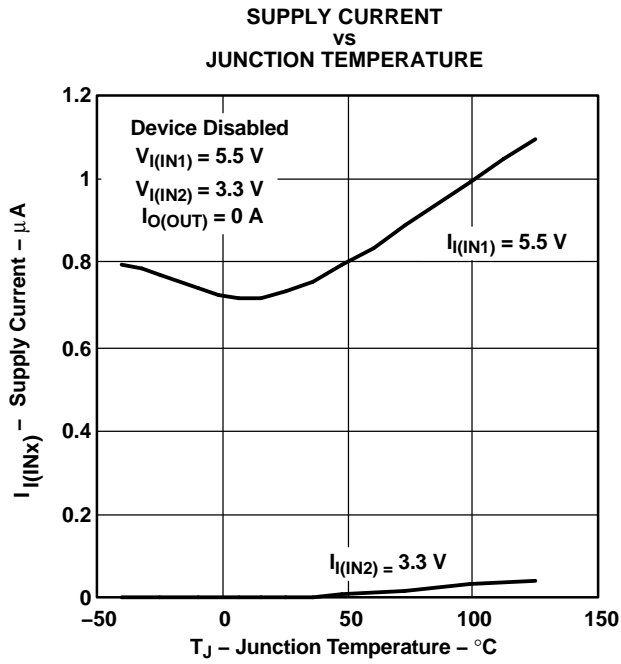


Figure 11.

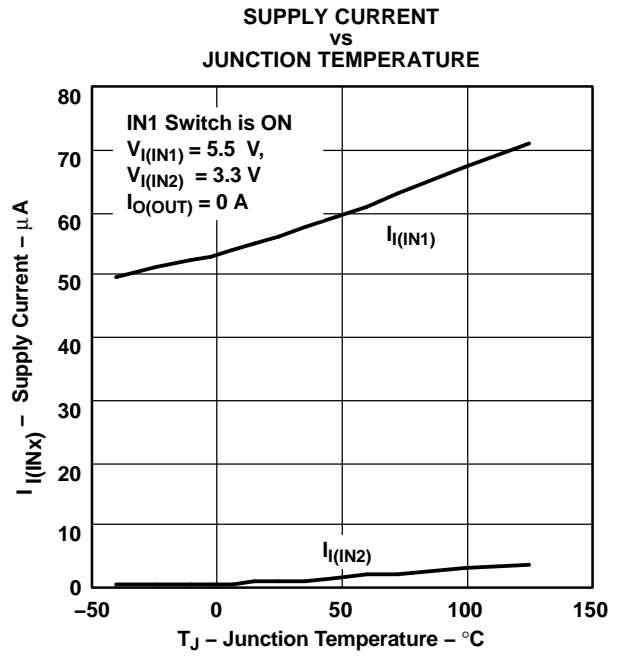
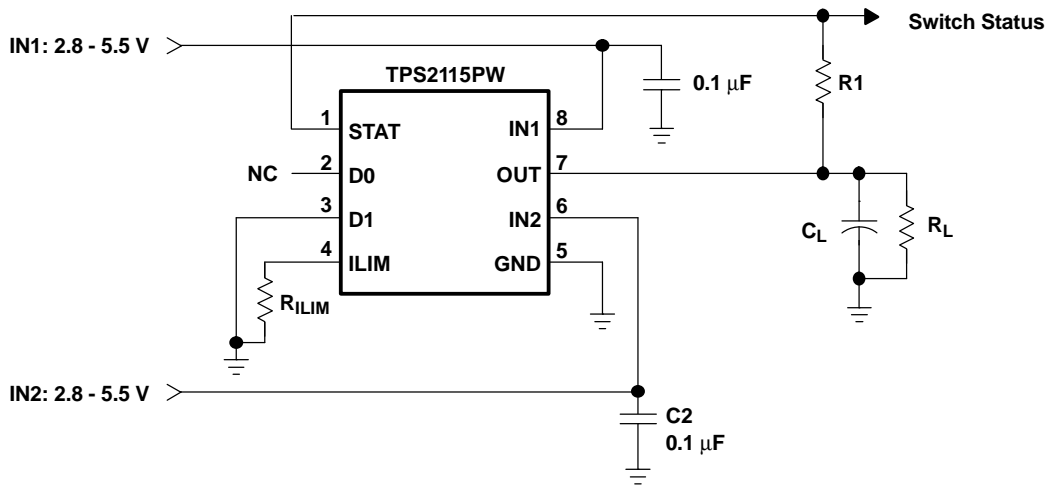


Figure 12.

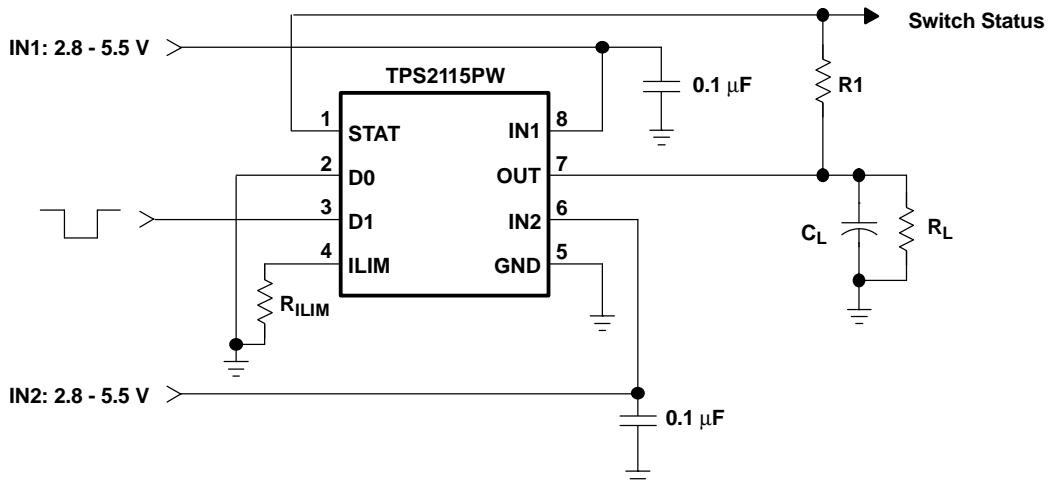
## APPLICATION INFORMATION

The circuit in Figure 13 allows one or two battery packs to power a system. Two battery packs allow a longer run time. The TPS2114/5 cycles between the battery packs until both packs are drained.



**Figure 13. Running a System From Two Battery Packs**

In Figure 14, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1, otherwise OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.



**Figure 14. Manually Switching Power Sources**

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## DETAILED DESCRIPTION

### AUTO-SWITCHING MODE

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

### MANUAL SWITCHING MODE

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

### N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turnon of a FET switch if the output voltage is greater than the input voltage.

### CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turnon threshold voltage.

### REVERSE-CONDUCTION BLOCKING

When the TPS211x switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211x does not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it remains connected regardless of output voltage.

### CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

### CURRENT LIMITING

A resistor  $R_{(ILIM)}$  from ILIM to GND sets the current limit to  $250/R_{(ILIM)}$  and  $500/R_{(ILIM)}$  for the TPS2114 and TPS2115, respectively. Setting resistor  $R_{(ILIM)}$  equal to zero is not recommended as that disables current limiting.

### OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2114/5 slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can adversely effect the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot plugging a load like a PCI card. The TPS2114/5 slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2114PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2114	<a href="#">Samples</a>
TPS2115PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2115	<a href="#">Samples</a>
TPS2115PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2115	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

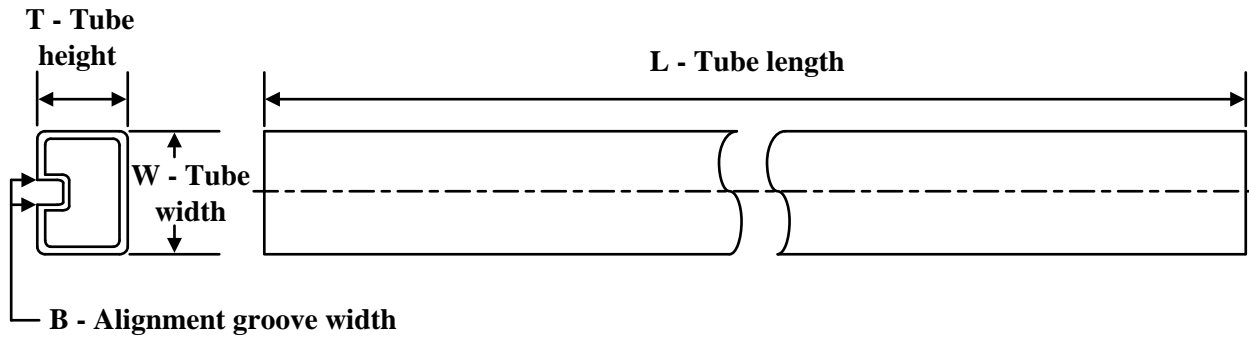

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2115PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2115PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS2114PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2115PW	PW	TSSOP	8	150	530	10.2	3600	3.5

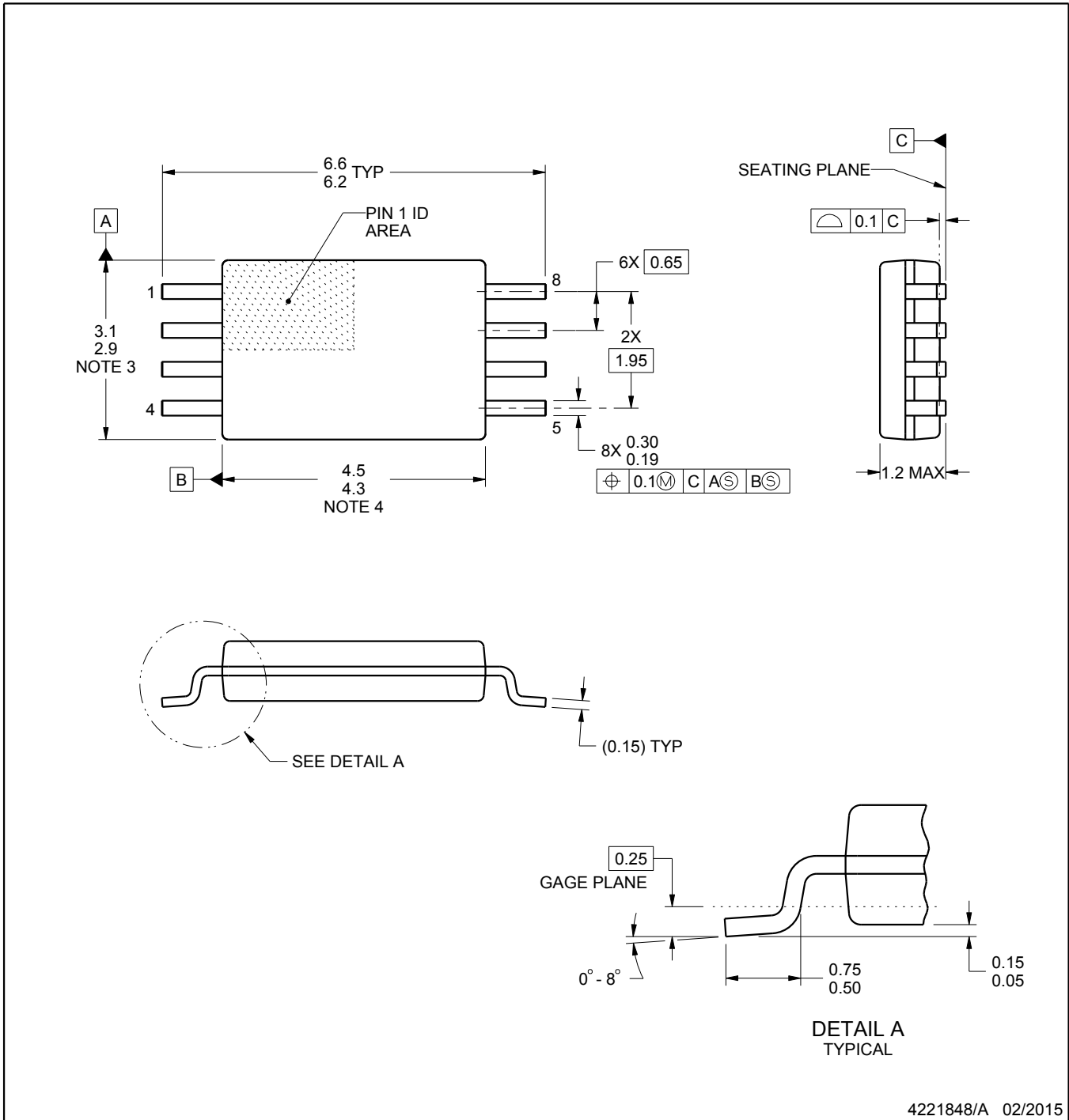
PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

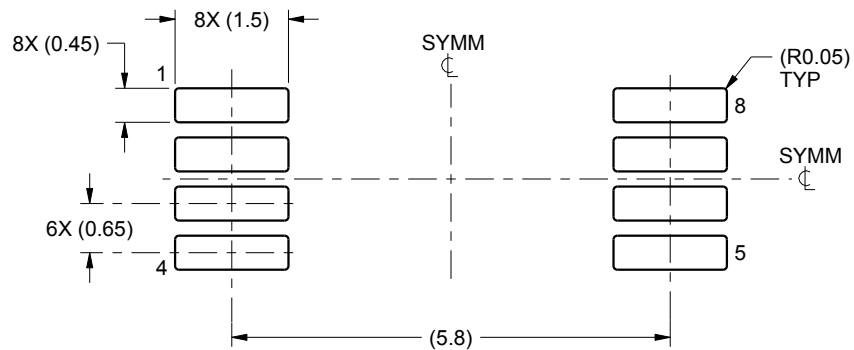
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

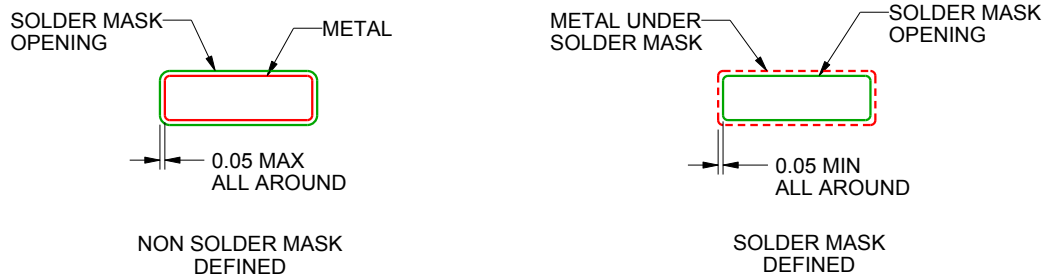
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

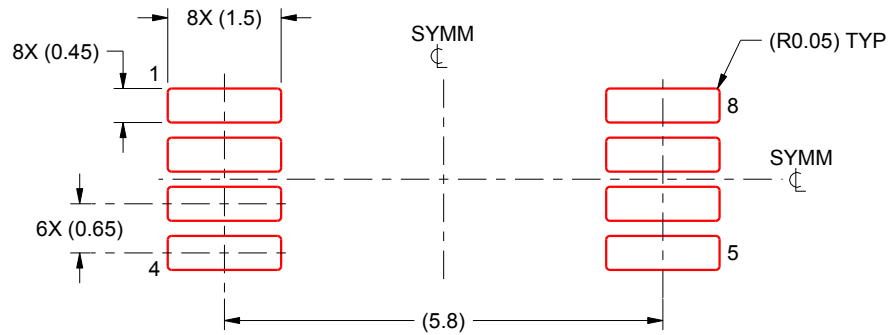
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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