ANALOG DEVICES

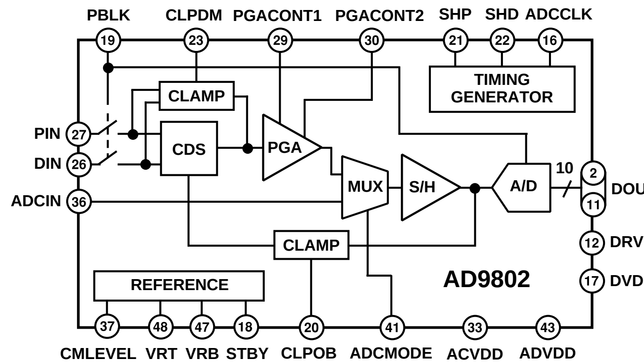
CCD Signal Processor For Electronic Cameras

AD9802

FEATURES

10-Bit, 18 MSPS A/D Converter
18 MSPS Full Speed Correlated Double Sampler (CDS)
Low Noise, Wideband PGA
Internal Voltage Reference
No Missing Codes Guaranteed
+3 V Single Supply Operation
Low Power CMOS: 185 mW
48-Terminal TQFP Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9802 is a complete CCD signal processor developed for electronic cameras. It is suitable for both camcorder and consumer-level still camera applications.

The signal processing chain is comprised of a high speed CDS, variable gain PGA and 10-bit ADC. Required clamping circuitry and an onboard voltage reference are provided as well as a direct ADC input. The AD9802 operates from a single +3 V supply with a typical power consumption of 185 mW.

The AD9802 is packaged in a space saving 48-terminal thin quad flatpack (TQFP) and is specified over an operating temperature range of 0°C to +70°C.

PRODUCT HIGHLIGHTS

1. On-Chip Input Clamp and CDS
   Clamp circuitry and high speed correlated double sampler allow for simple ac-coupling to interface a CCD sensor at full 18 MSPS conversion rate.
2. On-Chip PGA
   The AD9802 includes a low-noise, wideband amplifier with analog variable gain from 0 dB to 31.5 dB (linear in dB).
3. Direct ADC Input
   A direct input to the 10-bit A/D converter is provided for digitizing video signals.
4. 10-Bit, High Speed A/D Converter
   A linear 10-bit ADC is capable of digitizing CCD signals at the full 18 MSPS conversion rate. Typical DNL is ±0.5 LSB and no missing code performance is guaranteed.
5. Low Power
   At 185 mW, and 15 mW in power-down, the AD9802 consumes a fraction of the power of presently available multichip solutions.
6. Digital I/O Functionality
   The AD9802 offers three-state digital output control.
7. Small Package
   Packaged in a 48-terminal, surface-mount thin quad flatpack, the AD9802 is well suited to very compact, low headroom designs.

REV. 0

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AD9802–SPECIFICATIONS
(T_{MIN} to T_{MAX} with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
TEMPERATURE RANGE				
Operating	0		70	°C
Storage	–65		150	°C
POWER SUPPLY VOLTAGE (For Functional Operation)				
ACVDD	3.00	3.15	3.50	V
ADVDD	3.00	3.15	3.50	V
DVDD	3.00	3.15	3.50	V
DRVDD	3.00	3.15	3.50	V
POWER SUPPLY CURRENT				
ACVDD		39.5		mA
ADVDD		14.6		mA
DVDD		4.7		mA
DRVDD		0.07		mA
POWER CONSUMPTION				
Normal Operation		185		mW
Power-Down Mode		15		mW
MAXIMUM SHP, SHD, ADCCLK RATE	18			MHz
ADC				
Resolution	10			Bits
Differential Nonlinearity		±0.5		LSBs
No Missing Codes		GUARANTEED		
ADCCLK Rate			18	MHz
Reference Top Voltage		1.75		V
Reference Bottom Voltage		1.25		V
Input Range		1.0		V p-p
CDS				
Maximum Input Signal	500			mV p-p
Pixel Rate			18	MHz
PGA[1]				
Maximum Gain		31.5		dB
High Gain	14.5	19	23.5	dB
Medium Gain	1.0	4.0	7.0	dB
Minimum Gain	–4.0	0	+4	dB
CLAMP (During CLPOB. Only Stable over PGA Range 0.3 V to 2.7 V)				
Average Black Level		32		LSBs
Pixel-to-Pixel Offset (See Black Level Clamping for Description)		2	8	LSBs

NOTES

[1]PGA test conditions: maximum gain PGACONT1 = 2.7 V, PGACONT2 = 1.5 V; high gain PGACONT1 = 2.0 V, PGACONT2 = 1.5 V; medium gain PGACONT1 = 0.5 V, PGACONT2 = 1.5 V; minimum gain PGACONT1 = 0.3 V, PGACONT2 = 1.5 V.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS
(T_{MIN} to T_{MAX} with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.4			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	2.4			V
Low Level Output Voltage	V_{OL}			0.6	V
	I_{OH}		50		µA
	I_{OL}		50		µA

TIMING SPECIFICATIONS

(T_{MIN} to T_{MAX} with ACVDD = 3.15 V, ADVDD = 3.15 V, DVDD = 3.15 V, DRVDD = 3.15 V unless otherwise noted)

Parameter	Min	Typ	Max	Units
ADCCLK Clock Period	55.6			ns
ADCCLK Hi-Level Period	24.8	27.8		ns
ADCCLK Lo-Level Period	24.8	27.8		ns
SHP, SHD Clock Period	55.6			ns
SHP, SHD Minimum Pulse Width	12.5			ns
SHP Rising Edge to SHD Rising Edge	28			ns
Digital Output Delay		20		ns

Digital Output Data Control

PBLK	MODE1	MODE2	Digital Output Data (D9–D0)
0	0	0	0 0 0 0 0 0 0 0 0 0
1	0	0	Normal Operation
1	0	1	1 0 1 0 1 0 1 0 1 0
1	1	0	0 1 0 1 0 1 0 1 0 1
1	1	1	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Units
ADVDD	ADVSS, SUBST	–0.3	6.5	V
ACVDD	ACVSS, SUBST	–0.3	6.5	V
DVDD	DVSS, DSUBT	–0.3	6.5	V
DRVDD	DRVSS, DSUBST	–0.3	6.5	V
SHP, SHD	DSUBST	–0.3	DVDD + 2.0	V
ADCCLK, CLPOB, CLPDM	DSUBST	–0.3	DVDD + 0.3	V
PGACONT1, PGACONT2	SUBST	–0.3	ACVDD + 0.3	V
PIN, DIN	SUBST	–0.3	ACVDD + 0.3	V
DOUT	DSUBST	–0.3	DRVDD + 0.3	V
VRT, VRB	SUBST	–0.3	ADVDD + 0.3	V
CLAMP_BIAS	SUBST	–0.3	ACVDD + 0.3	V
CCDBYP1, CCDBYP2	SUBST	–0.3	ACVDD + 0.3	V
STBY	DSUBST	–0.3	DVDD + 0.3	V
MODE1, MODE2	SUBST	–0.3	ADVDD + 0.3	V
DRVSS, DVSS, ACVSS, ADVSS	SUBST, DSUBST	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

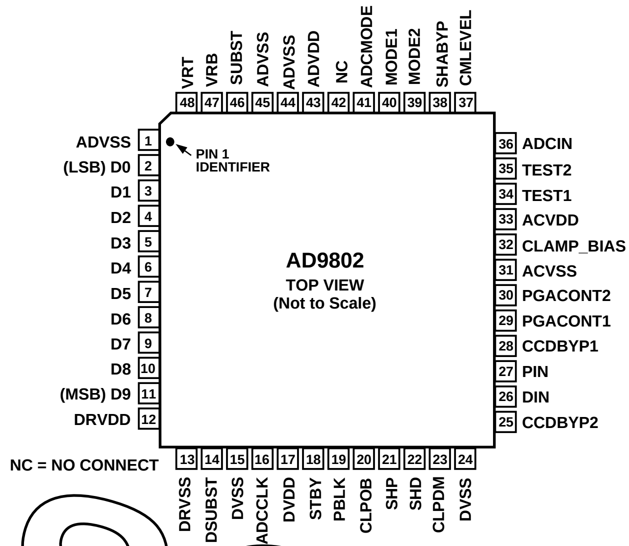
Model	Temperature Range	Package Description	Package Option
AD9802JST	0°C to +70°C	48-Terminal Plastic Thin Quad Flatpack	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9802 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Type	Description
1	ADVSS	P	Analog Ground
2–11	D0–D9	DO	Digital Data Outputs: D0 = LSB, D9 = MSB
12	DRVDD	P	+3 V Digital Driver Supply
13	DRVSS	P	Digital Driver Ground
14	DSUBST	P	Digital Substrate
15	DVSS	P	Digital Ground
16	ADCCLK	DI	ADC Sample Clock Input
17	DVDD	P	+3 V Digital Supply
18	STBY	DI	Power-Down (Active High)
19	PBLK	DI	Pixel Blanking (Active Low)
20	CLPOB	DI	Black Level Restore Clamp (Active Low)
21	SHP	DI	Reference Sample Clock Input
22	SHD	DI	Data Sample Clock Input
23	CLPDM	DI	Input Clamp (Active Low)
24	DVSS	P	Digital Ground
25	CCDBYP2	AO	CCD Bypass. Decouple to analog ground through 0.1 µF.
26	DIN	AI	CDS Input. Tie to Pin 27 and AC-Couple to CCD output through 0.1 µF.
27	PIN	AI	CDS Input. See above.
28	CCDBYP1	AO	CCD Bypass. Decouple to analog ground through 0.1 µF.
29	PGACONT1	AI	Coarse PGA Gain Control (0.3 V–2.7 V). Decoupled to analog ground through 0.1 µF.
30	PGACONT2	AI	Fine PGA Gain Control
31	ACVSS	P	Analog Ground
32	CLAMP_BIAS	AO	Clamp Bias Level. Decouple to analog ground through 0.1 µF.
33	ACVDD	P	+3 V Analog Supply
34, 35	TEST1, TEST2	AI	Reserved Test Pins. Should be left NC or pulled high to ACVDD.
36	ADCIN	AI	Direct ADC Analog Input (See Driving the Direct ADC Input)
37	CMLEVEL	AO	Common-Mode Level. Decouple to analog ground through 0.1 µF.
38	SHABYP	AO	Internal Bias Level. Decouple to analog ground through 0.1 µF.
39	MODE2	DI	ADC Test Mode Control (See Digital Output Data Control.)
40	MODE1	DI	ADC Test Mode Control (See Digital Output Data Control.)
41	ADCMODE	DI	ADC Input Control. Logic low for CDS/PGA, high for direct input.
42	NC		No Connect
43	ADVDD	P	+3 V Analog Supply
44, 45	ADVSS	P	Analog Ground
46	SUBST	P	Substrate. Connect to analog ground.
47	VRB	AO	Bottom Reference Bypass. Decouple to analog ground through 0.1 µF.
48	VRT	AO	Top Reference Bypass

NOTE
Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

EQUIVALENT INPUT CIRCUITS

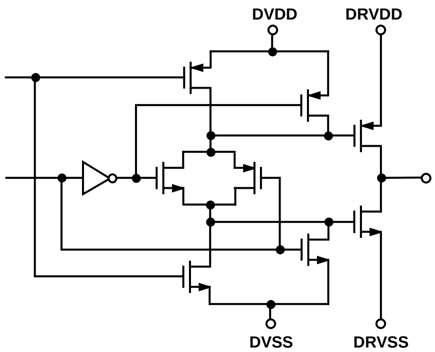


Figure 1. Pins 2–11 (DB0–DB9)

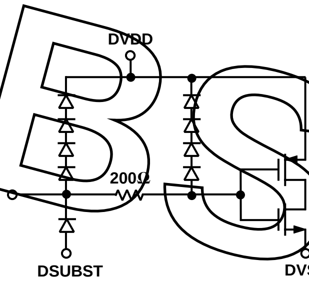


Figure 2. Pin 21 (SHP) and Pin 22 (SHD)

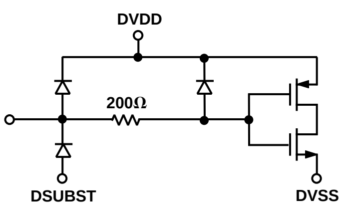


Figure 3. Pin 16 (ADCCLK)

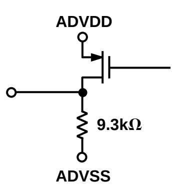


Figure 4. Pin 37 (CMLEVEL)

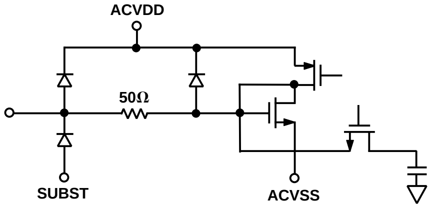


Figure 5. Pin 25 (CCDBYP2) and Pin 28 (CCDBYP1)

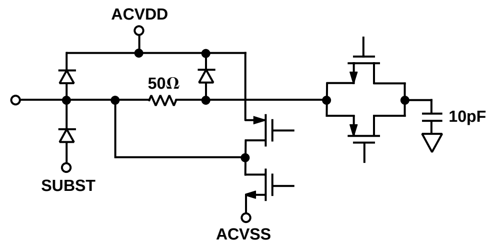


Figure 6. Pin 26 (DIN) and Pin 27 (PIN)

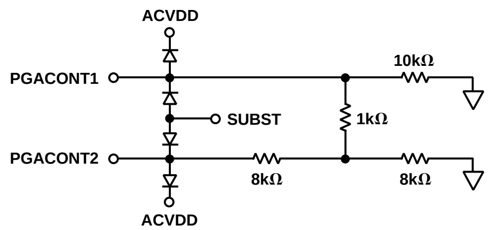


Figure 7. Pin 29 (PGACONT1) and Pin 30 (PGACONT2)

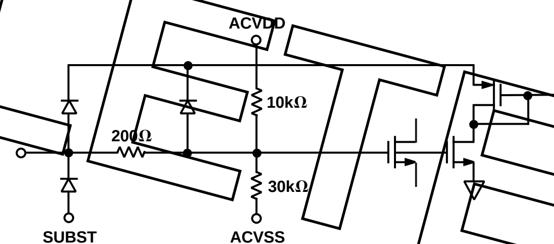


Figure 8. Pin 32 (CLAMP BIAS)

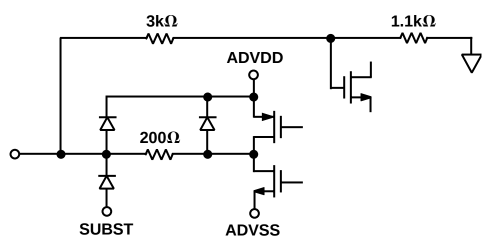


Figure 9. Pin 48 (VRT) and Pin 47 (VRB)

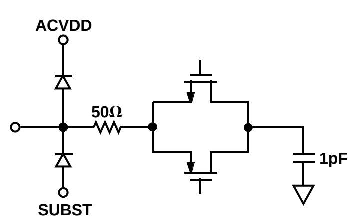


Figure 10. Pin 36 (ADCIN) and Pin 38 (SHABYP)

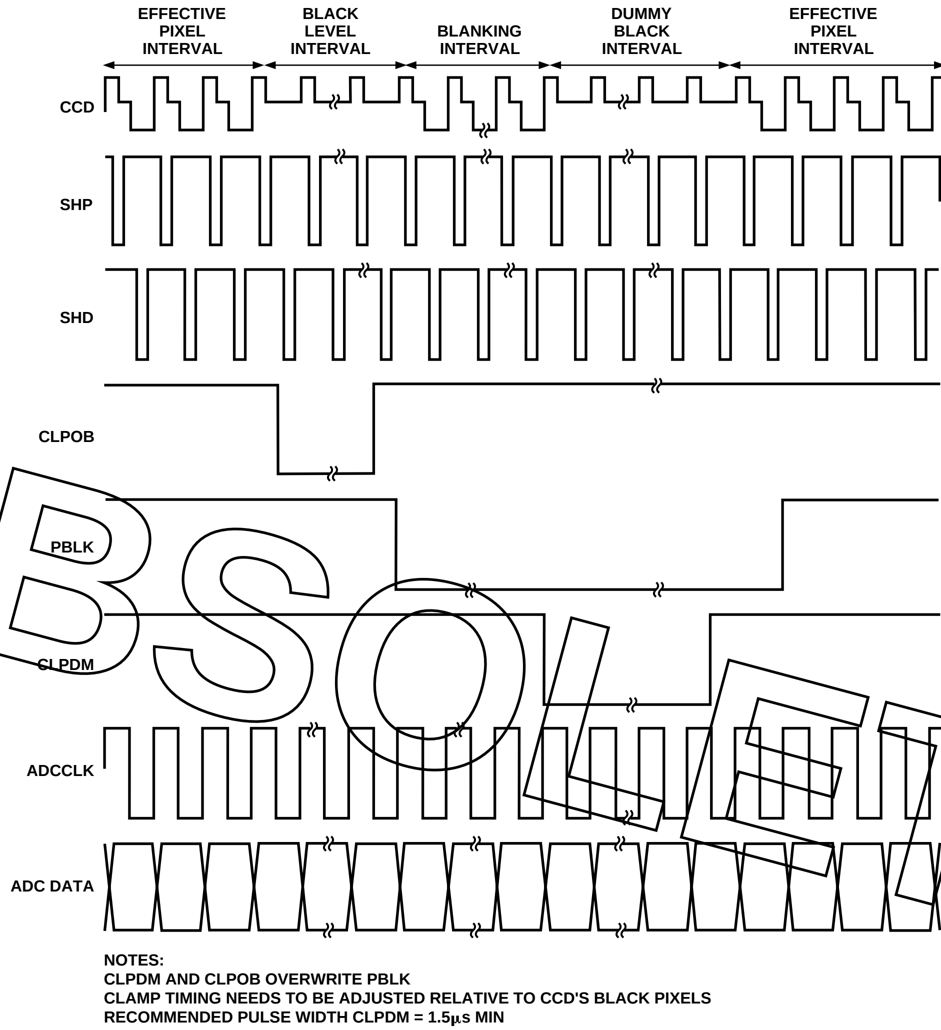


Figure 11. Typical Horizontal Interval Timing

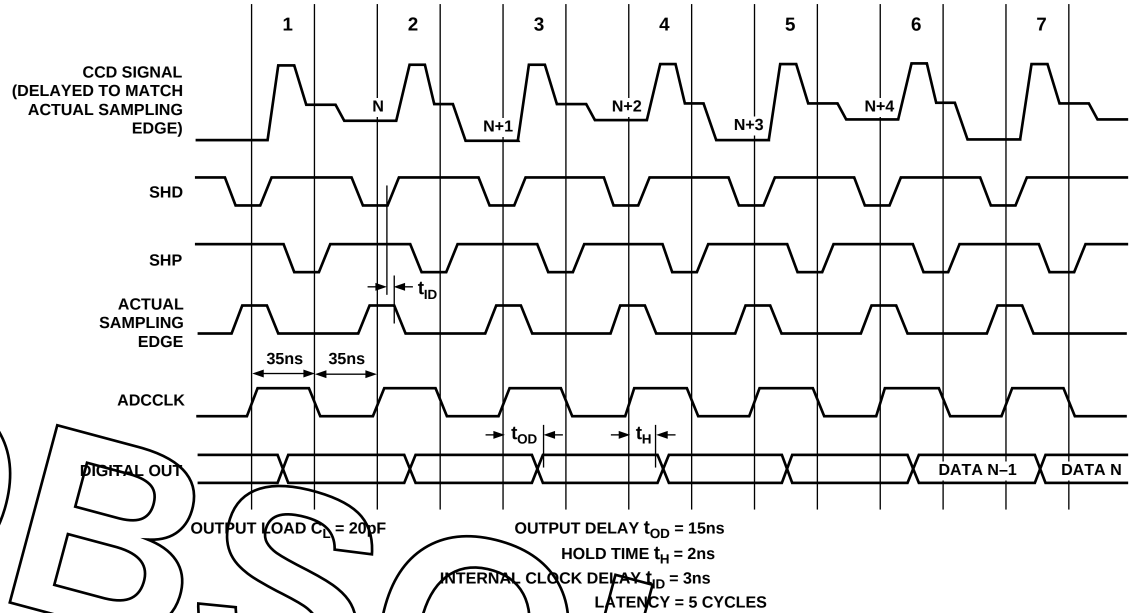


Figure 12. Timing Diagram

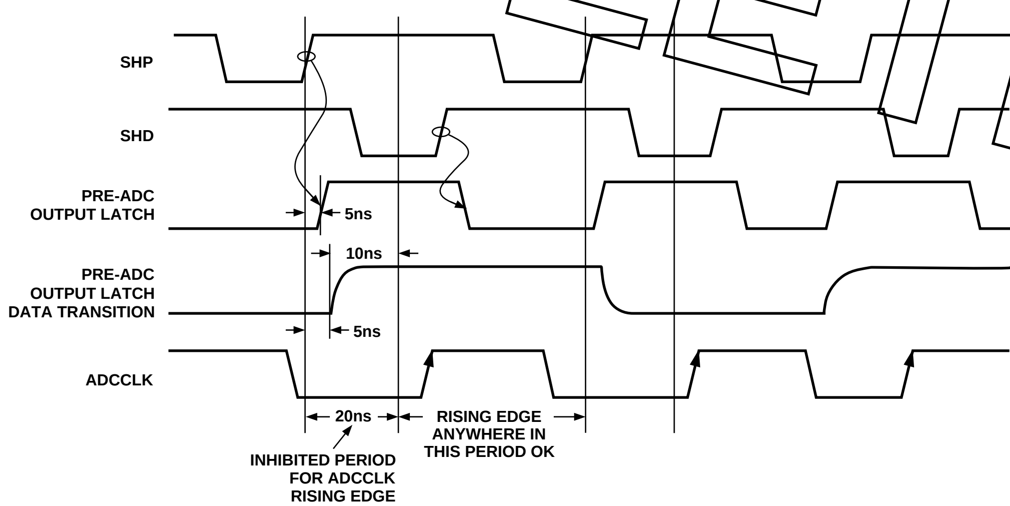


Figure 13. ADCCLK Timing Edge

THEORY OF OPERATION

Introduction

The AD9802 is a 10-bit analog-to-digital interface for CCD cameras. The block level diagram of the system is shown in Figure 14. The device includes a correlated double sampler (CDS), 0 dB–31 dB variable gain amplifier (PGA), black level correction loop, input clamp and voltage reference. The only external analog circuitry required at the system level is an emitter follower buffer between the CCD output and AD9802 inputs.

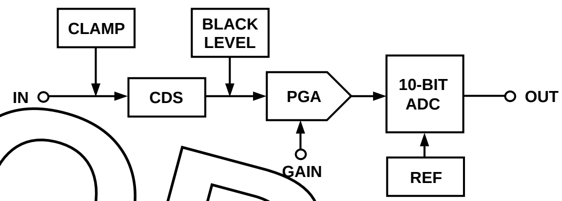


Figure 14.

Correlated Double Sampling (CDS)

CDS is important in high performance CCD systems as a method for removing several types of noise. Basically, two samples of the CCD output are taken: one with the signal present (data) and one without (reference). Subtracting these two samples removes any noise that is common to—or correlates with—both.

Figure 15 shows the block diagram of the AD9802's CDS. The S/H blocks are directly driven by the input and the sampling function is performed passively, without the use of amplifiers. This implementation relies on the off-chip emitter follower buffer to drive the two 10 pF sampling capacitors. Only one capacitor at a time is seen at the input pin.

The AD9802 actually uses two CDS circuits in a "ping-pong" fashion to allow the system more acquisition time. In this way, the output from one of the two CDS blocks will be valid for an entire clock cycle. Thus, the bandwidth requirement of the subsequent gain stage is reduced as compared to that for a single CDS channel system. This lower bandwidth translates to lower power and noise.

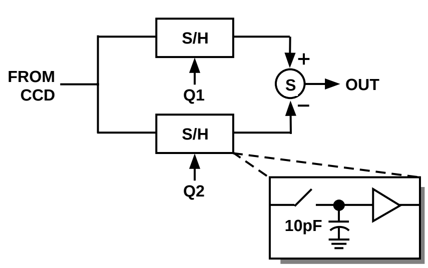


Figure 15.

Programmable Gain Amplifier (PGA)

The on-chip PGA provides a (linear in dB) gain range of 0 dB–31.5 dB. A typical gain characteristic plot is shown in Figure 16. Only the range from 0.3 V to 2.7 V is intended for actual use.

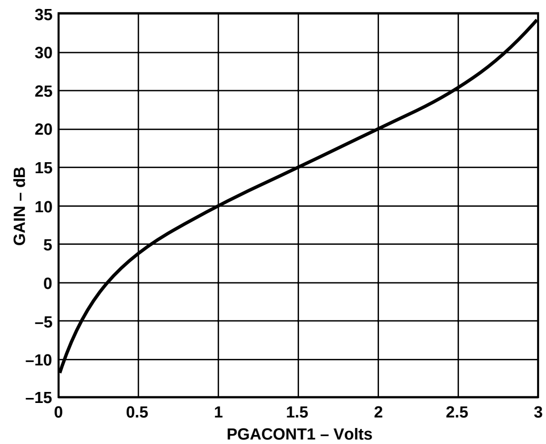


Figure 16.

As shown in Figure 17, PGA control is provided through the PGACONT1 and PGACONT2 inputs. PGACONT1 provides coarse, and PGACONT2 fine (1/16), gain control.

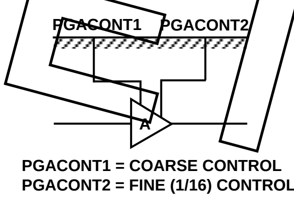


Figure 17.

Black Level Clamping

For correct processing, the CCD signal must be referenced to a well established "black level" by the AD9802. At the edge of the CCD, there is a collection of pixels covered with metal to prevent any light penetration. As the CCD is read out, these "black pixels" provide a calibration signal that is used to establish the black level.

The feedback loop shown in Figure 18 is closed around the PGA during the calibration interval (CLPOB = LOW) to set the black level. As the black pixels are being processed, an integrator block measures the difference between the input level and the desired reference level. This difference, or error, signal is amplified and passed to the CDS block where it is added to the incoming pixel data. As a result of this process, the black pixels are digitized at one end of the ADC range, taking maximum advantage of the available linear range of the system.

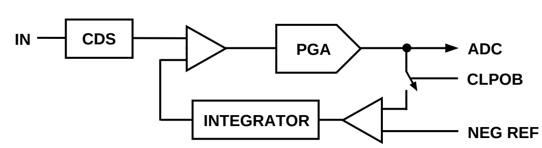


Figure 18.

The actual implementation of this loop is slightly more complicated as shown in Figure 19. Because there are two separate CDS blocks, two black level feedback loops are required and two offset voltages are developed. Figure 19 also shows an additional PGA block in the feedback loop labeled "RPGA." The RPGA uses the same control inputs as the PGA, but has the inverse gain. The RPGA functions to attenuate by the same factor as the PGA amplifies, keeping the gain and bandwidth of the loop constant.

There exists an unavoidable mismatch in the two offset voltages used to correct both CDS blocks. This mismatch causes a slight difference in the offset level for odd and even pixels, called "pixel-to-pixel offset" (see Specifications). The pixel-to-pixel offset is an output referred specification, because the black level correction is done using the output of the PGA.

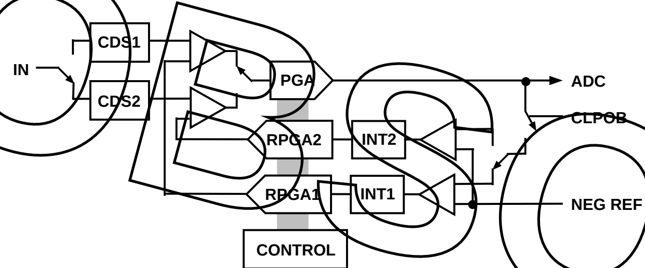


Figure 19.

Input Bias Level Clamping

The buffered CCD output is connected to the AD9802 through an external coupling capacitor. The dc bias point for this coupling capacitor is established during the clamping (CLPDM = LOW) period using the "dummy clamp" loop shown in Figure 20. When closed around the CDS, this loop establishes the desired dc bias point on the coupling capacitor.

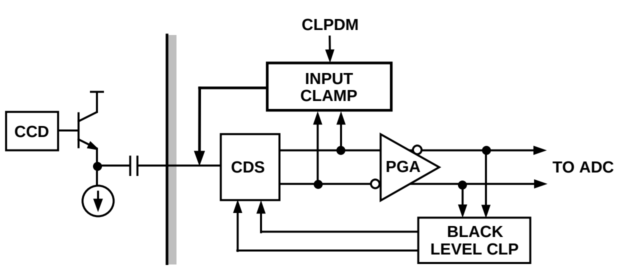


Figure 20.

Input Blanking

In some applications, the AD9802's input may be exposed to large signals from the CCD. These signals can be very large, relative to the AD9802's input range, and could thus saturate on-chip circuit blocks. Recovery time from such saturation conditions could be substantial.

To avoid problems associated with processing these transients, the AD9802 includes an input blanking function. When active (PBLK = LOW) this function stops the CDS operation and allows the user to disconnect the CDS inputs from the CCD buffer.

If the input voltage exceeds the supply rail by more than 0.3 V, then protection diodes will be turned on, increasing current flow into the AD9802 (see Equivalent Input Circuits). Such voltage levels should be externally clamped to prevent device damage or reliability degradation.

10-Bit Analog-to-Digital Converter (ADC)

The ADC employs a multibit pipelined architecture that is well suited for high throughput rates while being both area and power efficient. The multistep pipeline presents a low input capacitance resulting in lower on-chip drive requirements. A fully differential implementation was used to overcome headroom constraints of the single +3 V power supply.

Direct ADC Input

The analog processing circuitry may be bypassed in the AD9802. When ADCMODE (Pin 41) is taken high, the ADCIN pin provides a direct input to the SHA. This feature allows digitization of signals that do not require CDS and gain adjustment. The PGA output is disconnected from the SHA when ADCMODE is taken high.

Differential Reference

The AD9802 includes a 0.5 V reference based on a differential, continuous-time bandgap cell. Use of an external bypass capacitor reduces the reference drive requirements, thus lowering the power dissipation. The differential architecture was chosen for its ability to reject supply and substrate noise. Recommended decoupling shown in Figure 21.

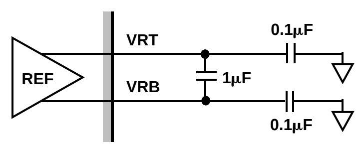


Figure 21.

Internal Timing

The AD9802's on-chip timing circuitry generates all clocks necessary for operation of the CDS and ADC blocks. The user needs only to synchronize the SHP and SHD clocks with the CCD waveform, as all other timing is handled internally. The ADCCLK signal is used to strobe the output data, and can be adjusted to accommodate desired timing.

APPLICATIONS INFORMATION

Generating Clock Signals

For best performance, the AD9802 should be driven by 3 V logic levels. As shown in the Equivalent Input Circuits, the use of 5 V logic for ADCCLK will turn on the protection diode to DVDD, increasing the current flow into this pin. As a result, noise and power dissipation will increase. The CDS clock inputs, SHP and SHD, have a additional protection and can withstand direct 5 V levels.

External clamping diodes or resistor dividers can be used to translate 5 V levels to 3 V levels, but the lowest power dissipation is achieved with a logic transceiver chip. National Semiconductor's 74LVX4245 provides a 5 V to 3 V level shift for up to eight clock signals, has a three-state option, and features low power consumption. Philips Semiconductor and Quality also manufacture similar devices.

Driving the Direct ADC Input

The AD9802 can be used in a "direct ADC input" mode, in which the input signal bypasses the input clamp, CDS and PGA, and is sent directly to the sample and hold amplifier (SHA) of the ADC. There are several methods that may be used to drive the direct ADC input.

To enable the direct input mode of operation, ADCMODE (Pin 41) is taken to logic high. This will internally disconnect the PGA output from the SHA input, and connect ADCIN (Pin 36) to the SHA input.

The SHA has a differential input, consisting of ADCIN (Pin 36) as the positive input, and SHABYP (Pin 38) as the negative input. Both pins must be properly dc biased.

Figures 22 through 25 show four circuits for driving the direct ADC input. Decoupling capacitors are not shown for CML, VRT, VRB and SHABYP pins.

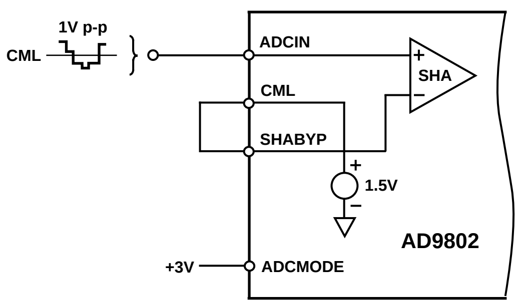


Figure 22. DC-Coupled Input

Figure 22 is a single-ended, dc-coupled circuit. SHABYP is connected to CML (1.5 V) to establish a midpoint bias. The input signal of 1 V p-p should be centered around CML.

Figure 23 shows an ac-coupled configuration, where both inputs are biased to CML. The input capacitor C_{IN} and bias resistors should be sized to set the appropriate high pass cutoff frequency for the application. To minimize the differential offset voltage due to the input bias currents, both resistors should be equal.

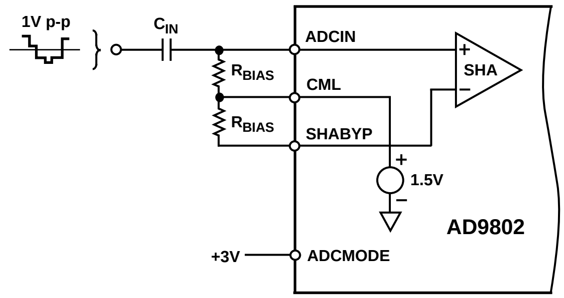


Figure 23. AC-Coupled Input

Figure 24 shows an alternative ac-coupled configuration. By connecting SHABYP to CML, the dc bias at Pin 36 (ADCIN) will internally track to the same voltage, automatically setting the input bias level. With a given input capacitor value, C_{IN}, the time constant in this configuration will be dependent on the sampling frequency F_S. Specifically:

$$\tau = (C_{IN}/F_S) \times 2E + 12$$

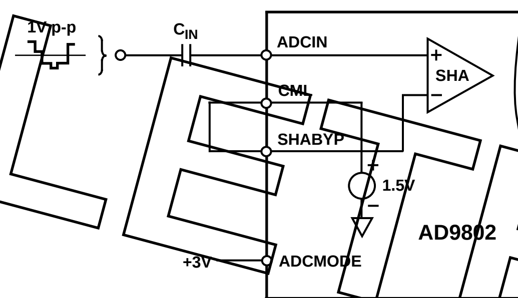


Figure 24. "Auto Bias" AC-Coupled Input

Figure 25 shows a true differential drive circuit. Each input would be 500 mV p-p, to achieve the 1 V full-scale input to the ADC. The common-mode input range for this configuration extends from about 500 mV to 2.5 V. This circuit could also be implemented with ac coupling, similar to Figure 23.

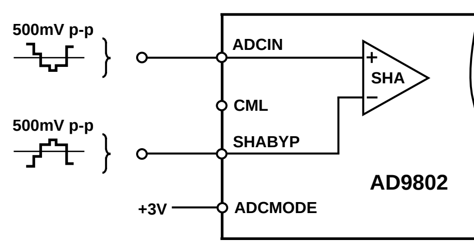


Figure 25. Differential Input

Figure 26 shows a video clamp circuit which may be used with the direct ADC mode of the AD9802 (supplies and decoupling not shown). The circuit will clamp the reference black level of an incoming video signal to 1.25 V dc. With SHABYP connected to 1.75 V (VRT), the ADCIN range spans from 1.25 V to 2.25 V. To accomplish this, the CLAMP pulse should be asserted during the horizontal sync interval, when the video is at its reference black level. A 5 V logic high applied to the gate of the SD210 will turn on the device, and the input capacitor C_{IN} will charge up to provide 1.25 V at the ADCIN pin of the AD9802. Other appropriate NMOS devices may be substituted for the SD210. The AD8047 op amp requires ±5 V supplies; appropriate single supply op amps may be substituted. The size of capacitor C_{IN} should be set to meet the acquisition time and droop specifications needed. A capacitor value of 0.01 µF will result in a droop of less than 10 LSB across one video line, and requires only a CLAMP pulse of 1 µs to charge up. A larger capacitor may be used to reduce droop, but then a longer CLAMP pulse may be necessary.

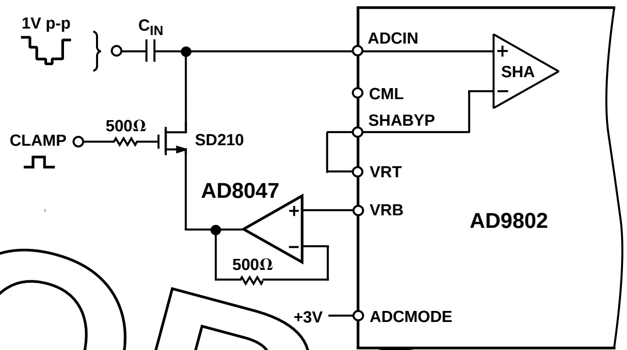


Figure 26. Video Clamp Circuit

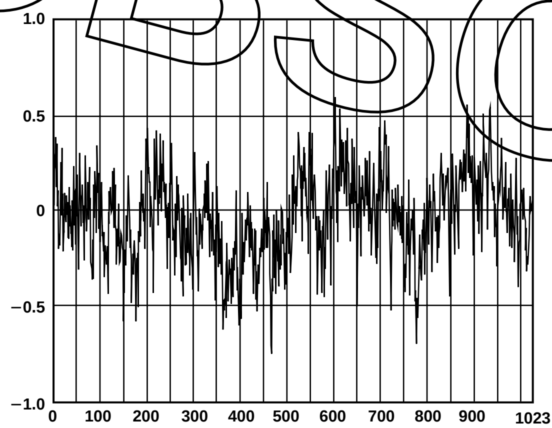


Figure 27. Direct ADC-Mode Typical INL

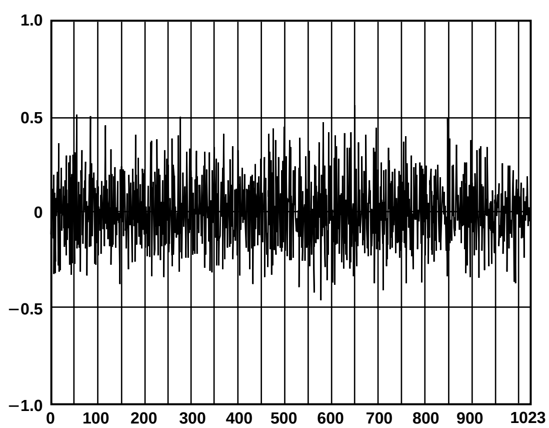


Figure 28. Direct ADC-Mode Typical DNL

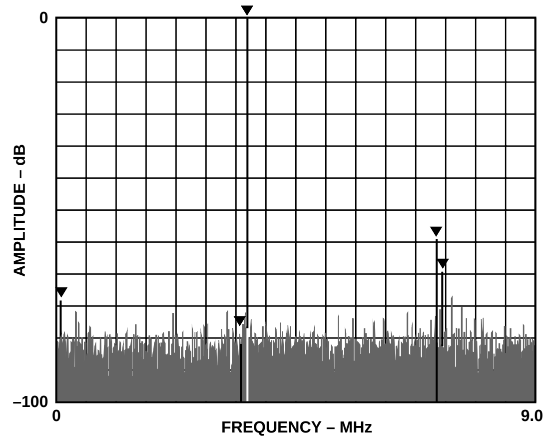


Figure 29. Direct ADC Mode Typical FFT; F_{IN} = 3.58 MHz, F_S = 18 MHz

Figures 27–29 show the typical linearity and distortion performance of the AD9802 in direct ADC mode.

Digitally Programmable Gain Control

The AD9802's PGA is controlled by an analog input voltage of 0.3 V to 2.7 V. In some applications, digital gain control is preferable. Figure 30 shows a circuit using Analog Devices' AD8402 Digital Potentiometer to generate the PGA control voltage. The AD8402 functions as two individual potentiometers, with a serial digital interface to program the position of each wiper over 256 positions. The device will operate with 3 V or 5 V supplies, and features a power-down mode and a reset function.

To keep external components to a minimum, the ends of the "potentiometers" can be tied to ground and +3 V. One pot is used for the coarse gain adjust, PGACONT1, with steps of about 0.2 dB/LSB. The other pot is used for fine gain control, PGACONT2, and is capable of around 0.01 dB steps if all eight bits are used. The two outputs should be filtered with 1 µF or larger capacitors to minimize noise into the PGACONT pins of the AD9802.

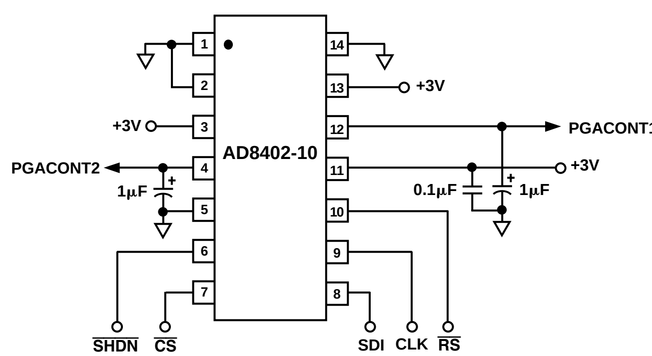


Figure 30. Digital Control of PGA

The disadvantage of this circuit is that the control voltage will be supply dependent. If additional precision is required, an external op amp can be used to amplify the VREFT (1.75 V) or VREFB (1.25 V) pins on the AD9802 to the desired voltage level. These reference voltages are stable over the operating supply range of the AD9802. Low power, low cost, rail-to-rail output amplifiers like the AD820, OP150 and OP196 are specified for 3 V operation. Alternatively, a precision voltage reference may be used. The REF193 from Analog Devices features low power, low dropout performance, maintaining a 3 V output with a minimum 3.1 V supply when lightly loaded.

Power and Grounding Recommendations

The AD9802 should be treated as an analog component when used in a system. The same power supply and ground plane should be used for all of the pins. In a two-ground system, this requires that the digital supply pins be decoupled to the analog ground plane and the digital ground pins be connected to analog ground for best noise performance. If any pins on the AD9802 are connected to the system digital ground, then noise can capacitively couple inside the AD9802 (through package and die parasitics) from the digital circuitry to the analog circuitry. Separate digital supplies can be used, particularly if slightly different driver supplies are needed, but the digital power pins should still be decoupled to the same point as the digital ground pins (analog ground plane). If the AD9802 digital outputs need to drive a bus or substantial load, a buffer should be used at the AD9802's outputs, with the buffer referenced to system digital ground. In some cases, when system digital noise is not substantial, it is acceptable to split the ground pins on the AD9802 to separate analog and digital ground planes. If this is done, be sure to connect the ground pins together at the AD9802.

To further improve performance, isolating the driver supply DRVDD from DVDD with a ferrite bead can help reduce kickback effects during major code transitions. Alternatively, the use of damping resistors on the digital outputs will reduce the output rise times, reducing the kickback effect.

Evaluation Board

An evaluation board for the AD9802 is available. The board includes circuitry for manual PGA gain adjustment, input signal buffering, and logic level translation for 3 V or 5 V digital signals.

Documentation for the AD9802-EB is included, consisting of a board description, schematic and layout information.

AD9801/AD9802 EVALUATION BOARD DESCRIPTION

Power Supply Connectors

J1 VDD: +3 V supply for the AD9801/AD9802. Data sheet specifications are given for +3.15 V. Operational range is from +3 V to +3.5 V.

J2 AVCC: +5 V supply for the AD8047 buffer, and for the PGACONT and PIN potentiometers. If the buffer amplifier is not needed, AVCC may be connected to the VDD supply.

J3 AVSS: –5 V supply for the AD8047 buffer. If the buffer amplifier is not needed, AVSS may be connected to J4.

J4 AGND: This is the analog ground plane for the AD9801/AD9802 and the buffer amplifier. The two ground planes are already connected together in one place on the evaluation board.

J5 DGND: This is the digital ground plane for the LVXC3245 transceivers. The two ground planes are already connected together in one place on the evaluation board.

J6 +3D: +3 V digital supply for the LVXC3245 transceivers.

J7 +3/5D: +3 V or +5 V digital supply for the LVXC3245 transceivers. This voltage determines the logic compatibility of the evaluation board. If 3 V clock levels and 3 V digital output levels are to be used, connect +3 V to J7. If +5 V clock levels and +5 digital output levels are to be used, connect +5 V to J7.

Input Connectors

J8 DIN: Unbuffered input to the AD9801/AD9802. This input is 50 Ω terminated by R4, which may be removed if no termination is required. See Input Configurations for more information.

J9 VIN: Input to the AD8047 buffer amplifier. This input is 50 Ω terminated by R5, which may be removed if no termination is required. This op amp can be used as a buffer to drive the DIN pin on the AD9801/AD9802, or as a buffer for driving the direct ADC input on the AD9802. See Input Configurations and the AD9802 data sheet for more information.

Clock Connectors

J10 CLPDM
J11 SHD
J12 SHP
J13 CLPOB
J14 PBLK
J15 ADCCLK

All of the clock inputs are 50 Ω terminated and buffered by an LVXC3245 transceiver. The supply level at J7 determines the input clock level compatibility. The outputs of the LVXC3245 always send +3 V clock levels to the AD9801/AD9802.

Jumper Descriptions

JP1 Connect to bypass the input coupling capacitor C18.
JP2 Connect to short PIN and DIN (Pins 26 and 27 of the AD9801) together.
JP3 Connects PIN to the dc level set by the wiper of R1.
JP4 Connect to short the input coupling capacitor to ground, for test purposes.
JP5 Connects the output of the buffer amplifier to the AD9801/AD9802 input.
JP6 Connects the AD9801/AD9802's DRVDD pin to the VDD supply through ferrite bead FB6.
JP7 Connects the AD9801/AD9802's DRVDD pin to the +3D supply.
JP8 Connects the output of the AD8047 op amp to the direct ADC input of the AD9802. This jumper should never be connected on the AD9801-EB.
JP9 Selects the regular camera mode of operation on the AD9802. This jumper should always be in place on the AD9801-EB.
JP10 Selects the direct ADC input mode on the AD9802. This jumper should never be connected on the AD9801-EB.

Test Point Descriptions

TP1 Input signal at J8.
TP2 Input signal at PIN/DIN of AD9801/AD9802.
TP3 PGACONT1 voltage.
TP4 PGACONT2 voltage.
TP5 STANDBY pin, pull high to enable power-down mode.
TP6 CLPDM at AD9801/AD9802.
TP7 SHD at AD9801/AD9802.
TP8 SHP at AD9801/AD9802.
TP9 CLPOB at AD9801/AD9802.
TP10 PBLK at AD9801/AD9802.
TP11 ADCCLK at AD9801/AD9802.
TP12 VDD
TP13 AVCC
TP14 AVSS
TP15 AGND
TP16 DGND
TP17 +3D
TP18 +3/5D

Prototype Area

The top left hole in the prototyping area is connected to AGND. The bottom right hole is connected to AVCC.

Input Configurations

	Input	JP1	JP2	JP3	JP4	JP5	JP8	JP9	JP10
Standard CCD Input	J8	open	short	open	open	open	open	short	open
Grounded Input Test	none	open	short	open	short	open	open	short	open
Buffered Input*	J9	open	short	open	open	short	open	short	open
Direct ADC Input (9802 only)	J9	[	... don't care...			]	short	open	short

*When using the buffer amplifier, ±5 V must be connected to AVCC and AVSS, and R4 should be removed.

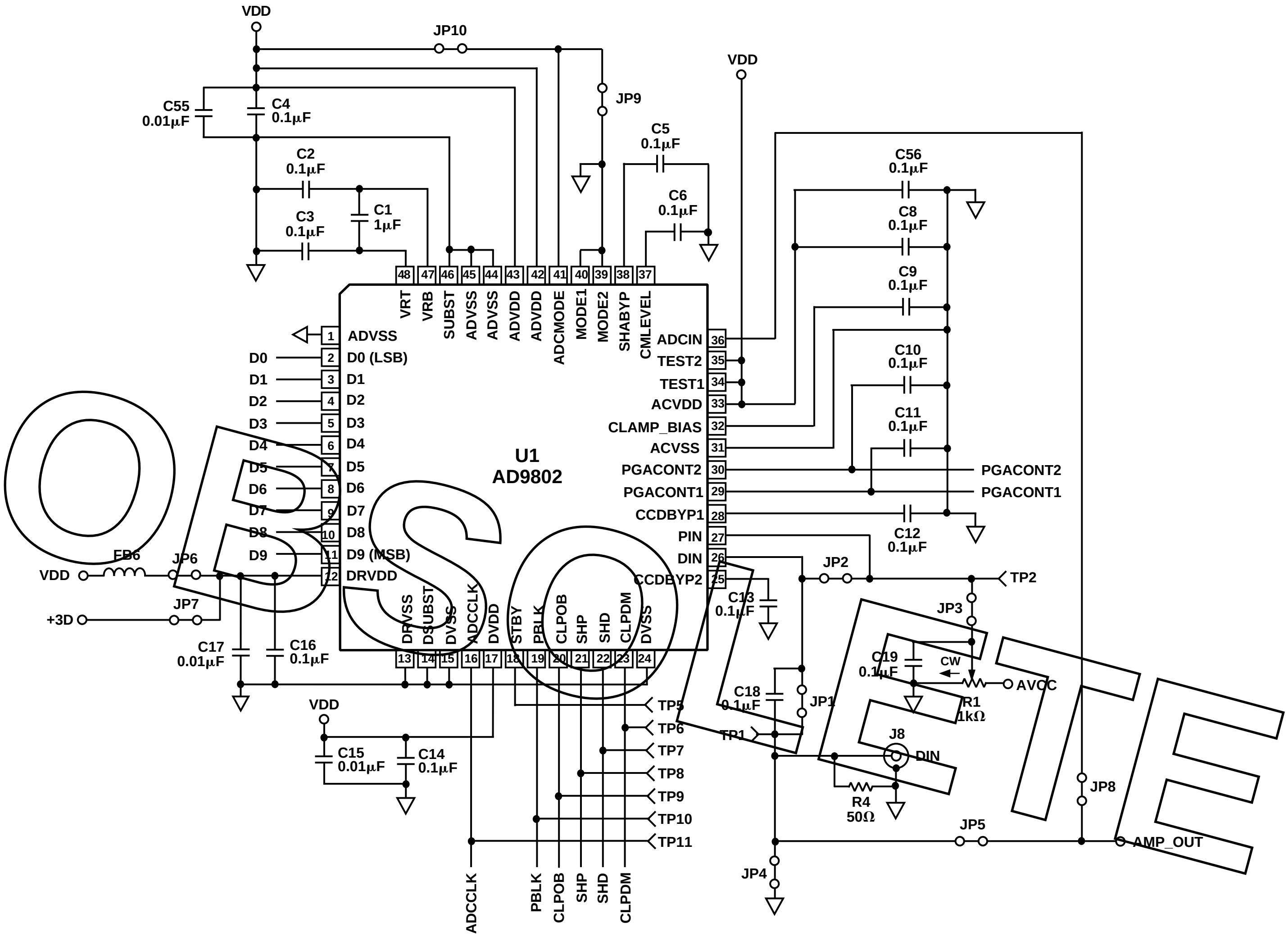


Figure 31. Evaluation Board

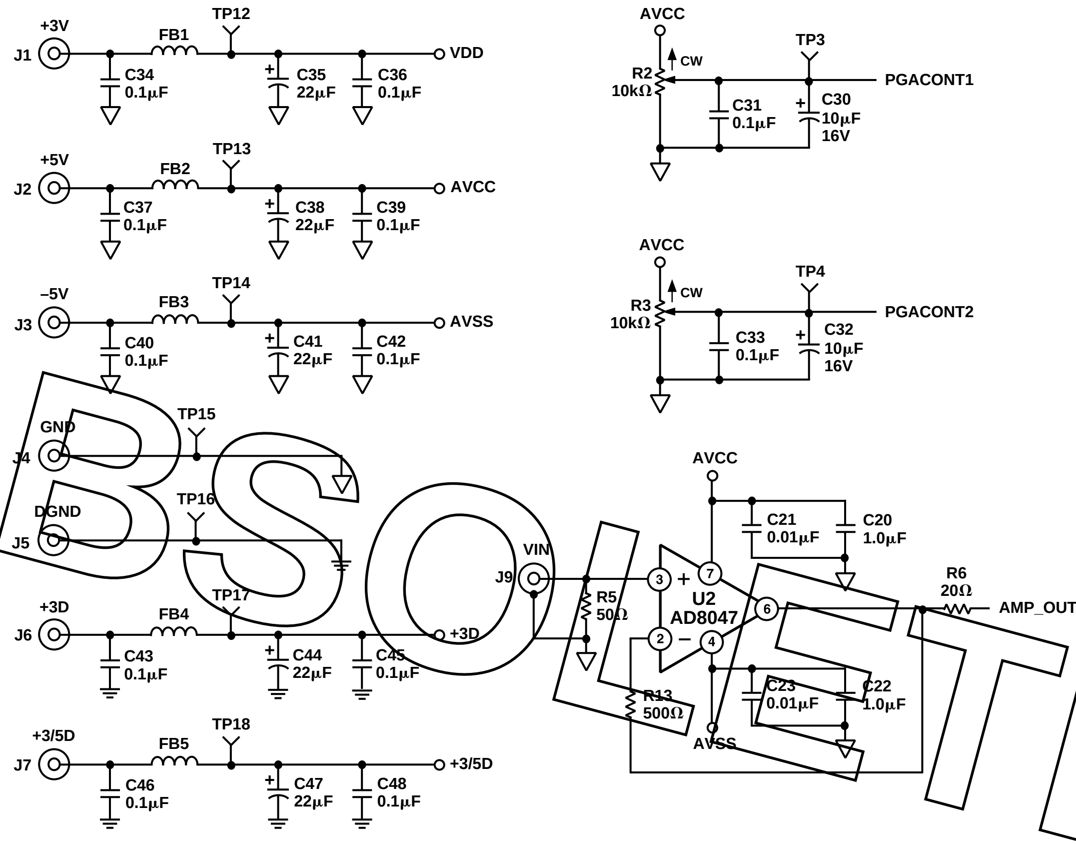


Figure 32. Evaluation Board

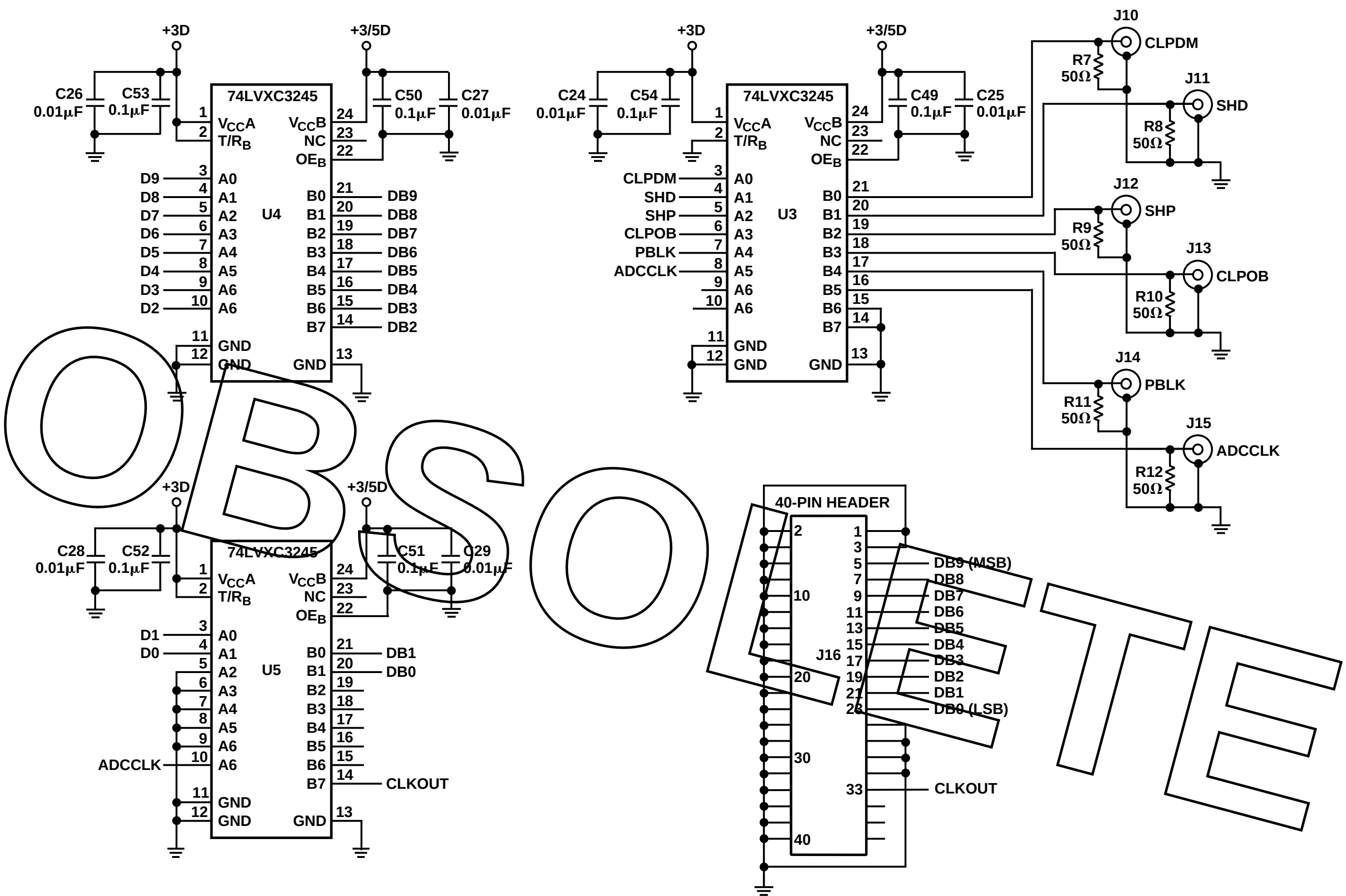


Figure 33. Evaluation Board

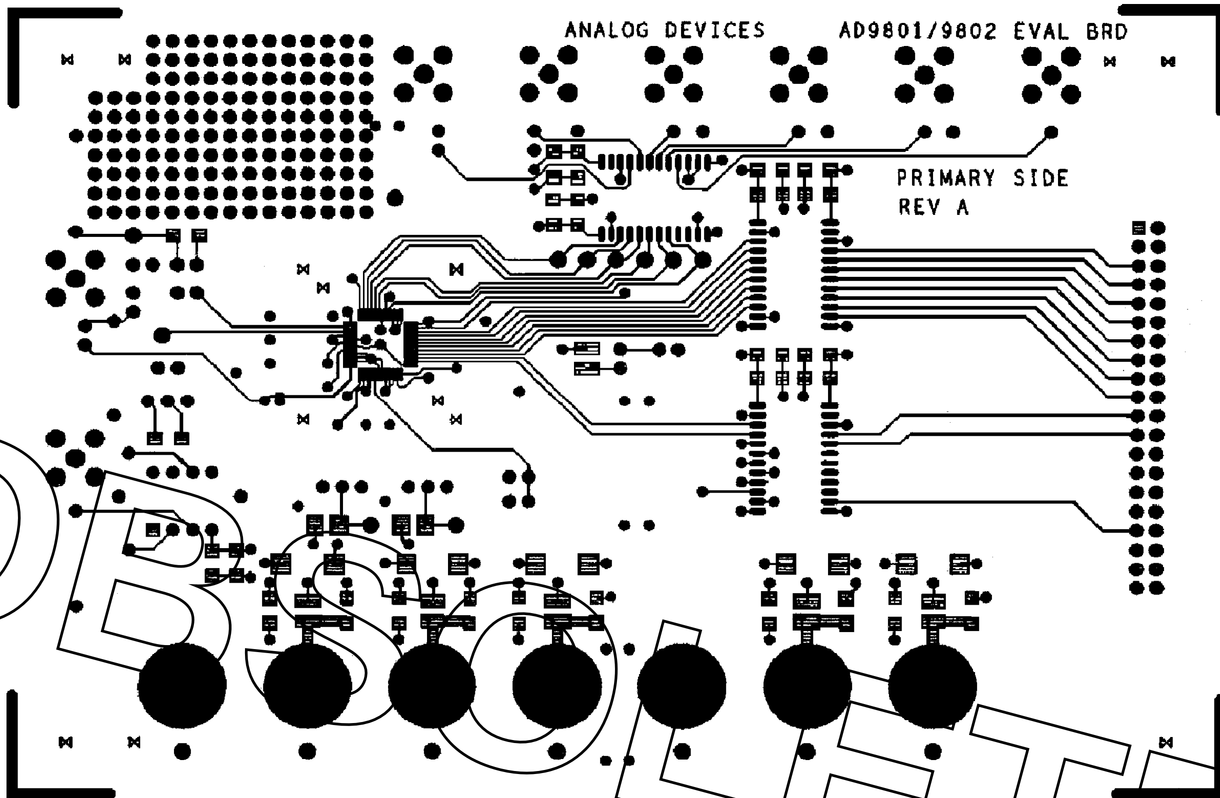


Figure 34. Primary Side (Layer 1)

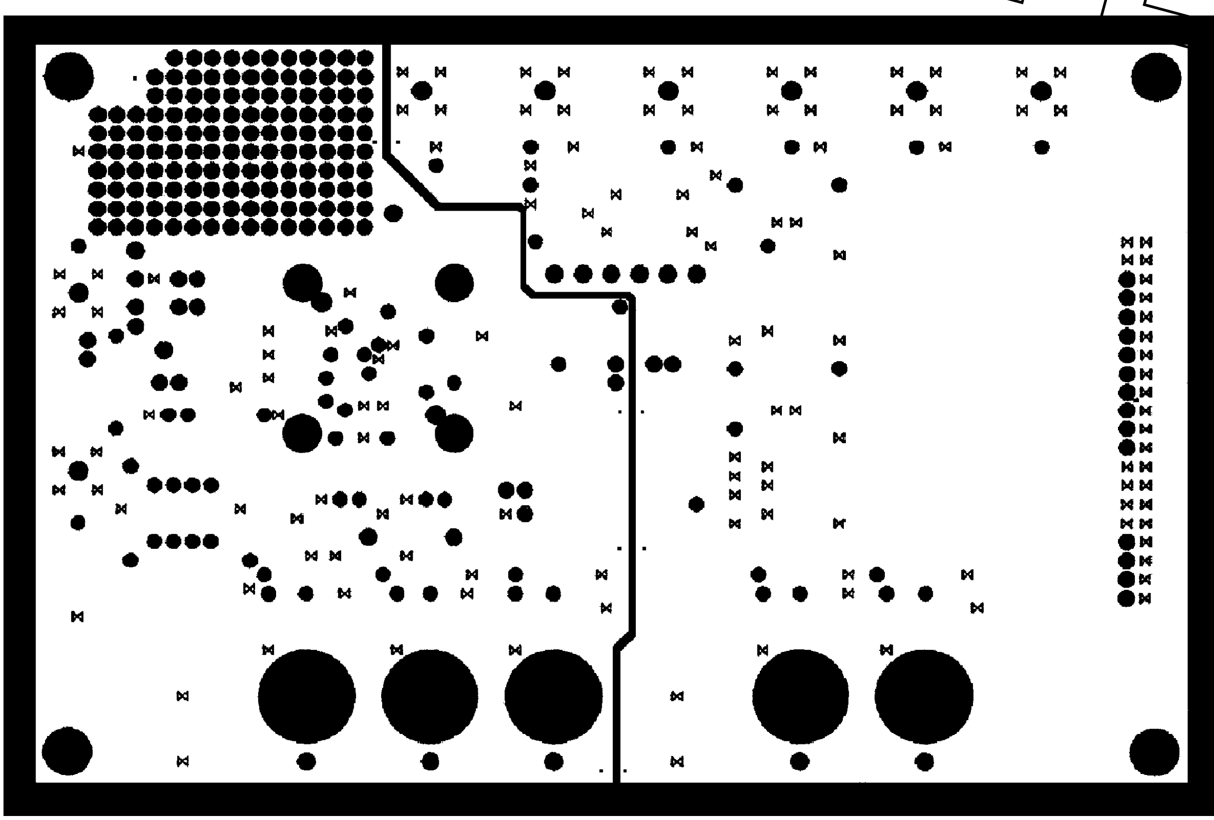


Figure 35. Ground Plane (Layer 2)

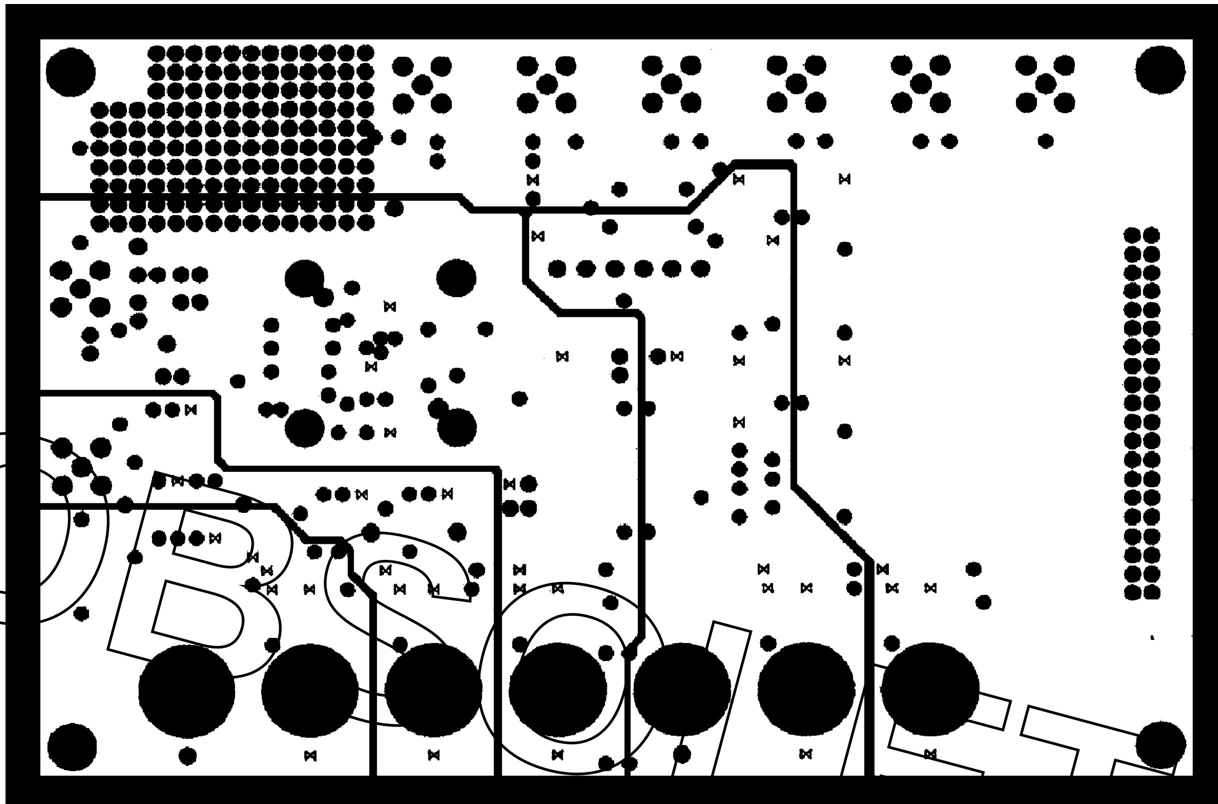


Figure 36. Power Plane (Layer 3)

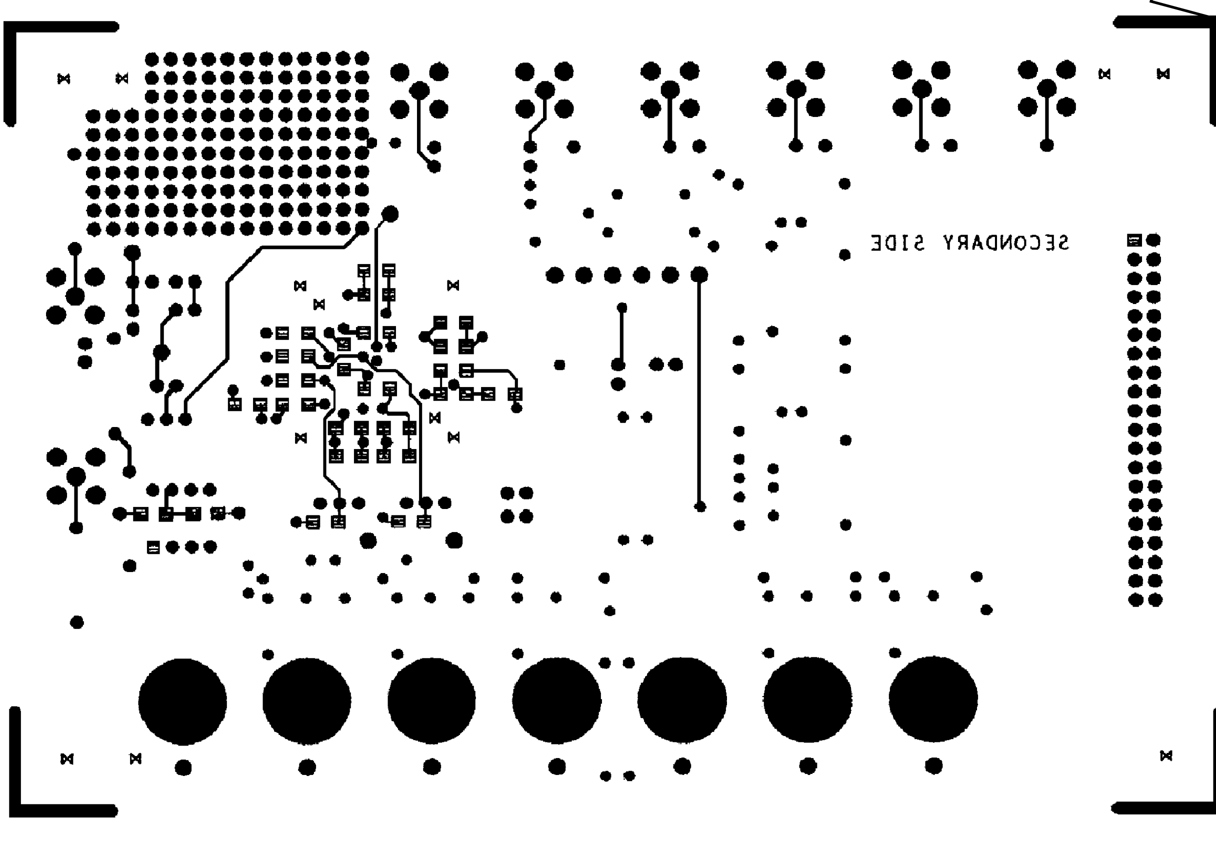


Figure 37. Secondary Layer (Layer 4)

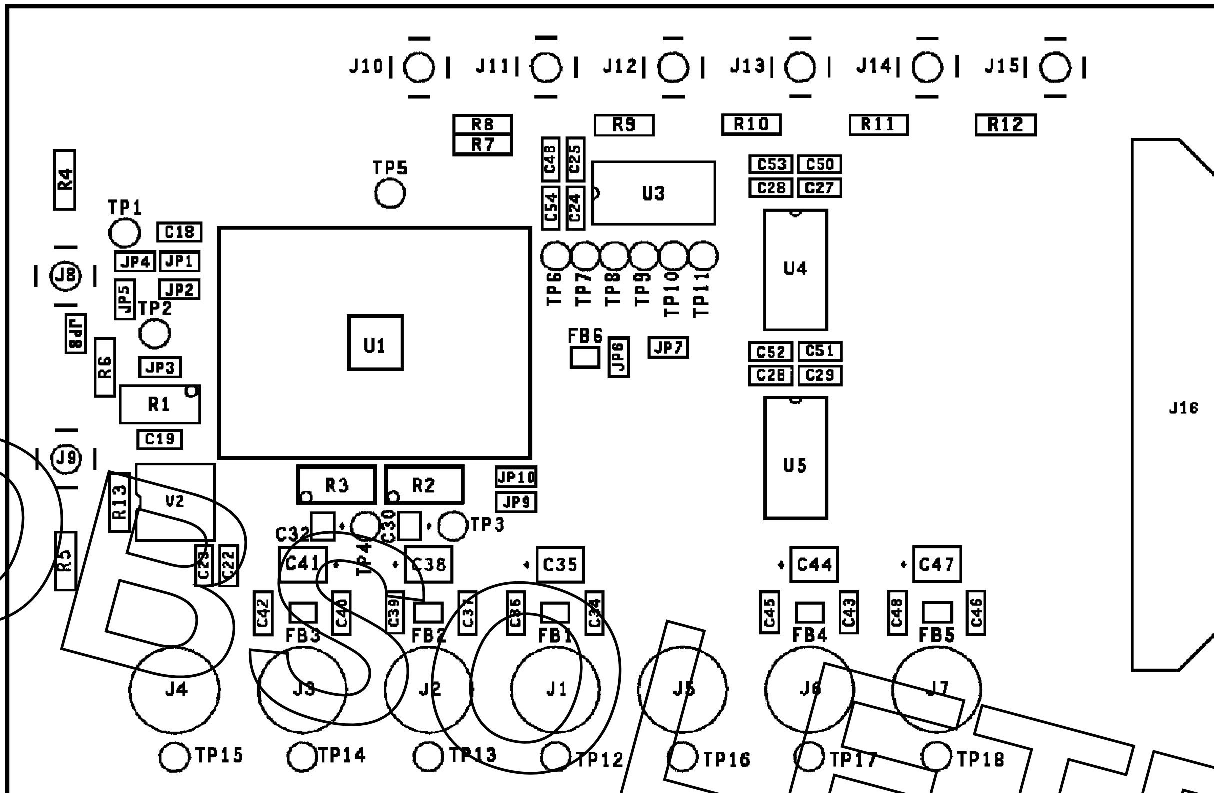


Figure 38. Primary Side Assembly

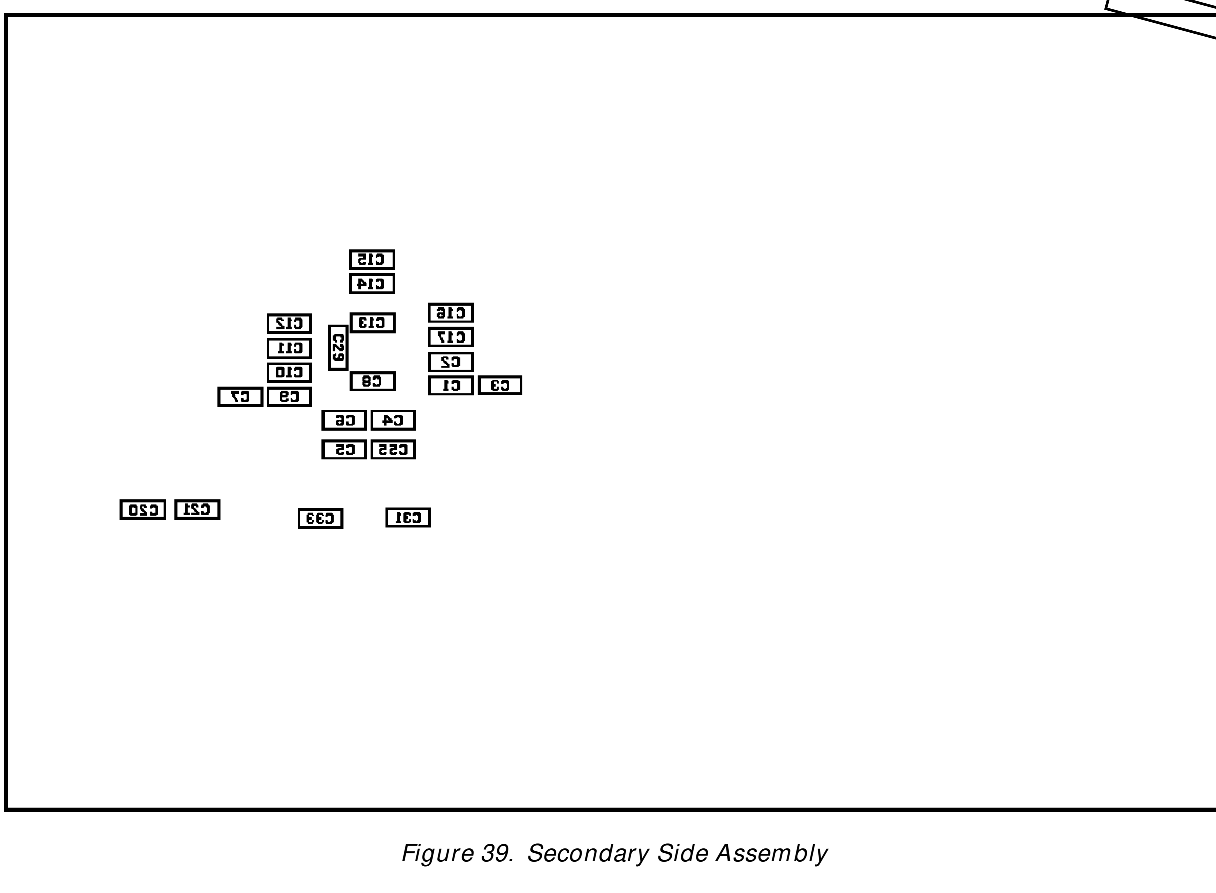
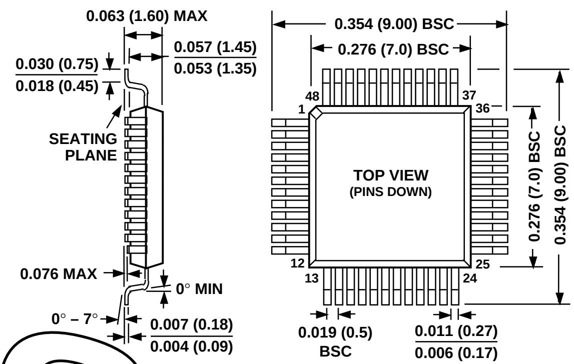


Figure 39. Secondary Side Assembly

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Terminal Plastic Thin Quad Flatpack (TQFP) (ST-48)



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