National Semiconductor

MICROCIRCUIT DATA SHEET

CN74F74-X REV 1A0

Original Creation Date: 11/18/96
Last Update Date: 06/19/97
Last Major Revision Date: 04/17/97

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

General Description

The F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary ($Q/\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse Input threshold voltage has been passed, the Data inputs is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW Input to $\overline{S}d$ sets Q to HIGH level
- LOW Input to $\overline{C}d$ sets Q to LOW level
- Clear and Set are Independent of clock
- Simultaneous LOW on $\overline{C}d$ and $\overline{S}d$ makes both Q and Q HIGH

Industry Part Number

74F74

NS Part Numbers

74F74DC

Prime Die

M074

Processing

Quality Conformance Inspection

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+70
3	Static tests at	0
4	Dynamic tests at	+25
5	Dynamic tests at	+70
6	Dynamic tests at	0
7	Functional tests at	+25
8A	Functional tests at	+70
8B	Functional tests at	0
9	Switching tests at	+25
10	Switching tests at	+70
11	Switching tests at	0

Features

- Guaranteed 4000V minimum ESD protection

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 1)	-0.5V to +7.0V
Input Current (Note 1)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these condtions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Supply Voltage	
Commercial	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIH	Input HIGH Voltage	Recognized as a HIGH Signal	1	INPUTS	2.0		V	1, 2, 3
VIL	Input LOW Voltage	Recognized as a LOW Signal	1	INPUTS		0.8	V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IIN=-18mA	2, 3	INPUTS		-1.2	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, IOH=-1.0mA	2, 3	OUTPUTS	2.5		V	1, 2, 3
		VCC=4.75V, IOH=-1.0mA	2, 3	OUTPUTS	2.7		V	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, IOL=20mA	2, 3	OUTPUTS		0.5	V	1, 2, 3
IIH	Input HIGH Current	VCC=5.5V, VIN=2.7V	2, 3	INPUTS		5.0	uA	1, 2, 3
IBVI	Input HIGH Current Breakdown Test	VCC=5.5V, VIN=7.0V	2, 3	INPUTS		7.0	uA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VOUT = VCC	2, 3	OUTPUTS		100	uA	1, 2, 3
VID	Input Leakage Test	VCC = 0.0V, IID = 1.9uA, All other pins grounded	2, 3	INPUTS	4.75		V	1, 2, 3
IOD	Output Leakage Circuit Current	VCC = 0.0V, VIOD = 150mV, All other pins grounded	2, 3	OUTPUTS		4.75	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VIN=0.5V	2, 3	INPUTS		-0.6	mA	1, 2, 3
		VCC=5.5V, VIN = 0.5V	2, 3	INPUTS		-1.8	mA	1, 2, 3
IOS	Output Short-Circuit Current	VCC=5.5V, VOUT = 0V	2, 3	OUTPUTS	-60	-150	mA	1, 2, 3
ICC	Power Supply Current	VCC=5.5V	2, 3	VCC		16.0	mA	1, 2, 3

Electrical Characteristics

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS. Temp Range: 0C to +70C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fMAX	Maximum Clock Frequency	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4		100		MHz	9, 10, 11
tpLH(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	CPn/Qn or $\overline{Q}$n	3.8	6.8	ns	9
			2, 3	CPn/Qn or $\overline{Q}$n	3.8	7.8	ns	10, 11
tpHL(1)	Propagation Delay	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3	CPn/Qn or $\overline{Q}$n	4.4	8.0	ns	9
			2, 3	CPn/Qn or $\overline{Q}$n	4.4	9.2	ns	10, 11
tpLH(2)	Propagation Delay $\overline{C}$Dn or $\overline{S}$Dn/Qn or $\overline{Q}$n	VCC=+5.0V @+25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3		3.2	6.1	ns	9
tpLH(2)	Propagation Delay $\overline{C}$Dn or $\overline{S}$Dn/Qn or $\overline{Q}$n	VCC=+5.0V @+25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3		3.2	7.1	ns	10, 11
tpHL(2)	Propagation Delay $\overline{C}$Dn or $\overline{S}$Dn/Qn or $\overline{Q}$n	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3		3.5	9.0	ns	9
tpHL(2)	Propagation Delay $\overline{C}$Dn or $\overline{S}$Dn/Qn or $\overline{Q}$n	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	2, 3		3.5	10.5	ns	10, 11
ts(H)	Setup Time HIGH	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	Dn to CPn	2.0		ns	9, 10, 11
ts(L)	Setup Time LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	Dn to CPn	3.0		ns	9, 10, 11
th(H/L)	Hold Time HIGH or LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	Dn to CPn	1.0		ns	9, 10, 11
tw(H)	Pulse Width HIGH	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	CPn	4.0		ns	9, 10, 11
tw(L)	Pulse Width LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	CPn	5.0		ns	9, 10, 11
tw (L)	Pulse Width LOW	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	$\overline{C}$Dn or $\overline{S}$Dn	4.0		ns	9, 10, 11
tREC	Recovery Time	VCC=+5.0V @ +25C, VCC=4.5V & 5.5V @ 0/+70C	4	$\overline{C}$Dn/$\overline{S}$Dn to CP	2.0		ns	9, 10, 11

Note 1: Guaranteed by applying specific input condition and testing VOL & VOH.
Note 2: Screen tested 100% on each device at +75C temperature only, subgroups A2 & A10.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +75C temperature only, subgroups A2 & A10.
Note 4: Guaranteed but not tested.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0001326	06/19/97	Donald B. Miller	