19-3782; Rev 1; 1/06

EVALUATION KIT AVAILABLE

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

General Description

The MAX9756/MAX9757/MAX9758 combine dual, 2.3W, bridge tied load (BTL) stereo audio power amplifiers and a DirectDrive™ headphone amplifier in a single device. These devices feature single-supply voltage operation, shutdown mode, logic-selectable gain, a headphone sense input, a 31-step analog volume control, and industry-leading click-and-pop suppression. The headphone amplifier uses Maxim's DirectDrive architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors.

The MAX9756/MAX9757 feature automatic level control (ALC) that automatically limits output power to the speaker in the event of an overpowered output.

The MAX9756/MAX9758s' 150mA internal linear regulator provides a complete solution for DAC- or CODEC-based designs.

The MAX9756/MAX9757/MAX9758 are offered in space-saving, thermally efficient 32-pin (5mm x 5mm x 0.8mm) and 36-pin thin QFN (6mm x 6mm x 0.8mm) packages. All devices are specified over the extended -40°C to +85°C temperature range.

Applications

Notebook PCs
Tablet PCs
Portable DVD Players
Flat-Panel TVs
PC Displays
LCD Projectors
Portable Audio

Features

- ♦ **Automatic Level Control—Protects Speakers**
- ♦ **Analog Volume Control**
- ♦ **120mW DirectDrive Headphone Amplifiers (16Ω)**
- ♦ **150mA Adjustable LDO**
- ♦ **Class AB, 2.3W, Stereo BTL Speaker Amplifiers (3Ω)**
- ♦ **High 95dB PSRR**
- ♦ **Low-Power Shutdown Mode**
- ♦ **Industry-Leading Click-and-Pop Suppression**
- ♦ **Short-Circuit and Thermal Protection**
- ♦ **Beep Input**

Ordering Information

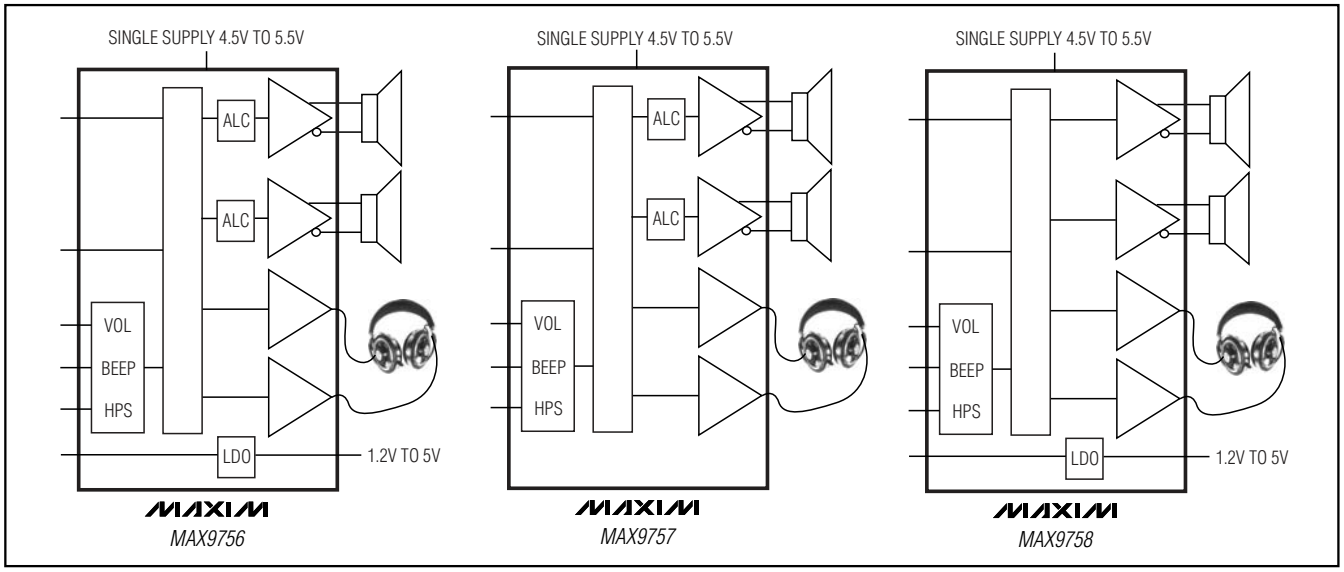
PART	ALC	LDO	PIN-PACKAGE
MAX9756ETX+	√	√	36 Thin QFN-EP*
MAX9757ETJ+	√	—	32 Thin QFN-EP*
MAX9758ETJ+	—	√	32 Thin QFN-EP*

Note: *All devices specified for -40°C to +85°C operating temperature range.*

+Denotes lead-free package.

**EP = Exposed paddle.*

Simplified Block Diagrams



2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD}, PV_{DD}, HPV_{DD}, CPV_{DD}, IN to GND) ....+6V
PGND, CPGND to GND .....±0.3V
CPV_{SS}, C1N, V_{SS} to GND.....-6.0V to +0.3V
HP_ to GND .....±3V
Any Other Pin .....-0.3V to (V_{DD} + 0.3V)
Duration of OUT_ Short Circuit to GND or PV_{DD}.....Continuous
Duration of OUT_+ Short Circuit to OUT_-.....Continuous
Duration of HP_ Short Circuit to GND, V_{SS}, or HPV_{DD}.....Continuous
Duration of OUT Short Circuit to GND.....Continuous
Continuous Current (PV_{DD}, OUT_, PGND) 1.7A
Continuous Current (CPV_{DD}, C1N, CPGND, C1P, CPV_{SS}, V_{SS}, HPV_{DD}, HP_, IN, OUT).....0.85A
Continuous Input Current (all other pins) .....±20mA
Continuous Power Dissipation (T_A = +70°C, single-layer board)
32-Pin Thin QFN (derate 18.6mW/°C above +70°C).....1490mW
36-Pin Thin QFN (derate 20.4mW/°C above +70°C).....1633mW
Continuous Power Dissipation (T_A =+70°C, multilayer board)
32-Pin Thin QFN (derate 24.9mW/°C above +70°C).....1990mW
36-Pin Thin QFN (derate 27.7mW/°C above +70°C).....2180mW
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0, $\overline{SHDN}$ = V_{DD}, REGEN = V_{DD}, DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, speaker loads terminated between OUT_+ and OUT_-, headphone load terminated between HP_ and GND, GAIN1 = GAIN2 = GAIN3 = VOL = 0 ($A_{V(SP)}$ = 15dB, $A_{V(HP)}$ = 0dB), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	V_{DD}, PV_{DD}	Inferred from PSRR test		4.5		5.5	V
Headphone Supply Voltage	HPV_{DD}	Inferred from PSRR test		3.0		5.5	V
Quiescent Supply Current	I_{DD}	I_{DD} = I_{VDD} + I_{HPVDD} + I_{CPVDD}	HPS = GND, speaker mode, R_L = ∞		14	29	mA
			HPS = 5V, headphone mode, R_L = ∞		7	13	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = REGEN = GND			0.2	5	µA
Bias Voltage	V_{BIAS}			2.2	2.43	2.65	V
Switching Time	t_{SW}	Gain or input switching			10		µs
Input Resistance	R_{IN}	INL and INR		10	20	30	kΩ
Turn-On Time	t_{SON}				25		ms
SPEAKER AMPLIFIERS (HPS = GND)							
Output Offset Voltage	V_{OS}	Measured between OUT_+ and OUT_-, T_A = +25°C			±0.4	±15	mV
Power-Supply Rejection Ratio (Note 2)	PSRR	PV_{DD} = 4.5V to 5.5V, T_A = +25°C		75	95		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			83		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}			68		
Output Power (Note 3)	P_{OUT}	THD+N = 1%, f = 1kHz (T_A = +25°C)	R_L = 8Ω	0.9	1.3		W
			R_L = 4Ω		2.0		
			R_L = 3Ω		2.3		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 8Ω, BTL P_{OUT} = 1W, f = 1kHz			0.009		%
		R_L = 4Ω, BTL P_{OUT} = 1W, f = 1kHz			0.015		
Signal-to-Noise Ratio	SNR	R_L = 8Ω, BTL P_{OUT} = 1W, BW = 22Hz to 22kHz, unweighted			92		dB
		R_L = 8Ω, BTL P_{OUT} = 1W, A weighted			95		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0, $\overline{SHDN}$ = V_{DD}, REGEN = V_{DD}, DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, speaker loads terminated between OUT_+ and OUT_-, headphone load terminated between HP_ and GND, GAIN1 = GAIN2 = GAIN3 = VOL = 0 ($A_{V(SP)}$ = 15dB, $A_{V(HP)}$ = 0dB), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Noise	V_n	BW = 22Hz to 22kHz, unweighted, measured at output, input at AC GND				71		$µV_{RMS}$
Capacitive-Load Drive	C_L	No sustained oscillations				200		pF
Crosstalk		L to R, R to L, f = 10kHz				80		dB
Slew Rate	SR	Measured between OUT_+ and OUT_-				1.3		V/µs
Gain (Maximum Volume Settings) (Note 4)	A_{VMAX} (SPKR)	GAIN3 = 0	GAIN2 = 0	GAIN1 = 0		15		dB
		GAIN3 = 0	GAIN2 = 0	GAIN1 = 1		16.5		
		GAIN3 = 0	GAIN2 = 1	GAIN1 = 0		18		
		GAIN3 = 0	GAIN2 = 1	GAIN1 = 1		19.5		
		GAIN3 = 1	GAIN2 = 0	GAIN1 = 0		21		
		GAIN3 = 1	GAIN2 = 0	GAIN1 = 1		22.5		
		GAIN3 = 1	GAIN2 = 1	GAIN1 = 0		24.0		
		GAIN3 = 1	GAIN2 = 1	GAIN1 = 1		25.5		
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A weighted (Note 5)		Into shutdown		65		dBV
				Out of shutdown		38.5		
HEADPHONE AMPLIFIERS (HPS = V_{DD})								
Output Offset Voltage	$V_{OS(HP)}$	T_A = +25°C				±2	±7	mV
Power-Supply Rejection Ratio (Note 2)	PSRR	HPV_{DD} = 3V to 5.5V, T_A = +25°C			70	90		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}				72		
		f = 10kHz, V_{RIPPLE} = 200mV_{P-P}				70		
Output Power (Note 3)	P_{OUT}	THD+N = 1%, f = 1kHz (T_A = +25°C)		R_L = 32Ω	40	68		mW
				R_L = 16Ω		130		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 32Ω, V_{OUT} = $1V_{RMS}$, f = 1kHz				0.02		%
		R_L = 16Ω, V_{OUT} = $1V_{RMS}$, f = 1kHz				0.04		
Signal-to-Noise Ratio	SNR	R_L = 32Ω, BTL P_{OUT} = 65mW, BW = 22Hz to 22kHz, unweighted				97		dB
		R_L = 32Ω, BTL P_{OUT} = 65W, BW = 22Hz to 22kHz, A weighted				100		
Noise	V_n	BW = 22Hz to 22kHz				20.4		$µV_{RMS}$
Capacitive-Load Drive	C_L	No sustained oscillations				200		pF
Crosstalk		L to R, R to L, f = 10kHz				60		dB
Slew Rate	SR					1.4		V/µs
Gain (Maximum Volume Settings) (Note 6)	$A_{VMAX(HP)}$	GAIN2 = 0, HPS = 1				0		dB
		GAIN2 = 1, HPS = 1				3.0		
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A weighted (Note 4)		Into shutdown		62		dBV
				Out of shutdown		50		

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0, $\overline{SHDN}$ = V_{DD}, REGEN = V_{DD}, DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, speaker loads terminated between OUT_+ and OUT_-, headphone load terminated between HP_ and GND, GAIN1 = GAIN2 = GAIN3 = VOL = 0 ($A_{V(SP)}$ = 15dB, $A_{V(HP)}$ = 0dB), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE PUMP						
Charge-Pump Frequency	f_{OSC}		500	550	600	kHz
VOLUME CONTROL						
VOL Input Impedance	R_{VOL}			100		MΩ
VOL Input Hysteresis				10		mV
Full Mute Voltage		(Note 7)		0.858 x HPV_{DD}		V
Full Mute Attenuation		f_{IN} = 1kHz		-85		dB
Input Impedance	$R_{VOL\_}$	Any gain setting		100		MΩ
Channel Matching		A_V = +15dB to 0dB		±0.2		dB
		A_V = -2dB to -20dB		±0.3		
		A_V = -22dB to -56dB		±1.0		
BEEP INPUT						
Beep Signal Amplitude Threshold		T_A = +25°C, R_B = 47kΩ (see *BEEP Input* section)	0.3			V
Beep Signal Frequency Threshold		T_A = +25°C	300			Hz
AUTOMATIC LEVEL CONTROL SPEAKER AMPLIFIER (MAX9756/MAX9757)						
PREF Threshold Accuracy		R_{PREF} = 180kΩ		5	8.1	%
Maximum Gain Compression			6.0	6.3		dB
Attack Time		C_T = 1µF (Note 8)		15		ms
Hold Time		Time between attack and release phases		50		ms
Release Time (Note 9)		C_T = 1µF, release from 6dB; 0V < V_{DR} < (0.3V x V_{DD})		30		s
		C_T = 1µF, release from 6dB; 0.4V < V_{DR} < (0.6V x V_{DD})		9.5		
		C_T = 1µF, release from 6dB; 0.8V < V_{DR} < V_{DD}		3		
DR INPUT (TRI-STATE INPUT)						
DR Input Voltage High	V_{DRH}		0.8 x V_{DD}		V_{DD}	V
DR Input Voltage Middle	V_{DRM}		0.4 x V_{DD}		0.6 x V_{DD}	V
DR Input Voltage Low	V_{DRL}		0		0.3 x V_{DD}	V
Input Leakage Current		0V ≤ V_{DR} ≤ V_{DD}			±1	µA
LOGIC INPUTS (GAIN_, $\overline{SHDN}$, REGEN)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}				±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0, $\overline{SHDN}$ = V_{DD}, REGEN = V_{DD}, DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, speaker loads terminated between OUT_+ and OUT_-, headphone load terminated between HP_ and GND, GAIN1 = GAIN2 = GAIN3 = VOL = 0 ($A_{V(SP)}$ = 15dB, $A_{V(HP)}$ = 0dB), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUT HEADPHONE (HPS)							
Input High Voltage	V_{IH}			2			V
Input Low Voltage	V_{IL}					0.8	V
HPS Pullup Current					35		µA
LOW-DROPOUT LINEAR REGULATOR							
Input Voltage Range	V_{IN}	Inferred from line regulation		3.5		5.5	V
Supply (Ground) Current	I_Q	I_{OUT} = 0mA, $\overline{SHDN}$ = GND			100	160	µA
		I_{OUT} = 150mA			350		
Shutdown Current	I_{SHDN}	REGEN = 0V			0.1	3	µA
Output Current	I_{OUT}			150			mA
Fixed Output Voltage Accuracy		I_{OUT} = 1mA				±1.5	%
Adjustable Output Voltage Range				V_{SET}		4.85	V
SET Reference Voltage	V_{SET}			1.19	1.21	1.23	V
SET Dual-Mode Threshold					200		mV
SET Input Leakage Current	I_{SET}				±20	±500	nA
Dropout Voltage (Note 10)	ΔV_{OD}	V_{OUT} = 4.65V (fixed output operation)	I_{OUT} = 50mA		25	50	mV
			I_{OUT} = 150mA		100	150	
Output Current Limit	I_{LIM}				300		mA
Startup Time					20		µs
Line Regulation		V_{IN} = 3.5V to 5.5V, V_{OUT} = 2.5V, I_{OUT} = 1mA		-0.1	+0.01	+0.1	%/V
Load Regulation		V_{OUT} = 4.65V, 1mA < I_{OUT} < 150mA			0.5		%
Ripple Rejection		V_{RIPPLE} = 200mV_{P-P}	f = 1kHz		60		dB
			f = 10kHz		50		
Output Voltage Noise		20Hz to 22kHz, C_{OUT} = 2 x 1µF, I_{OUT} = 150mA, V_{OUT} = 4.65V			100		μV_{RMS}

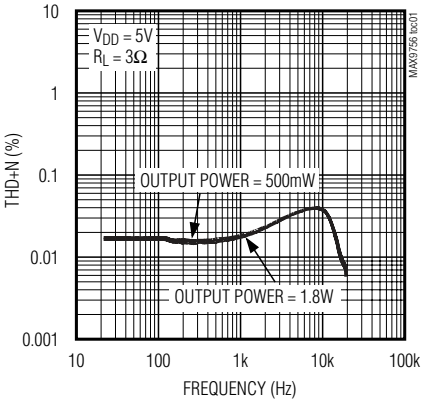
Note 1: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.
Note 2: PSRR is specified with the amplifier input connected to GND through R_{IN} and C_{IN}.
Note 3: Output power levels are measured with the TQFN's exposed paddle soldered to the ground plane.
Note 4: Speaker path gain is defined as: A_{VSPKR} = (V_{OUT+} - V_{OUT-})/$V_{IN\_\_}$).
Note 5: Speaker mode testing performed with 8Ω resistive load connected across BTL output. Headphone mode testing performed with 32Ω resistive load connected between HP_ and GND. Mode transitions are controlled by $\overline{SHDN}$.
Note 6: Headphone path gain is defined as: A_{VHP} = $V_{HP\_}$/$V_{IN\_\_}$.
Note 7: See Table 3 for detains on the mute levels.
Note 8: Attack envelope is exponential. Attack time is defined as the 15 x 10^3 x C_T.
Note 9: Time for the gain to return to within 10% of nominal gain setting after the input signal has fallen below the PREF threshold. Release is linear in dB. Release time is proportional to magnitude of gain compression.
Note 10: Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} for V_{IN} = $V_{OUT(NOM)}$ + 1V.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

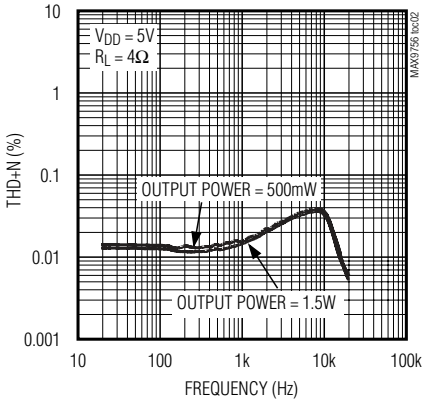
Typical Operating Characteristics

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

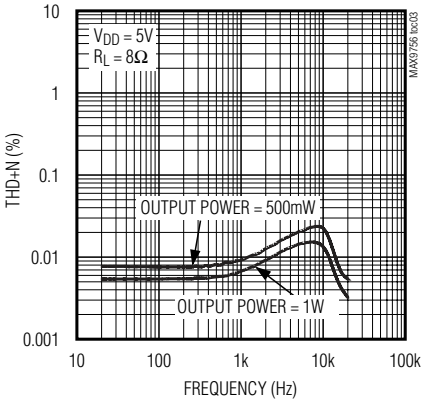
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



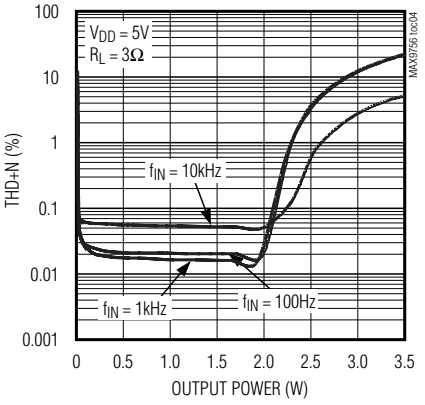
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



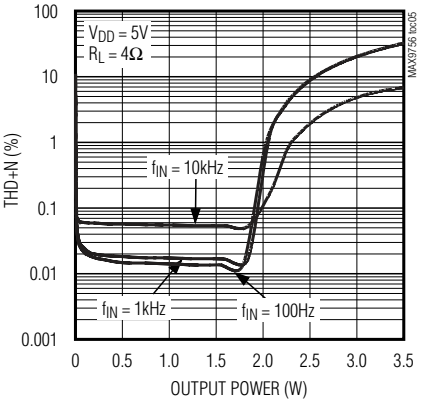
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



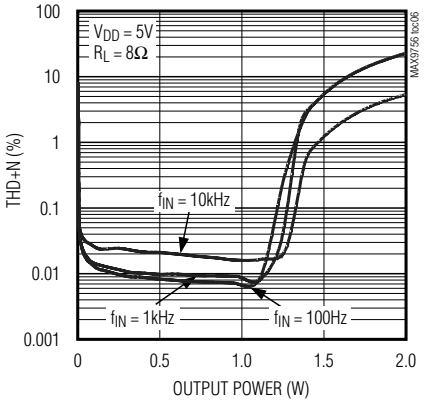
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



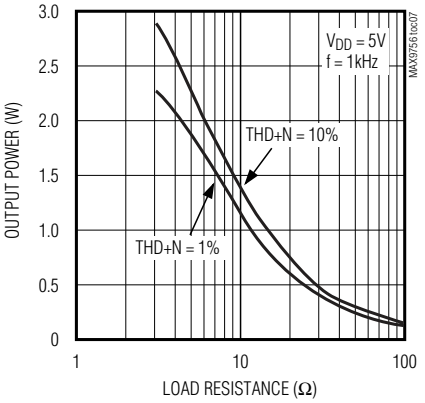
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



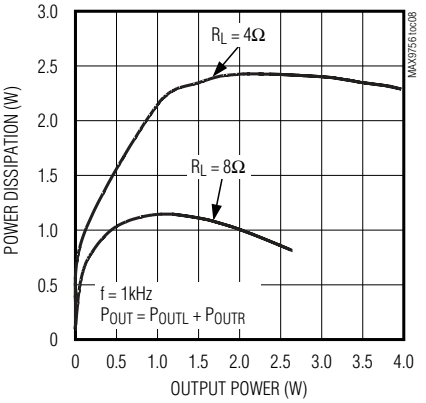
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



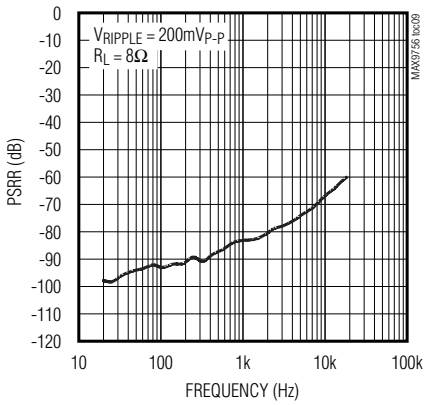
OUTPUT POWER vs. LOAD RESISTANCE (SPEAKER MODE)



POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



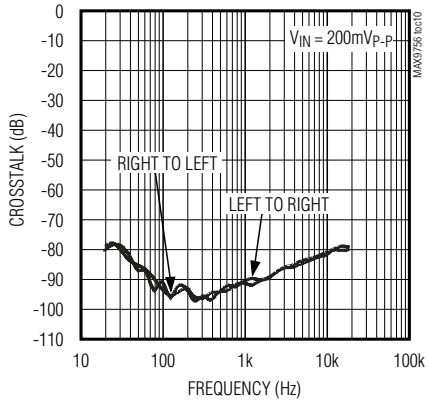
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPEAKER MODE)



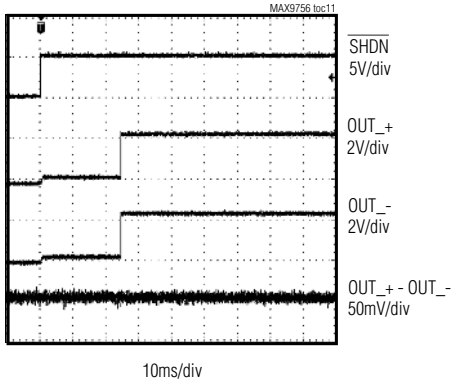
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

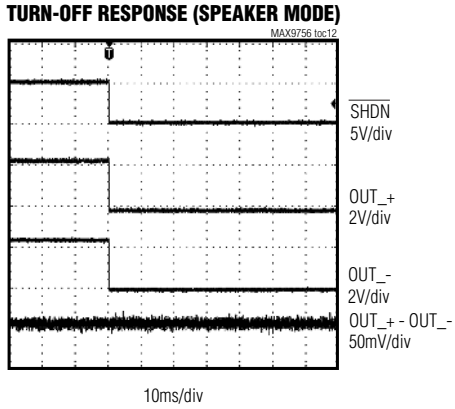
CROSSTALK vs. FREQUENCY (SPEAKER MODE)



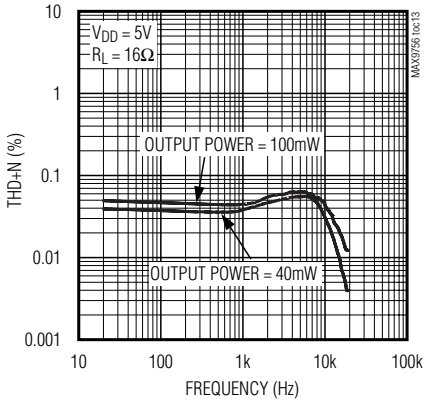
TURN-ON RESPONSE (SPEAKER MODE)



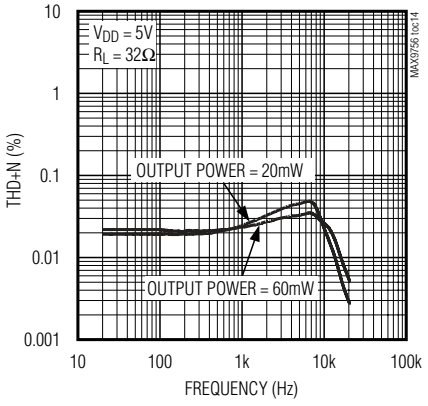
TURN-OFF RESPONSE (SPEAKER MODE)



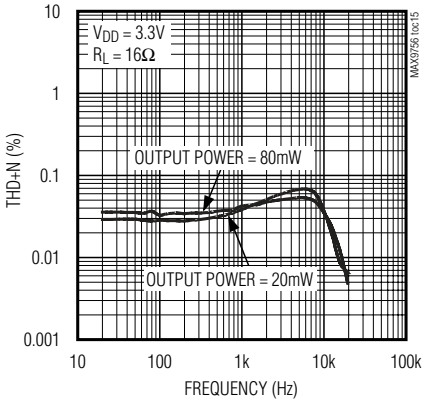
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



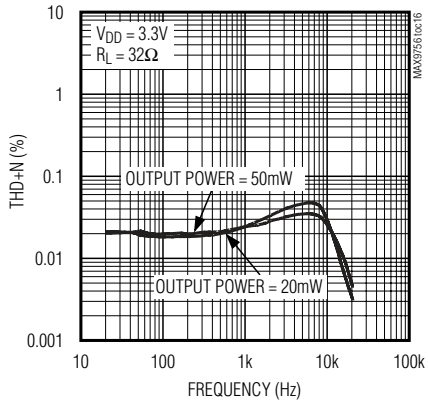
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



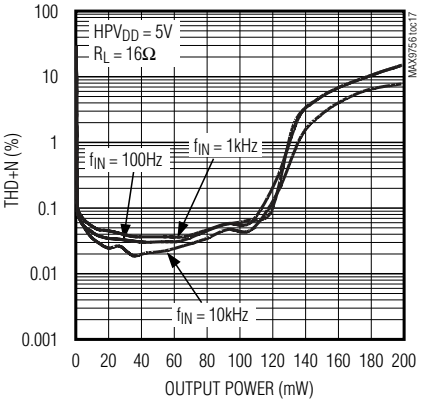
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



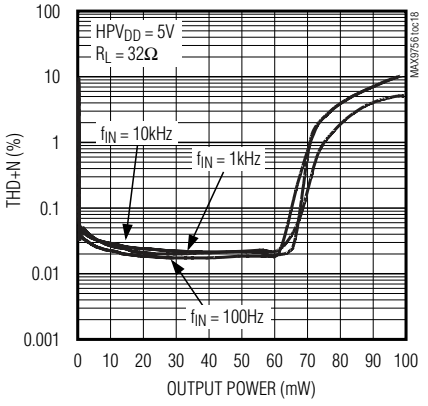
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)

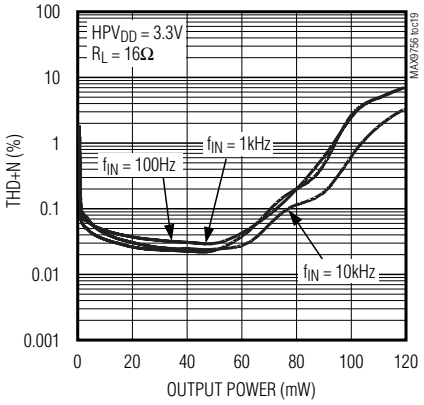


2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

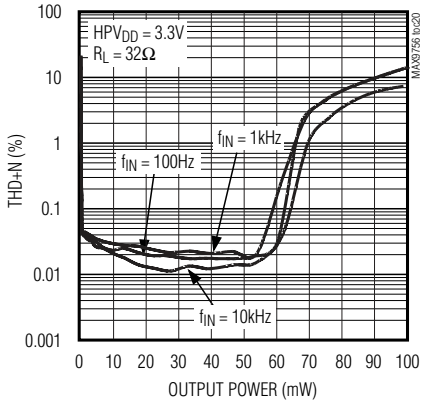
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

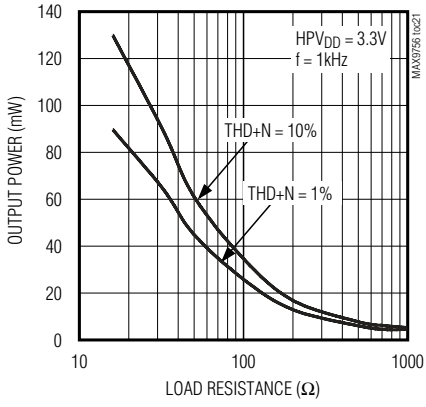
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



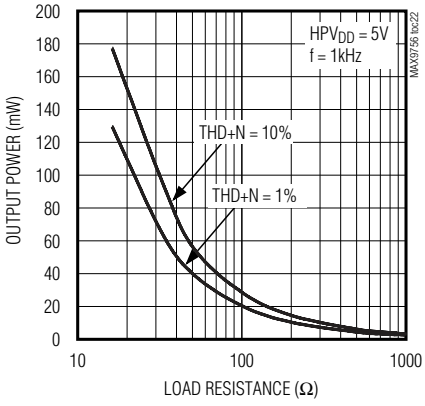
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



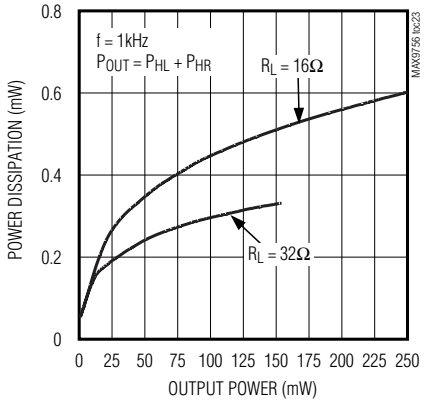
OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



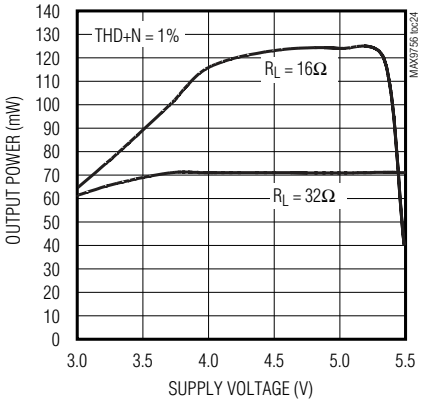
OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



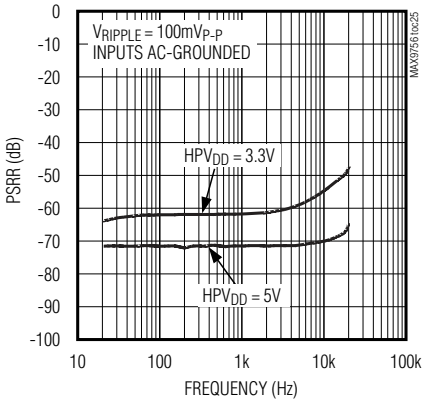
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



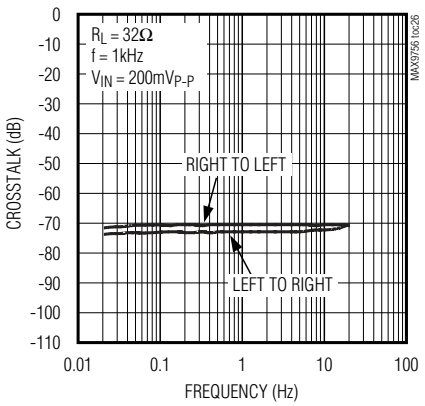
OUTPUT POWER vs. SUPPLY VOLTAGE (HEADPHONE MODE)



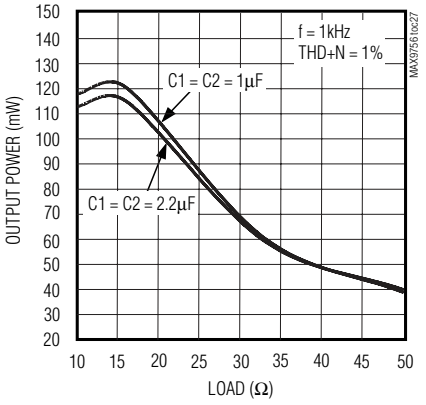
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (HEADPHONE MODE)



CROSSTALK vs. FREQUENCY (HEADPHONE MODE)



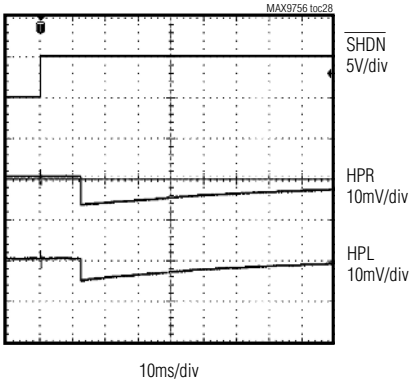
OUTPUT POWER vs. CHARGE-PUMP CAPACITANCE (HEADPHONE MODE)



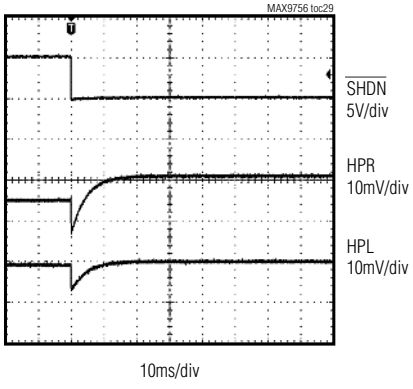
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

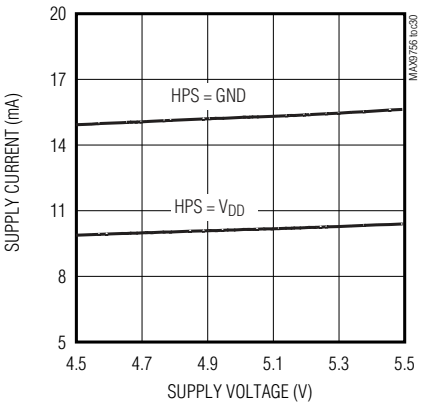
TURN-ON RESPONSE (HEADPHONE MODE)



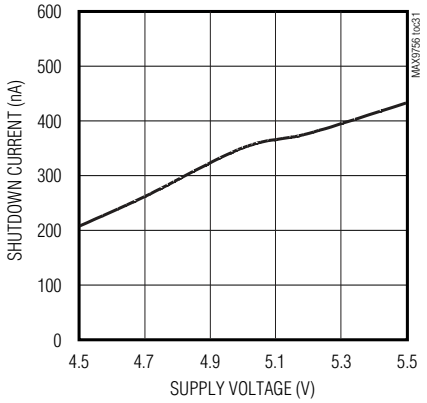
TURN-OFF RESPONSE (HEADPHONE MODE)



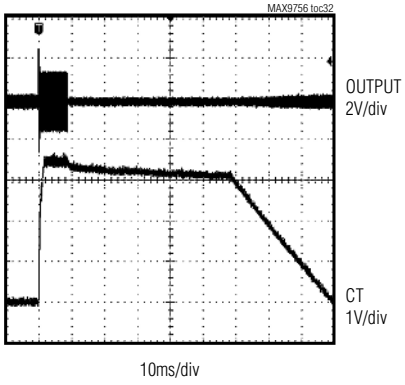
SUPPLY CURRENT vs. SUPPLY VOLTAGE



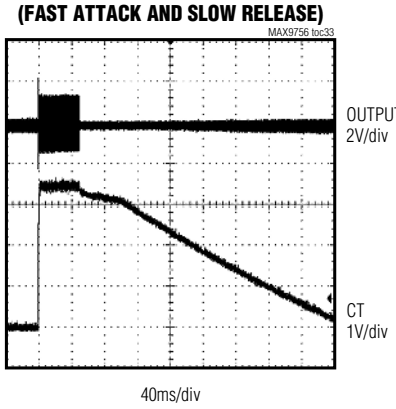
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



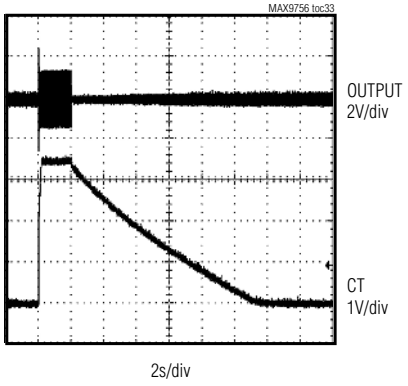
POWER LIMITING OF SINE BURST (FAST ATTACK AND FAST RELEASE)



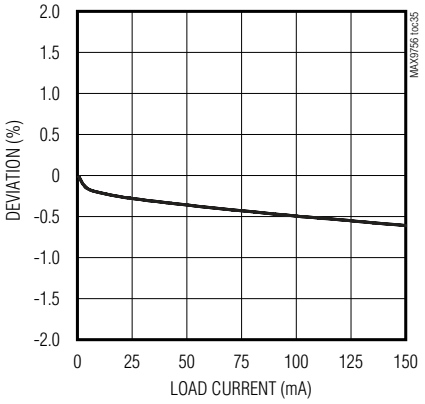
POWER LIMITING OF SINE BURST (FAST ATTACK AND SLOW RELEASE)



POWER LIMITING OF SINE BURST (SLOW ATTACK AND SLOW RELEASE)



LDO OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT

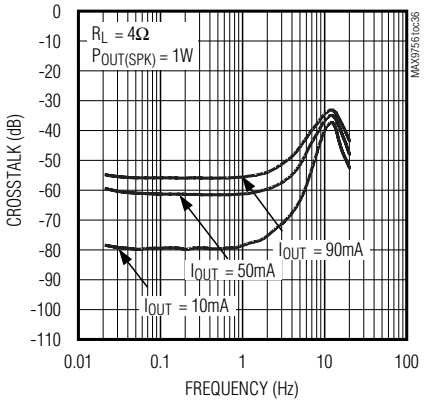


2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

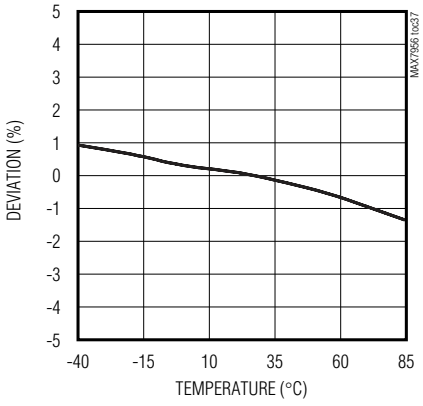
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

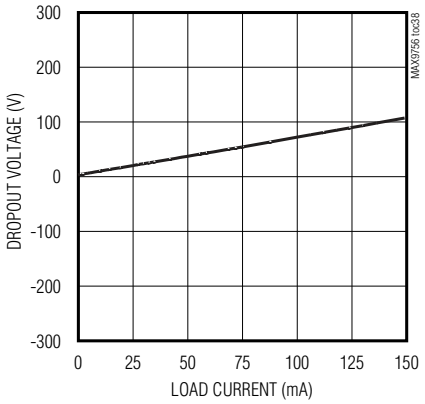
CROSSTALK vs. FREQUENCY (LDO)



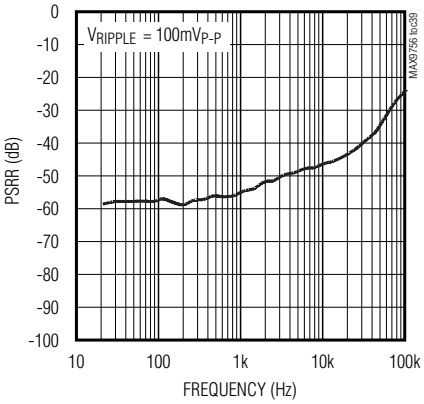
LDO OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE



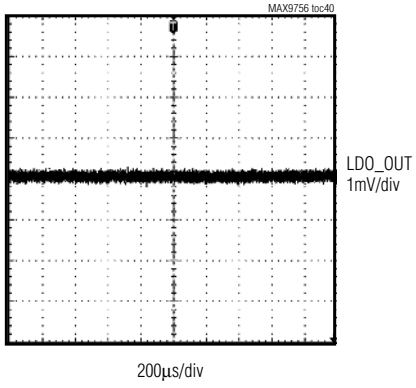
DROPOUT VOLTAGE vs. LOAD CURRENT



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LDO)



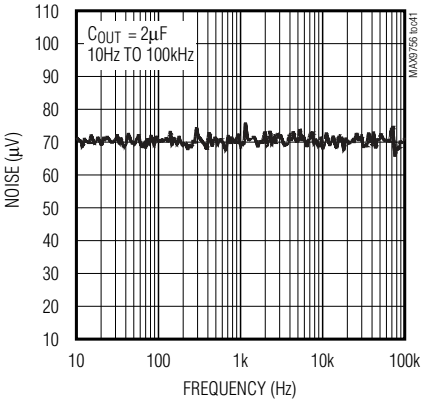
LDO OUTPUT NOISE



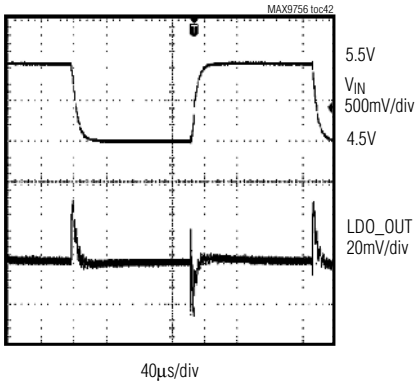
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = HPV_{DD} = CPV_{DD} = IN = +5.0V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, REGEN = DR = SET = GND, C_{BIAS} = 1µF, C_{PVSS} = 1µF, C1 = C2 = 1µF, PREF = unconnected, GAIN1 = 1, GAIN2 = GAIN3 = VOL = 0V, measurement BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

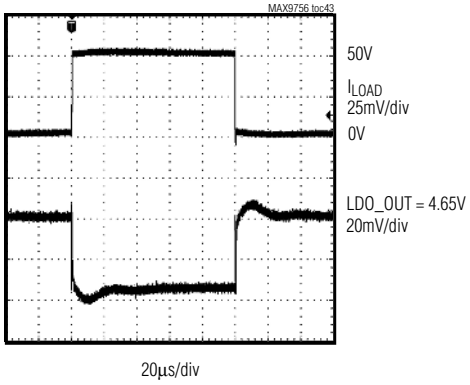
OUTPUT NOISE vs. FREQUENCY (LDO)



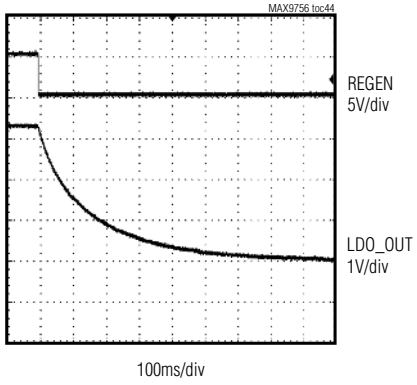
LINE-TRANSIENT RESPONSE



LOAD-TRANSIENT RESPONSE



LDO SHUTDOWN RESPONSE



Pin Description

PIN			NAME	FUNCTION
MAX9756	MAX9757	MAX9758		
1	32	32	INL	Left-Channel Audio Input
2	1	1	GAIN1	Gain Control Input 1
3	2	2	GAIN2	Gain Control Input 2
4	3	3	GAIN3	Gain Control Input 3
5	4	4	BEEP	Audible Alert Beep Input
6, 22	5, 21	5, 21	PGND	Power Ground
7	6	6	OUTL+	Left-Channel Positive Speaker Output
8	7	7	OUTL-	Left-Channel Negative Speaker Output
9,19	8,18	8, 18	PV_{DD}	Speaker Amplifier Power Supply. Bypass with 1µF ceramic capacitor to PGND.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

Pin Description (continued)

PIN			NAME	FUNCTION
MAX9756	MAX9757	MAX9758		
10	9	9	CPV_{DD}	Charge-Pump Power Supply. Bypass with 1µF ceramic capacitor to CPGND.
11	10	10	C1P	Charge-Pump Flying-Capacitor Positive Terminal. Connect a 1µF capacitor from C1P to C1N.
12	11	11	CPGND	Charge-Pump Ground
13	12	12	C1N	Charge-Pump Flying-Capacitor Negative Terminal. Connect a 1µF capacitor from C1P to C1N.
14	13	13	CPV_{SS}	Charge-Pump Negative Output. Connect to V_{SS}.
15	14	14	V_{SS}	Headphone Amplifier Negative Power Supply. Bypass with 1µF ceramic capacitor to GND.
16	15	15	HPR	Right Headphone Output
17	16	16	HPL	Left Headphone Output
18	17	17	HPV_{DD}	Headphone Positive Power Supply. Bypass with 1µF ceramic capacitor to GND.
20	19	19	OUTR-	Right-Channel Negative Speaker Output
21	20	20	OUTR+	Right-Channel Positive Speaker Output
23	22	22	HPS	Headphone Sense Input. Leave HPS unconnected if automatic headphone sensing is not used.
24	—	23	REGEN	LDO Enable. Connect REGEN to V_{DD} to enable the LDO. Connect to GND to disable LDO.
25	23	—	DR	Automatic Level Control Attack to Release Time Ratio Select. Hardwired to V_{DD}, GND, or BIAS to set the attack to release ratio; see the *ALC* section.
26	24	24	BIAS	Common-Mode Bias Voltage. Bypass with a 1.0µF capacitor to GND.
27	25	25	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to disable the audio amplifiers. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
28	26	26	VOL	Analog Volume Control Input
29	27	—	PREF	Power-Limiting Input. Connect a resistor from PREF to GND to set the speaker output clamping level. Leave PREF unconnected to disable ALC; see the *ALC section.*
30	—	27	SET	Regulator Feedback Input. Connect to GND for 4.65V fixed output. Connect to resistor-divider for adjustable output; see the *Low-Dropout Linear Regulator* section.
31	28	28	GND	Ground
32	29	—	V_{DD}	Power Supply
33	—	—	IN	LDO Input. Bypass with two 1µF ceramic capacitors to GND.
34	—	30	OUT	LDO Output. Bypass with two 1µF ceramic capacitors to GND.
35	30	—	CT	Automatic Level Control Attack and Release Timing Capacitor. Connect CT to GND to disable ALC; see the *ALC section.*
36	31	31	INR	Right-Channel Audio Input
—	—	29	V_{DD}	Power-Supply and LDO Input. Bypass with two 1µF ceramic capacitors to GND.
EP	EP	EP	EP	Exposed Pad. The external pad lowers the package's thermal impedance by providing a direct-heat conduction path from the die to the PC board. **Connect the exposed thermal pad to GND.**

Detailed Description

The MAX9756/MAX9757/MAX9758 combine dual, 2W BTL stereo audio power amplifiers with a DirectDrive headphone amplifier in a single device. The stereo power amplifiers deliver up to 2.3W per channel into a 3Ω speaker from a 5V supply and the stereo headphone amplifiers deliver up to 130mW per channel into a 16Ω headphone from a 5V supply.

The MAX9756/MAX9757 feature ALC that automatically controls output power to the speaker, preventing loudspeaker, overload and provides optimized dynamic range.

The MAX9756/MAX9757/MAX9758 feature 31-step analog volume control and a BEEP input. The amplifier gain is pin programmable. These devices feature click-and-pop suppression, eliminating the need for discrete muting circuitry. Speaker and headphone outputs have short-circuit and thermal protection.

The MAX9756/MAX9758s' internal LDO features Maxim's Dual Mode™ feedback. The LDO output voltage is either fixed at 4.65V (SET = GND), or adjusted between 1.23V and 5V using a resistive divider at SET. The LDO delivers up to 150mA of continuous current, and can be enabled independently from the audio amplifiers. Short-circuit and thermal-overload protection are provided for the LDO.

All devices feature a single-supply voltage, a shutdown mode, logic-selectable gain, and a headphone sense input. Industry-leading click-and-pop suppression eliminates audible transients during power and shutdown cycles.

Each signal path consists of an input amplifier that sets the signal-path gain and feeds both the speaker and headphone amplifiers (Figure 1). The speaker amplifier uses a BTL architecture, doubling the voltage drive to the speakers and eliminating the need for DC-blocking capacitors. The output consists of two signals, identical in magnitude, but 180° out of phase.

The headphone amplifiers use Maxim's DirectDrive architecture that eliminates the bulky output DC-blocking capacitors required by traditional headphone amplifiers. A charge pump inverts the positive supply (CPV_{DD}), creating a negative supply (CPV_{SS}). The headphone amplifiers operate from these bipolar supplies with their outputs biased about GND (Figure 2).

The amplifiers have almost twice the supply range compared to other single-supply amplifiers, nearly quadrupling the available output power. The benefit of the GND bias is that the amplifier outputs do not have a DC component (typically $V_{DD}/2$). This eliminates the large DC-blocking capacitors required with conventional headphone amplifiers, conserving board space and system cost while improving frequency response.

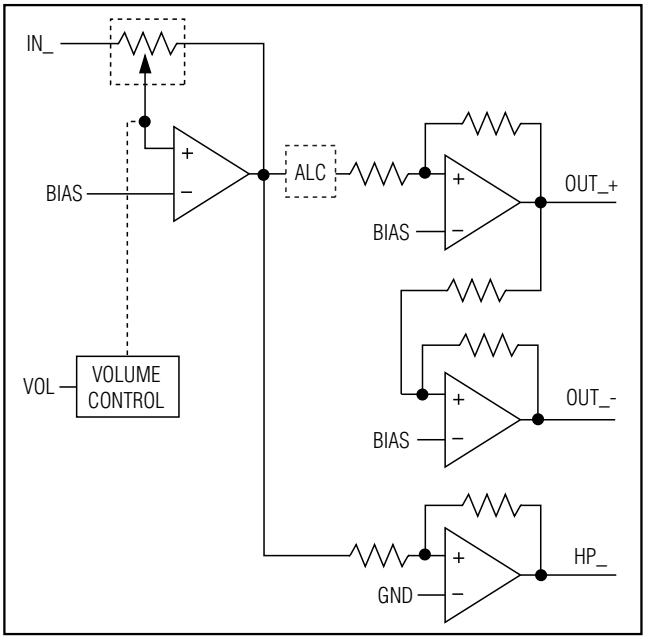


Figure 1. MAX9756/MAX9757 Signal Path

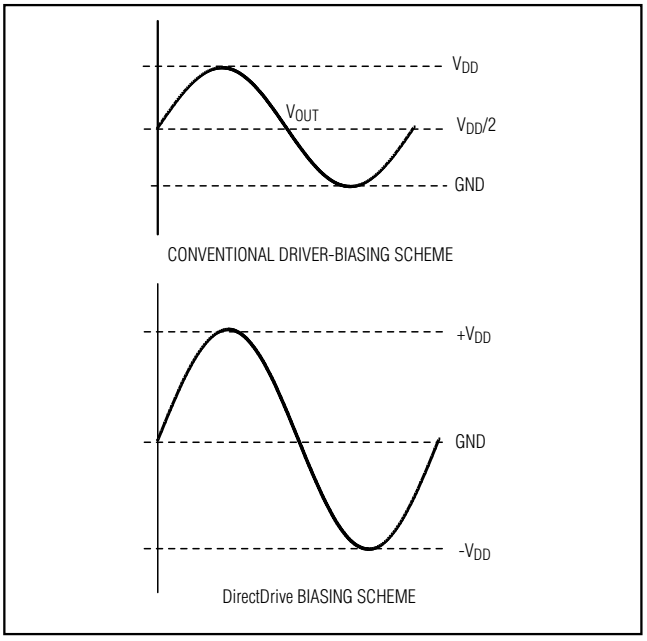


Figure 2. Traditional Headphone Amplifier Output Waveform vs. DirectDrive Headphone Amplifier Output Waveform

Dual Mode is a trademark of Maxim Integrated Products, Inc.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

The MAX9756/MAX9757/MAX9758 feature an undervoltage lockout that prevents operation from an insufficient power supply and click-and-pop suppression that eliminates audible transients on startup and shutdown. The amplifiers include thermal-overload and short-circuit protection. An additional feature of the amplifiers is that there is no phase inversion from input to output.

Automatic Level Control (ALC)

Two-watt amplifiers are commonly used in notebook PCs (almost always powered from a 5V supply). With an 8Ω speaker driven from a BTL amplifier, the maximum theoretical continuous power available is:

$$P_{OUT} = \frac{\left(\frac{V_{PEAK}}{\sqrt{2}}\right)^2}{R_{SPEAKER}} = \frac{\left(\frac{5}{\sqrt{2}}\right)^2}{8} = 1.56W$$

See Figure 5 for suggested ALC component values. The ALC feature offers two benefits:

1) To limit amplifier power to protect a loudspeaker.
2) To make input signals with a wide dynamic range more intelligible by boosting low-level signals without distorting the high-level signals.

A device without ALC experiences clipping at the output when too much gain is applied to the input. ALC prevents clipping at the output when too much gain is applied to the input, eliminating output clipping. Figure 3 shows a comparison of an overgained speaker input with and without ALC.

The MAX9756/MAX9758 control the gain to the speakers by first detecting that the output voltage to the speaker has exceeded a preset limit. The speaker amplifier gain is rapidly reduced to correct for the excessive output power. This process is known as the attack time. When the signal subsequently lowers in amplitude, the gain is held at the reduced state for a short period before slowly increasing to the normal value. This process is known as the hold and release time. The speed at which the amplifiers adjust to changing input signals is set by the external timing capacitor C_{CT} and the setting of logic input DR. The output power limit can be set by adjusting the value of the external resistor connected to PREF. Gain reduction is a function of input signal amplitude with a maximum ALC attenuation of 6dB. Figure 4 shows the effect of an input burst exceeding the preset limit, output attack, hold and release times.

This process (referred to as "limiting" in audio) limits the amplifier output power so loudspeaker overload can be prevented. If the attack and release times are configured to respond too fast, audible artifacts often, described as "pumping" or "breathing," can occur as the gain is rapidly adjusted to follow the dynamics of the signal. For best results, adjust the time constant of the ALC to accommodate the source material. Notebook applications in which music CDs and DVDs are the main audio source, a 495µs attack time with a 990ms release time is recommended with a 1.2W output into an 8Ω load.

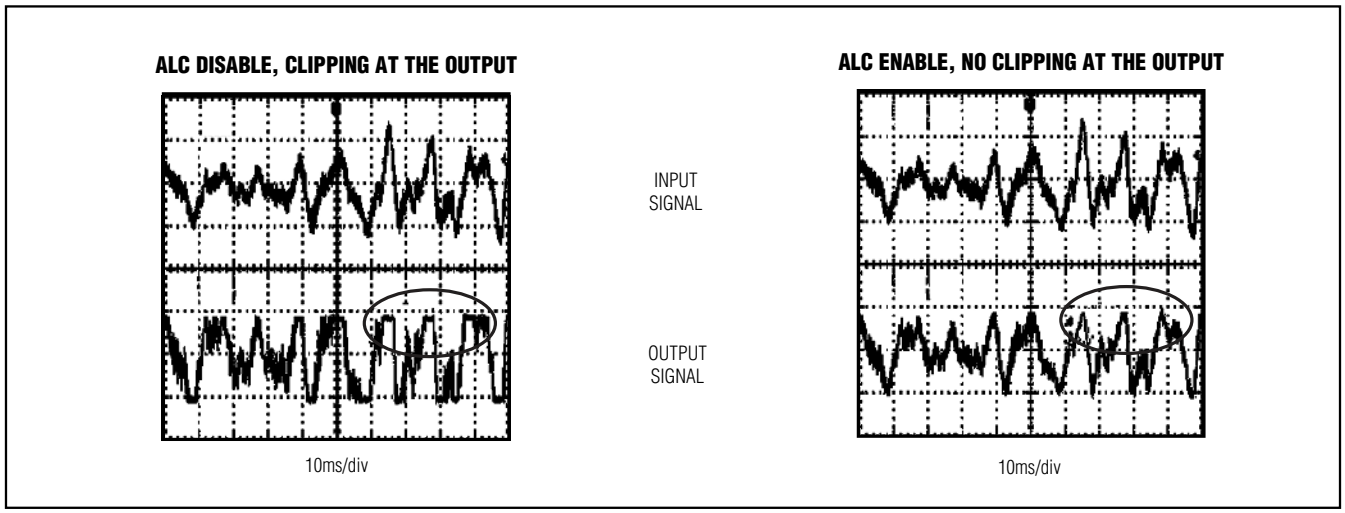


Figure 3. ALC Disabled vs. ALC Enabled

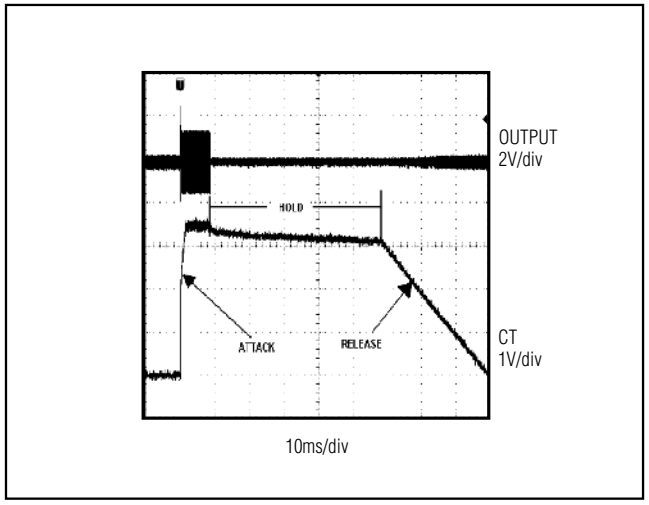


Figure 4. Attack, Hold, and Release Time

Attack Time

The attack time is the time it takes to reduce the gain after the input signal has exceeded the threshold level. Suggested attack time range is from 150µs to 50ms. The gain attenuation in attack is exponential and the attack time is defined as one time constant. The time constant of the attack is given by 15,000 x C_{CT} seconds (where C_{CT} is the external timing capacitor).

- Use a short attack time for the ALC to react quickly to transient signals, such as snare drum beats (music) or gun shots (DVD). Fast attack times can lead to gain "pumping" where rapid ALC action can be heard reacting to dynamic material.
- Use a longer attack time to allow the ALC to ignore short-duration peaks and only reduce the gain when a noticeable increase in loudness occurs. Short-duration peaks are not reduced, but louder passages are. This allows the louder passages to be reduced in volume, thereby maximizing output dynamic range. Having the attack time too long can possibly result in some damage to the loudspeaker under harsh conditions.

Hold Time

Hold time is the delay after the signal falls below the threshold level before the release phase is initiated. Hold time is internally set to 50ms and nonadjustable. The hold time is cancelled by any signal exceeding the set threshold level and attack is reinitiated.

Release Time

The release time is how long it takes for the gain to return to its normal level after the input signal has fallen below the threshold level and 50ms hold time has expired. Release time is defined as release from a 6dB gain compression to 10% of the nominal gain setting after the input signal has fallen below PREF threshold and the 50ms hold time has expired. Release time is adjustable between 95ms and 10s. The release time is set by picking an attack time using C_{CT} and setting the attack to release time ratio by configuring DR as shown in Table 2. Release time is linear in dB with time and is inversely proportional to the magnitude of gain compression:

- Use a small ratio to maximize the speed of the ALC.
- Use a large ratio to maximize the sound quality and prevent repeated excursions above the threshold from being independently adjusted by the ALC.

Release and attack times are set by selecting the capacitance value between CT and GND, and by setting the logic state of DR (Table 1). DR is a tristate logic input that sets the attack-to-release time ratio. A fixed hold time of 50ms is internally added to the release time.

Table 1. Attack and Release Time

TIMING CAPACITOR (C_{CT})	ATTACK TIME	RELEASE TIME		
	DR = 'X'	DR = V_{DD}	DR = V_{BIAS}	DR = GND
10nF	150µs	30ms	95ms	300ms
33nF	**495µs**	**99ms**	**313ms**	**990ms**
100nF	1.5ms	300ms	950ms	3s
330nF	4.95ms	990ms	3.1s	9.9s
1µF	15ms	3s	9.5s	—
2.2µF	33ms	6.6s	—	—
3.3µF	49.5ms	10s	—	—

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

The release/attack time ratio that can be achieved by programming DR is listed in Table 2.

Table 2. Release to Attack Ratio

DR	RELEASE/ATTACK RATIO
V_{DD}	200
V_{BIAS}	633
GND	2000

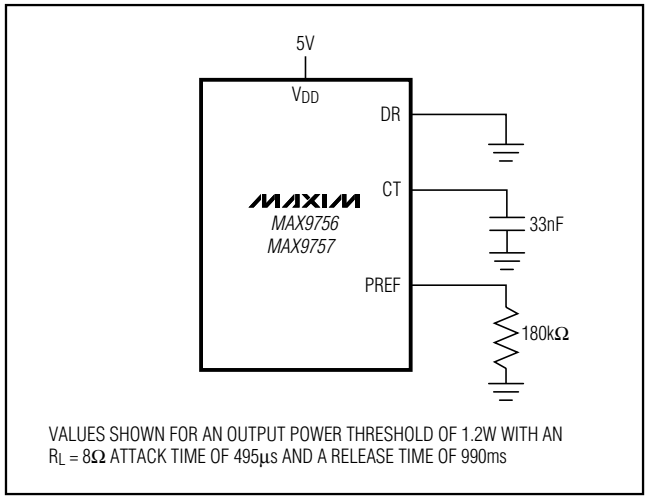


Figure 5. Recommended Output Power Threshold, Attack, and Release Time Components

Output Power Threshold

To set the threshold at which speaker output is clamped, an external resistor must be connected from PREF to ground. The suggested external resistor range is from 100kΩ to 200kΩ (for best results use a 1% resistor). Leaving PREF unconnected disables the ALC function. A constant current of 12µA is sourced at PREF, so that a 180kΩ resistor results in 1.2W clamp limit on an 8Ω load and a 200kΩ resistor results in a 1.5W clamp limit on an 8Ω load (Figure 6).

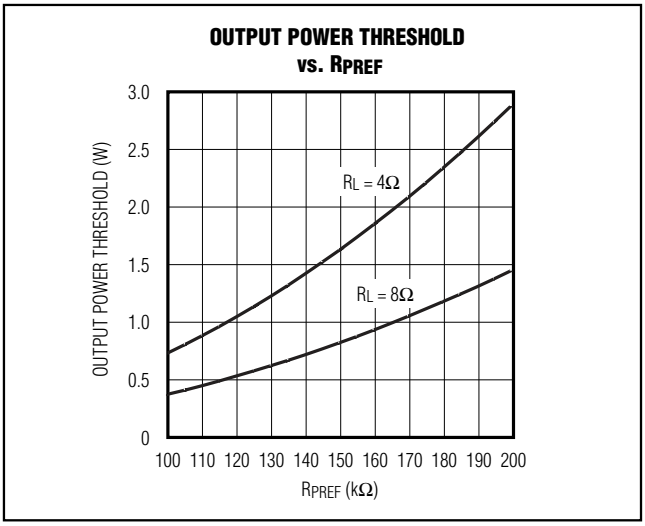


Figure 6. Output Power Threshold vs. RPREF

Use the following equation to choose the value for R_{PREF} for the desired maximum output power level based on a sine wave input:

$$R_{PREF} = 180k\Omega \left(\left(\sqrt{\frac{P_{OUT}}{1.166}} \right) \times \left(\sqrt{\frac{R_L}{8}} \right) \right)$$

Gain Selection

The MAX9756/MAX9757/MAX9758 feature an internally set, selectable gain. The GAIN1, GAIN2, and GAIN3 inputs set the maximum gain for the speaker and headphone amplifiers (Table 3). The gain of the device can vary based upon the voltage at VOL but does not exceed the maximum gain listed below (see the *Analog Volume (VOL) Control* section).

Table 3. Maximum Gain Settings

GAIN3	GAIN2	GAIN1	SPEAKER MODE GAIN (dB)	HEADPHONE MODE GAIN (dB)
0	0	0	+15	0
0	0	1	+16.5	0
0	1	0	+18	+3
0	1	1	+19.5	+3
1	0	0	+21	0
1	0	1	+22.5	0
1	1	0	+24	+3
1	1	1	+25.5	+3

Analog Volume Control (VOL)

The MAX9756/MAX9757/MAX9758 feature an analog volume control that varies the gain of the device in 31 discrete steps based upon the DC voltage applied to VOL (see Table 4). The input range of VOL is from 0 (full volume) to HPV_{DD} (full mute), with example step sizes shown in Table 3. Connect the reference of the device driving VOL (Figure 7) to HPV_{DD}. Connect VOL to GND (full volume) if volume control is not used.

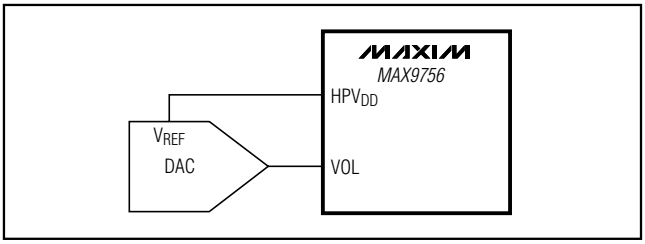


Figure 7. Volume Control Circuit

Table 4. Volume Levels

V_{VOL} (V) = MULTIPLIER x HPV_{DD}			SPEAKER MODE GAIN (dB)								HEADPHONE MODE GAIN (dB)	
MULTIPLIER	V_{VOL} (MIN)*	V_{VOL} (MAX)*	GAIN3 = 0 GAIN2 = 0 GAIN1 = 0	GAIN3 = 0 GAIN2 = 0 GAIN1 = 1	GAIN3 = 0 GAIN2 = 1 GAIN1 = 0	GAIN3 = 0 GAIN2 = 1 GAIN1 = 1	GAIN3 = 1 GAIN2 = 0 GAIN1 = 0	GAIN3 = 1 GAIN2 = 0 GAIN1 = 1	GAIN3 = 1 GAIN2 = 1 GAIN1 = 0	GAIN3 = 1 GAIN2 = 1 GAIN1 = 1	GAIN3 = X GAIN2 = 0 GAIN1 = X	GAIN3 = X GAIN2 = 1 GAIN1 = X
0.07	0.00	0.49	15	16.5	18	19.5	21	22.5	24	25.5	0	3
0.16	0.49	0.57	14	16	17.5	19	20	22	23.5	25	-1	2.5
0.18	0.57	0.64	13	15	17	18.5	19	21	23	24.5	-2	2
0.21	0.64	0.72	12	14	16.5	18	18	20	22.5	24	-3	1.5
0.23	0.72	0.80	10	13	16	17.5	16	19	22	23.5	-5	1
0.25	0.80	0.88	8	12	15	17	14	18	21	23	-7	0
0.28	0.88	0.95	6	10	14	16.5	12	16	20	22.5	-9	-1
0.30	0.95	1.03	4	8	13	16	10	14	19	22	-11	-2
0.32	1.03	1.11	2	6	12	15	8	12	18	21	-13	-3
0.35	1.11	1.19	0	4	10	14	6	10	16	20	-15	-5
0.37	1.19	1.26	-2	2	8	13	4	8	14	19	-17	-7
0.39	1.26	1.34	-4	0	6	12	2	6	12	18	-19	-9
0.42	1.34	1.42	-6	-2	4	10	0	4	10	16	-21	-11
0.44	1.42	1.50	-8	-4	2	8	-2	2	8	14	-23	-13
0.46	1.50	1.57	-10	-6	0	6	-4	0	6	12	-25	-15
0.49	1.57	1.65	-12	-8	-2	4	-6	-2	4	10	-27	-17
0.51	1.65	1.73	-14	-10	-4	2	-8	-4	2	8	-29	-19
0.54	1.73	1.80	-16	-12	-6	0	-10	-6	0	6	-31	-21
0.56	1.80	1.88	-18	-14	-8	-2	-12	-8	-2	4	-33	-23
0.58	1.88	1.96	-20	-16	-10	-4	-14	-10	-4	2	-35	-25
0.61	1.96	2.04	-22	-18	-12	-6	-16	-12	-6	0	-37	-27
0.63	2.04	2.11	-24	-20	-14	-8	-18	-14	-8	-2	-39	-29
0.65	2.11	2.19	-26	-22	-16	-10	-20	-16	-10	-4	-41	-31
0.68	2.19	2.27	-28	-24	-18	-12	-22	-18	-12	-6	-43	-33
0.70	2.27	2.35	-32	-26	-20	-14	-26	-20	-14	-8	-47	-35
0.72	2.35	2.42	-36	-28	-22	-16	-30	-22	-16	-10	-51	-37
0.75	2.42	2.50	-40	-32	-24	-18	-34	-26	-18	-12	-55	-39
0.77	2.50	2.58	-44	-36	-26	-20	-38	-30	-20	-14	-59	-41
0.79	2.58	2.66	-48	-40	-28	-22	-42	-34	-22	-15	-63	-43
0.82	2.66	2.73	-52	-44	-32	-24	-46	-38	-26	-18	-67	-47
0.84	2.73	2.81	-56	-48	-36	-26	-50	-42	-30	-20	-71	-51
0.93	2.81	3.30	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

**Based on HPV_{DD} = 3.3V.*

X = Don't care.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

Since the volume control (VOL) ADC is ratiometric to HPV_{DD}, any variations in HPV_{DD} are negated. The gain step sizes are not constant; the step sizes are 0.5dB/step at the upper extreme, 2dB/step in the midrange, and 4dB/step at the lower extreme. Figure 8 shows the transfer function of the volume control for a 3.3V supply.

Low-Dropout Linear Regulator

The MAX9756/MAX9758s' low-dropout linear regulator (LDO) can be used to provide a clean power supply to a CODEC or other circuitry. The LDO can be enabled independently of the audio amplifiers. REGEN enables/disables the LDO, set REGEN = V_{DD} to enable the LDO or set REGEN = GND to disable. The LDO is capable of providing up to 150mA continuous current and features Maxim's Dual Mode feedback. When SET is connected to GND, the output is internally set to approximately 4.65V. Adjust the output from 1.23V to 5V by connecting two external resistors, used as a voltage-divider, at SET (Figure 9).

The output voltage is set by the following equation:

$$V_{OUT} = V_{SET}\left(1+\frac{R1}{R2}\right)$$

where V_{SET} = 1.23V.

To simplify resistor selection:

$$R1 = R2\left(\frac{V_{OUT}}{V_{SET}}-1\right)$$

Since the input bias current at SET is nominally zero, large resistance values can be used for R1 and R2 to minimize power consumption without losing accuracy. Up to 1.5MΩ is acceptable for R2.

To minimize the current consumption, it is desirable to use high-value resistors (> 10kΩ for the external feedback divider (R1, R2). The input capacitance at SET and the stray and wiring capacitance should be compensated by placing a small capacitor (in the 10pF range) across the upper feedback resistor R1 (see Figure 9).

This capacitor creates a zero in the feedback loop to reduce overshoot. Overcompensation can cause poor stability in the high current range.

The regulator should be compensated with two 1µF ceramic capacitors connected between IN and GND and OUT and GND. X7R dielectric with 10% tolerance is recommended.

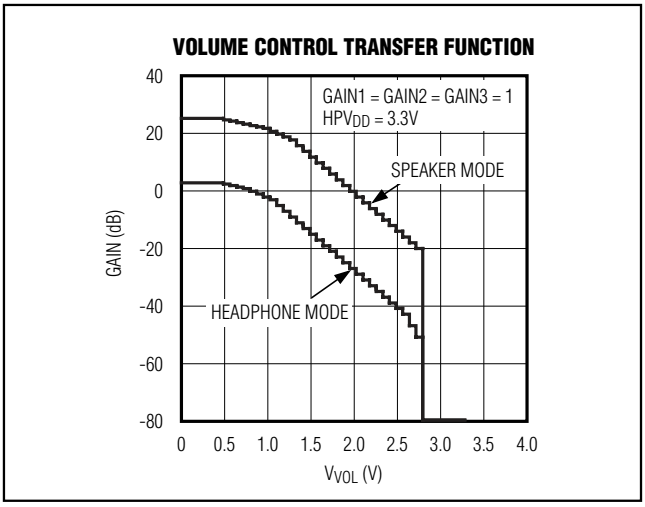


Figure 8. Volume Control Transfer Function

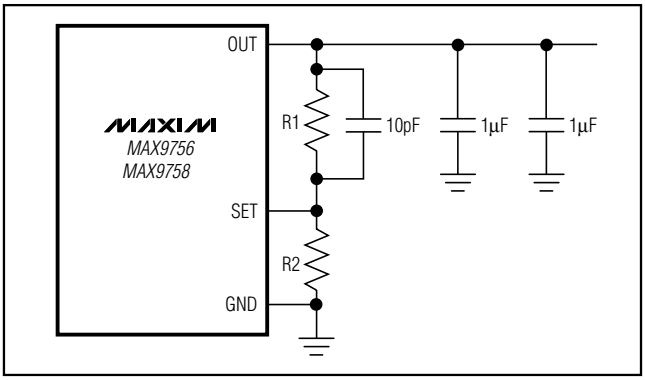


Figure 9. Adjustable Output Using External Feedback Resistors

The ESR of each capacitor should not exceed 40mΩ for good stability up to the full-rated current (150mA). Place the capacitors as close as possible to the device to limit the parasitic resistance and inductance. There is no upper limit to the amount of additional bypass capacitance.

DirectDrive Headphone Amplifier

Unlike the MAX9756/MAX9757/MAX9758, conventional single-supply headphone amplifiers typically have their outputs biased at half the supply voltage for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphones. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9756/MAX9757/MAX9758 headphone amplifier output to be biased at GND, almost doubling the dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large capacitors (220µF, typ), the MAX9756/MAX9757/MAX9758 charge pump requires only two small ceramic capacitors (1µF typ), conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance graph in the *Typical Operating Characteristics* for details of the possible capacitor values.

Low-Frequency Response

In addition to the cost and size disadvantages, the DC-blocking capacitors limit the low-frequency response of the amplifier. The impedance of the headphone load to the DC-blocking capacitor forms a highpass filter with the -3dB point determined by:

$$f-3dB = \frac{1}{2\pi R_L C_{OUT}}$$

where R_L is the impedance of the headphone and C_{OUT} is the value of the DC-blocking capacitor.

The highpass filter is required by conventional single-ended, single-supply headphone amplifiers to block the midrail DC component of the audio signal from the headphones. Depending on the -3dB point, the filter can attenuate low-frequency signals within the audio band. Larger values of C_{OUT} reduce the attenuation but are physically larger, more expensive capacitors. Figure 10 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16Ω headphone with a 100µF-blocking capacitor is 100Hz, well within the audio band.

Charge Pump

The MAX9756/MAX9757/MAX9758 feature a low-noise inverting charge pump to generate the negative rail necessary for DirectDrive headphone operation. The switching frequency is well beyond the audio range, and does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump minimizes the di/dt noise caused by the parasitic bond wire and trace inductance.

Headphone Sense Input (HPS)

The headphone sense input (HPS) monitors the headphone jack and automatically configures the MAX9756/MAX9757/MAX9758 based upon the voltage applied at HPS. A voltage of less than 0.8V enables the speaker amplifier. A voltage of greater than 2V disables the speaker amplifiers and enables the headphone amplifiers. For automatic headphone detection, connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 11. With no headphone present, the output impedance of the headphone amplifier pulls HPS low. When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact and HPS is pulled to V_{DD} with 35µA.

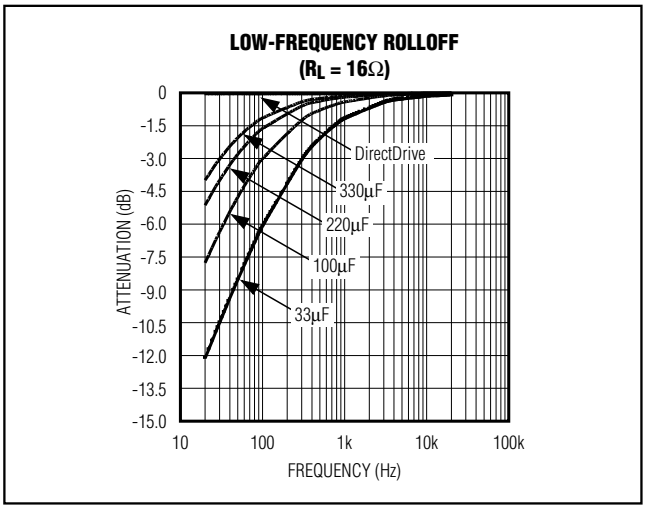


Figure 10. Low-Frequency Attenuation of Common DC-Blocking Capacitor Values

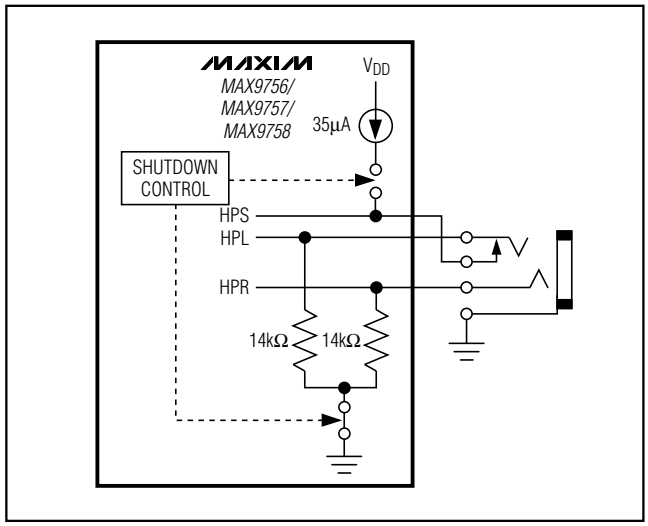


Figure 11. HPS Configuration

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

BIAS

The MAX9756/MAX9757/MAX9758 feature an internally generated, power-supply independent, common-mode bias voltage of 2.5V referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the amplifiers. Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. No external load should be applied to BIAS. Any load lowers the BIAS voltage, affecting the overall performance of the device.

BEEP Input

The MAX9756/MAX9757/MAX9758 feature an audible alert beep input (BEEP) that accepts a mono system alert signal and mixes it into the stereo audio path. When the amplitude of V_{BEEP} exceeds $300mV_{P-P}$ and the frequency of the beep signal is greater than 300Hz, the beep signal is mixed into the active audio path (speaker or headphone). If the signal at V_{BEEP} is either $< 300mV_{P-P}$ or < 300Hz, the BEEP signal is not mixed into the audio path. The amplitude of the BEEP signal at the device output is roughly the amplitude V_{BEEP} times the gain of the selected signal path.

The input resistor (R_B) sets the gain of the BEEP input amplifier, and thus the amplitude of V_{BEEP}. Choose R_B based on:

$$R_B \leq \frac{V_{IN(BEEP)} \times 47k\Omega}{V_{BEEP}}$$

The total BEEP gain is given by:

$$\left|\frac{V_{OUT(BEEP)}}{V_{IN(BEEP)}}\right| = \left(\frac{47k\Omega}{R_B} + A_{V(BEEPOUT)}\right)$$

where 47kΩ is the value of the BEEP amplifier feedback resistor, V_{BEEP} is the BEEP amplifier output, $V_{IN(BEEP)}$ is the BEEP input amplitude, and $V_{OUT(BEEP)}$ is the total BEEP output signal. $A_{V(BEEPOUT)}$ is given by the values listed in Table 5. Note that V_{BEEP} must be higher than $300mV_{P-P}$. The BEEP amplifier can be set up as either an attenuator, if the original alert signal amplitude is too large, or to gain up the alert signal if it is below $300mV_{P-P}$. AC-couple the alert signal to BEEP. Choose the value of the coupling capacitor as described in the *Input Filtering* section. Multiple beep inputs can be summed (Figure 12).

Table 5. BEEP Output Gain

$A_{V(BEEPOUT)}$		GAIN3	GAIN2	GAIN1
HEADPHONE * (V/V)	SPEAKER* (V/V)			
1.5	8.4	0	0	0
1.5	9.4	0	0	1
1.78	10	0	1	0
1.78	10	0	1	1
1.5	15.8	1	0	0
1.5	18.8	1	0	1
1.78	20	1	1	0
1.78	20	1	1	1

**All output gains are for V_{VOL} = GND.*

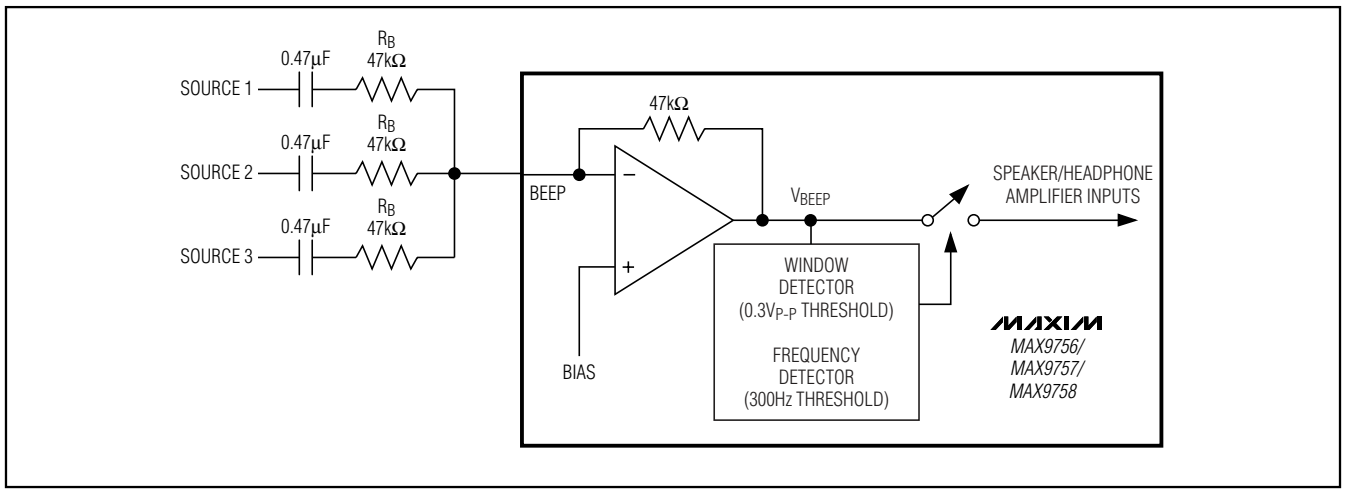


Figure 12. Beep Input

Shutdown ($\overline{SHDN}$)

The MAX9756/MAX9757/MAX9758 feature a 0.2µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. Driving $\overline{SHDN}$ low disables the drive amplifiers, bias circuitry, and charge pump, and drives BIAS and all outputs to GND. Connect $\overline{SHDN}$ to V_{DD} for normal operation.

Click-and-Pop Suppression

Speaker Amplifier

The MAX9756/MAX9757/MAX9758 speaker amplifiers feature Maxim's comprehensive, industry-leading click-and-pop suppression. During startup, the click-and-pop suppression circuitry eliminates any audible transient sources internal to the device. When entering shutdown, both amplifier outputs ramp to GND quickly and simultaneously.

Headphone Amplifier

In conventional single-supply headphone amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Since the MAX9756/MAX9757/MAX9758 do not require output-coupling capacitors, no audible transient occurs.

Additionally, the MAX9756/MAX9757/MAX9758 feature extensive click-and-pop suppression that eliminates any audible transient sources internal to the device. The Turn-On/Turn-Off waveforms in the *Typical Operating Characteristics* show that there are minimal spectral components in the audible range at the output upon startup and shutdown.

Applications Information

BTL Speaker Amplifiers

The MAX9756/MAX9757/MAX9758 feature speaker amplifiers designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 13) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions.

Since the differential outputs are biased at 2.5V, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large and expensive, can consume board space, and can degrade low-frequency performance.

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9756/MAX9757/MAX9758 can dissipate a significant amount of power. The maximum power dissipation for each

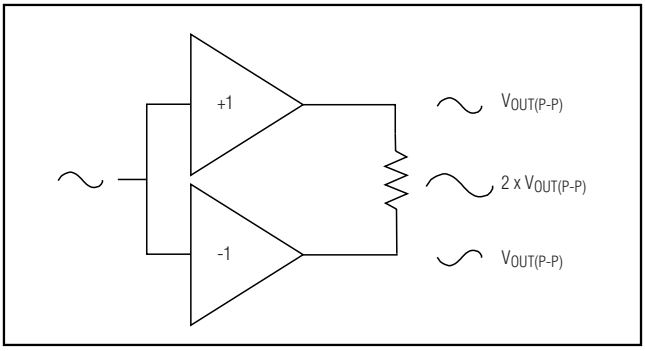


Figure 13. Bridge-Tied Load Configuration

package is given in the *Absolute Maximum Ratings* under Continuous Power Dissipation, or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} of the 32-pin thin QFN package is +40.2°C/W. For optimum power dissipation, the exposed paddle of the package should be connected to the ground plane (see the *Layout and Grounding* section).

Output Power (Speaker Amplifier)

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{DISS(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device or setting PREF to limit output power to a safe level. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package. Thermal-overload protection limits total power dissipation in these devices. When the junction temperature exceeds +160°C, the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal-overload conditions as the device heats and cools.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

Output Power (Headphone Amplifier)

The headphone amplifiers have been specified for the worst-case scenario—when both inputs are in phase. Under this condition, the drivers simultaneously draw current from the charge pump, leading to a slight loss in headroom of V_{SS}. In typical stereo audio applications, the left and right signals have differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power. Figure 14 shows the two extreme cases for in and out of phase. In reality, the available power lies between these extremes.

Power Supplies

The MAX9756/MAX9757/MAX9758 have different supplies for each portion of the device, allowing for the optimum combination of headroom and power dissipation and noise immunity. The speaker amplifiers are powered from PV_{DD}. PV_{DD} ranges from 4.5V to 5.5V. The headphone amplifiers are powered from HPV_{DD} and V_{SS}. HPV_{DD} is the positive supply of the headphone amplifiers and ranges from 3V to 5.5V. V_{SS} is the negative supply of the headphone amplifiers. Connect V_{SS} to CPV_{SS}. The charge pump is powered by CPV_{DD}. CPV_{DD} ranges from 3V to 5.5V and should be the same potential as HPV_{DD}. The charge pump inverts the voltage at CPV_{DD}, and the resulting voltage appears at CPV_{SS}. The remainder of the device is powered by V_{DD}.

Component Selection

Input Filtering

The input capacitor (C_{IN}), in conjunction with the amplifier input resistance (R_{IN}), forms a highpass filter that removes the DC bias from an incoming signal (see the *Typical Application Circuit*). The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

R_{IN} is the amplifier's internal input resistance value given in the *Electrical Characteristics*. Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest.

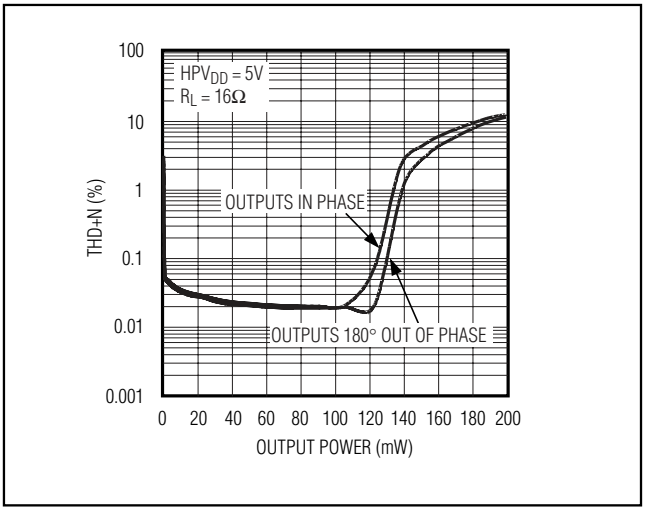


Figure 14. Total Harmonic Distortion Plus Noise vs. Output Power with Inputs In/Out of Phase (Headphone Mode)

Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

BIAS Capacitor

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the startup/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric. Table 6 lists suggested manufacturers.

Table 6. Suggested Capacitor Manufacturers

SUPPLIER	PHONE	FAX	WEBSITE
Taiyo Yuden	800-384-2496	800-925-0899	www.t-yuden.com
TDK	807-803-6100	847-390-4405	www.component.tdk.com

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the load regulation and output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Charge-Pump Capacitance graph in the *Typical Operating Characteristics*. Above 2.2µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at CPV_{SS}. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance graph in the *Typical Operating Characteristics*.

CPV_{DD} Bypass Capacitor

The CPV_{DD} bypass capacitor (C3) lowers the output impedance of the power supply and reduces the impact of the MAX9756/MAX9757/MAX9758's charge-pump switching transients. Bypass CPV_{DD} with C3, the same value as C1, and place it physically close to CPV_{DD} and PGND (refer to the MAX9756/MAX9757/MAX9758 Evaluation Kit for a suggested layout).

Powering Other Circuits from a Negative Supply

An additional benefit of the MAX9756/MAX9757/MAX9758 is the internally generated negative supply voltage (CPV_{SS}). CPV_{SS} is used by the MAX9756/MAX9757/MAX9758 to provide the negative supply for the headphone amplifiers. It can also be used to power other devices within a design. Current draw from CPV_{SS} should be limited to 5mA; exceeding this affects the operation of the headphone amplifier. A typical application is a negative supply to adjust the contrast of LCD modules.

When considering the use of CPV_{SS} in this manner, note that the charge-pump voltage of CPV_{SS} is roughly proportional to CPV_{DD} and is not a regulated voltage.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route heat away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect CPGND, PGND, and GND together at a single point on the PC board. Route CPGND and all traces that carry switching transients away from GND, PGND, and the traces and components in the audio signal path.

Connect all components associated with the charge pump (C2 and C3) to the CPGND plane. Connect V_{SS} and CPV_{SS} together at the device. Place the charge-pump capacitors (C1, C2, and C3) as close to the device as possible. Bypass HPV_{DD} and PV_{DD} with a 1µF capacitor to GND. Place the bypass capacitors as close to the device as possible.

Use large, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decrease the power delivered to the load.

For example, when compared to a 0Ω trace, a 100mΩ trace reduces the power delivered to a 4Ω load from 2.1W to 2W. Large output, supply, and GND traces also improve the power dissipation of the device. The MAX9756/MAX9757/MAX9758 thin QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct-heat conduction path from the die to the PC board. **Connect the exposed thermal pad to GND by using a large pad and multiple vias to the GND plane**.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

MAX9756 Block Diagram

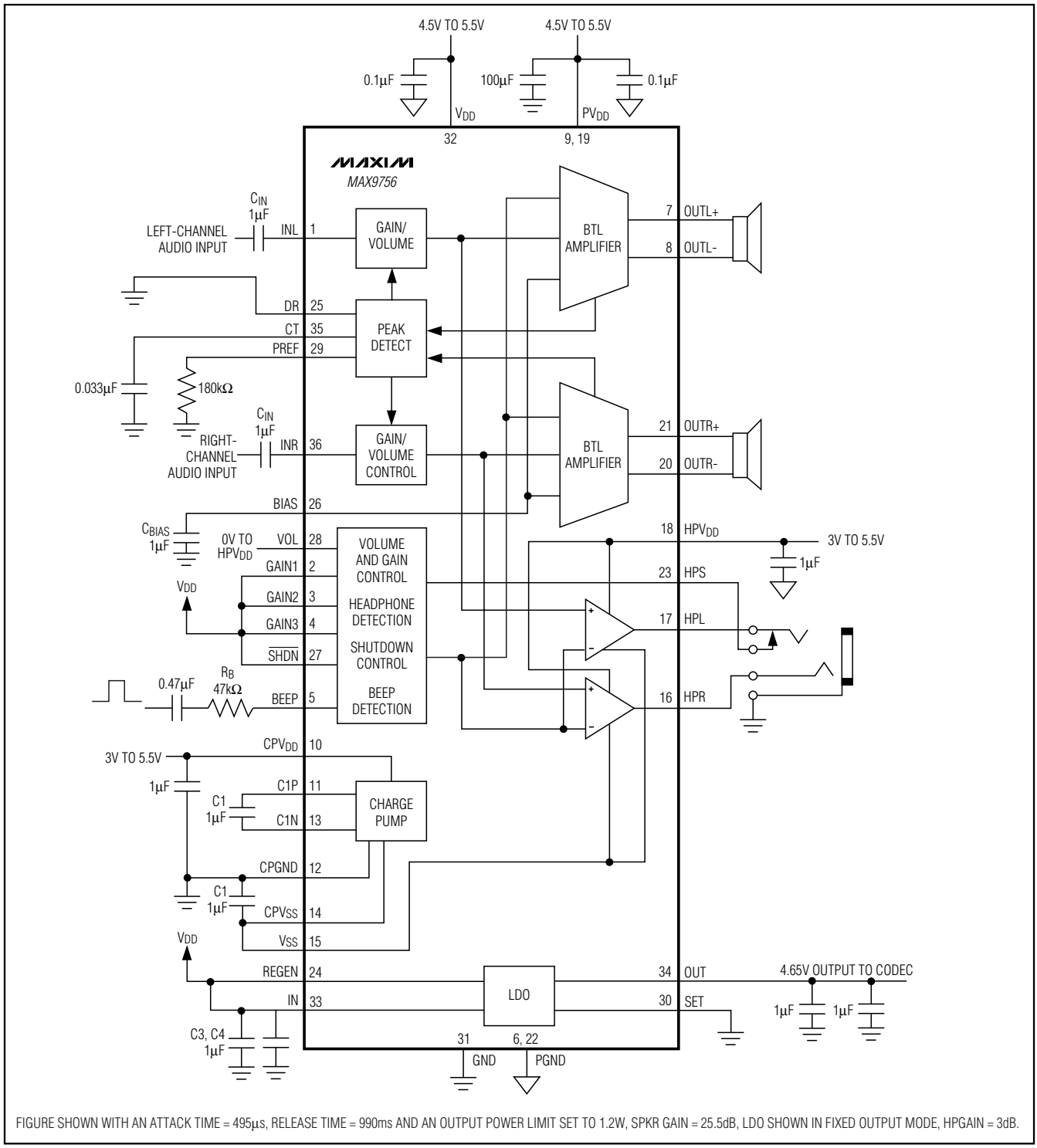


FIGURE SHOWN WITH AN ATTACK TIME = 495µs, RELEASE TIME = 990ms AND AN OUTPUT POWER LIMIT SET TO 1.2W, SPKR GAIN = 25.5dB, LDO SHOWN IN FIXED OUTPUT MODE, HPGAIN = 3dB.

MAX9757 Block Diagram

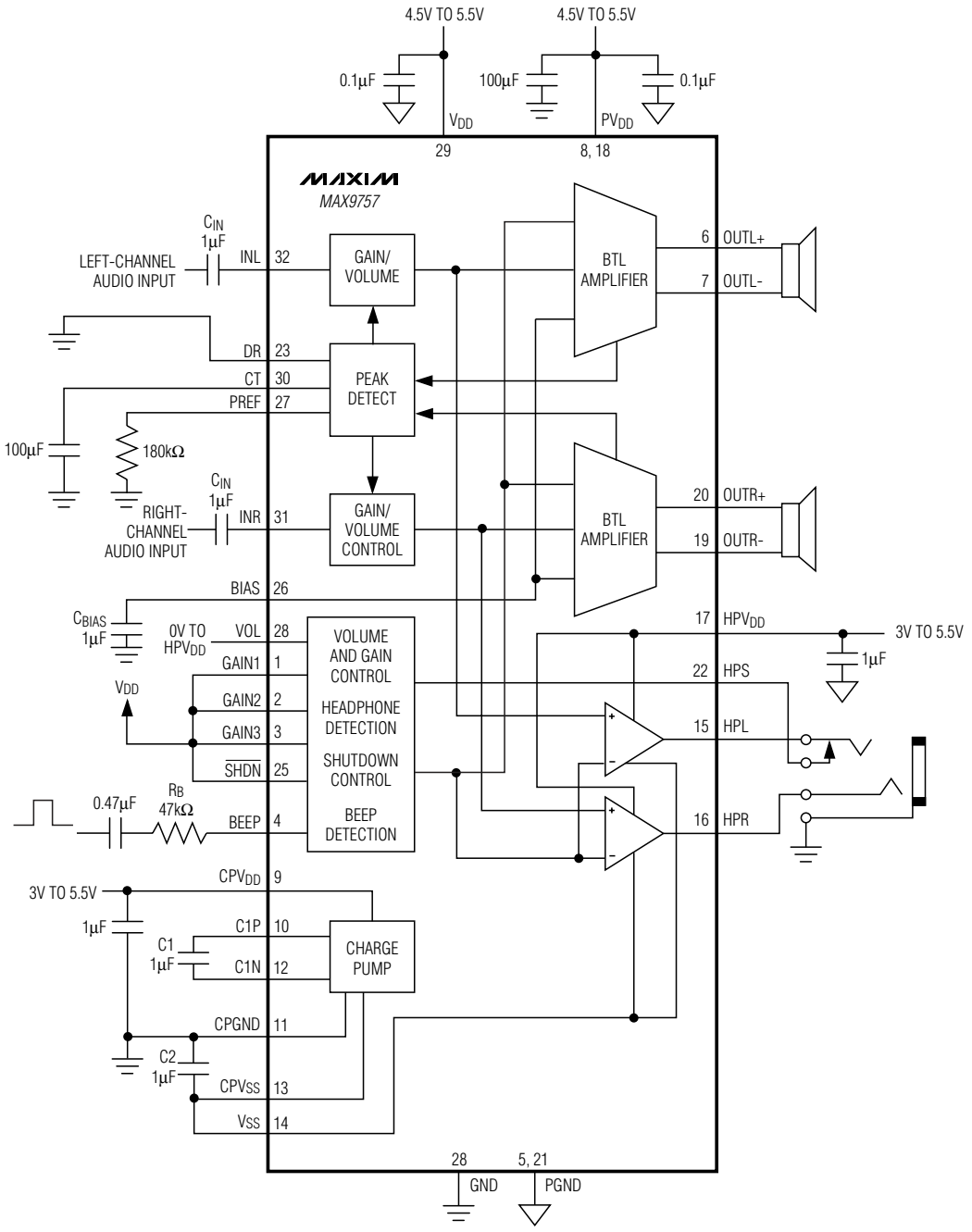


FIGURE SHOWN WITH AN ATTACK TIME = 495µs, RELEASE TIME = 990ms AND AN OUTPUT POWER LIMIT SET TO 1.2W, SPKR GAIN = 25.5dB, HP GAIN = 3dB.

2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

MAX9758 Block Diagram

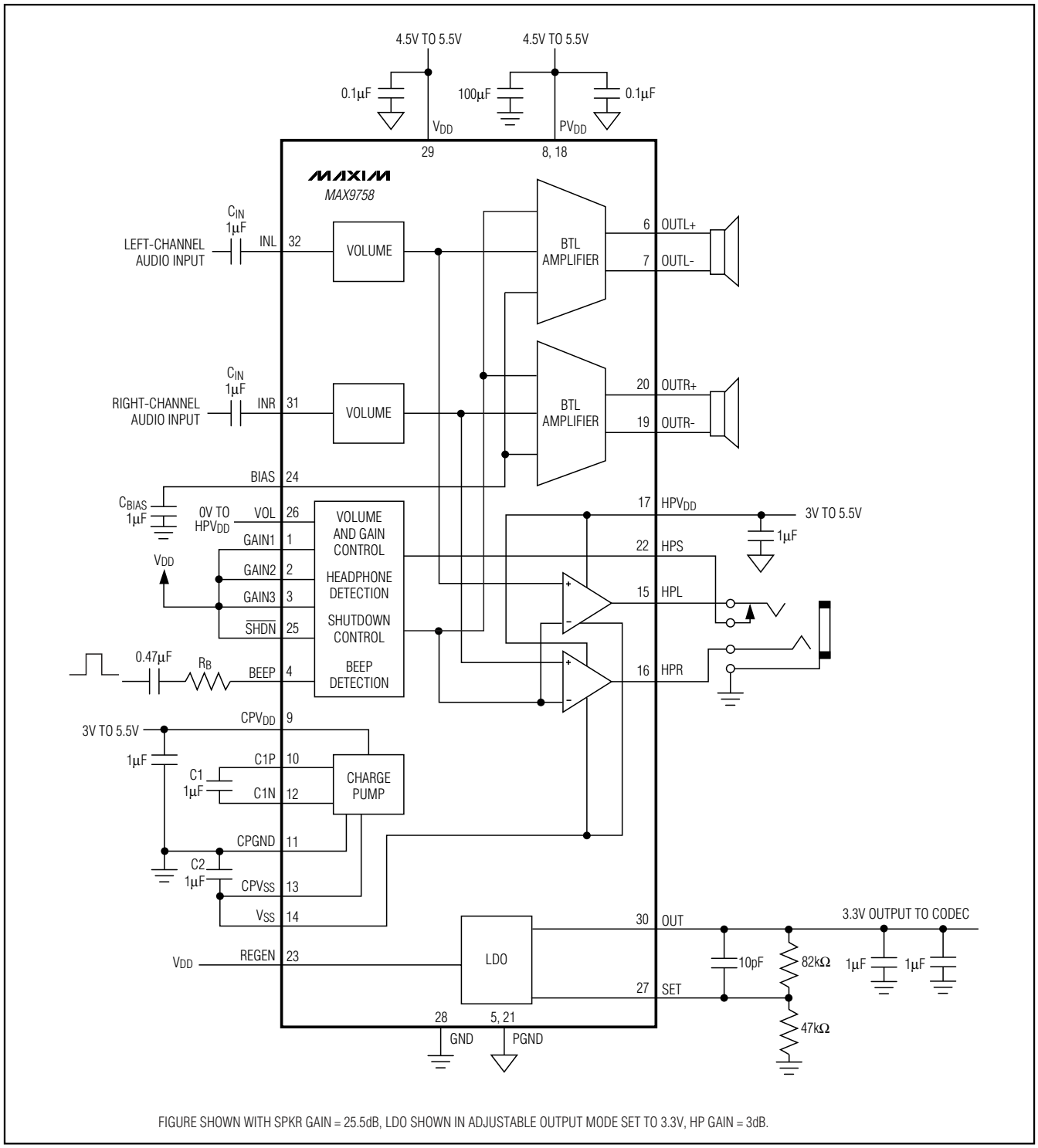
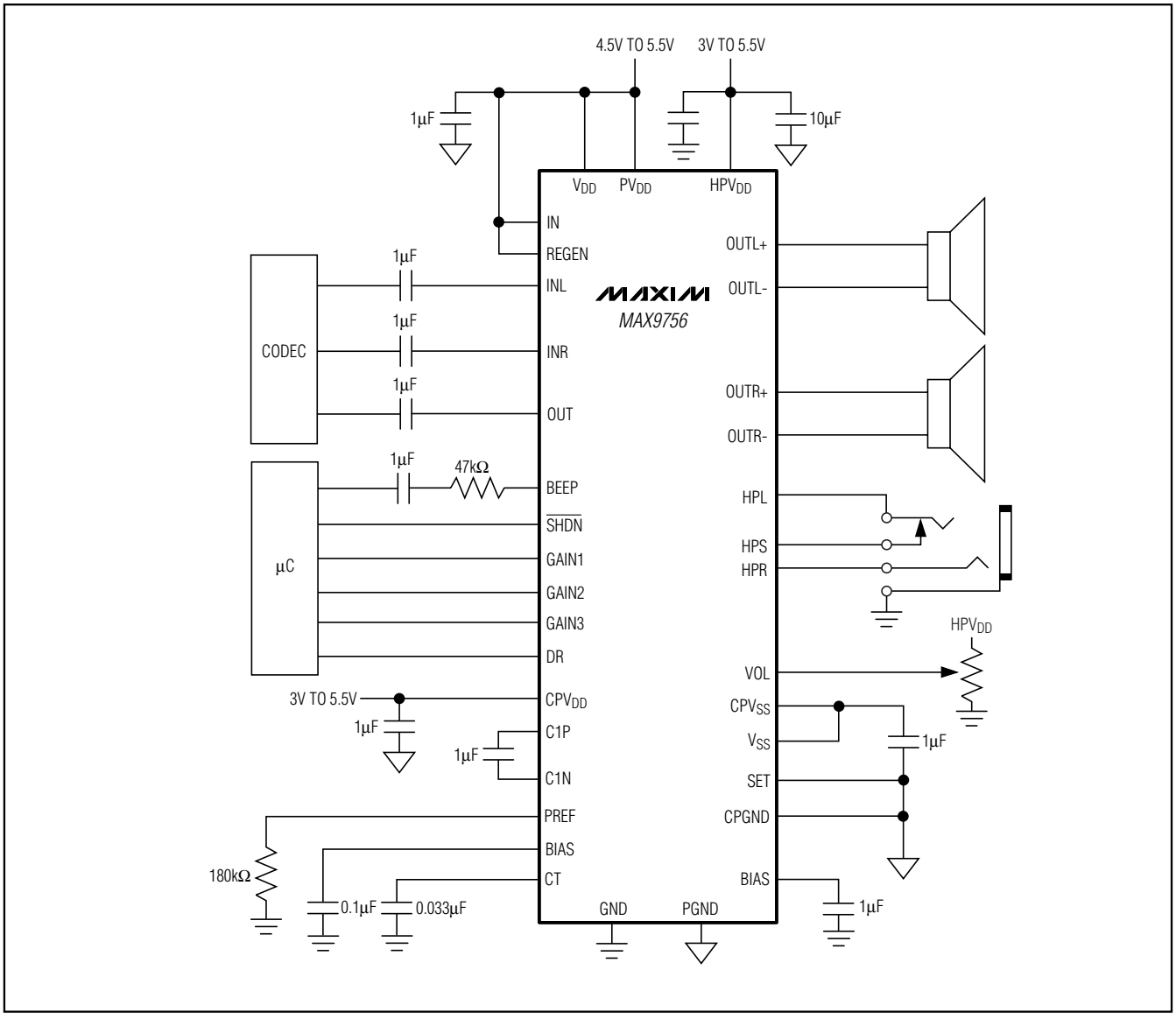


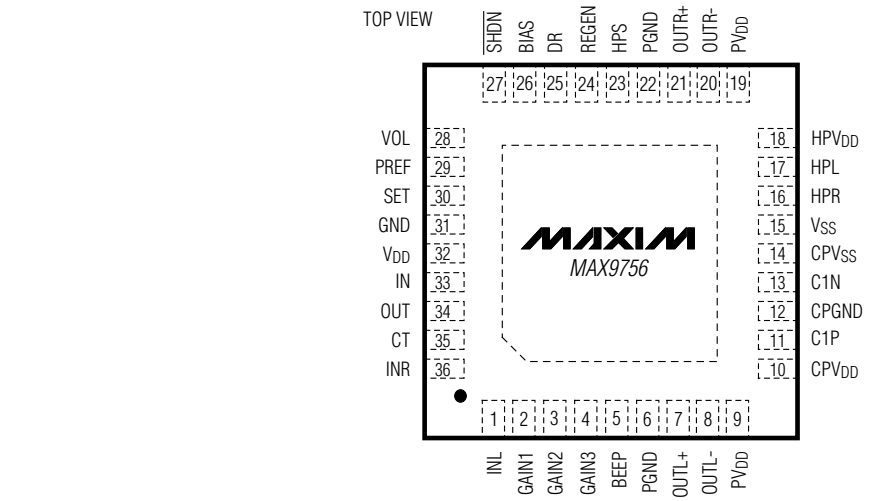
FIGURE SHOWN WITH SPKR GAIN = 25.5dB, LDO SHOWN IN ADJUSTABLE OUTPUT MODE SET TO 3.3V, HP GAIN = 3dB.

System Diagram

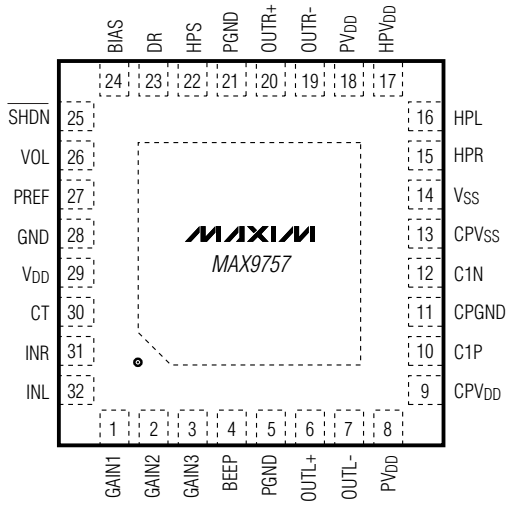


2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

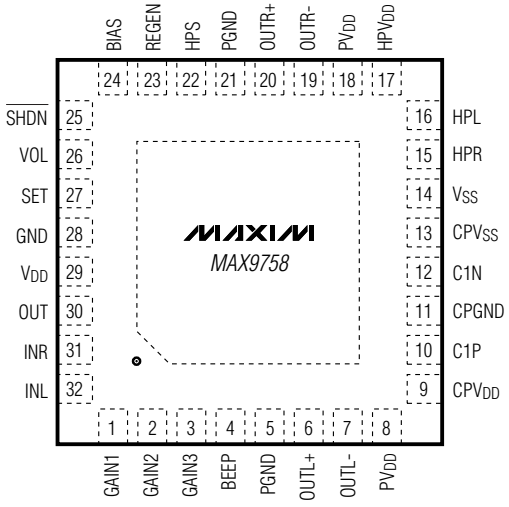
Pin Configurations



TQFN
6mm x 6mm



THIN QFN
5mm x 5mm



THIN QFN
5mm x 5mm

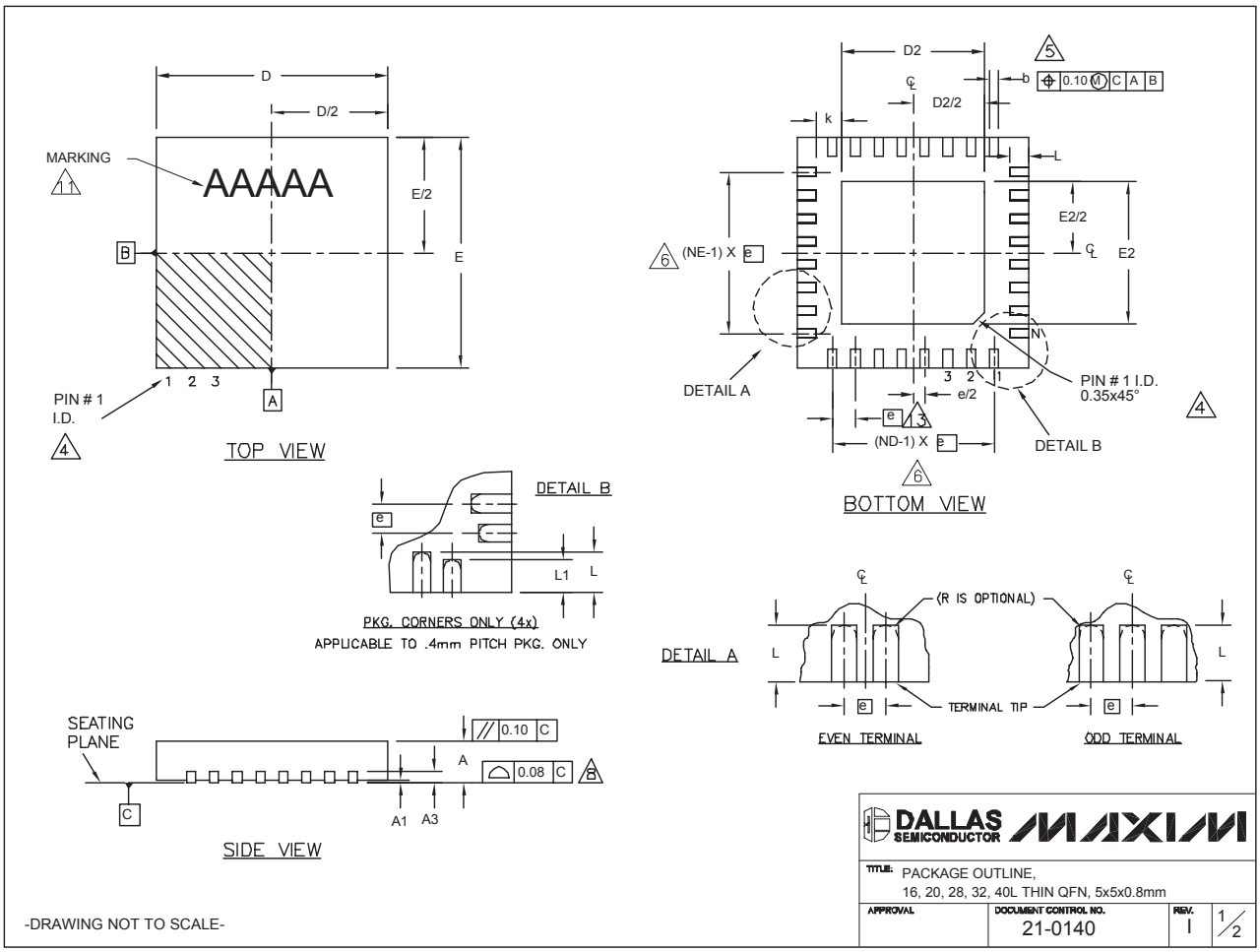
Chip Information

PROCESS: BICMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



2.3W Stereo Speaker Amplifiers and DirectDrive Headphone Amplifiers with Automatic Level Control

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L exceptions	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	**3**.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	**3**.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

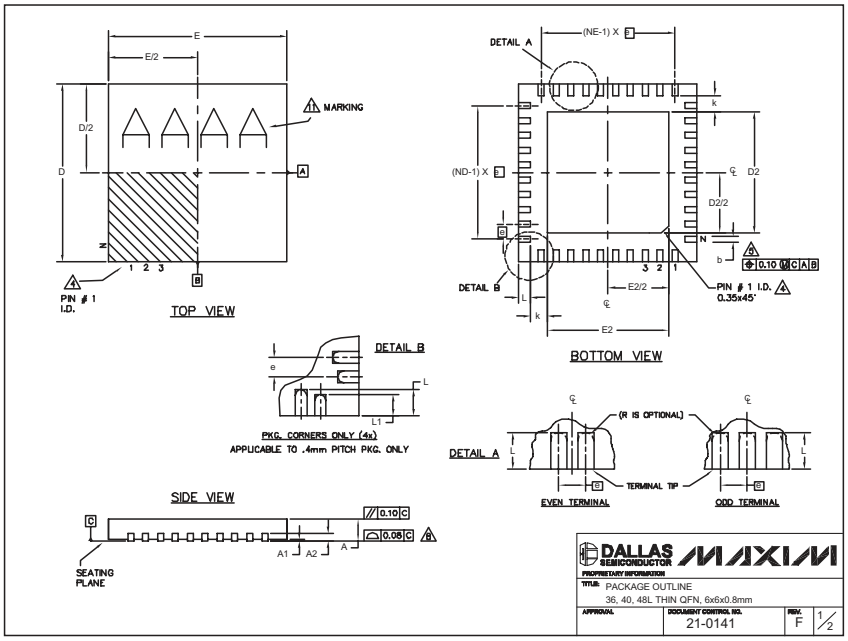
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	I	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	F	1/2

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	F	2/2