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Issue No. :	UCH2003421
Date of Issue :	
	■ New □ Changed □ Revised

PRODUCT SPECIFICATION FOR INFORMATION

Product Description : Multilayer Ceramic Chip Capacitors						
Product Part Number :		ECJCV50J106M (0805 VA Type, Temp.Char.X5R)				
		ECJDV50J106M (1206 VA Type, Temp.Char.X5R)				
		ECJDV50J226M (1206 VA Type, Temp.Char.X5R)				
Classification of Spec : Specifications						
Applications	:	Consumer Type Electric Equipment				
	I	For other applications contact our person signed below.				
Term of Validity	:	April 24.2008 from the date of issue				

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Ceramic Business Unit	Prepared by : EngineeringSection
LCR Device Company	Contact Person : <u>J Senshu</u>
Matsushita Electronic Components Co.,Ltd.	Title : Engineer
〒571-8506 1006 Kadoma, Osaka, Japan	Authorized by : H Hous
Tel : Osaka (06) 6908-1101	Title : Manager of Engineering
Fax : Osaka (06) 6908-7735	

•This product has not been manufactured with any ozone depleting chemical controlled under the Montreal Protocol.

•All the materials used in this part contain no brominated materials of PBBOs or PBBs as the flame retardant.

[•]All the materials used in this part are registered material under the Law Concerning the Examination and Regulation of Manufacture, etc. of Chemical Substances.

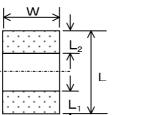
SUBJECT		PECIFICA	TIONS			No. 151S-EC	
	Multilayer Ceramic Chip Capacitor					PAGE 1	of 1
	"12" (EIA 0805) VA Type Individual Specification					DATE 23 th	Apr. 2003
•			'S Multilayer Cei Iominal Cap.10μF	•	capacit	or "0805 V	'A Type"
Style and Dimens	ions					T-1-1- 1	
	<mark>∢ W</mark> .	.			Symb	Table 1 ol Dimens	ions(mm)
			[•:•:•:•]		L		±0.20
			····		W	1.25	±0.20
					Т		±0.10
					L1,L2	2 0.50	±0.25
. Operating Tempe	erature Range	Ϋ́					
		Table 2		1			
Class2	<u>mperature Char</u> X5R	acteristics	Operating Temp. -55 to +85°				
018332	7.517		-55 10 185	0			
. Individual Specifi		Table 3					
Part Number	Rated	Temp. Char.	Nominal	Cap. Tole	ranco		
Fait Nullibei	Voltage	Temp. Char.	Capacitance		Tance		
ECJCV50J106M	D.C. 6.3V	X5R	10 μF	M: ±2	:0%		
Common Coc			Show in Fable 4		7	Tolerance Code	
	Packaging	Styles			oltage	 Show in Table 3	
Code Size	Code	Styles Packag		Code V	0	 Show in Table 3	
Code Size C 0805 VA Typ	De V ϕ 1	Styles Packag 80Reel Paper 1 Class 2 Capad	ging Faping 4000pcs	Code V	oltage		
Code Size C 0805 VA Typ	Code De V φ 1 aracteristics of Capacitance 0	Styles Packag 80Reel Paper T Class 2 Capac Table 4 Change rate fr	<u>ging</u> Faping 4000pcs citors om Temperature.	Code Vo 0J Do Measo	urement	Table 3	rence
Code Size C 0805 VA Typ	Code De V φ 1 aracteristics of	Styles Packag 80Reel Paper T Class 2 Capac Table 4 Change rate fr	<u>ging</u> Faping 4000pcs citors	Code Vo 0J Do Measu Temp	urement perature		
C 0805 VA Typ 6. Temperature Char Temp. Char.	Code De V φ 1 aracteristics of Capacitance 0	Styles Packag 80Reel Paper T Class 2 Capag Table 4 Change rate fr Without vol	<u>ging</u> Faping 4000pcs citors om Temperature.	Code Vo 0J Do Measu Temp Ra	urement	Table 3	erature
Code Size C 0805 VA Type 6. Temperature Char. Code 5 7. Soldering method Soldering method	Code De V φ 1 aracteristics of Capacitance (Temp. Char. X5R d	Styles Package 80Reel Paper T Class 2 Capace Table 4 Change rate fr Without vol +	<u>ging</u> Faping 4000pcs citors fom Temperature. Itage application	Code Vo 0J Do Measu Temp Ra -55 to	urement berature ange +85°C	Table 3 Refer Tempe	erature
Code Size C 0805 VA Typ S. Temperature Char. Temp. Char. Code 5 Y. Soldering method	aracteristics of Capacitance (Temp. Char. X5R d hod of Multilaye	Styles Packag Packag Styles Packag Styles Packag Styles Packag Styles Packag Pa	ging Faping 4000pcs citors for Temperature. Itage application -/-15%	Code Vo 0J Do Measo Temp Ra -55 to	urement berature ange +85°C	Table 3 Refer Tempe +25	erature

CLASSIFICATION	SPECIFICATIONS	No. 151S-ECJ-KAD39E
SUBJECT	Multilayer Ceramic Chip Capacitor	PAGE 1 of 1
	"13" (EIA 1206) VA Type Individual Specification	DATE 23 th Apr. 2003

1.Scope

This specification applies to MATSUSHITA'S Multilayer Ceramic Chip Capacitor "1206 VA Type" Temp. Char: X5R Rated voltage DC6.3V Nominal Cap.10µF,22µF.

2.Style and Dimensions



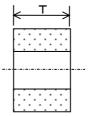


Table 1					
Symbol	Dimensions(mm)				
L	3.20 ± 0.20				
W	1.60 ± 0.20				
Т	0.85 ± 0.10				
L1,L2	0.60 ± 0.30				

3. Operating Temperature Range

	Table 2	
	Temperature Characteristics	Operating Temp. Range.
Class2	X5R	-55 to +85°C

4. Individual Specification

Table 3								
Part Number	Rated Voltage	Temp. Char.	Nominal Capacitance	Cap. Tolerance				
ECJDV50J106M	ECJDV50J106M D.C. 6.3V		10 μF	M: ±20%				
ECJDV50J226M	D.C. 6.3V	X5R	22 μF	M: ±20%				

5. Explanation of Part Numbers

•	ECJ Common Code	<u>D</u>	<u>v</u>	<u>5</u> Temp. Char. Show in	0	J <u>1 0 6</u> Nominal Cap.	<u>M</u> Cap. Tolerance Code
				Table 4		Rated Voltage	
Size C	ode	Packaging S	tyles			Code Voltage	Show in
Code	Size	Code	Pa	ckaging		0J DC6.3V	Table 3
D	1206 VA type	V φ18	0Reel Pa	per Taping 4000	ocs		

6. Temperature Characteristics of Class 2 Capacitors

		Table 4		
Temp. Char.	Capacitance C	Change rate from Temperature.	Measurement	Reference
Code	Temp. Char.	Without voltage application	Temperature	Temperature
0000			Range	remperature
5	X5R	+/-15%	-55 to +85°C	+25°C

7. Soldering method

Soldering method of Multilayer ceramic chip capacitor shall be reflow soldering.

Note :

Ceramic Business Unit LCR Device Company	APPROVAL	CHECK	DESIGN
Matsushita Electronic Components Co.,Ltd.			
Kadoma, Osaka, Japan	H.Itow	A.Omi	T.Senshu

CLASSIFICATION	SPECIFICA	ATIONS		No. 151S	-ECJ-KZ	.D38E
SUBJECT	Multilayer Ceramic	Chip Capacitor		PAGE	1 of	7
Com	mon Specifications (Cla	ass2 Large Capacitan	ce)	DATE	23 th . Apr.	. 2003
Char:X5R Rated	ence between this common					emp. II be
visual, househ However, dep failure modes Especially for trouble with t Ex. ①ensure Ex. ②ensure a single Such failsafe- 2.2 Whenever a d consultation v 2.3 For the follow 2.3.1 When it 2.3.2 Any app indirectly Ex. ①A ②S ③T ④T ⑤F	shall be used for general product, office, information & con- bending on ways of application of performance deterioration is such product design needer his product affects end product. If a safety as a system by adding a trouble with this productdesign considerations shall loubt about safety arises frowithout fail. Wing applications, please consistent of the safety arises frow the safety arises from the safety are safety arises from the safety are safety arises from the safety arises from the safety are	mmunication) equipment. ion there might be possib in or short/open circuits. d a high level of safety, a duct shall be recommended ing protective devices or ci- g a redundant-design cir- be practiced for a higher I ion this product, please info sult us for a different spec- the instructions below for rerroneous operation with a could result in death or in ce Equipment (artificial sat arine repeating equipment, vehicles, airplane, trains, suppent c power, thermal power pla port equipment, a pacemak ment (a large scale compu- Burning Apparatus	ilities to accele careful pre-st d; rcuits. cuits not to bed evel of safety. orm us immedia sification from t safety or hand n this product njury; cellite, rocket, e etc.) ship, traffic sign ant control syst er for the hear	erate the udy about come unsa itely for te this specif lling. may cause tc.) ial control	life-end a t how a s ofe becaus echnical fication. e direct lers)	as in ingle se of ly or
3. Part Number Code	$\frac{V}{3} \frac{5}{4} \frac{0}{5} \frac{1}{6}$	<u>6</u> <u>M</u> (7)				
3.2 Size②, Packa Rated Voltage Shown in Indiv 3.3 Nominal Capa The Nominal (and is identifie	layer Ceramic Chip Capacito aging Styls③. Temperature ⑤, Capacitance Tolerance(vidual Specification. citance⑥ Capacitance value is express ed by a three-digit number ; nificant figures and the last o	Characteristic④, ⑦ sed in Pico farads(pF) the first two digit	Symbol (E 104 105 106	ix.) N	lominal Ca 0. 1 μ F 1 μ F 10 μ F	-
Note ;						
Ceramic Business U	nit LCR Device Compar	201	APPROVAI	- CHEC		SIGN

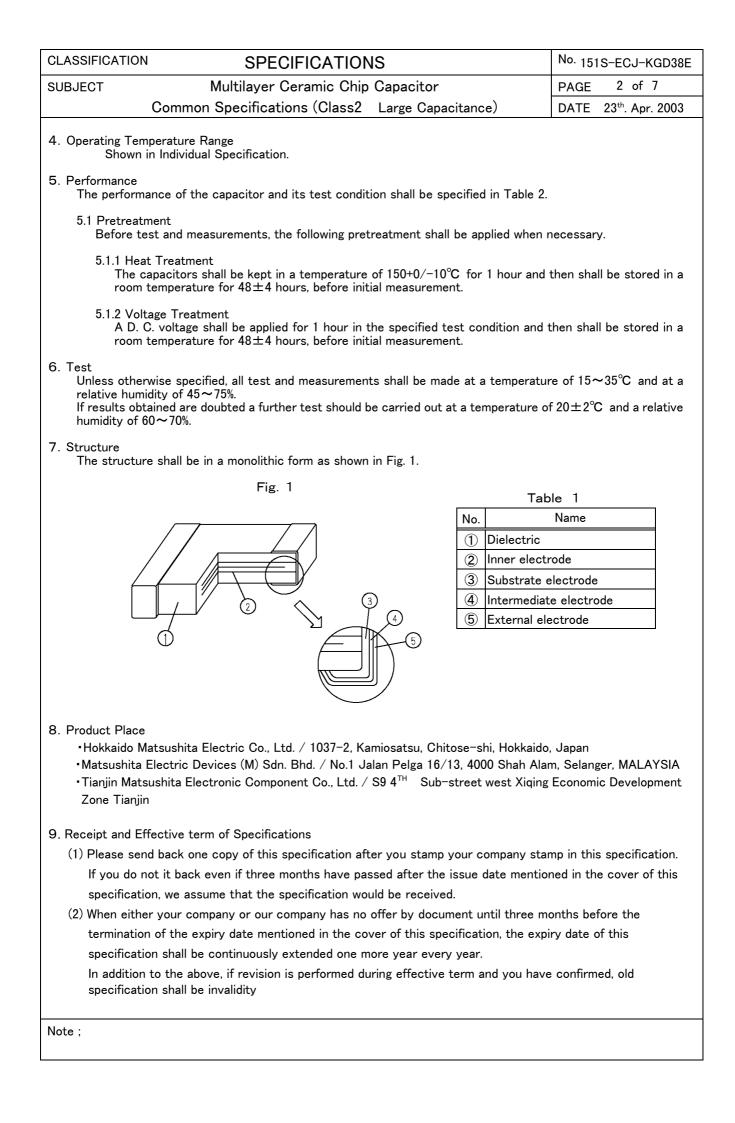
H.Itow

A.Omi

T.Senshu

Matsushita Electronic Components Co.,Ltd.

Kadoma, Osaka, Japan



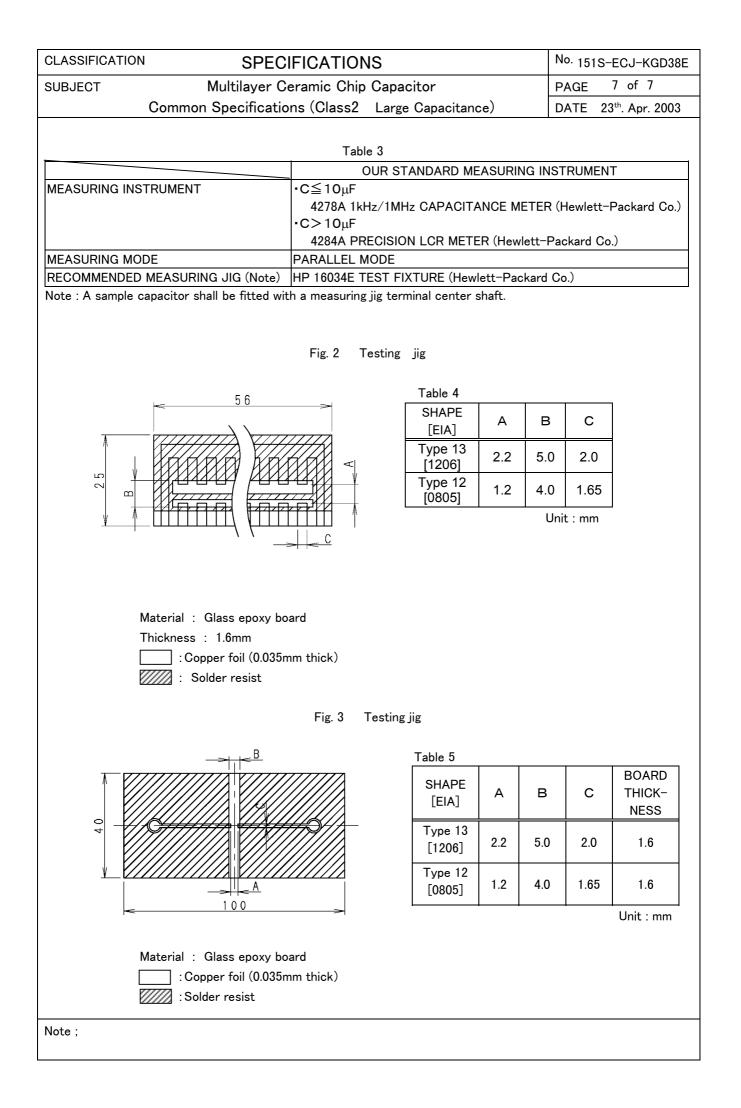
	SSIFICATION		SPECIFICATIONS			INO. 15	1S-ECJ-KGD3
SUB	JECT		Multilayer Ceramic Chip Capacit	or		PAGE	3 of 7
		Commo	on Specifications (Class2 Large C	Capacitance)		DATE	23 th . Apr. 200
			Table 2				
No.	Conter	nts	Performance		Test N	Method	
1	Appearance		There shall be no defects which affect	With a magnifyin			es).
•	, , , , , , , , , , , , , , , , , , , ,		the life and use.		00		
2	Dimensions		Shown in Individual Specification.	With slide calipe	rs and	a micro	ometer.
3	Dielectric		There shall be no dielectric breakdown	Test voltage :			
	Withstanding	voltage	or damage.	250% of rated vo	ltage		
				Apply a D. C. vol	ltage o	f the at	pove value for
				to 5 seconds.			
				Charge/discharg			
4	Insulation	- \	More than $100/C$ M Ω .	Measuring voltag			-
	Resistance(I.	R.)	(C : Rated Cap. in μF)	Measuring voltag Charge/discharg			
5	Capacitance		Shall be within the specified tolerance.		Meas		Measuring
5	Sapaonanoe		enal be want the specified tolerallee.	Cap.	Frequ	-	Voltage
6	Dissipation F	actor	0.15 max.	<u>C≦10µ</u> F	1kHz		1.0±0.2Vr.m.s.
	(tanδ)			C>10µF	120Hz	±20%	0.5±0.1Vr.m.s.
				For the class2 C			form the
				heat treatment i	•		
				Our Measurement instrument is shown Table 3.			is shown in the
	Characteris-						
	tics	Appli- cation		to 4 shown in t rate of change stage 3 as the re	regard	ling the	
	tics	Appli-		rate of change stage 3 as the re Temp. C	regard eferenc har.	ling the	capacitance X5R
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage	regard eferenc har. 1	ling the	x5R 25±2
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage	regard eferenc har. 1 2	ling the	x5R 25±2 -55±3
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage	regard eferenc har. 1 2 3	ling the	x5R 25±2 -55±3 25±2
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage Stage	regard eferenc har. 1 2 3 4	ling the	x5R 25±2 -55±3 25±2 85±2
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage	regard eference har. 1 2 3 4 5		x5R 25±2 -55±3 25±2 85±2 25±2
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage Stage	regard eference har. 1 2 3 4 5 5 Meas	uring the	e capacitance X5R 25±2 -55±3 25±2 85±2 25±2 25±2 Measuring
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage Stage Stage	regard eference har. 1 2 3 4 5	uring the	x5R 25±2 -55±3 25±2 85±2 25±2
	tics	Appli-		rate of change stage 3 as the re Temp. C Stage Stage Stage Stage Stage Cap.	regard eference har. 1 2 3 4 5 5 Meas Frequ	uring the uring the tent tent tent tent tent tent tent	x5R 25±2 -55±3 25±2 85±2 25±2 25±2 Measuring Voltage
8	tics Adhesion	Appli-	The terminal electrode shall be free from peeling or signs of peeling.	rate of change stage 3 as the re Temp. C Stage Stage Stage Stage Cap. C≦10μF	regard eference har. 1 2 3 4 5 5 5 5 5 5 5 5 7 7 8 4 5 5 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8	ling the ce. uring lency $\pm 10\%$ $\pm 20\%$	x5R 25±2 -55±3 25±2 85±2 25±2 Measuring Voltage 0.5±0.1Vr.m.s. 0.5±0.1Vr.m.s.
8		Appli-	The terminal electrode shall be free from peeling or signs of peeling.	rate of change stage 3 as the re Temp. C Stage Stage Stage Stage Cap. C≦10μF C≥10μF Solder the speci	regard eference har. 1 2 3 4 5 5 5 5 6 7 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8	uring the ce.	x5R 25±2 -55±3 25±2 85±2 25±2 Measuring Voltage 0.5±0.1Vr.m.s. 0.5±0.1Vr.m.s. sting jig shown rce in the arro
8		Appli-		rate of change stage 3 as the rest Temp. C Stage Stage Stage Cap. C≤10μF C>10μF Solder the speci the figure., and direction for 10 s	regard eference har. 1 2 3 4 5 5 5 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	uring uring uency ±10% ±20% the te a 5N fo ls. Samp d (95% for	x5R 25±2 -55±3 25±2 85±2 25±2 Measuring Voltage 0.5±0.1Vr.m.s. 0.5±0.1Vr.m.s. sting jig shown rce in the arro

SUBJ				IFICATIONS Ceramic Chip Ca)r		PAGE	-ECJ-KGD381
SORJ	EGI	Commo	-	-	-				
		Commo	on Specificatio	ons (Class2 L		apacit	ance)	DATE 2	3 th . Apr. 2003
			_	Table 2	2				
No.	Conter	-		erformance		A ()	Test Method		
	Bending Strength	Appea− rance	There shall be mechanical dam		l	After soldering capacitor on the substrate 1mr of bending shall be applied for 5 seconds. Bending speed : 1mm/s			
		Capac-	X5R	Within $\pm 12.5\%$, ,	(showr	in Fig. 3)	_	
		itance					20 45±2	↓ R 3 4 0	Bending Value
10	Vibration	Appea-	There shall be r	no cracks and othe	er I	For the	e class 2 Capa	citors, perfo	rm the heat
	Proof	rance	Mechanical dam	nage.	1	treatm	ent in par. 5.1.	1.	
		Capac-	Shall be within t	the specified toler	ance.	Solder	the specimen	to the testir	ng jig shown
		itance			i	in Fig 2	2. Apply a varia	able vibration	n of 1.5mm
		tan δ	Shall meet the :	specified initial val	1	freque perpen	mplitude in the ncy range swe dicular directio f 6 hours.	pt in 1 min. i	n 3 mutually
	Resistance to Solder Heat	Appea- rance Capac- itance	Mechanical da Characteristic	no cracks and othe mage. Change from the v before test. Within $\pm 12.5\%$		(1)Solder both method Preconditioning : Heat Temperatu (See 5.1.1)/Class Solder temperature : 270±5℃ Dipping period : 3±0.5s			lass2
		tan δ	Shall meet the	specified initial val			eat condition Temp.	Peri	od(s)
		I.R.		specified initial val		Order	(°C)	Type"12"	Type"13"
		With-		no dielectric break		1 2	80 to 100 150 to 200	120 to 180 120 to 180	300 to 360 300 to 360
		stand voltage	or damage.		 	Use so use ro: concer tweeze	Ider H63A(JIS sin (JIS-K-590 otration of abo ers for the hold ery : 48±4 hold	-Z-3282).Fo 02) ethanol s ut 25% by we der to dip the	r the flux, colution of a eight. Use
				(continue	e)				

SUB	JECT		Multilayer (Ceramic Chip	Capacit	or		PAGE	5 of 7
		Commo	on Specificati	-	Large C		nce)	DATE	23 th . Apr. 2003
				Table	_				
No.	Conte	ote		Performance	2	· · · · ·	Tost	Mathaa	4
	Solderability	11.5		of the soldered	area of	Test Method Solder temperature : 230±5°C Dipping period : 4±1s			
. –				electrodes shall b					
			covered with f	resh solder.		Dip the	specimen in so	older so	that both
									letely submerge
							der H63A(JIS−) IIS−K−5902) of). For the flux us
							tration of about		
							eezers for the l		
						specim			-
13	Temperature	Appea-	There shall be	no mechanical d	amage.	Solder	the specimen t	o the t	esting jig shown
	cycle	rance	T O			in Fig.2	. Condition the	specim	nen to each
		Capac- itance	Temp. Char.	Change from the before test.	e value	temper	ature from ste	o 1 to 4	in this order fo
		Itance	X5R	Within $\pm 12.5\%$		the per	riod shown in th	ne table	below. Regard-
		$tan \delta$		specified initial	value.	ing this	conditioning a	s one c	ycle, perform
		I.R.		specified initial		5 cycle	s continuously		
		With-	There shall be	no dielectric br	reakdown	STEP	TEMPERATUR	RE (°C)	PERIOD (min)
		stand voltage	or damage.			1	Minimum oper temperature		30±3
						2	Room temper		3 max.
						3	Maximum ope temperature		30±3
						4	Room temper	ature	3 max.
						For the	e class2 capacit	tors, pe	rform the heat
						treatm	ent in par. 5.1.1	•	
						Before	the measurem	ent afte	er test, the
						specim	en shall be left	to star	nd at room
						tempe 48±4	erature for the [.] h	followin	g period :
14	Moisture	Appea-	There shall be	no mechanical d			class2 capacit		rform the heat
	Resistance	rance	Charatt	Change from 1			ent in par. 5. 1. the specimen t		oting lig chause
		Capac- itance	Unaracteristic	Change from t before test	ne value	in Fig.2			soung jig shown
			X5R	Within $\pm 20\%$					
		tan δ	0.25 max.				mperature : 40		
							e humidity : 90)
		I.R.	More than 10/			lest pe	eriod : 500+24.	∕Uh	
			(C : Rated Cap	.ın μ⊢)		Before	the measureme	ent afte	r test. the
							en shall be left		
							ature for the fo	llowing	period :
						48±4	h		
				(contir	iue)				

CLASSIFICATION SPECIFICATI				ICATIONS		No. 151S-ECJ-KGD38	
UB	JECT		Multilayer Cer	amic Chip Capacit	or	PAGE 6 of 7	
		Commo	on Specifications (Class2 Large C		Capacitance)	DATE 23 th . Apr. 2003	
				Table 2			
No.	Conter	nts	Per	omance	Test Method		
15	Moisture Resistant	Appea− rance	There shall be no	mechanical damage.	For the class2 capacitors, perform the voltage reatment in par. 5. 1. 2.		
Loading	Capac- itance	Characteristic	value before test.	Solder the specimen to the testing jig show in Fig 2.			
		tan δ	X5R	Within $\pm 20\%$	Test temperature : 40)+2°C	
			0.25 max.	0	Relative humidity : 90		
		I.R.	More than 5/C M (C : Rated Cap. in		Applied voltage : Rated Voltage (D. C. Voltage) Charge/discharge current shall be within 50mA Test period : 500+24/0 h		
					Before the measurement after test, the specimen shall be left to stand at room temperature for the following period : 48±4 h For the class2 capacitors, perform the volta		
10	High Temperature	Appea- rance	There shall be no	mechanical damage.	For the class2 capaci treatment in par. 5.1.2		
	Resistant Loading	Capac- itance	Characteristic	Change from the value before test.		 to the testing jig shown	
		t S	X5R	Within $\pm 20\%$	Test temperature :	Max. Rated temp.±3°C	
		tanδ I.R.	0.25 max. More than 10/C M (C : Rated Cap. in		Applied voltage : R	ated Voltage (D. C. Voltage) current shall be	
					Before the measurem specimen shall be left temperature for the f 48±4 h	t to stand at room	

hig 1g), 1 p itself.



CLASSIFICATION SPECIFICATIONS No. 151S-ECJ-SS								
SUBJECT	Multilayer Ceramic Chip Capacitor		PAGE 1	of 12				
	Common Specifications (Precautions for Use)		DATE 1st.	Apr. 2002				
Such as use If it is used the capacito	acked ceramic capacitor (hereafter referred to as capacitor) is a environment, design requirements, and installation requirement in the shorted state, a large current will flow through it when a pr body, and possibly burn the circuit board out . assembly cautions are described below. Confirm them sufficie	nts, it will be sl voltage is app	hort-circuited a plied which will	at worst.				
1. 1. 1 Desi	gn of Circuit							
1. 1. 1. 1	Working temperature The working temperature must be within the range specified The working temperatures must not exceed the maximum we							
 1. 1. 1. 2 Working voltage The voltage across the terminals of the capacitor must be equal to or less than the rated voltage. Do not use the capacitor in a circuit where an abnormal voltage exceeding the rated voltage (surge voltage, pulse voltage, electrostatic voltage) may be applied to the capacitor. The capacitor may be shorted. If a DC voltage is superimposed with an AC voltage, take care that the peak voltage (Vp - p) is equal to or less than the rated voltage. Even if the voltage is equal to or less than the rated voltage, when the capacitor is used in a circuit where a high frequency voltage or a steep pulse voltage is applied continuously to it, closely examine the reliability of the capacitor. If such a voltage is applied continuously to the capacitor, the service life of it will be affected. 								
1. 1. 1. 3	Working current If the capacitor causes a short-circuit at the secondary side current will flow through it to heat the capacitor body, and th Sufficiently examine the safety of use, and install a protectiv	e circuit board	d may be burnt					
1. 1. 1. 4	Self-heating When self-heating is caused by an AC voltage or a pulse volt around the capacitor in use is room temperature (about 25° C (a difference between the surface temperature of the capacitor it) comes within 20° C or below. The surface temperature of the capacitor including an amount equal to or less than the maximum working temperature spec For the temperature rise of the capacitor according to the us operating conditions of the equipment in use.), take care so or and the am t increased by ified in the de	b that a temper bient temperatu the self-heatin livery specificat	ature rise ure around g must be tion.				
 1. 1. 1. 5 Limitation of use places Do not use the capacitor in the places indicated below. It may cause a short-circuit. (1) Peripheral environmental (weatherproofness) conditions (a) Places where water or salt water is applied directly (b) Places where dewatering state occurs (c) Places where corrosive gases (hydrogen sulfide, sulfurous acid, chlorine, and ammonia) are filled out (2) Places for which the requirements of vibration or impact are so severe as to exceed the range specified in the delivery specification. 								
Note ;								
Ceramic Busines Matsushita Elec	ss Unit LCR Device Company tronic Components Co.,Ltd.	APPROVAL	CHECK	DESIGN				

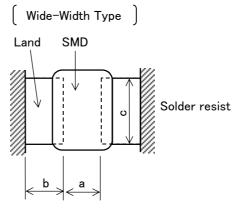
Kadoma, Osaka, Japan

H.Itow Y.Tsutsumi K.Ohishi

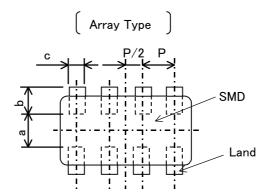
e Chip Capacitor (Precautions for Use) r (type 2) causes a piezoelectricity (or an may occur. quency is applied to the capacitor, the natu- ize of the capacitor may cause resonance effective to change the size of the capacit nange the material of the capacitor to a lo ectricity or to use a type 1 capacitor. d to the capacitor, a mechanical force is c bise. (Particularly, care must be taken whe Iternative method of changing the material (or with small) piezoelectricity or the use of it does not cause any problem with the pe	cural frequency of the e and generate noise. itor to change its w loss material without converted to electric en the capacitor is used I of the capacitor to a low
r (type 2) causes a piezoelectricity (or an may occur. quency is applied to the capacitor, the nati- tize of the capacitor may cause resonance effective to change the size of the capaci- nange the material of the capacitor to a lo ectricity or to use a type 1 capacitor. d to the capacitor, a mechanical force is c bise. (Particularly, care must be taken whe lternative method of changing the material (or with small) piezoelectricity or the use of	electrostriction). Eural frequency of the e and generate noise. itor to change its we loss material without converted to electric en the capacitor is used I of the capacitor to a low
may occur. quency is applied to the capacitor, the naturate ize of the capacitor may cause resonance effective to change the size of the capacit mange the material of the capacitor to a lo lectricity or to use a type 1 capacitor. d to the capacitor, a mechanical force is co bise. (Particularly, care must be taken whe Iternative method of changing the material (or with small) piezoelectricity or the use of	cural frequency of the e and generate noise. itor to change its w loss material without converted to electric en the capacitor is used I of the capacitor to a low
(or with small) piezoelectricity or the use o	
quipment manufacturer is worried about the, check the equipment for operation. To so tor with a different shape, size, and charae) and (2) above. It may also be effective to suppress the resonance with the cabinet of the printed circuit board with	erformance and reliability the sound. Since it may solve the problem, it is acteristics of the to change the direction et of a printed circuit
alumina board, it is expected to deteriorat cle). board, sufficiently examine the actual boar fected	
ases, stress applied to the capacitor incre oblem, when designing the land of a circuit nt of solder is of appropriate volume. Installed on a common land, separate them ely for both parts at the solder resist.	board, set the shape and
n dimensions not causing an excessive an commended cases are shown below.	nount of solder, cases
ded land dimensions(Ex.) Equipment , High Value Capacitance s Type , 100V•200V series	
SMD	it
	SMD

CLASSIFICATION	SPECIFICATIONS	No. 151S-ECJ-SS001E		
SUBJECT	Multilayer Ceramic Chip Capacitor	PAGE 3 of 12		
	Common Specifications (Precautions for Use)	DATE 1st. Apr. 2002		

						Unit: : mm
Size Code	Com	ponent Di	mension		٦	
	L	W	Т	а	b	с
"06" (0201)	0.6	0.3	0.3	0.2~0.3	0.25~0.3	0.2~0.3
"10" (0402)	1.0	0.5	0.5	0.4~0.5	0.4~0.5	0.5~0.6
"11" (0603)	1.6	0.8	0.8	0.8~1.0	0.6~0.8	0.6~0.8
"12" (0805)	2.0	1.25	0.6~1.25	0.8~1.2	0.8~1.0	0.8~1.0
"13" (1206)	3.2	1.6	0.6~1.6	1.8~2.2	1.0~1.2	1.0~1.3
"23" (1210)	3.2	2.5	1.4~2.5	1.8~2.2	1.0~1.2	1.8~2.3
"34" (1812)	3.2	2.5	2.5~3.2	3.0~3.5	1.2~1.6	2.3~3.0



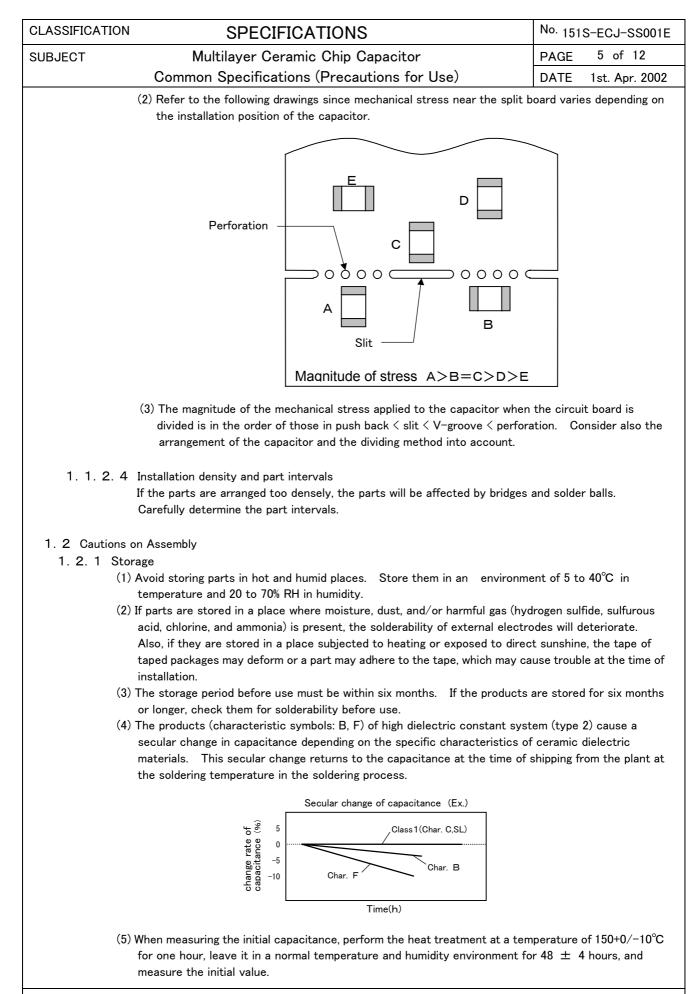
				I		Unit: : mm
Size Code	Com	ponent Di	mension		٩	
Size Code	L	W	Т	а	d	с
"21" (0508)	1.25	2.0	0.85	0.5~0.7	0.5~0.6	1.4~1.9
"31" (0612)	1.6	3.2	0.85	0.8~1.0	0.6~0.7	2.5~3.0



11.	nit		m	\mathbf{m}

	Size Code	Comp	onent Dime	ension		L	с	Б	
	Size Code	L	W	Т	а	a b		F	
	"12" (0805)	0.0 1.05	1.05 0.05	0.85	0.05	0.55~	0.5~	0.2~	0.4~
	12 (0805)	2.0	1.25		0.75	0.6	0.3	0.6	
ĺ	"10" (100c)	2.0	1.6	0.05	0.9~	0.7~	0.35~	0.7~	
	"13" (1206)	3.2	1.6	0.85	1.1	0.9	0.45	0.9	

LASSIFICATION	SPECIFICATIONS		No. 151S-ECJ-SS00
JBJECT M	ultilayer Ceramic Chip Ca	apacitor	PAGE 4 of 12
Commo	n Specifications (Precaut	ions for Use)	DATE 1st. Apr. 200
	Cases that should be avoided ar	nd recommended cases	
Item	Cases that should be avoid	led Case of improven	nent by pattern division
mixed mounting together with parts with lead	The lead of part w		Sectional plan
arrangement near chassis	Chassis Solder (groung solder) Electrode pattern Section	onal plan	Sectional plan
retrofitting of parts with lead		on ofitted parts Solder resist —	Sectional plan
lateral arrangement	Land portion excessive soldered	/ely	Solder resist I
later at the	time of cooling. Recommended amou	int of solder	
(a) Too la	rge amount of (b) Proper a		amount
solder		r of solder	
	solder	Solder ↑ PC board	<u>←</u> solder
PCt	board PC board	PC board	
capacitor may	t of part oard is bent in the process or o y cause a crack. To prevent t n of the circuit board can be mir	his problem, arrange the par	
	nmended example of arrangemen eflection of a circuit board can b		echanical stress caused b
	Cases that should be avoided	Recommen	
C	ases that should be avoided		ded cases



CLASSIFICAT	TION	SPECIFICATIONS		No. 151S-ECJ-SS001
SUBJECT	Multi	ayer Ceramic Chip Capac	itor	PAGE 6 of 12
	Common S	pecifications (Precautions	s for Use)	DATE 1st. Apr. 2002
1. 2. 2	so that the adhes (2) If the amount is to (3) If the viscosity is t (4) Heat hardening is from being oxidize (5) If the hardening is resistance betwee	adhesive agent amount of application of adhesive ive agent does not expand to the bo small, the capacitor may fall d ioo low, the installation position made by ultraviolet and far infrar d, perform the heat hardening at not sufficient, the capacitor ma en the terminal electrodes may d problems, sufficiently examine th	e land due to a flow at the luring flow-soldering. of the capacitor may be di red radiation. To prevent a temperature of 160°C y fall during flow soldering leteriorate due to moisture	time of heating isplaced. the terminal electrode for within two minutes . Also, insulation
1. 2. 3	 absorbing nozzles impact load such capacitor body. (2) The maintenance (3) If the bottom dead capacitor at the ting 1) Set and adjust board after correct 2) Set the nozzle 3) For double surficient on the rear surfice example is show 4) Adjust the adsoc lowered excess (4) If the positioning of capacitor will be a these problems, or 	capacitor on a circuit board, take at the time of installation do not as a mechanical impact and stre and inspections of the mounting center of the adsorbing nozzles ime of installation causing cracking the bottom dead center of the a recting the warpage of the circuing pressure at the time of installation ace installation, to minimize the face of the circuit board to supp win in the following. orbing nozzles so that their botto	occur on the capacitor bo ss, at the time of position machine must be perform is too low, an excessive fing. Use the following can dsorbing nozzles to the up t board. Ton to 1 to 3 N or below in impact of the adsorbing no ress the deflection of the om dead center at the time of positioning, the mechan chipping or cracking on th he positioning claw, and p	ody and that an excessive ing, is not applied to the ed regularly. orce will be applied to the utions for your reference. oper surface of the circuit static load. ozzles, apply a support pin circuit board. A typical e of installation is not ical impact applied to the e capacitor. To prevent erform the maintenance,
			recommende	d aaaaa
		Cases that should be avoided	recommende	
	One surface installation	Crack		

 One surface
 Image: Crack of addition

 Installation
 Image: Crack of addition

 Double surface
 Image: Crack of addition

 Separation
 Image: Crack of addition

 Support pin
 Image: Crack of addition

CLASSIFICATION	SPECIFICATIONS	S	^{No.} 151	S-ECJ-SS001E
SUBJECT	Multilayer Ceramic Chip (Capacitor	PAGE	7 of 12
	Common Specifications (Preca	utions for Use)	DATE	1st. Apr. 2002
1. 2. 4 Sele	ction of Flux			
Flux	may seriously affect the performance of th	ne capacitor. Therefore, check	the follow	ing before use.
(1) Us	se flux having a halogen based content of 0	0.1 wt. % (converted to chlorine)	or below.	
	o not use flux with strong acid.			
(2) Th	ne coated amount of flux when the capacito	or is soldered to the circuit boar	d must be	confirmed.
(3) Wł	hen using soluble flux, wash clean the capa	citor sufficiently.		
1. 2. 5 Sold	ering			
1. 2. 5. 1	Flow Soldering			
	By flow-soldering, stress due to an abrupt	t temperature change is applied	directly to	the part body.
	Therefore, take sufficient care to control t			
	Capacitors particularly dislike abrupt heati		-	-
	cooled, a strain will be produced inside the may cause thermal cracking. To prevent			
	difference.		:	
	(1) Coating of flux: Apply a thin coat of flu	ux uniformly. For flow-solderin	g, the coat	ing of flux using
	the foaming method is generally used.			
	(2) Preheating: Sufficiently preheat the ca	apacitor so that a difference be	tween the	solder
	temperature and the surface tempera	ture of the capacitor is $150^\circ C$ of	or below (1	00 to 130°C).
	(3) Immersion into solder: Immerse the ca	apacitor in a molten solder bath	of 240 to 2	260°C for 3 to 5
	seconds.			
	(4) After soldering, gradually cool the cap	acitor. Avoid cooling it abruptl	y (forcibly)). Failure to do
	so may cause thermal cracking.			
	(5) Cleaning: If the capacitor is immersed	into the cleaning solvent imme	diately afte	er soldering,
	confirm that the surface temperature	of the capacitor is $100^\circ C$ or be	low before	ehand.
	(6) The one time of flow-soldering in the	conditions shown in the figure b	elow [reco	ommended
	profile of flow-soldering (example)] do	o not cause any problems.		
	However, take sufficient care with reg	gards to warpage and possible d	eflection o	f the circuit
	board.			
	Recommended profile	e of Flow Soldering [Ex.]		
	Recommended prom	C OI T IOW CONCERNING [EX.]		
	240 Soldering			
	~260°C	Gradual cooling (Leave undisturbed		
	Temp.	at room temperature)		
	(°C) (3°)			
		Time		
	الاستى 60∼120s 3∼5s			
	60~120s 3~5s			
	〈Allowable temper	rature difference $\Delta T \rangle$		
	Size	Temp. Tol.		
	0603 to 1206	∆T≦150°C		
	0508,0612			

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SUBJECT	Multilayer Cera	mic Chip Ca	acitor		PAGE	8 of 12	
	Common Specificatio	ns (Precauti	ons for Use)		DATE	1st. Apr. 2002	
1. 2. 5. 2	Reflow Soldering						
	The temperature conditions for	r reflow solderin	ig are formed of	the temperati	ure curve	s of the preheat	
	section, temperature rise sec					·	
	If heat is abruptly applied to a	-	-	-		due to the large	
	temperature difference, which	may cause the	mal cracking.	To prevent thi	s problen	n, take sufficient	
	care with the temperature dif		-		-		
	The preheat section is a critic	al area for prev	ention of tombs	stone (chip sta	nding) an	ld, therefore,	
	control the temperature with	sufficient care.					
	(1) Preheat: Increase the su	face temperatu	re of the circuit	board to 140	to 160°C		
	(2) Temperature increasing s	tage : 150 to 22	0°C at a rate c	of 2 to 5°C/sec	.		
	(3) Heating section: $220^{\circ}C$ c	r above within 2	0 sec.				
	(4) Gradual cooling section: Leave undisturbed at room temperature						
	Avoid cooling the gradua	cooling sectior	abruptly (forcil	oly). Failure t	o do so r	nay cause	
	thermal cracking.						
	230 to 100°C at a rate of 1 to $4^{\circ}C/sec$.						
	(5) Cleaning: If the capacitor					oldering, confirm	
	that the surface tempera						
	(6) The two times of flow-so				elow [Re	commended	
	profile of reflow-solderin						
	However, take sufficient board.	care with regard	is to warpage a	nd the possible	deflection	on of the circuit	
					_		
	240		③Solderi	ng			
	~260°C	1		-			
	220°C	-					
	Temp.	T		(4)Cooling			
	(°C)	<u> </u>					
			2 Temp.				
	/	①Preheating1	increasing				
			stage	Tim			
		→ ls min.			6		
			20s ma:	Χ.			
	7	120s max.	1				
		le temperature		<u>r></u>			
	Siz		Temp. Tol.				
	0201 to 1		∆T≦150℃				
	0508,06	IZ					

1. 2. 5. 3 Soldering with soldering iron

1210 to 2220

In soldering with a soldering iron, stress due to an abrupt temperature change is applied directly to the capacitor body. Accordingly, carefully control the temperature of the soldering iron tip. Take care that the soldering iron tip does not come directly into contact with the capacitor body and the terminal electrode.

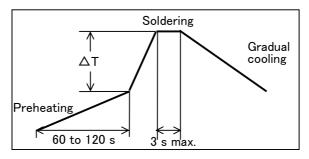
∆T≦130°C

CLASSIFICATION	SPECIFICATIONS		No. 151S-ECJ-SS001E	
SUBJECT Multilayer Ceramic Chip Capacitor		PAGE	9 of 12	
	Common Specifications (Precautions for Use)	DATE	1st. Apr. 2002	

Capacitors particularly dislike abrupt heating and cooling. If the capacitor is abruptly heated or cooled, a strain will be produced inside the capacitor due to the large temperature difference, which may cause thermal cracking. To prevent this problem, take sufficient care of the temperature difference. Solder with the soldering iron taking care so as not to heat or cool abruptly before and after the soldering. The product once removed with the soldering iron cannot be re-used.

- (1) Condition 1 (with preheating)
 - 1) Solder: Use a wire solder requiring a smaller amount of flux chlorine for precision electronic equipment (wire diameter: 1.0 mm dia. or less).
 - 2) Preheating: Preheat sufficiently so that the difference between the solder temperature and the surface temperature of the capacitor is 150°C or below.
 - 3) Iron tip temperature: $300^{\circ}C$ or below
 - (Fuse the required amount of solder at the tip of the soldering iron beforehand.)
 - 4) Gradual cooling: After soldering, leave the capacitor undisturbed at room temperature to allow it to cool gradually.

Recommended profile for soldering with a soldering iron[Ex.]



Allowable temperature	difference	$\Delta T \rangle$
-----------------------	------------	--------------------

Size	Temp. Tol.	
0201 to 1206	∆T≤150℃	
0508,0612		
1210 to 2220	∆T≦130°C	

(2) Condition 2 (without preheating)

Without preheating, the soldering iron can be corrected within the range specified below.

- 1) The soldering iron tip must not directly touch the ceramic dielectric of the capacitor.
- 2) After preheating the land section sufficiently with the soldering iron tip, slide the soldering iron tip to the terminal electrode of the capacitor for soldering.

Conditions of soldering non-tip without preneating					
Condition					
Chip size	0201 to 0805 , 0508	1206 to 2220 , 0612			
Temperature of soldering iron	270°C Max.	250°C Max.			
Wattage	20W Max.				
Shape of soldering iron tip	ϕ 3mm Max.				
Soldering time with soldering iron	3s Max.				

Conditions of soldering iron tip without preheating

1. 2. 6 Cleaning

- (1) If the cleaning solvent is not appropriate, residue and other foreign matter of the flux may adhere to the surface of the capacitor and deteriorate the performance (particularly, insulation resistance) of the capacitor.
- (2) If the cleaning conditions are not appropriate (insufficient cleaning, excessive cleaning), the performance of the capacitor may be impaired.
 - 1) If cleaning is insufficient:
 - ① The metal of the terminal electrode may be corroded by the halogen substance contained in the residue of the flux.
 - (2) The halogen substance contained in the residue of the flux may adhere to the surface of the capacitor and lower the insulation resistance.
 - (3) The tendencies of items 1) and 2) above may be remarkable for soluble flux more than those for rosin flux.
 - 2) If cleaning is excessive:
 - (1) For ultrasonic cleaning, if output is too large, the circuit board may cause resonance to develop cracking in the body of the capacitor or solder, which will lower the strength of the terminal electrode.
 - To prevent these problems, perform cleaning as follows.
 - Ultrasonic wave output: 20 W/L or below
 - Ultrasonic wave frequency: 40 kHz or below
 - Ultrasonic wave cleaning time: 5 min. or shorter
 - 3) If the cleaning solvent is contaminated, the density of liberated halogen may be increased to induce the same results as those obtained when the cleaning is insufficient.

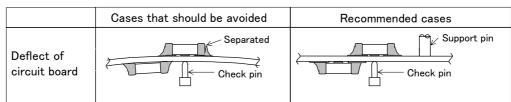
1. 2. 7 Inspections

When inspecting a capacitor on the circuit board after installation, check whether the circuit board is fixed by a support pin or a dedicated jig.

- (1) Take care so that the circuit board is not deflected by the pressure of the check pin.
- (2) Take care so that the circuit board is not vibrated by the impact at the time of contact.

When the operational check of the circuit board is performed, the pressing force of the check pin may be increased to prevent poor contact of the check pin of the board checker.

By the force, the circuit board may be deflected, and the capacitor may be broken or the solder at the terminal electrode may be separated by the stress due to the deflection. Accordingly, referring to the following figure, take an appropriate measure against possible deflection of the circuit board.



1. 2. 8 Protective Coat

(1) When resin is coated on the installation surface for moistureproofing and dustproofing after the capacitor is installed on the circuit board, check the actual equipment that the quality of the capacitor is not affected by the protective coat.

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SUBJECT	Multilayer Ceramic Chip Capacitor	PAGE	11 of 12
	Common Specifications (Precautions for Use)	DATE	1st. Apr. 2002

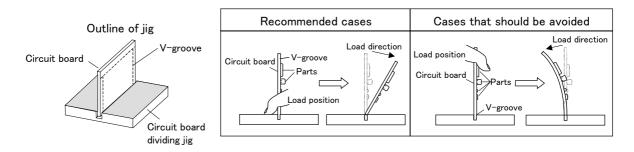
- (2) Select those materials which do not generate cracked gas nor reaction gas that may affect the members forming the capacitor.
- (3) If large stress is applied to the capacitor due to thermal expansion or thermal contraction at the time of curing the resin, cracking may occur in the capacitor.
- 1. 2. 9 Division of multiple printed circuit board
 - (1) During the circuit board dividing operation after the installation of the parts including the capacitor, take care not to provide deflective or torsional stress to the circuit board.
 - If stress such as deflection or torsion, shown in the following figure, is applied to the circuit board when the circuit board is divided, cracking may occur in the capacitor. To prevent this problem, take care not to apply any stress to it.



- (2) When dividing a circuit board, avoid dividing manually, but use a dedicated jig to prevent mechanical stress from being applied to the circuit board.
- (3) Example of circuit board dividing jig

The outline of the circuit board dividing jig is shown below. It is recommended that you hold the circuit board at the portion near the jig so that the board is not deflected and divide the stress caused so that only compressive stress is applied to the part such as the capacitor.

Avoid holding the circuit board at any position apart from the jig, as the board will be easily deflected, and divide it so that tensile stress is not applied to the capacitor, which may cause cracking in the capacitor

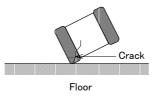


1. 2. 10 Mechanical Impact

(1) Take care not to apply any excessive mechanical impact to the capacitor.

Since the capacitor body is made of ceramics, it may become damaged or cracked by a drop impact. The quality of the dropped capacitor may already be lost, and its failure level of significance may be increased. Never use it.

Particularly, capacitors of a large size tend to be damaged or cracked more easily.



CLASSIFICATION	SPECIFICATIONS	No. 151S-ECJ-SS001E				
SUBJECT	Multilayer Ceramic Chip Capacitor	PAGE 12 of 12				
	Common Specifications (Precautions for Use)	DATE 1st. Apr. 2002				
(2)	(2) When handling a circuit board with a capacitor, take care that another circuit board does not					
	collide with the capacitor.					
When circuit boards after installation are stored in a stacked state or handled, the them may collide with a capacitor causing damage or cracking in the capacitor by t						
						which may lead to a deterioration of the withstand voltage and a reduction in insu resistance.
	Circuit	boards				
	Crack after in	stallation				
1.3 Remarks						
The above o	cautions are typical ones.					
For special i	installation conditions, contact us.					
Cautions of	Operations above are from					
The Tech	nical Report EIAJ RCR-2333 Caution Guide Line					
	tion of Fixed Multilayer Ceramic Capacitors for					
	Equipment by Electronic Industries Association					
	(March 1995 issued)					
or dapan.						
The Techr	nical Report EIAJ RCR-2335 Caution Guide					
	peration of Fixed Multilayer Ceramic Capaci-					
	lectronic Equipment by Japan Electronics &					
	n Technology Industries Association					
	etment in 2002)					
Please refer	to above technical report for details.					
Note ;						

CLASSIFICATION	ICATION SPECIFICATIONS	
SUBJECT	SUBJECT Multilayer Ceramic Chip Capacitor	
Taped and Reeled Packaging Specifications		DATE 1st. Apr. 2002

1. Scope

This specification applies to taped and reeled packing for MATSUSHITA's multilayer ceramic chip capacitors.

2. Applicable Standards

EIAJ (Electric Industries Association of Japan) Standard EIAJ RC-1009B JIS (Japanese Industrial Standard) Standard JIS C 0806

3. Packing Specification

3. 1 Structure and Dimensions

Paper taping packaging is carried out according the following diagram

(1) Carrier tape : Shown in Fig. 5.

(2) Reel : Shown in Fig. 6.

(3) Packaging : We shall pack suitably in order prevent damage during transportation or storage.

3. 2 Packing Quantity

		Carrier ⁻	-Tape	Qu	antity (pcs.⁄ree	I)
Type Thickness of				ϕ 180mm Reel		ϕ 330m	m Reel
.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Capacitor(mm)	Material	1 0	Packaging Code	Quantity	Packaging Code	Quantity
"06"(0201)	0.30 ± 0.03	Paper Taping	2mm	E	15000		
"10"(0402)	0.50 ± 0.05	Paper Taping	2mm	E	10000	W	50000
"11"(0603)	0.8 ± 0.1	Paper Taping	4mm	V	4000	Z	10000
	0.6 ± 0.1	Paper Taping	4mm	V	5000	Z	20000
"12"(0805)	0.85 ± 0.10	Paper Taping	4mm	V	4000	Z	10000
	$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	Embossed Tap.	4mm	F	3000		
	0.6 ± 0.1	Paper Taping	4mm	V	5000	Z	20000
	0.85 ± 0.10	Paper Taping	4mm	V	4000	Z	10000
"13"(1206)	1.15 ± 0.10	Embossed Tap.	4mm	F	3000		
	1.15 ± 0.10	Embossed Tap.	4mm	Y	2000		
	1.6 ± 0.2	Embossed Tap.	4mm	Y	2000		
"23"(1210)	2.0 ± 0.2	Embossed Tap.	4mm	Y	2000		
	2.5 ± 0.3	Embossed Tap.	4mm	Y	1000		
"34"(1812)	2.5 ± 0.3	Embossed Tap.	8mm	Y	500		
	3.2 ± 0.3	Embossed Tap.	8mm	Y	500		

Х	Explanation	of Part Numbers	(Example)
	ECJ	1	V

Packaging Code

1C

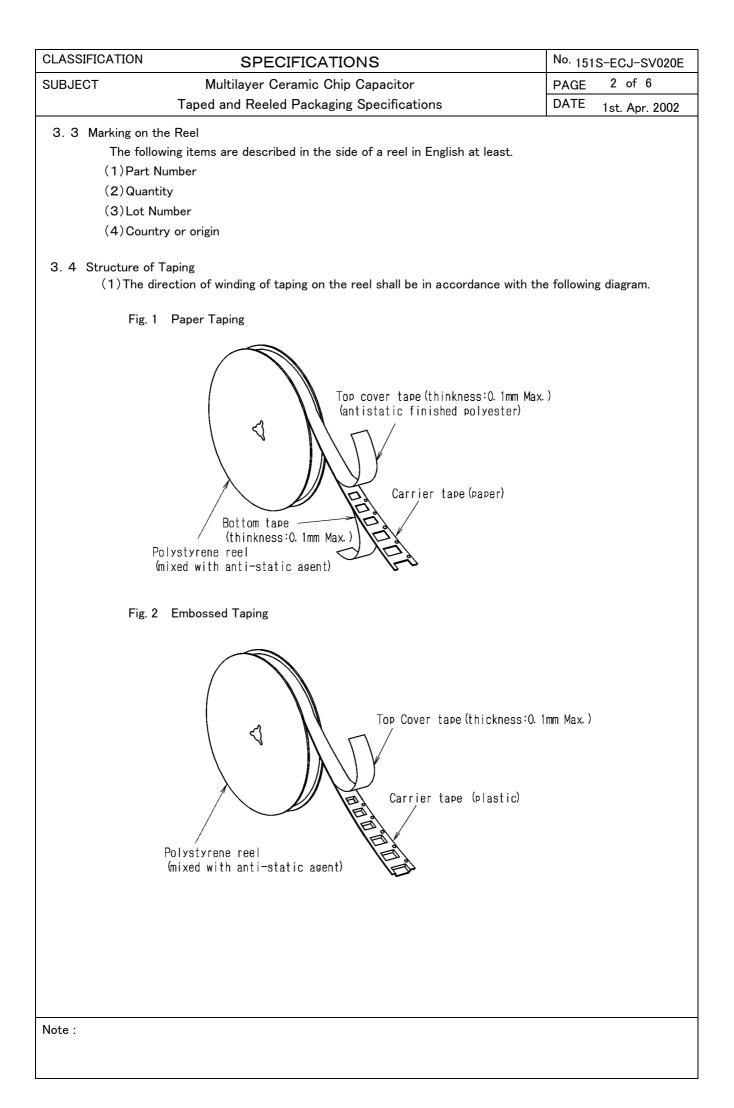
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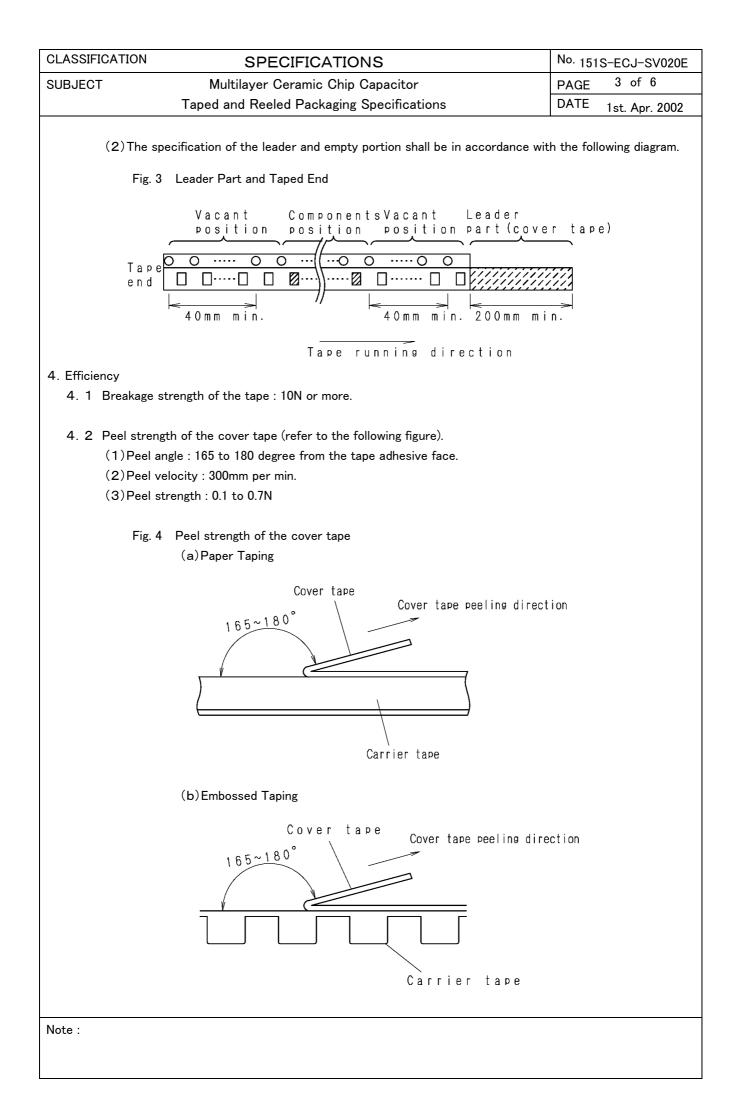
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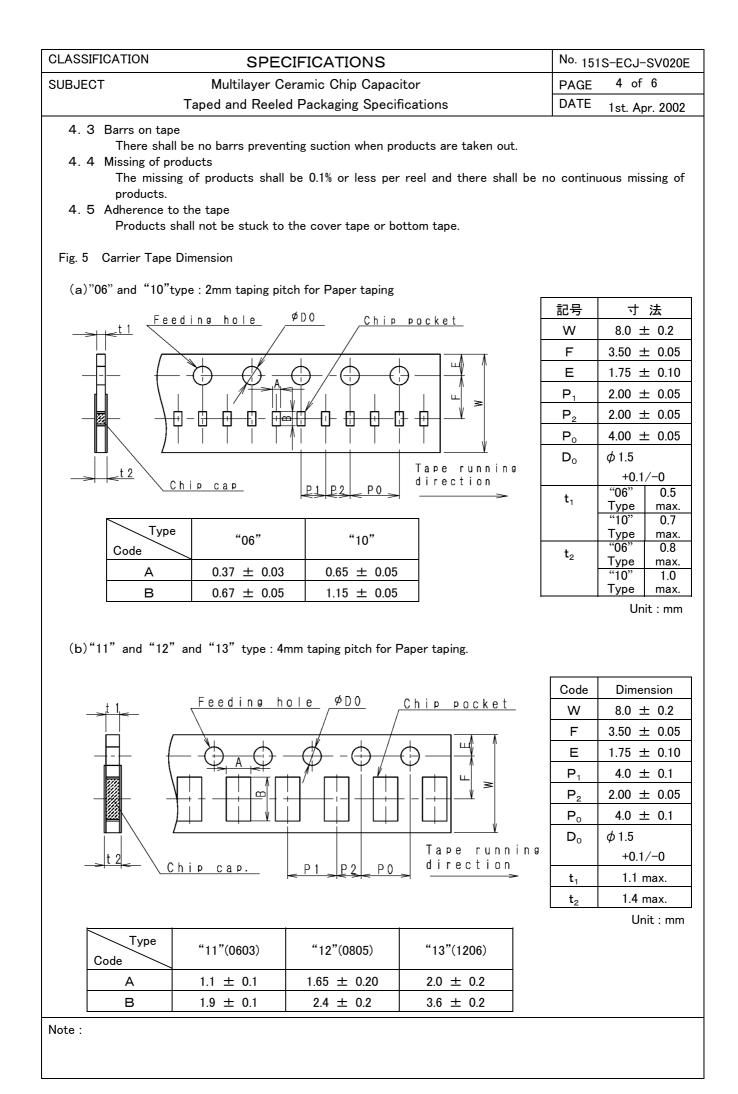
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Note :

Ceramic Business Unit LCR Device Company	APPROVAL	CHECK	DESIGN
Matsushita Electronic Components Co.,Ltd.			
Kadoma, Osaka, Japan	H.Itow	A.Omi	T.Shinriki





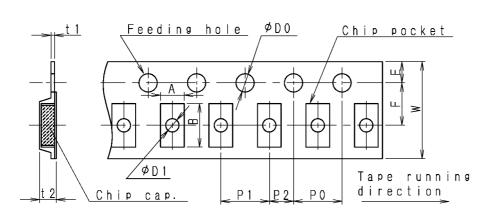


CLASSIFICATION

SUBJECT

ION	SPECIFICATIONS	No. 151	S-ECJ-SV020E
	Multilayer Ceramic Chip Capacitor	PAGE	5 of 6
	Taped and Reeled Packaging Specifications	DATE	1st. Apr. 2002

(c) "12" and "13" and "23" type : 4mm chip taping pitch for Embossed taping.

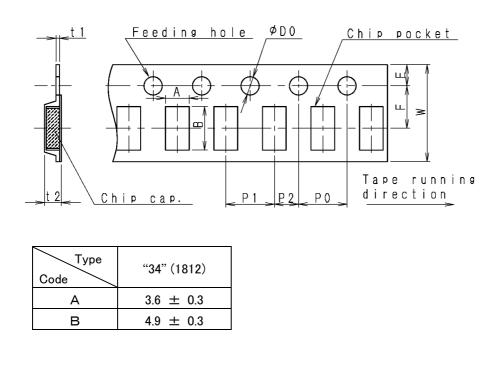


Code	Dimension	
W	8.0 ±	0.2
F	3.50 ±	0.05
Е	1.75 ±	0.10
P_1	4.0 ±	0.1
P ₂	2.00 ±	0.05
Po	4.0 ± 0.1	
D_0	φ1.5	
	+0.1/	/-0
D_1	ϕ 1.1 ± 0.1	
t ₁	0.6 max.	
	"12""13"	2.5
t ₂	type	max.
	"23"type	3.5
	20 type	max.

Unit : mm

Type Code	"12" (0805)	"13" (1206)	"23" (1210)
А	1.55 ± 0.20	1.95 ± 0.20	2.9 ± 0.2
В	2.35 ± 0.20	3.6 ± 0.2	3.6 ± 0.2

(d) "34" type : 8mm chip taping pitch for Embossed taping.



Code	Dimension	
W	12.0 ± 0.3	
VV	12.0 ± 0.3	
F	5.50 ± 0.05	
E	1.75 ± 0.10	
P ₁	8.0 ± 0.1	
P ₂	2.00 ± 0.05	
Po	4.0 ± 0.1	
Do	φ1.5	
	+0.1/-0	
t ₁	0.6 max.	
t ₂	4.0max.	

Unit : mm

Note :

