

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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**SWITCHING  
DUAL N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

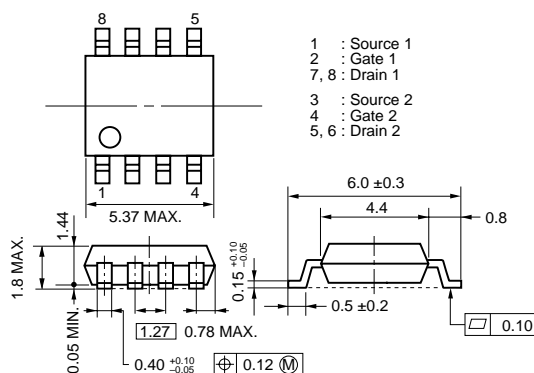
**DESCRIPTION**

The μ PA1764 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

**FEATURES**

- Dual chip type
- Low on-state resistance  
 $R_{DS(on)1} = 27 \text{ m}\Omega \text{ TYP. (} V_{GS} = 10 \text{ V, } I_D = 3.5 \text{ A)}$   
 $R_{DS(on)2} = 32 \text{ m}\Omega \text{ TYP. (} V_{GS} = 4.5 \text{ V, } I_D = 3.5 \text{ A)}$   
 $R_{DS(on)3} = 34 \text{ m}\Omega \text{ TYP. (} V_{GS} = 4.0 \text{ V, } I_D = 3.5 \text{ A)}$
- Low input capacitance  
 $C_{iss} = 1300 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

**PACKAGE DRAWING (Unit : mm)**



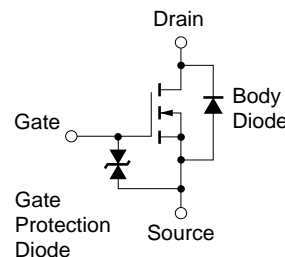
**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μPA1764G	Power SOP8

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±7	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±28	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	P <sub>T</sub>	1.7	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to + 150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	7	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	98	mJ

**EQUIVALENT CIRCUIT  
(1/2 Circuit)**



**Notes 1.** PW ≤ 10 μs, Duty cycle ≤ 1%

**2.** T<sub>A</sub> = 25°C, Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 30 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = 20 → 0 V

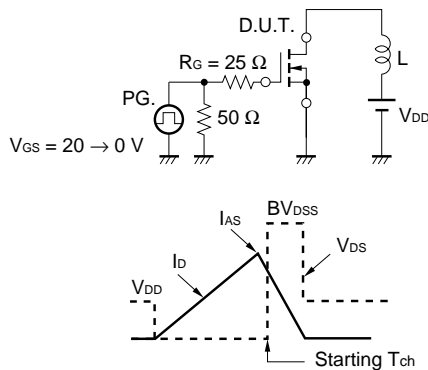
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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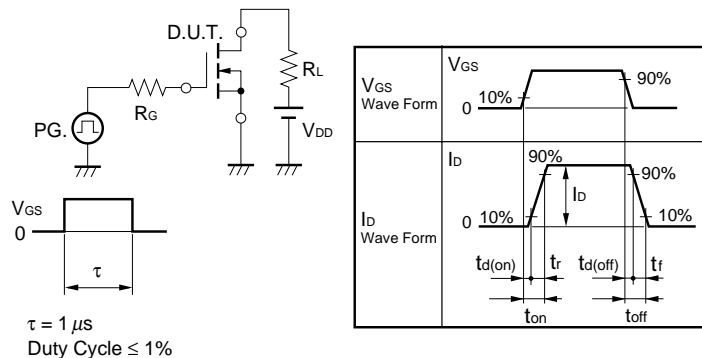
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A	5.0	9.0		S
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A		27	35	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.5 A		32	42	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 3.5 A		34	46	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		1300		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		230		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		110		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 3.5 A		15		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		69		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		65		ns
Fall Time	t <sub>f</sub>			27		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 48 V		29		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		3.6		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 7.0 A		7.4		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 7.0 A, V <sub>GS</sub> = 0 V		0.84		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 7.0 A, V <sub>GS</sub> = 0 V		40		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		66		nC

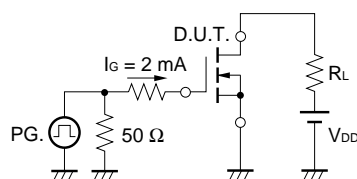
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



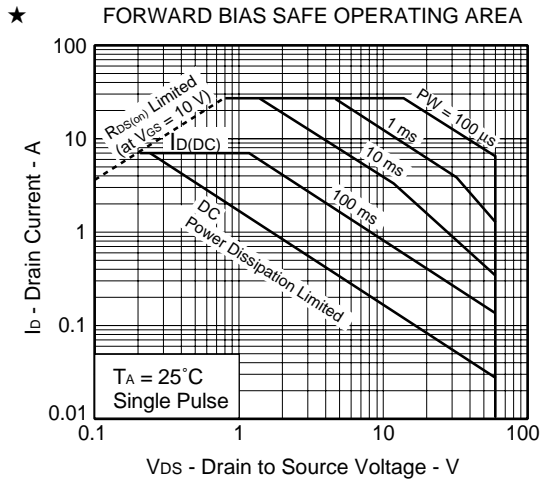
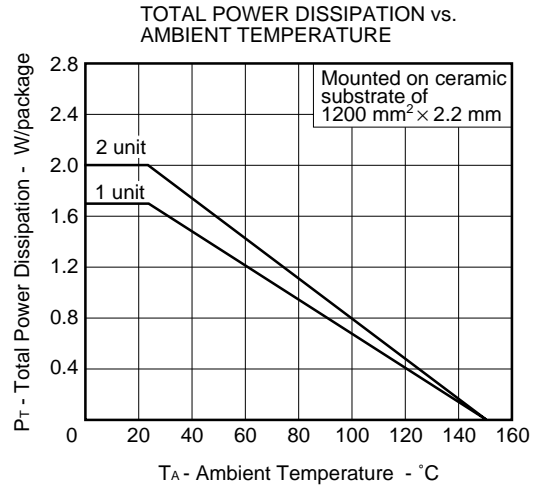
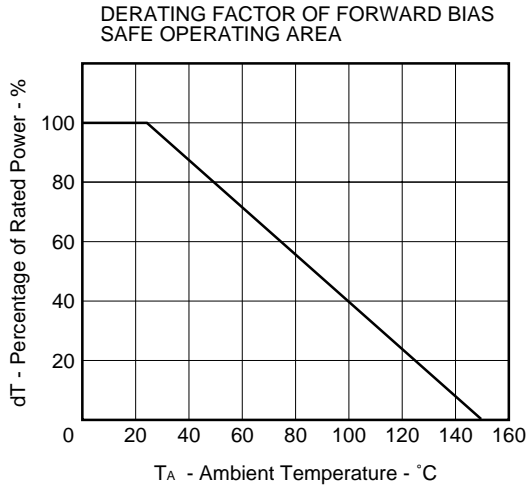
**TEST CIRCUIT 2 SWITCHING TIME**



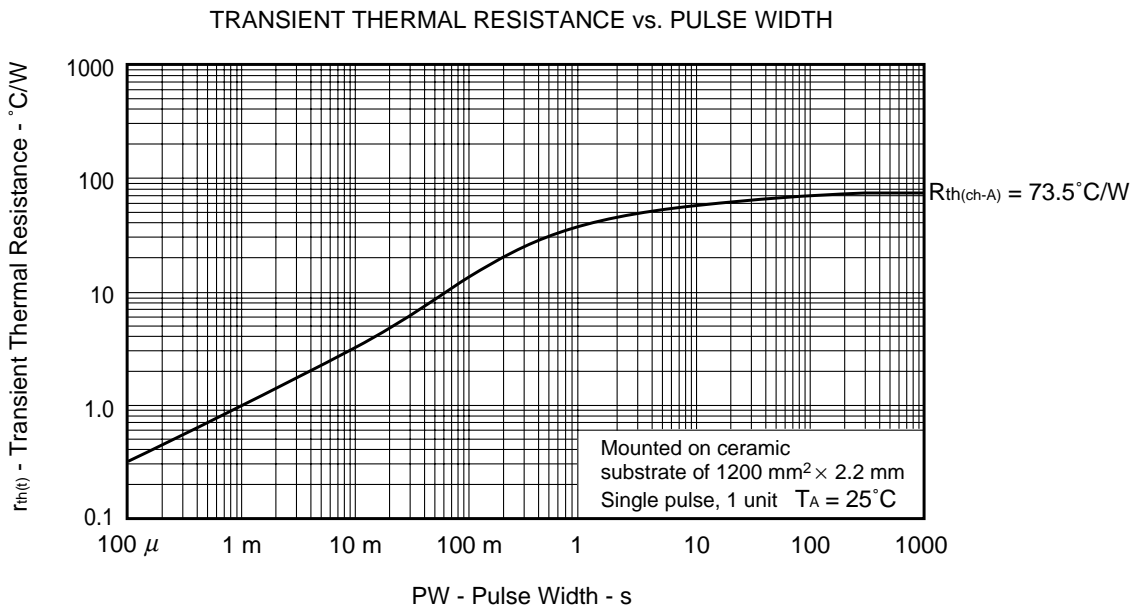
**TEST CIRCUIT 3 GATE CHARGE**



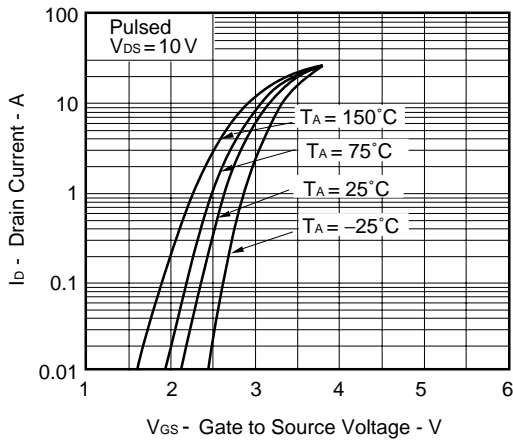
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)



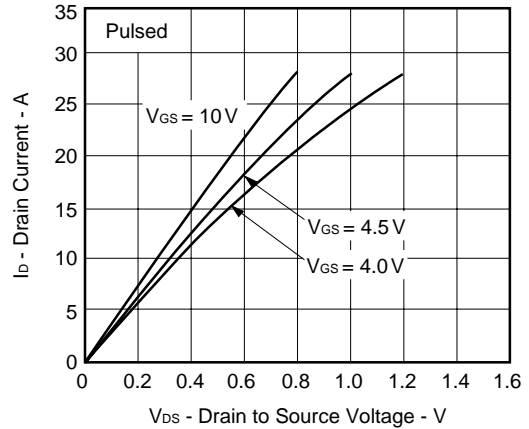
**Remark**  
Mounted on ceramic substrate of 1200 mm<sup>2</sup> × 2.2 mm



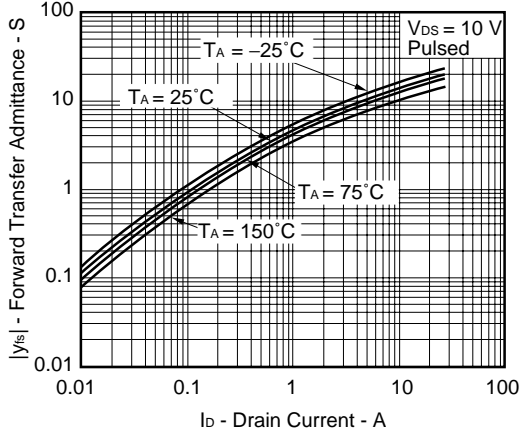
FORWARD TRANSFER CHARACTERISTICS



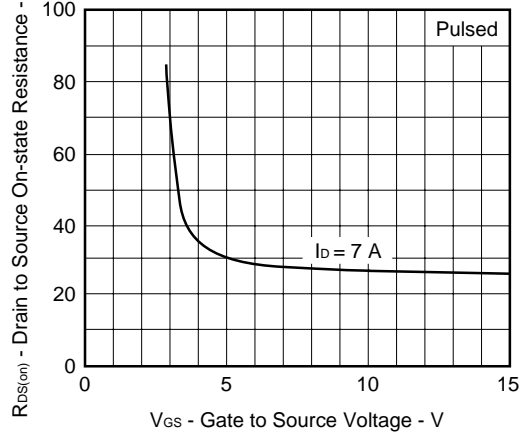
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



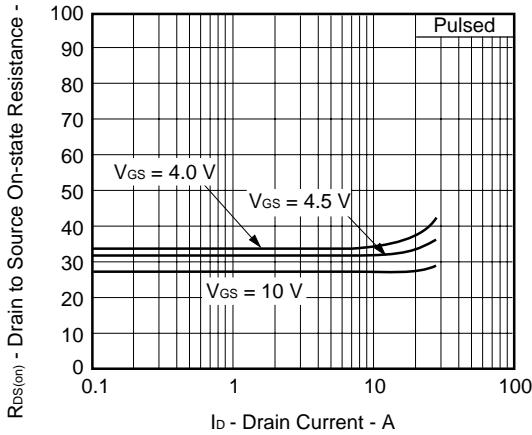
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



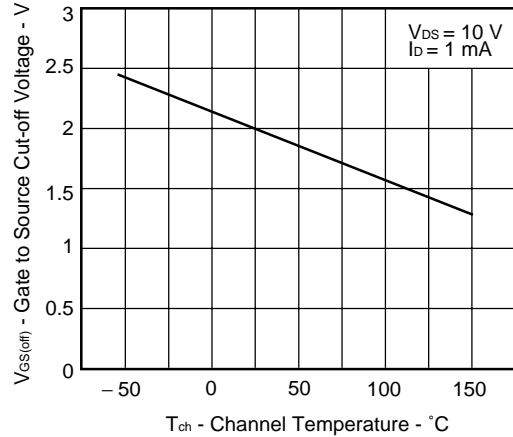
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

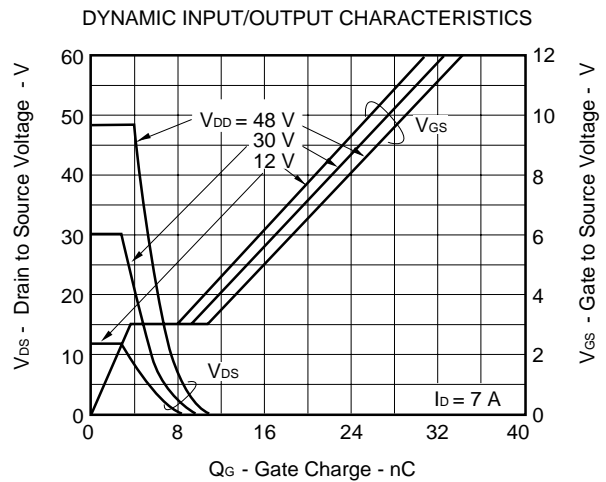
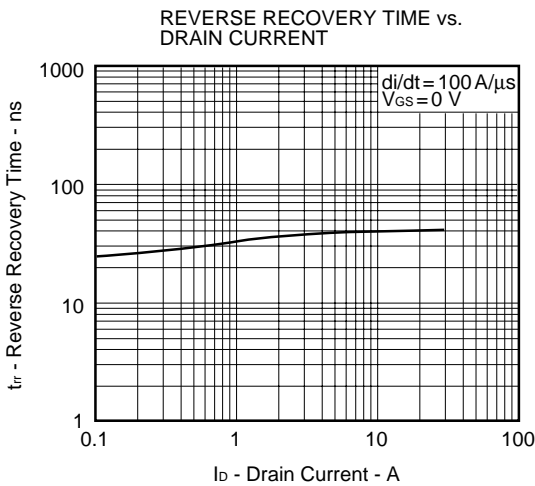
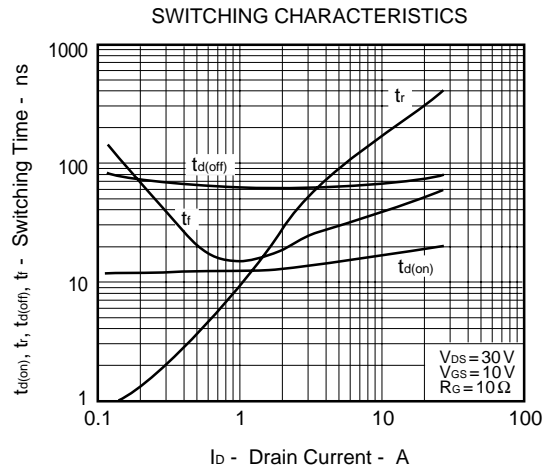
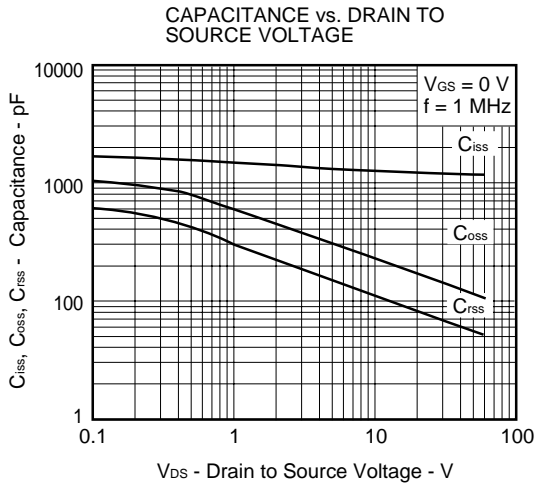
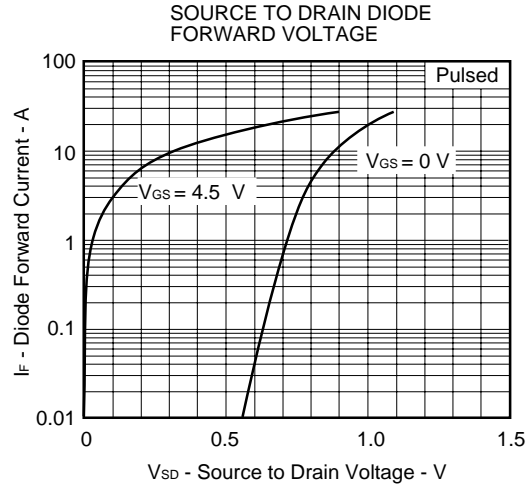
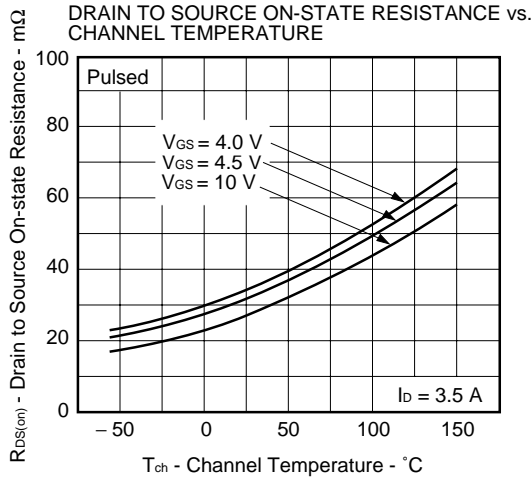


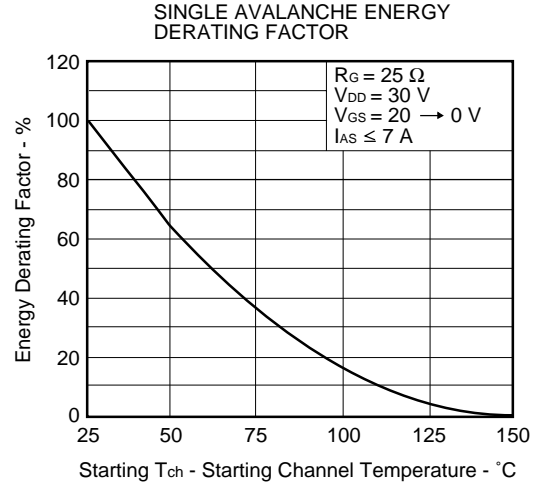
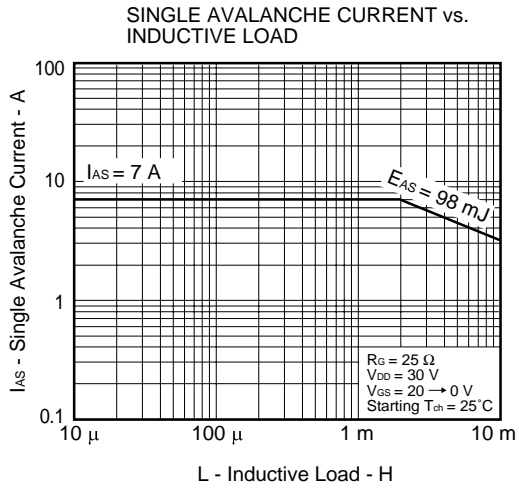
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE









[MEMO]

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