

# DATA SHEET

## **74LVT534**

**3.3 V Octal D-type flip-flop; inverting  
(3-State)**

Product data  
Supersedes data of 1998 Feb 19

2004 Aug 25

### 3.3 V Octal D-type flip-flop, inverting (3-State)

### 74LVT534

#### FEATURES

- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

#### DESCRIPTION

The LVT534 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ( $\overline{OE}$ ) control gates. The state of each D input (one set-up time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the clock operation.

When  $\overline{OE}$  is LOW, the stored data appears at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance "off" state, which means they will neither drive nor load the bus.

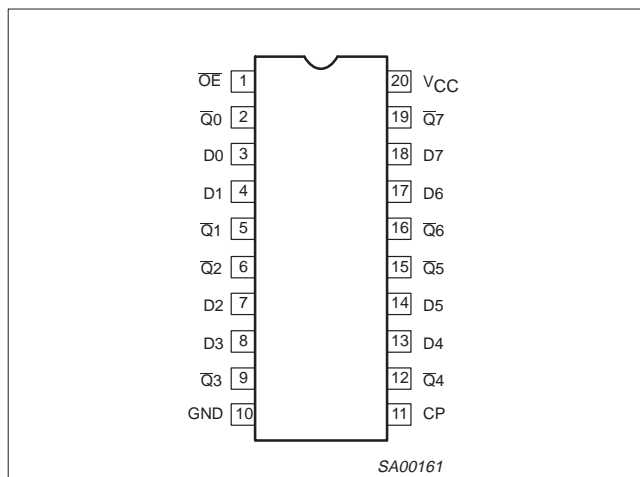
#### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}; \text{GND} = 0\text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $Q_n$	$C_L = 50\text{ pF};$ $V_{CC} = 3.3\text{ V}$	3.0 3.5	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{ V or }3.0\text{ V}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_{I/O} = 0\text{ V or }3.0\text{ V}$	7	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{ V}$	0.13	mA

#### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
20-Pin Plastic SOL	-40 °C to +85 °C	74LVT534D	SOT163-1
20-Pin Plastic SSOP Type II	-40 °C to +85 °C	74LVT534DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40 °C to +85 °C	74LVT534PW	SOT360-1

#### PIN CONFIGURATION



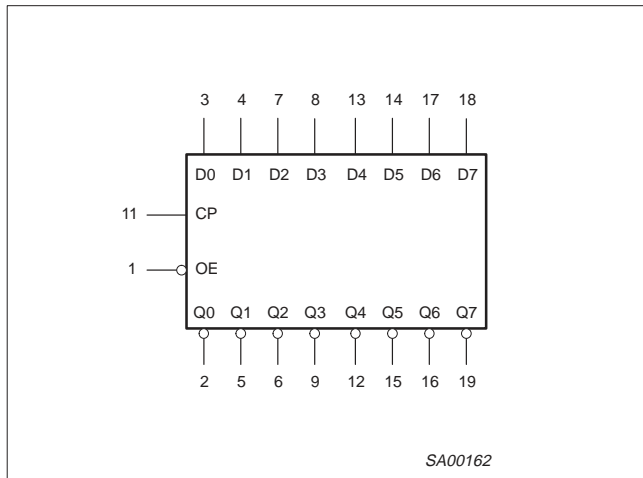
#### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-LOW)
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0}$ to $\overline{Q7}$	Inverting 3-State outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0 V)
20	$V_{CC}$	Positive supply voltage

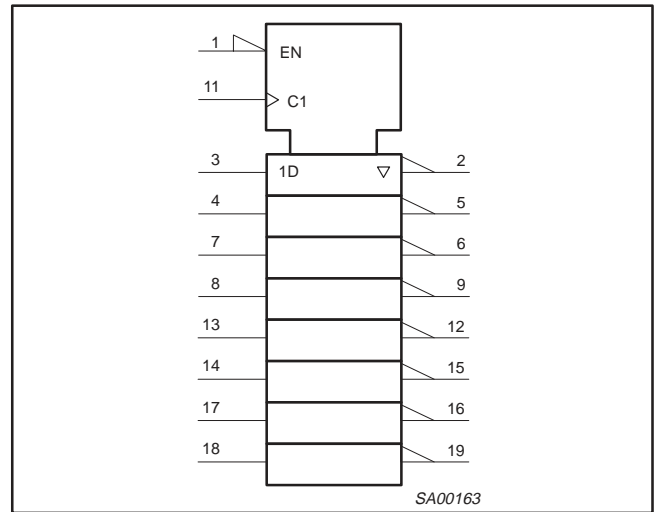
# 3.3 V Octal D-type flip-flop, inverting (3-State)

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## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

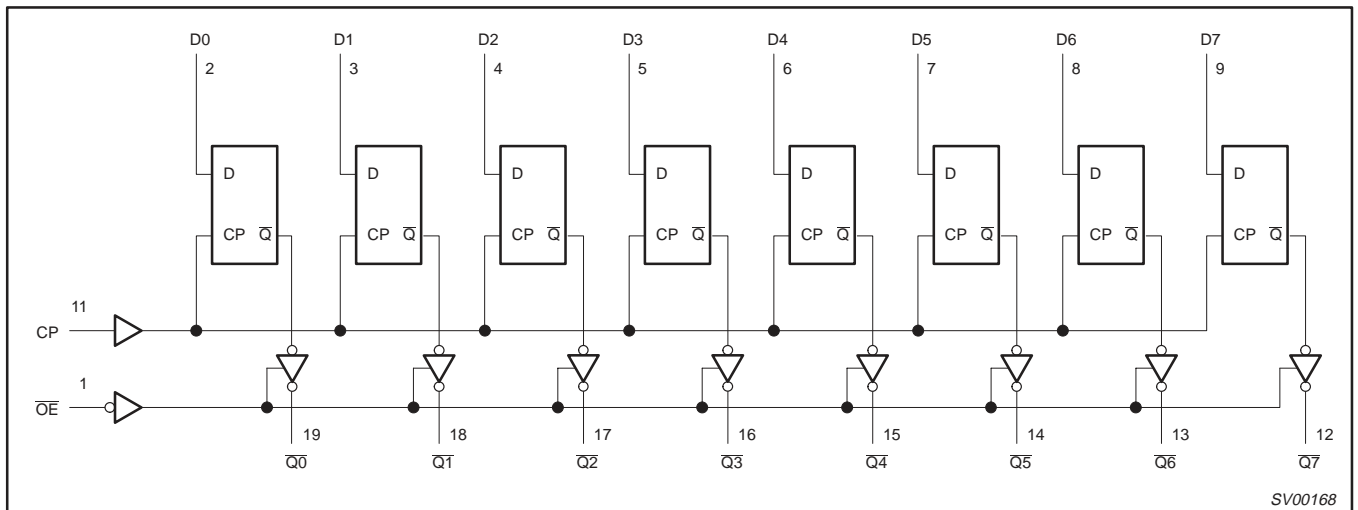


## FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OE	CP	Dn		Q0 to Q7	
L	↑	l	L	H	Latch and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
 NC= No change  
 X = Don't care  
 Z = high-impedance "off" state  
 ↑ = LOW-to-HIGH clock transition  
 ↕ = not a LOW-to-HIGH clock transition

## LOGIC DIAGRAM



## 3.3 V Octal D-type flip-flop, inverting (3-State)

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0 V	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0 V	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or HIGH state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in LOW state	128	mA
		Output in HIGH state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	2.0	-	V
V <sub>IL</sub>	Input voltage	-	0.8	V
I <sub>OH</sub>	HIGH-level output current	-	-32	mA
I <sub>OL</sub>	LOW-level output current	-	32	mA
	LOW-level output current; current duty cycle ≤ 50 %, f ≥ 1 kHz	-	64	
Δt/Δv	Input transition rise or fall rate; outputs enabled	-	10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			$T_{amb} = -40^{\circ}\text{C to }+85^{\circ}\text{C}$				
			MIN	TYP <sup>1</sup>	MAX		
$V_{IK}$	Input clamp voltage	$V_{CC} = 2.7\text{ V}; I_{IK} = -18\text{ mA}$	–	–0.9	–1.2	V	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}; I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	–	V	
		$V_{CC} = 2.7\text{ V}; I_{OH} = -8\text{ mA}$	2.4	2.5	–	V	
		$V_{CC} = 3.0\text{ V}; I_{OH} = -32\text{ mA}$	2.0	2.2	–	V	
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7\text{ V}; I_{OL} = 100\text{ }\mu\text{A}$	–	0.1	0.2	V	
		$V_{CC} = 2.7\text{ V}; I_{OL} = 24\text{ mA}$	–	0.3	0.5	V	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$	–	0.25	0.4	V	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$	–	0.3	0.5	V	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 64\text{ mA}$	–	0.4	0.55	V	
$V_{RST}$	Power-up output low voltage <sup>5</sup>	$V_{CC} = 3.6\text{ V}; I_O = 1\text{ mA}; V_I = \text{GND or }V_{CC}$	–	0.13	0.55	V	
$I_I$	Input leakage current	$V_{CC} = 0\text{ V or }3.6\text{ V}; V_I = 5.5\text{ V}$	–	1	10	$\mu\text{A}$	
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$	Control pins	–	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}$	Data pins <sup>4</sup>	–	0.1	1	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}; V_I = 0\text{ V}$		–	–1	–5	$\mu\text{A}$
$I_{OFF}$	Output off current	$V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 0\text{ V to }4.5\text{ V}$	–	1	$\pm 100$	$\mu\text{A}$	
$I_{HOLD}$	Bus Hold current A inputs <sup>7</sup>	$V_{CC} = 3\text{ V}; V_I = 0.8\text{ V}$	75	150	–	$\mu\text{A}$	
		$V_{CC} = 3\text{ V}; V_I = 2.0\text{ V}$	–75	–150	–	$\mu\text{A}$	
		$V_{CC} = 0\text{ V to }3.6\text{ V}; V_{CC} = 3.6\text{ V}$	$\pm 500$	–	–	$\mu\text{A}$	
$I_{EX}$	Current into an output in the HIGH state when $V_O > V_{CC}$	$V_O = 5.5\text{ V}; V_{CC} = 3.0\text{ V}$	–	60	125	$\mu\text{A}$	
$I_{PU/PD}$	Power-up/down 3-State output current <sup>3</sup>	$V_{CC} \leq 1.2\text{ V}; V_O = 0.5\text{ V to }V_{CC}; V_I = \text{GND or }V_{CC}; \text{OE/OE} = \text{Don't care}$	–	1	$\pm 100$	$\mu\text{A}$	
$I_{OZH}$	3-State output HIGH current	$V_{CC} = 3.6\text{ V}; V_O = 3\text{ V}; V_I = V_{IL}\text{ or }V_{IH}$	–	1	5	$\mu\text{A}$	
$I_{OZL}$	3-State output LOW current	$V_{CC} = 3.6\text{ V}; V_O = 0.5\text{ V}; V_I = V_{IL}\text{ or }V_{IH}$	–	1	–5	$\mu\text{A}$	
$I_{CCH}$	Quiescent supply current <sup>3</sup>	$V_{CC} = 3.6\text{ V}; \text{Outputs HIGH}; V_I = \text{GND or }V_{CC}; I_O = 0\text{ mA}$	–	0.13	0.19	mA	
$I_{CCL}$		$V_{CC} = 3.6\text{ V}; \text{Outputs LOW}; V_I = \text{GND or }V_{CC}; I_O = 0\text{ mA}$	–	3	12	mA	
$I_{CCZ}$		$V_{CC} = 3.6\text{ V}; \text{Outputs Disabled}; V_I = \text{GND or }V_{CC}; I_O = 0\text{ mA}$ <sup>6</sup>	–	0.13	0.19	mA	
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 3\text{ V to }3.6\text{ V}; \text{One input at }V_{CC} - 0.6\text{ V}; \text{Other inputs at }V_{CC}\text{ or GND}$	–	0.1	0.2	mA	

## NOTES:

- All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25^{\circ}\text{C}$ .
- This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.
- This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 msec. From  $V_{CC} = 1.2\text{ V to }V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of 100  $\mu\text{sec}$  is permitted. This parameter is valid for  $T_{amb} = 25^{\circ}\text{C}$  only.
- Unused pins at  $V_{CC}$  or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- $I_{CCZ}$  is measured with outputs pulled to  $V_{CC}$  or down to GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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**AC CHARACTERISTICS**GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$f_{MAX}$	Maximum clock frequency	1	100	150	–	100	–	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to Qn	1	1.7 2.2	3.0 3.5	4.6 4.9	– –	5.4 5.2	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to HIGH and LOW level	3 4	1.7 1.7	3.2 3.3	5.4 5.5	– –	7.0 5.6	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from HIGH and LOW level	3 4	2.1 2.1	3.5 3.4	4.8 4.8	– –	5.3 4.6	ns

**NOTE:**1. All typical values are at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.**AC SETUP REQUIREMENTS**GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  °C to +85 °C.

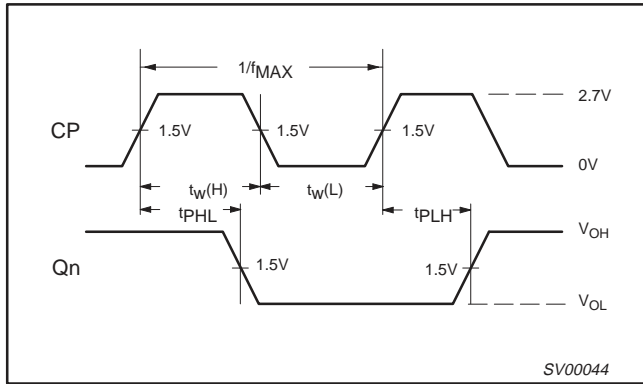
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$	
			MIN	TYP	MIN	
$t_{S(H)}$ $t_{S(L)}$	Setup time, HIGH or LOW, Dn to CP	2	2.0 2.6	1.0 1.3	2.0 3.2	ns
$t_{H(H)}$ $t_{H(L)}$	Hold time, HIGH or LOW, Dn to CP	2	0 0	–1.3 –0.9	0 0	ns
$t_{W(H)}$ $t_{W(L)}$	CP pulse width HIGH or LOW	1	1.5 4.2	0.8 3.0	1.5 5.0	ns

### 3.3 V Octal D-type flip-flop, inverting (3-State)

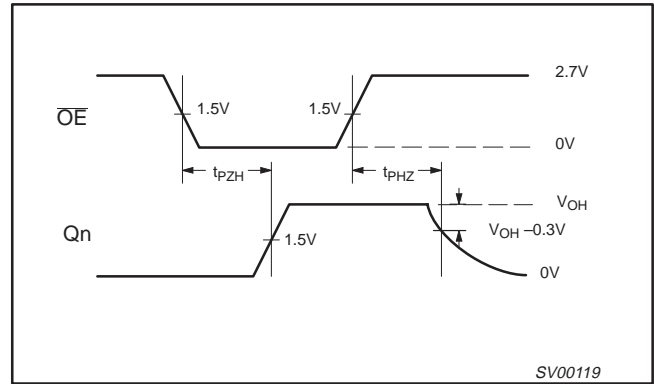
74LVT534

#### AC WAVEFORMS

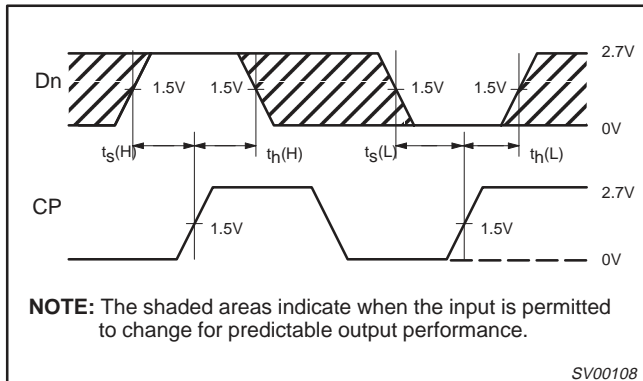
$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 2.7\text{ V}$



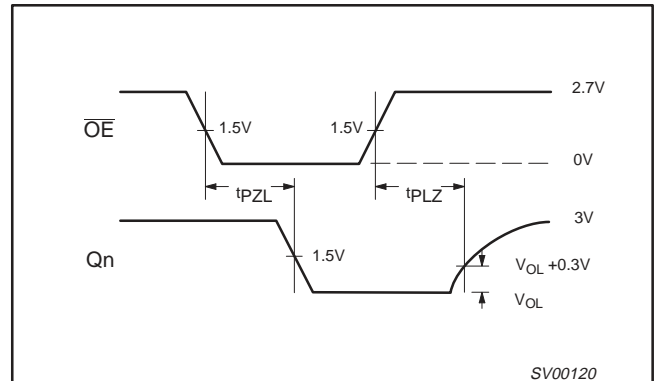
**Waveform 1. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency**



**Waveform 3. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level**



**Waveform 2. Data setup and hold times**

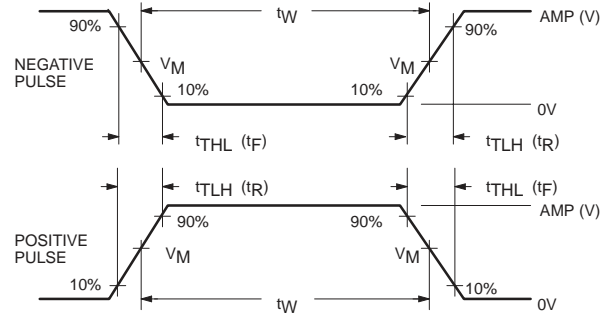
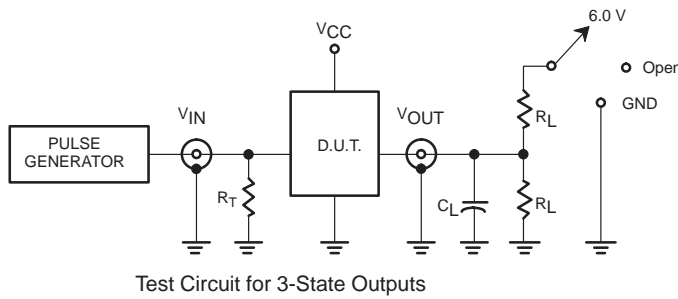


**Waveform 4. 3-State Output Enable time to LOW level and Output Disable time from LOW level**

### 3.3 V Octal D-type flip-flop, inverting (3-State)

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#### TEST CIRCUIT AND WAVEFORM



$V_M = 1.5\text{ V}$   
Input Pulse Definition

#### SWITCH POSITION

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

#### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_F$
74LVT	2.7 V	$\leq 10\text{ MHz}$	500 ns	$\leq 2.5\text{ ns}$	$\leq 2.5\text{ ns}$

SV00092

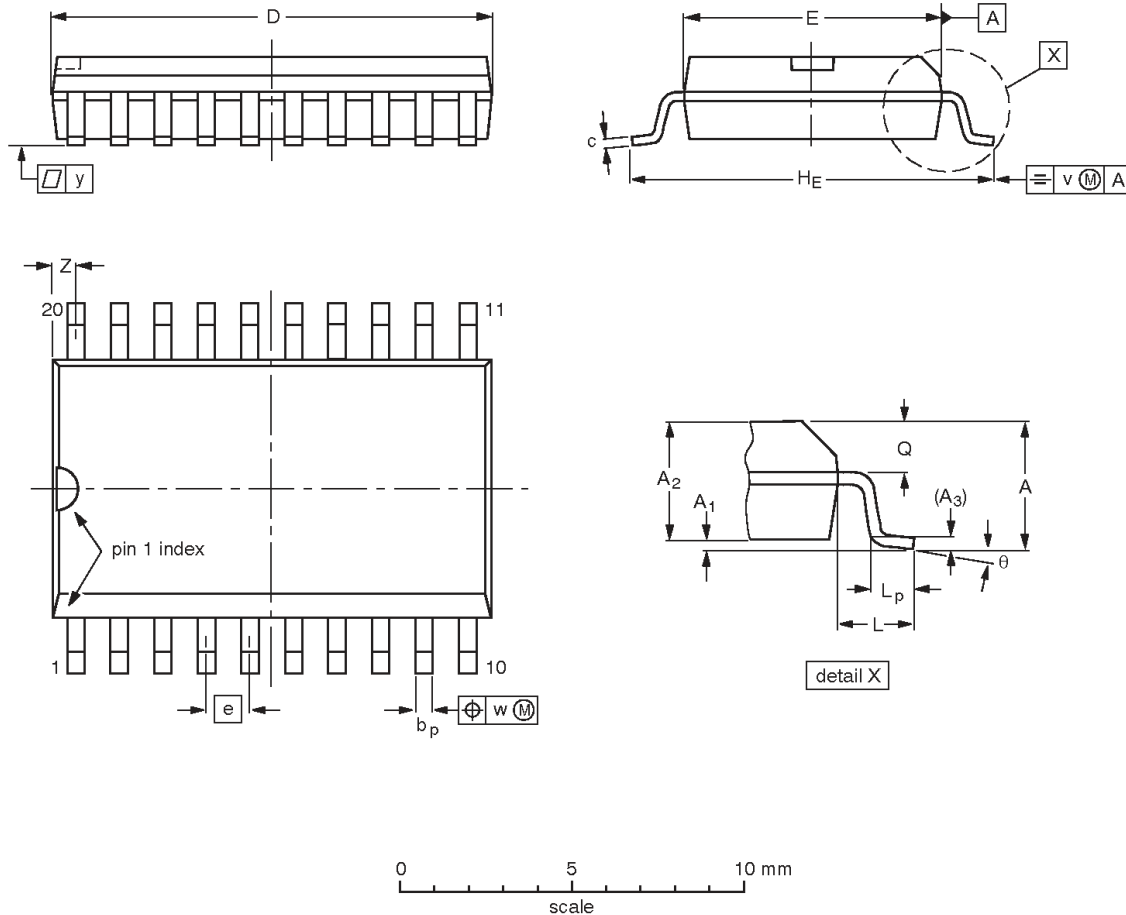


### 3.3 V Octal D-type flip-flop, inverting (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

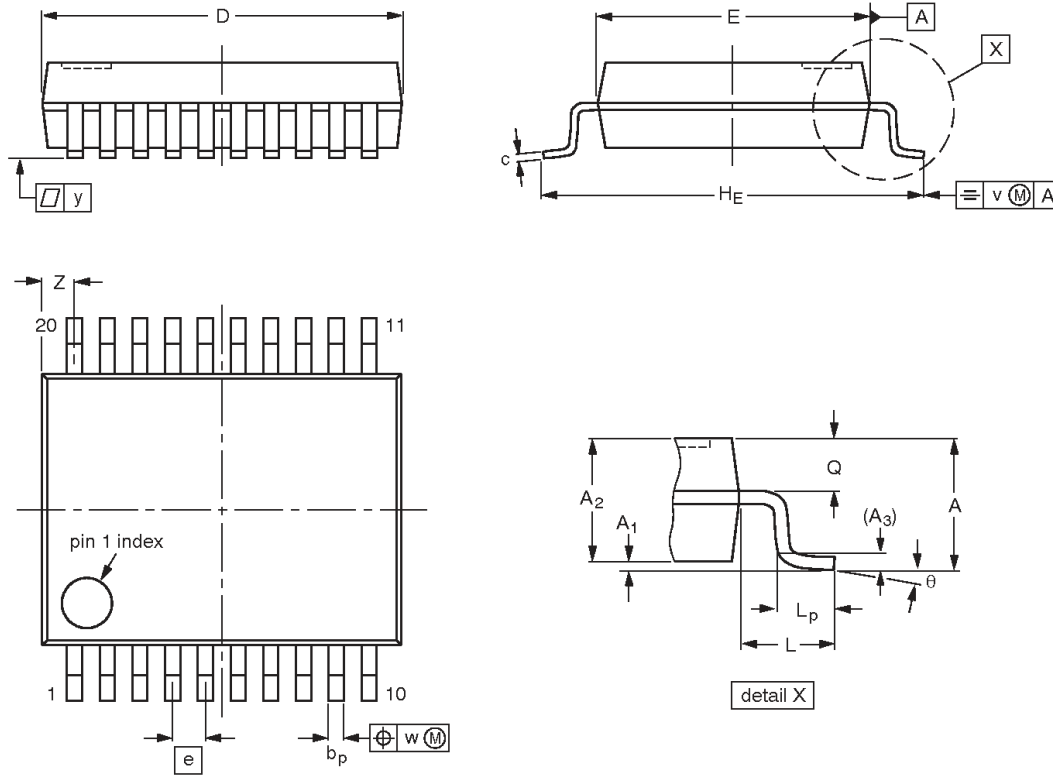
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				-99-12-27 03-02-19

### 3.3 V Octal D-type flip-flop, inverting (3-State)

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**SSOP20:** plastic shrink small outline package; 20 leads; body width 5.3 mm

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

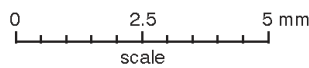
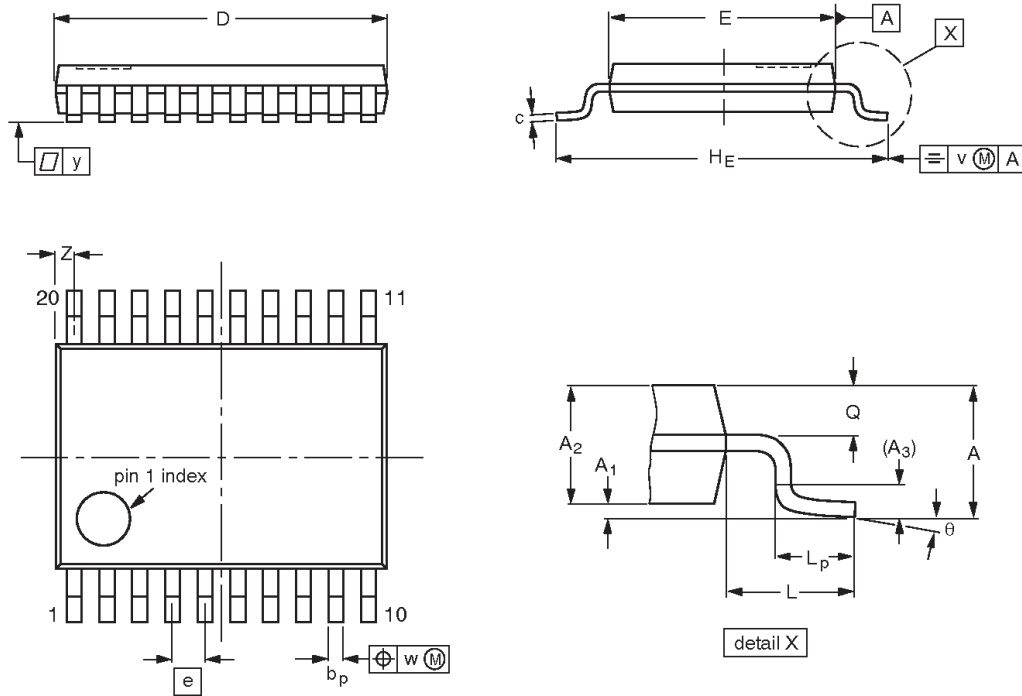
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

### 3.3 V Octal D-type flip-flop, inverting (3-State)

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**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				-99-12-27 03-02-19

## 3.3 V Octal D-type flip-flop, inverting (3-State)

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## REVISION HISTORY

Rev	Date	Description
_3	20040825	<p><b>Product data sheet (9397 750 14004). Supersedes Product specification of 1998 Feb 19 (9397 750 03536).</b></p> <p>Modifications:</p> <ul style="list-style-type: none"> <li>● Ordering information table on page 2: <ul style="list-style-type: none"> <li>– remove 'North America' column</li> <li>– change column heading 'Outside North America' to 'Type Number'</li> </ul> </li> <li>● AC characteristics table on page 6: change Max. value of <math>t_{PHZ}</math> from '3.0 ns' to '4.8 ns'</li> </ul>
_2	19980219	<p><b>Product specification (9397 750 03536). ECN 853-1855 18988 of 19 February 1998.</b></p> <p><b>Supersedes data of 1996 Aug 13.</b></p>
_1	19960813	

## 3.3 V Octal D-type flip-flop, inverting (3-State)

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## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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