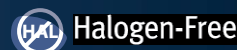


# EPC2103 – Enhancement-Mode GaN Power Transistor Half-Bridge

$V_{DS}$ , 80 V

$R_{DS(on)}$ , 5.5 mΩ

$I_D$ , 30 A



Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

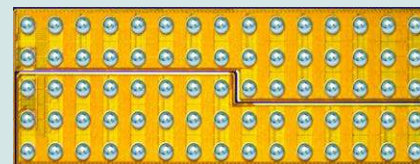
## Maximum Ratings

DEVICE	PARAMETER		VALUE	UNIT
Q1 & Q2	$V_{DS}$	Drain-to-Source Voltage (Continuous)	80	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
	$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 13^\circ\text{C/W}$ )	30	A
		Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	195	
	$V_{GS}$	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	$T_J$	Operating Temperature	-40 to 150	°C
	$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.2	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details



EPC2103 eGaN® ICs are supplied only in passivated die form with solder bumps  
Die Size: 6.05 mm x 2.3 mm

## Applications

- High Frequency DC-DC
- Motor Drive

## Benefits

- Ultra High Efficiency
- High Frequency Operation
- High Density Footprint

## Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1 & Q2	$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 0.5 \text{ mA}$	80			V
	$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 64 \text{ V}$ , $V_{GS} = 0 \text{ V}$		0.007	0.4	mA
	$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.013	6.5	mA
		Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.007	0.4	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 7 \text{ mA}$	0.8	1.3	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 20 \text{ A}$		4	5.5	mΩ
	$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$		1.8		V

Dynamic Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	$C_{ISS}$	Input Capacitance	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		730	880	pF
	$C_{RSS}$	Reverse Transfer Capacitance			7		
	$C_{OSS}$	Output Capacitance			445	670	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }40\text{ V}, V_{GS} = 0\text{ V}$		573		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			733		
	$Q_G$	Total Gate Charge	$V_{DS} = 40\text{ V}, V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		6.5	8	nC
	$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 40\text{ V}, I_D = 20\text{ A}$		2.2		
	$Q_{GD}$	Gate-to-Drain Charge			1.1		
	$Q_{G(TH)}$	Gate Charge at Threshold			1.5		
	$Q_{OSS}$	Output Charge	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		30	45	
	$Q_{RR}$	Source-Drain Recovery Charge			0		
Q2	$C_{ISS}$	Input Capacitance	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		730	880	pF
	$C_{RSS}$	Reverse Transfer Capacitance			7		
	$C_{OSS}$	Output Capacitance			525	790	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }40\text{ V}, V_{GS} = 0\text{ V}$		668		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			855		
	$Q_G$	Total Gate Charge	$V_{DS} = 40\text{ V}, V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		6.5	8	nC
	$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 40\text{ V}, I_D = 20\text{ A}$		2.2		
	$Q_{GD}$	Gate-to-Drain Charge			1.1		
	$Q_{G(TH)}$	Gate Charge at Threshold			1.5		
	$Q_{OSS}$	Output Charge	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		34	51	
	$Q_{RR}$	Source-Drain Recovery Charge			0		

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Figure 1 (Q1 & Q2): Typical Output Characteristics at 25°C

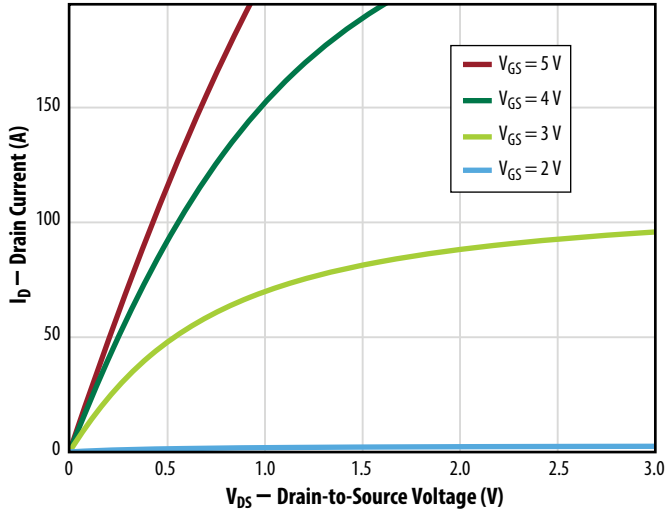


Figure 2 (Q1 & Q2): Transfer Characteristics

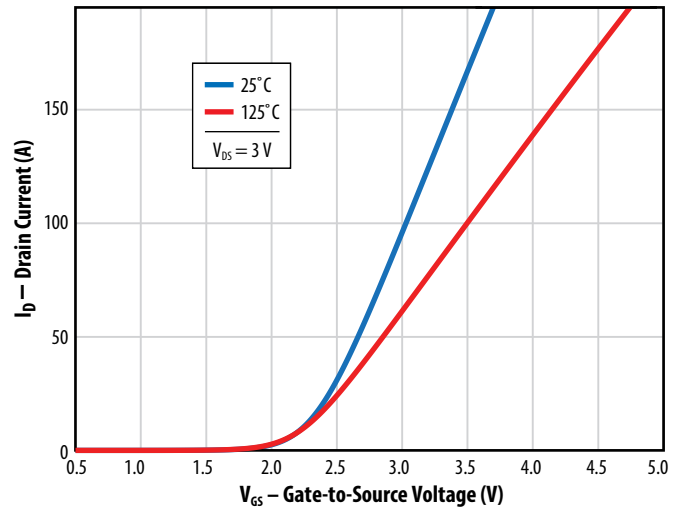


Figure 3 (Q1 & Q2):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

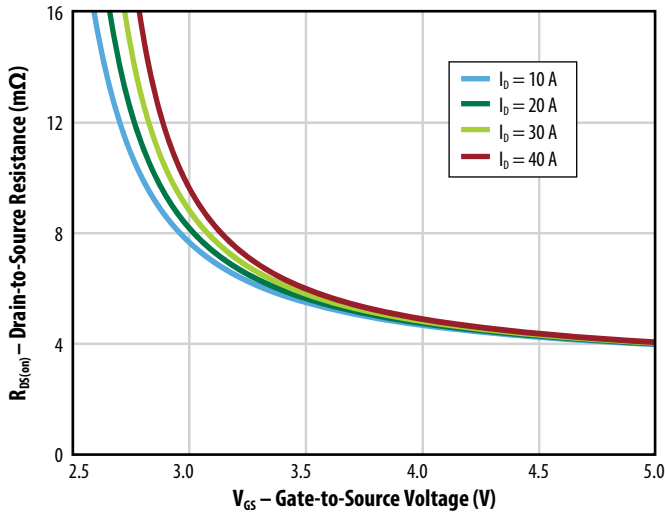


Figure 4 (Q1 & Q2):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

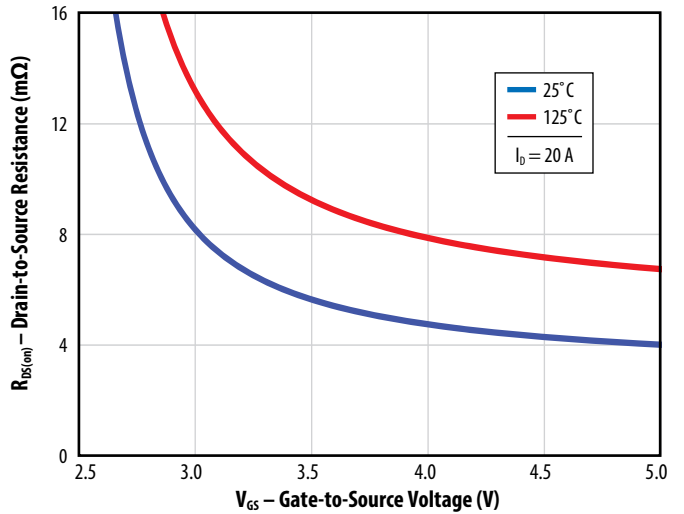


Figure 5a (Q1): Capacitance (Linear Scale)

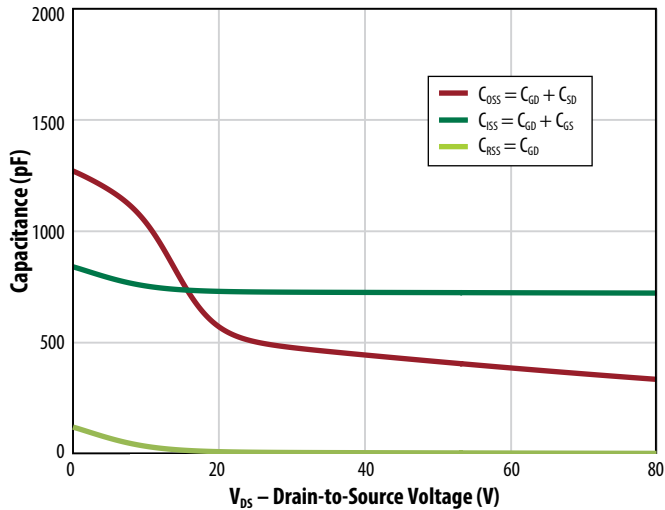


Figure 5b (Q1): Capacitance (Log Scale)

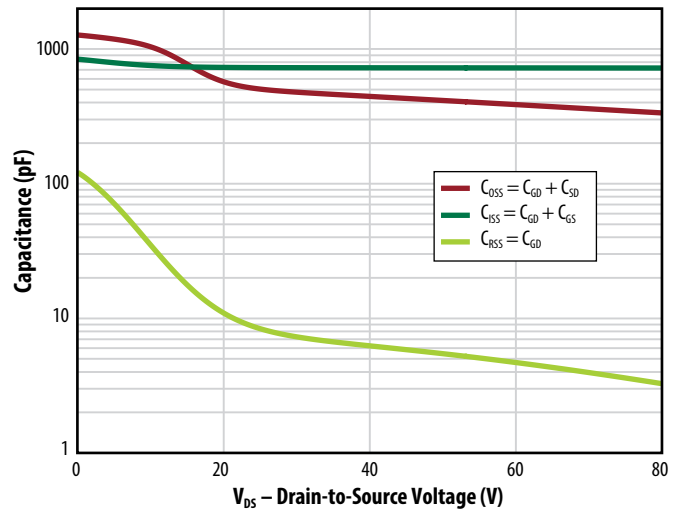


Figure 5c (Q2): Capacitance (Linear Scale)

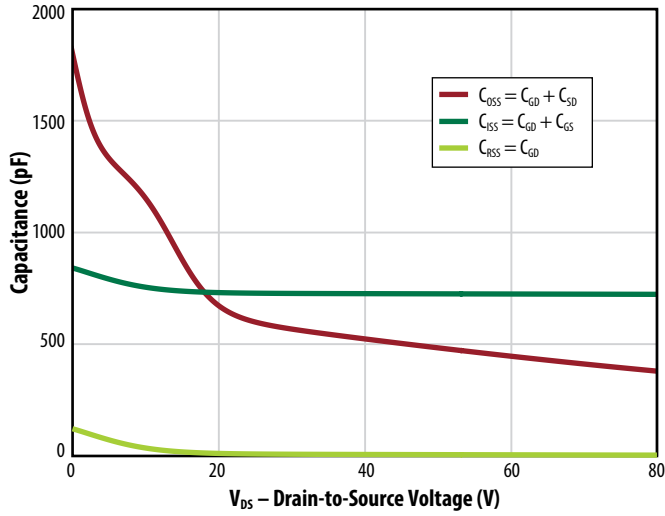


Figure 5d (Q2): Capacitance (Log Scale)

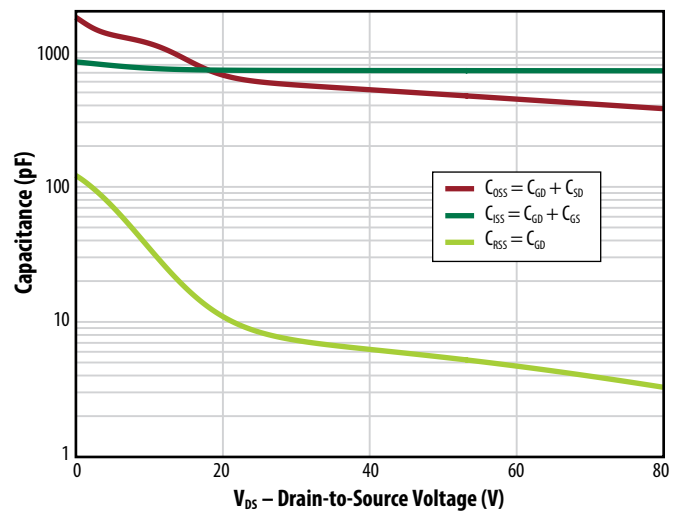


Figure 6a (Q1): Output Charge and Coss Stored Energy

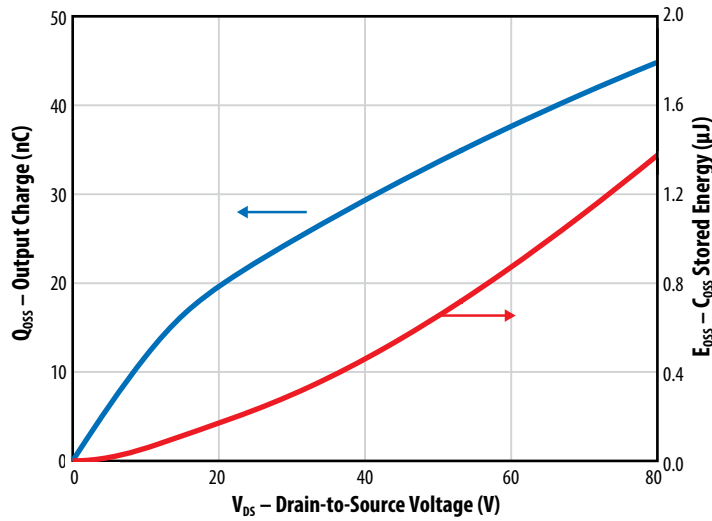


Figure 6b (Q2): Output Charge and Coss Stored Energy

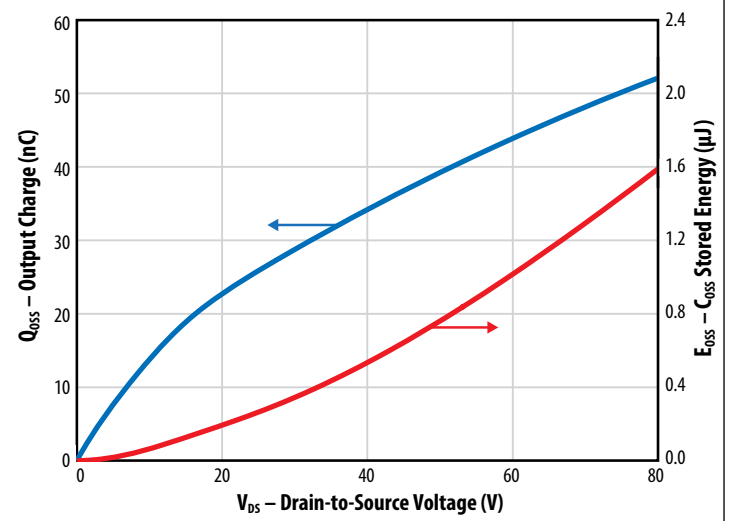


Figure 7 (Q1 & Q2): Gate Charge

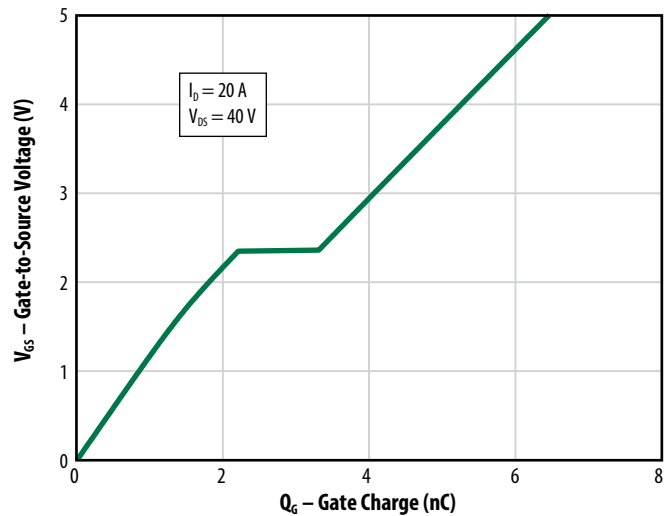
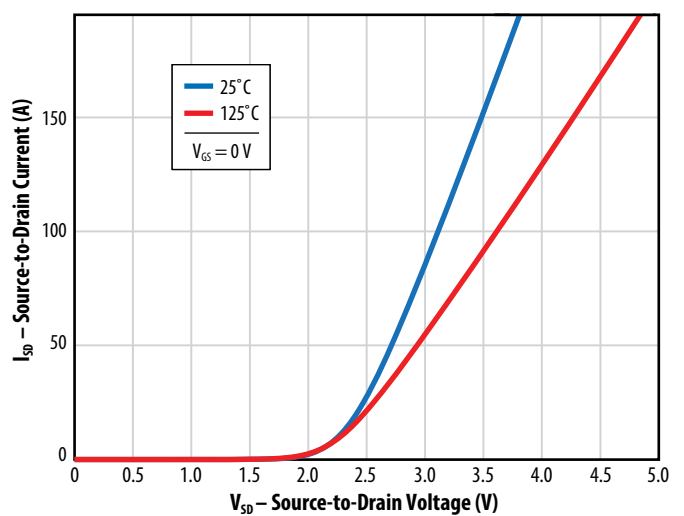
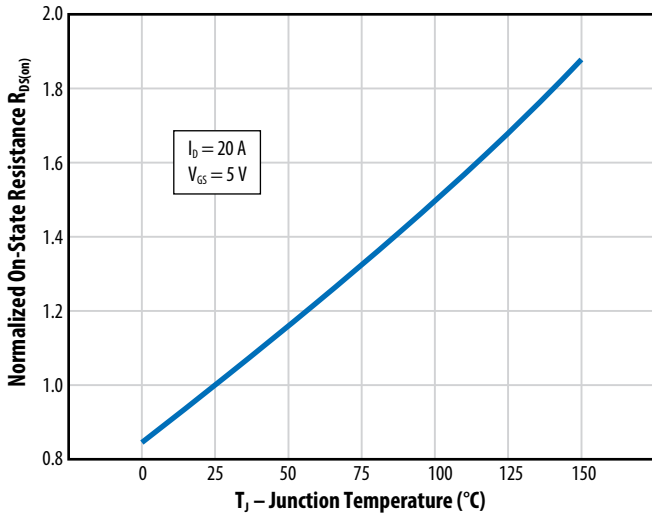


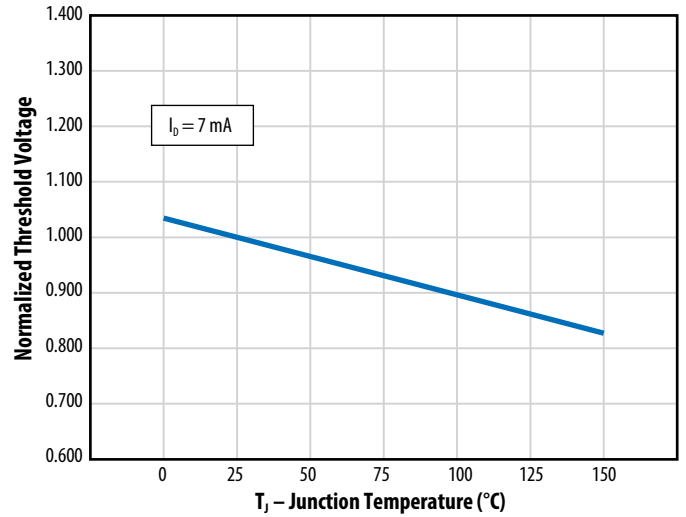
Figure 8 (Q1 & Q2): Reverse Drain-Source Characteristics



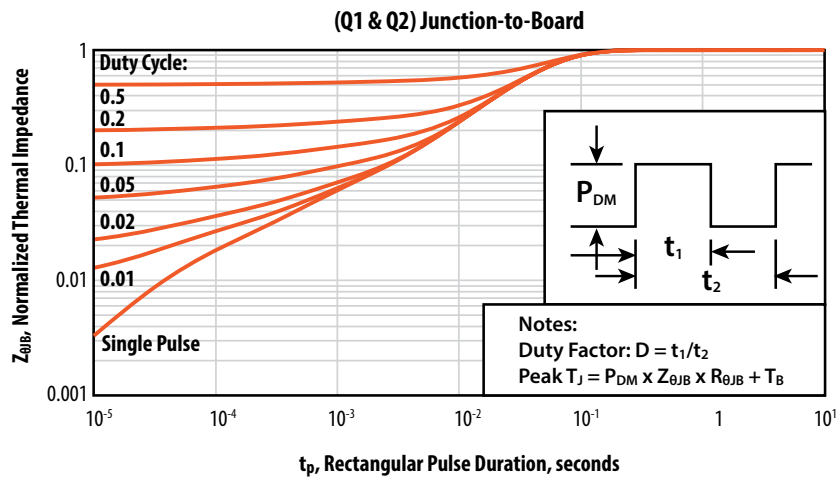
**Figure 9 (Q1 & Q2):**  
Normalized On-State Resistance vs. Temperature



**Figure 10 (Q1 & Q2):**  
Normalized Threshold Voltage vs. Temperature



**Figure 11a**  
Transient Thermal Response Curves



**Figure 11b**  
Transient Thermal Response Curves

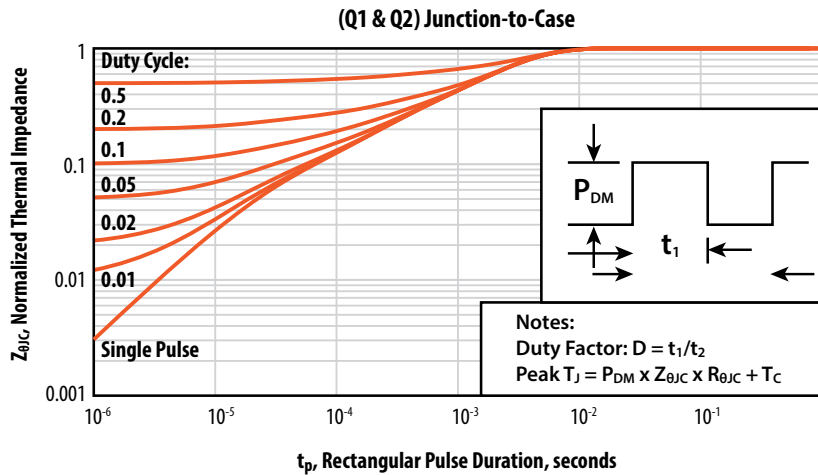


Figure 12 (Q1 & Q2): Safe Operating Area

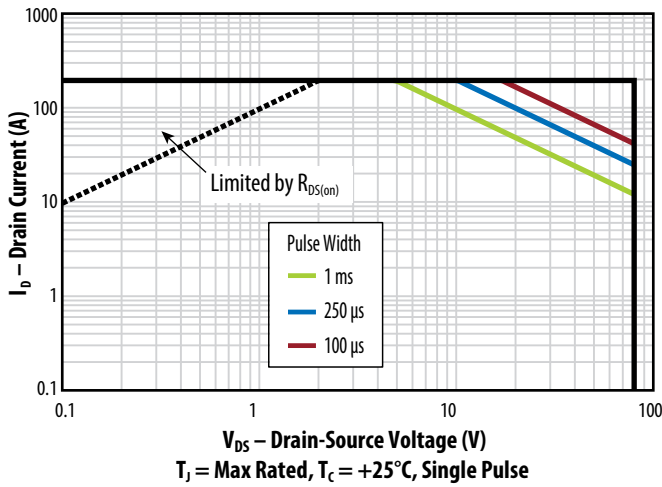
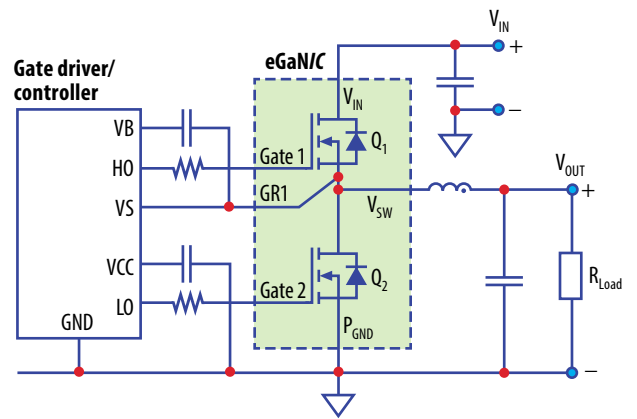
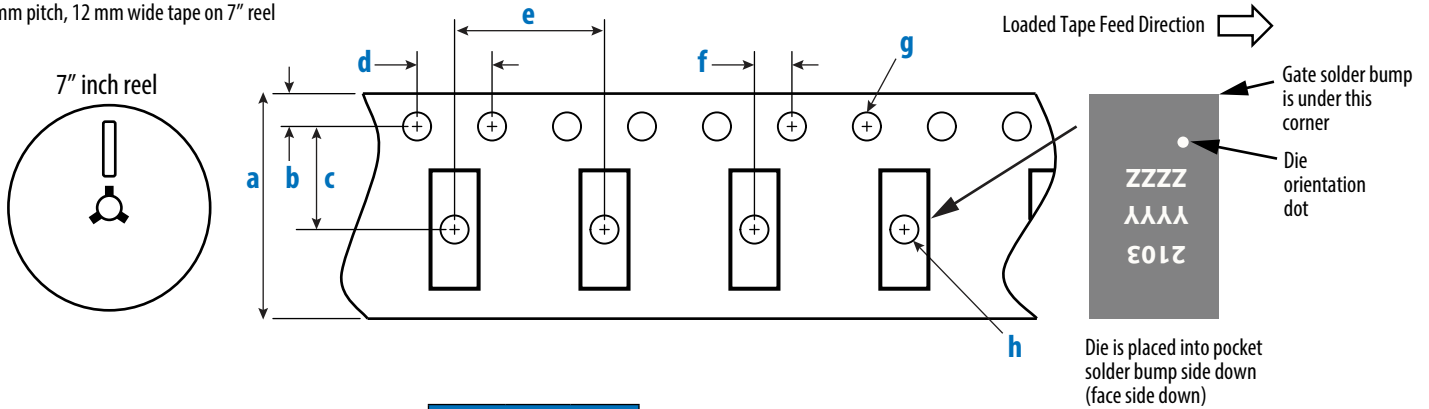


Figure 13: Typical Application Circuit



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

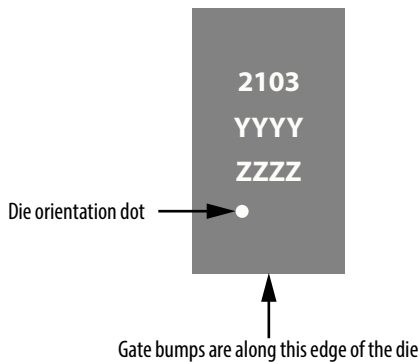


EPC2103 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

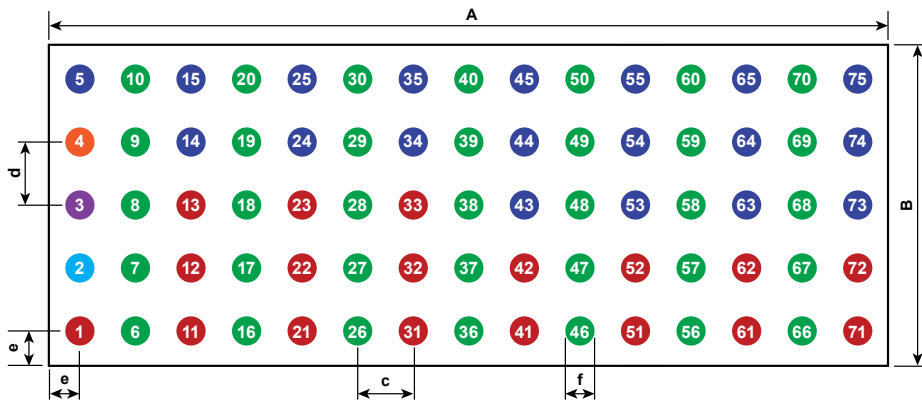
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2103	2103	YYYY	ZZZZ

**DIE OUTLINE**

Solder Bump View



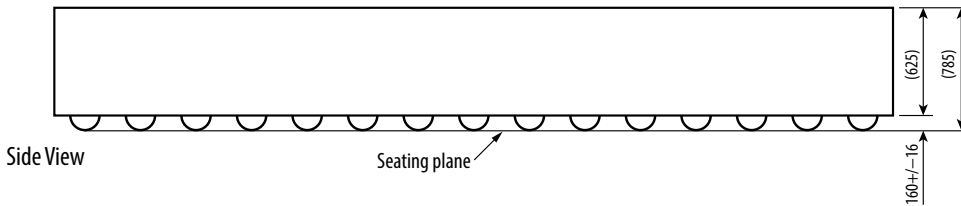
DIM	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	400	400	400
d	450	450	450
e	210	225	240
f	187	208	229

Pad 2 is Gate 1 (high side); Pad 3 is HS Gate Return; Pad 4 is G2;

Pads 1, 11, 12, 13, 21, 22, 23, 31, 32, 33, 41, 42, 51, 52, 61, 62, 71, 72 are  $V_{IN}$ ;

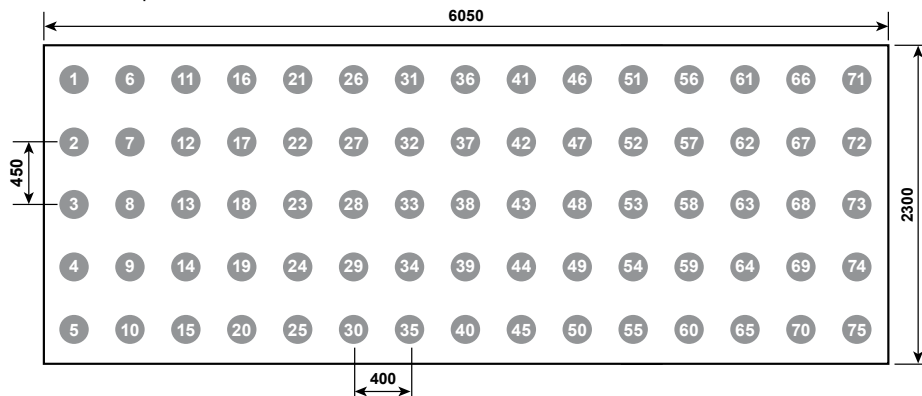
Pads 5, 14, 15, 24, 25, 34, 35, 43, 44, 45, 53, 54, 55, 63, 64, 65, 73, 74, 75 Ground;

Pads 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are Switch Node



**RECOMMENDED LAND PATTERN**

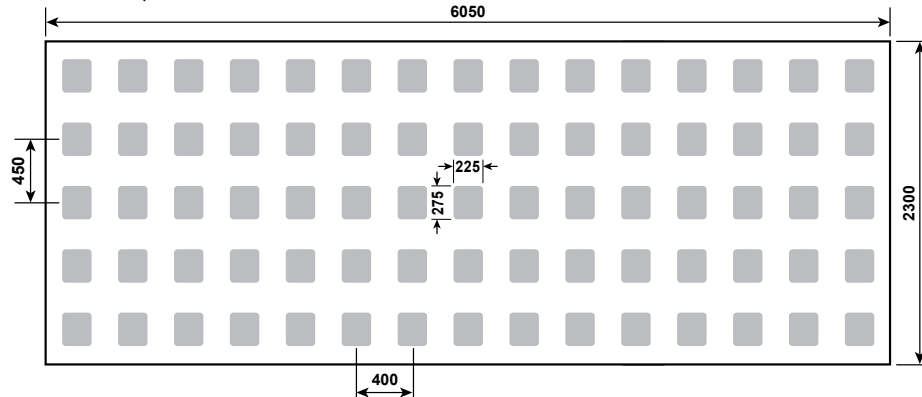
(measurements in  $\mu\text{m}$ )



The land pattern is solder mask defined. Suggest SMD Pads at  $200 +20/-10 \mu\text{m}$ .  $190 \mu\text{m}$  minimum.

**RECOMMENDED STENCIL DRAWING**

(measurements in  $\mu\text{m}$ )



Recommended stencil should be 4 mil ( $100 \mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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