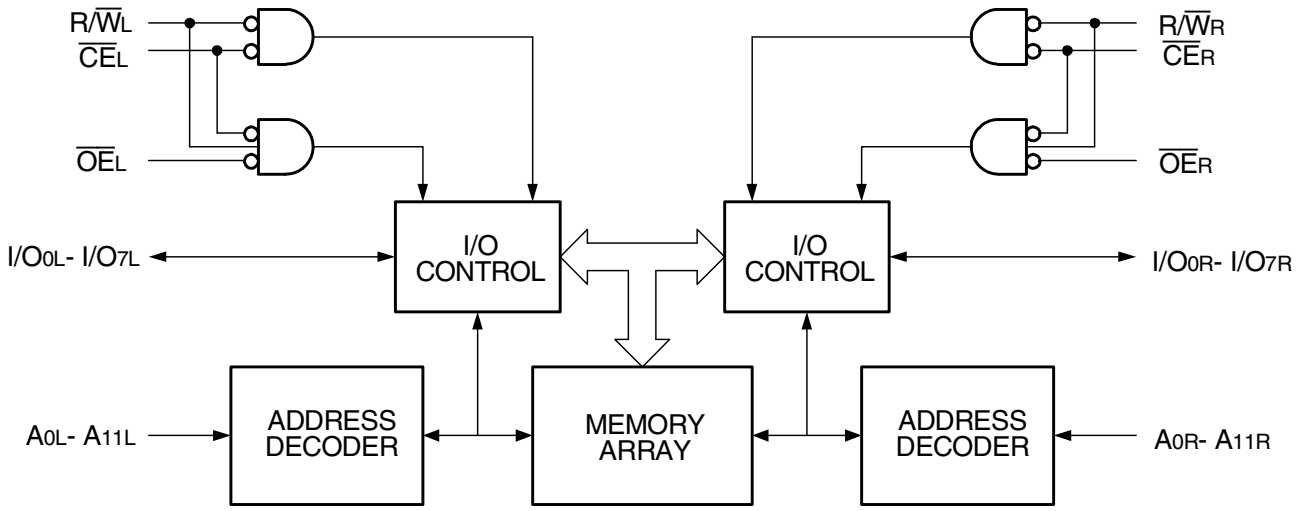
HIGH-SPEED 4K x 8 DUAL-PORT STATIC SRAM

7134SA/LA

Features

- High-speed access
  - *Commercial: 20/55ns (max.)*
  - *Industrial: 25ns (max.)*
  - *Military: 35/45/55/70ns (max.)*
- Low-power operation
  - *IDT7134SA*
    Active: 700mW (typ.)
    Standby: 5mW (typ.)
  - *IDT7134LA*
    Active: 700mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention (LA only)
- TTL-compatible; single 5V (±10%) power supply
- Available in 48-pin DIP, LCC, Flatpack and 52-pin PLCC
- Military product compliant to MIL-PRF-38535 QML
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



2720 drw 01

Description

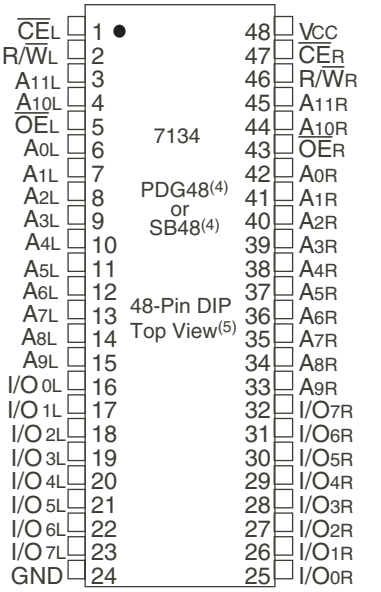
The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

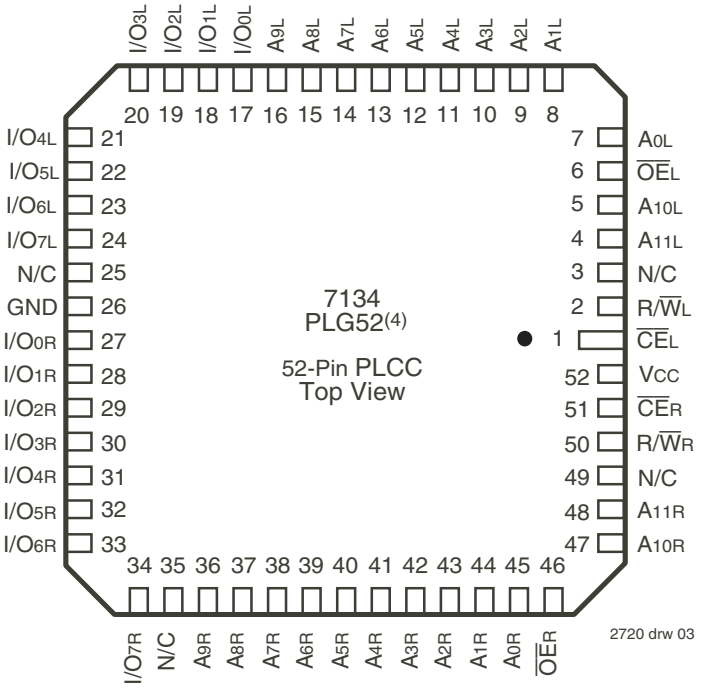
Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 700mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7134 is packaged in either a sidebraze or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack. Military grade product is manufactured in compliance with MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations[1,2,3]



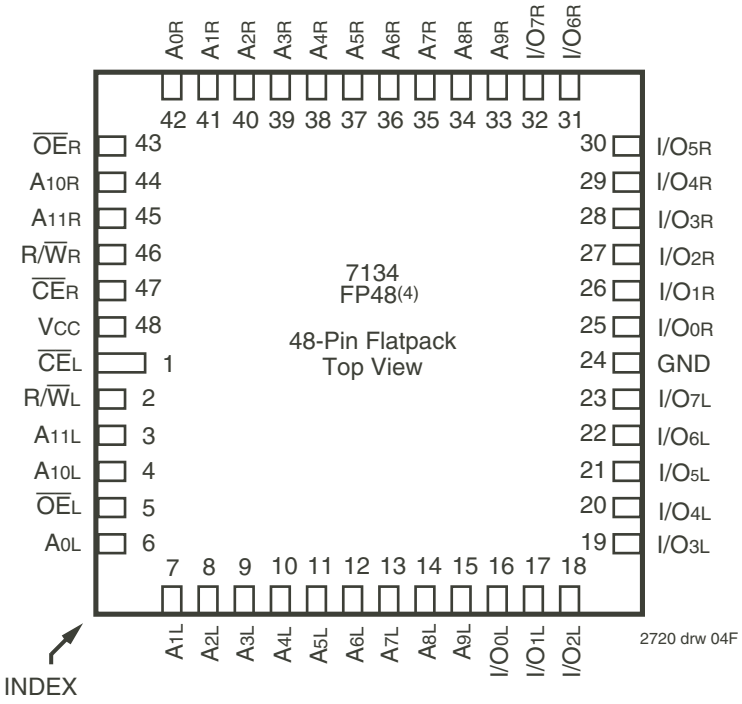
2720 drw 02a

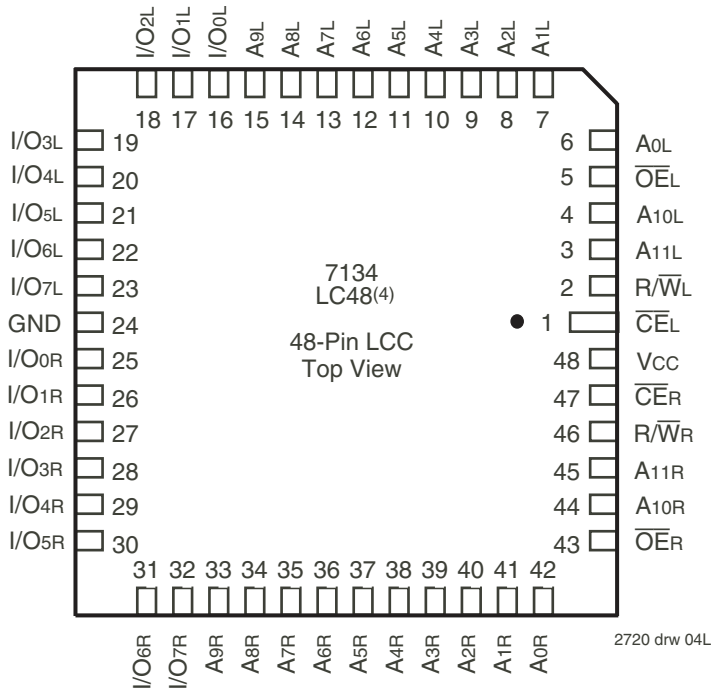


2720 drw 03

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. PDG48 package body is approximately .55 in x 2.43 in x .18 in.
   SB48 package body is approximately .62 in x 2.43 in x .15 in.
   PLG52 package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of actual part-marking.

Pin Configurations [1,2,3](con't.)





NOTES:
1. All VCC pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. LC48 package body is approximately .57 in x .57 in x .68 in. FP48 package body is approximately .75 in x .75 in x .11 in.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	-65 to +150	°C
P_T(3)	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

2720 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25%of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc +10%.
3. V_{TERM} = 5.5V.

Capacitance(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	11	pF

2720 tbl 02

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

Recommended Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2720 tbl 03

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2720 tbl 04

NOTES:
1. V_{IL} (min.) ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	7134SA		7134LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ - V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2720 tbl 05

NOTES:
1. At Vcc ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,2] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7134X20 Com'l Only Typ.	7134X20 Com'l Only Max.	7134X25 Com'l & Ind Typ.	7134X25 Com'l & Ind Max.	7134X35 Com'l & Military Typ.	7134X35 Com'l & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Disabled f = f_{MAX}[3]	COM'L	SA	170	280	160	280	150	260	mA
				LA	170	240	160	220	150	210	
			MIL & IND	SA	—	—	160	310	150	300	
				LA	—	—	160	260	150	250	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[3]	COM'L	SA	25	100	25	80	25	75	mA
				LA	25	80	25	50	25	45	
			MIL & IND	SA	—	—	25	100	25	75	
				LA	—	—	25	80	25	55	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH} Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	SA	105	180	95	180	85	170	mA
				LA	105	150	95	140	85	130	
			MIL & IND	SA	—	—	95	210	85	200	
				LA	—	—	95	170	85	160	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[3]	COM'L	SA	1.0	15	1.0	15	1.0	15	mA
				LA	0.2	4.5	0.2	4.0	0.2	4.0	
			MIL & IND	SA	—	—	1.0	30	1.0	30	
				LA	—	—	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}_{"A"}$ or $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled, f = f_{MAX}[3]	COM'L	SA	105	170	95	170	85	160	mA
				LA	105	130	95	120	85	110	
			MIL & IND	SA	—	—	95	210	85	190	
				LA	—	—	95	150	85	130	

2720 tbl 06a

Symbol	Parameter	Test Condition	Version		7134X45 Com'l & Military Typ.	7134X45 Com'l & Military Max.	7134X55 Com'l, Ind & Military Typ.	7134X55 Com'l, Ind & Military Max.	7134X70 Com'l & Military Typ.	7134X70 Com'l & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Disabled f = f_{MAX}[3]	COM'L	SA	140	240	140	240	140	240	mA
				LA	140	200	140	200	140	200	
			MIL & IND	SA	140	280	140	270	140	270	
				LA	140	240	140	220	140	220	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[3]	COM'L	SA	25	70	25	70	25	70	mA
				LA	25	40	25	40	25	40	
			MIL & IND	SA	25	70	25	70	25	70	
				LA	25	50	25	50	25	50	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH} Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	SA	75	160	75	160	75	160	mA
				LA	75	130	75	130	75	130	
			MIL & IND	SA	75	190	75	180	75	180	
				LA	75	150	75	150	75	150	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[3]	COM'L	SA	1.0	15	1.0	15	1.0	15	mA
				LA	0.2	4.0	0.2	4.0	0.2	4.0	
			MIL & IND	SA	1.0	30	1.0	30	1.0	30	
				LA	0.2	10	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}_{"A"}$ or $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Disabled, f = f_{MAX}[3]	COM'L	SA	75	150	75	150	75	150	mA
				LA	75	100	75	100	75	100	
			MIL & IND	SA	75	180	75	170	75	170	
				LA	75	120	75	120	75	120	

2720 tbl 06b

NOTES:
1. 'X' in part number indicates power rating (SA or LA).
2. V_{CC} = 5V, T_A = +25°C for typical, and parameters are not production tested.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.

Data Retention Characteristics Over All Temperature Ranges

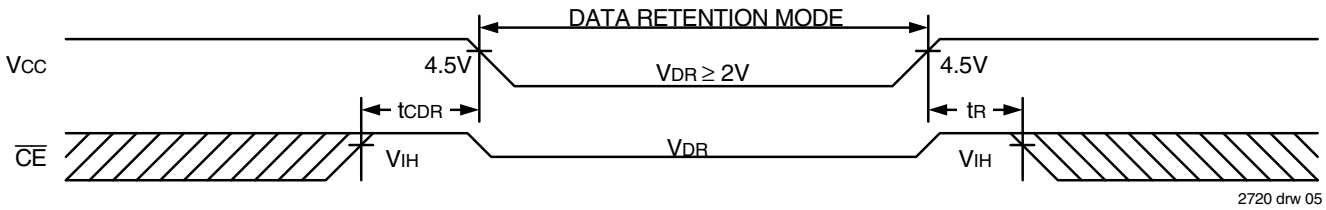
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL. & IND.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2720 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but not production tested.

Data Retention Waveform

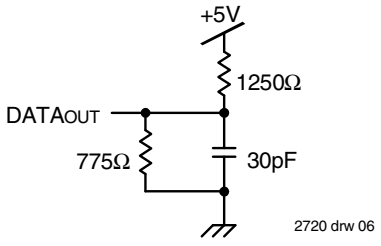


2720 drw 05

AC Test Conditions

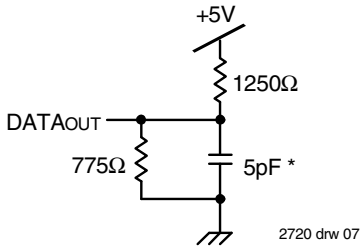
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2720 tbl 08



2720 drw 06

Figure 1. AC Output Test Load



2720 drw 07

Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[3]

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Ind		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

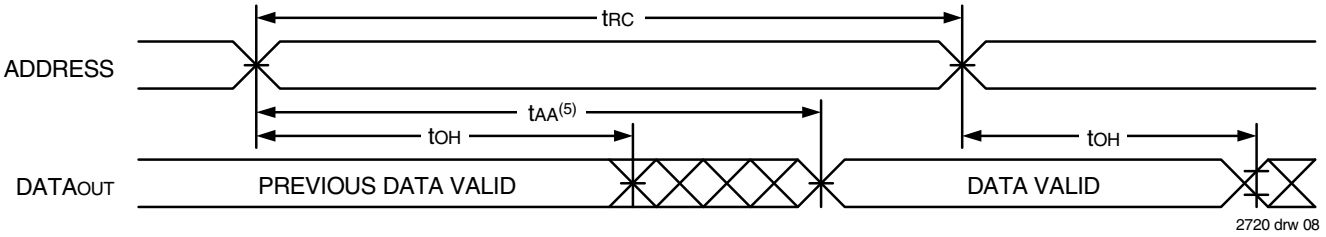
2720 tbl 09a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	45	—	50	—	50	ns

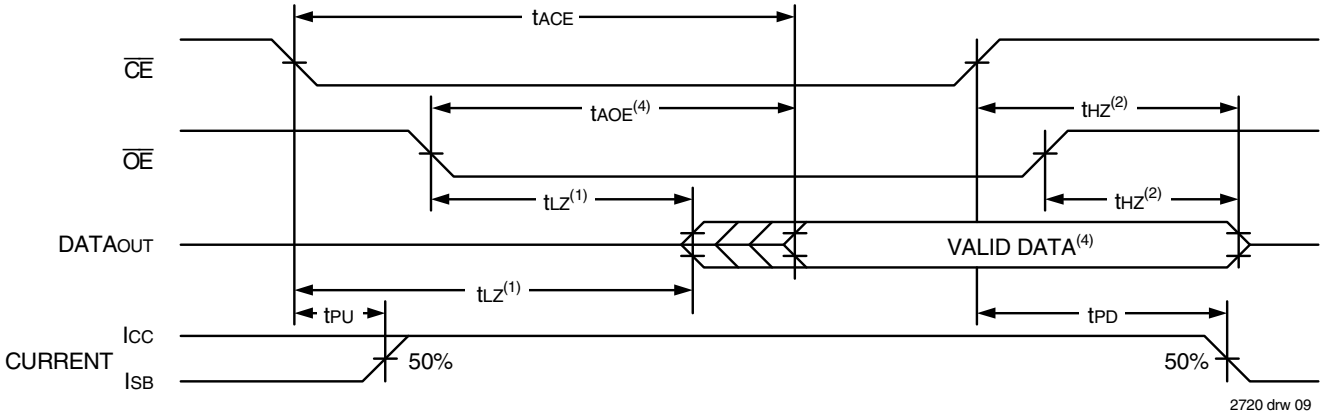
2720 tbl 09b

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

Timing Waveform of Read Cycle No. 1, Either Side(1,2,4)



Timing Waveform of Read Cycle No. 2, Either Side(1,3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH}.
4. Start of valid data depends on which timing becomes effective, t_{AOE}, t_{ACE} or t_{AA}
5. t_{AA} for RAM Address Access and t_{SAA} for Semaphore Address Access.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5]

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Ind		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	3	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	30	—	30	—	35	ns

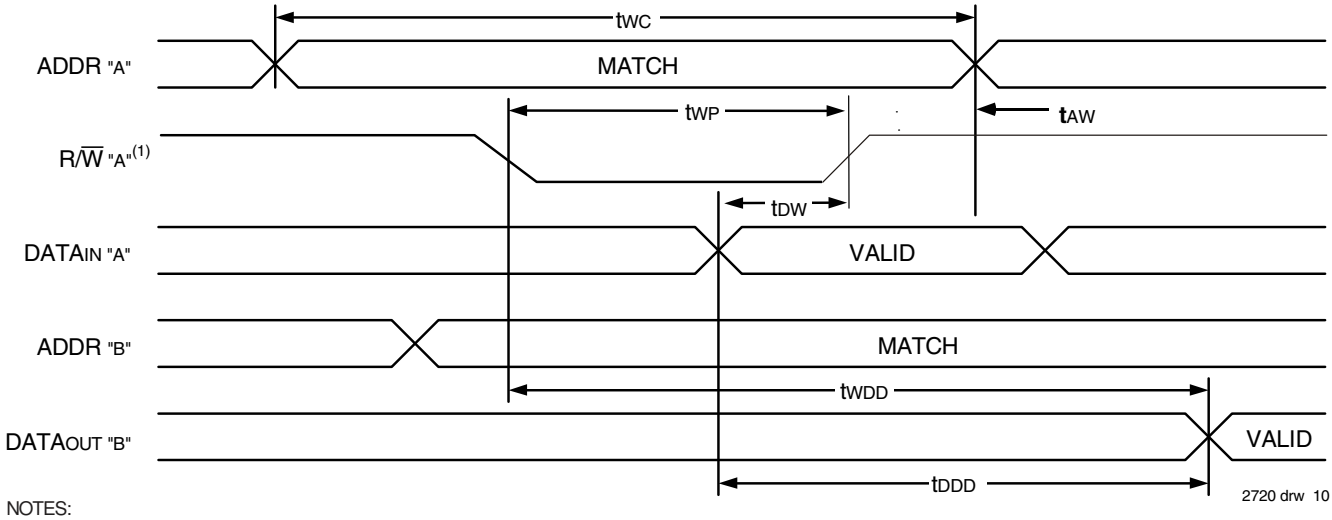
2720 tbl 10a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[3]	3	—	3	—	3	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	20	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2,3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	45	—	55	—	70	ns

2720 tbl 10b

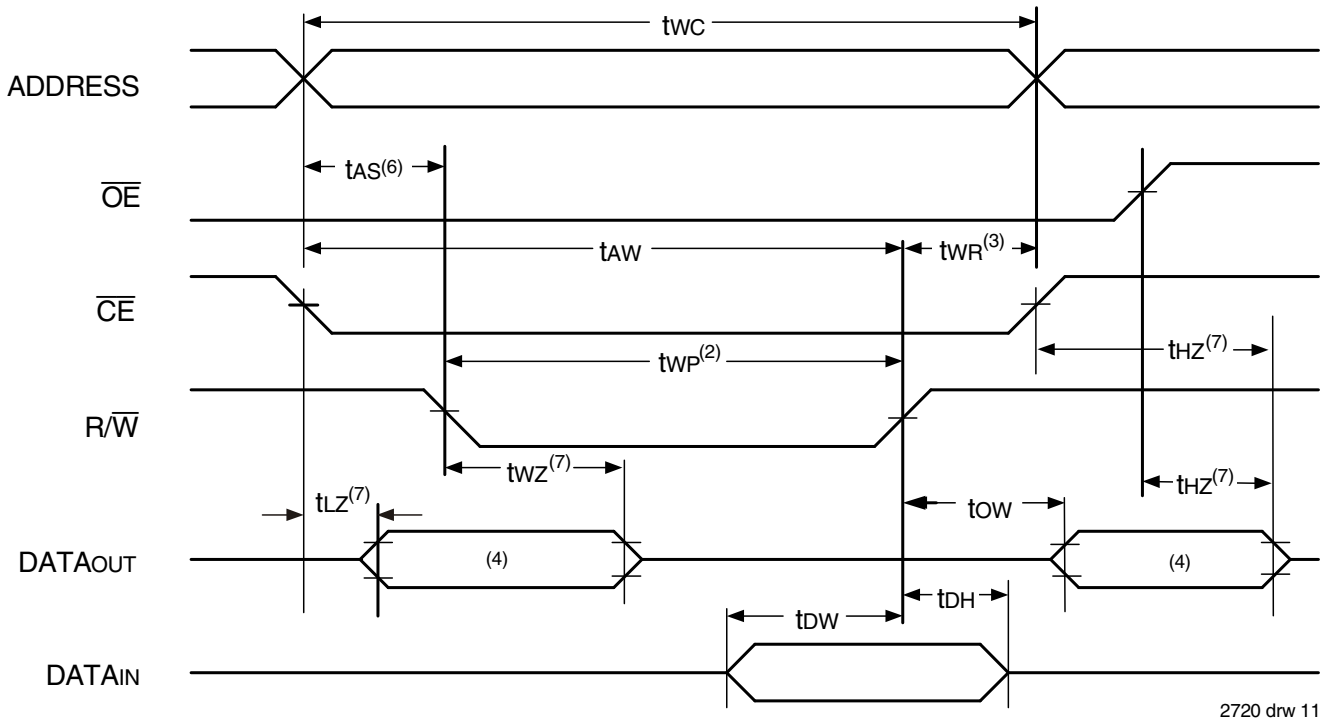
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read”.
5. 'X' in part number indicates power rating (SA or LA).

Timing Waveform of Write with Port-to-Port Read(1,2,3)



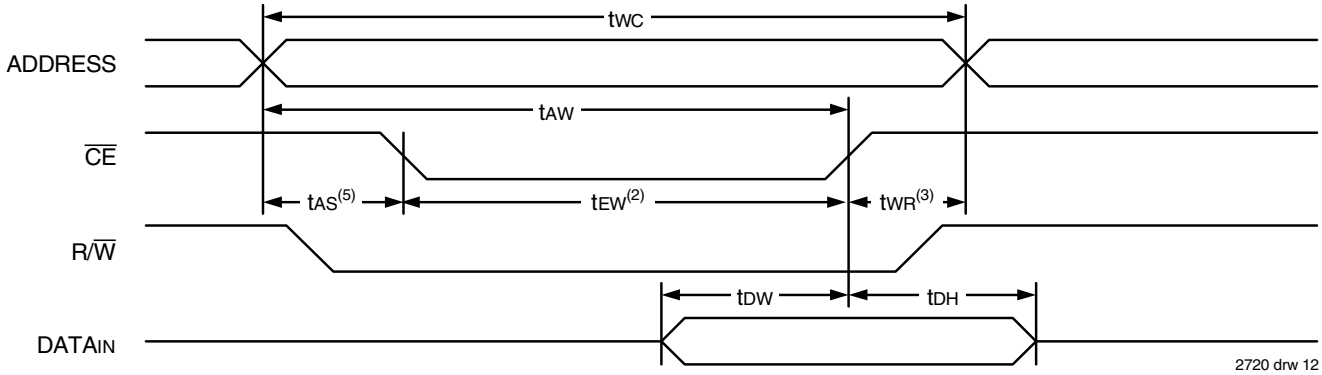
NOTES:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$. $\overline{OE}$ "B" = V_{IL}.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and R/$\overline{W}$ = V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going to V_{IH} to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ = V_{IL} during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,4)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ =V_{IL} and R/$\overline{W}$ = V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end-of-write cycle.
4. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
5. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.

Functional Description

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated inTruth Table I.

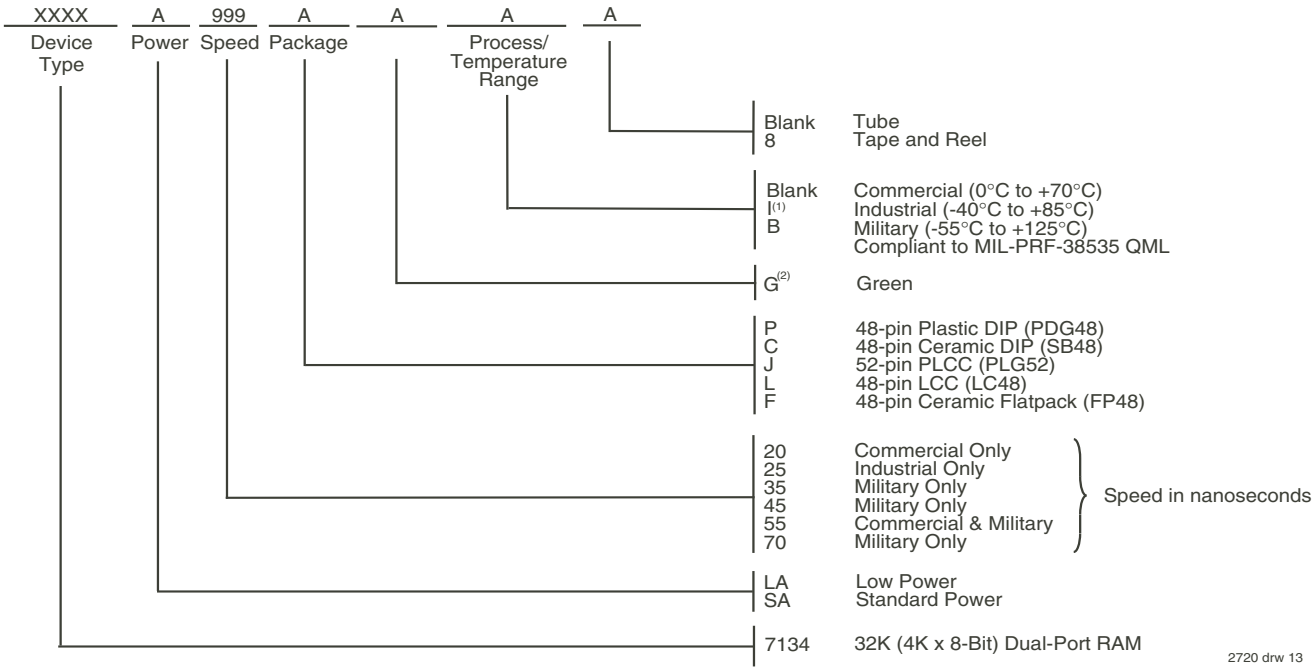
Truth Table I – Read/Write Control

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Deselected and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on port written into memory
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

2720 tbl 11

NOTE:
1. A_{0L} - A_{11L} ≠ A_{0R} - A_{11R}
"H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care, and "Z" = High Impedance

Ordering Information



NOTES:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are Obsolete excluding FP48, LC48 & SB48. Product Discontinuation Notice - PDN# SP-17-02
Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	7134LA20JG	PLG52	PLCC	C
	7134LA20JG8	PLG52	PLCC	C
	7134LA20PDG	PDG48	PDIP	C
25	7134LA25JGI	PLG52	PLCC	I
	7134LA25JGI8	PLG52	PLCC	I
	7134LA25PDGI	PDG48	PDIP	I
35	7134LA35CB	SB48	SB	M
	7134LA35FB	FP48	FPACK	M
	7134LA35L48B	LC48	LCC	M
45	7134LA45CB	SB48	SB	M
55	7134LA55CB	SB48	SB	M
	7134LA55L48B	LC48	LCC	M
70	7134LA70CB	SB48	SB	M
	7134LA70L48B	LC48	LCC	M

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
35	7134SA35CB	SB48	SB	M
	7134SA35L48B	LC48	LCC	M
45	7134SA45CB	SB48	SB	M
55	7134SA55CB	SB48	SB	M
	7134SA55JG	PLG52	PLCC	C
	7134SA55JG8	PLG52	PLCC	C
	7134SA55L48B	LC48	LCC	M
70	7134SA70CB	SB48	SB	M
	7134SA70L48B	LC48	LCC	M

Datasheet Document History

03/25/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Pages 2	Added additional notes to pin configurations
060/9/99:		Changed drawing format
10/01/99:		Added Industrial Temperature Ranges and removed corresponding notes
11/10/99:		Replaced IDT logo
12/22/99:	Page 1	Made corrections to drawing
03/03/00:		Corrected block diagram and pin configurations
		Changed ±500mV to 0mV
01/12/00:	Pages 1 2	Moved "Description to page 2 and adjusted page layout
	Page 1	Added "LA only)" to paragraph
	Page 2	Fixed P48-1 package description
	Page 3	Increased storage temperature parameters
		Clarified T_A parameter
	Page 4	DC Electrical parameters–changed wording from "open" to "disabled"
	Page 10	Fixed Truth Table specification in "Functional Description" paragraph
01/17/06:	Page 1	Added green availability to features
	Page 11	Added green indicator to ordering information
	Page 1 & 11	Replaced old IDT™ with new IDT™ logo
08/12/08:	Page 11	Corrected typo in the ordering information
10/21/08:	Page 11	Removed "IDT" from orderable part number
01/16/13:	Page 1, 4, 6 & 8	Removed Military 25ns & Industrial 35ns speed grades from Features and corrected the headers of the DC Chars and AC Chars tables to indicate this change
	Page 11	Added T& R indicator to and removed Military 25ns & Industrial 35ns speed grades from the ordering information
10/21/08:	Page 11	Removed "IDT" from orderable part number
02/04/13:	Page 1, 4, 6 & 8	Removed Military 25ns & Industrial 35ns speed grades from Features and corrected the headers of the DC Chars and AC Chars tables to indicate this change
	Page 11	Added T& R indicator to and removed Military 25ns & Industrial 35ns speed grades from the ordering information
	Page 2	Typo/correction
01/11/18:		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
05/10/21:	Pages 1 - 14	Rebranded as Renesas datasheet
	Page 2 & 3	Rotated LC48 LCC, FP48 Flatpack & PLG52 PLCC to accurately reflect pin 1 orientation
	Page 2, 3 & 12	Updated package codes
	Page 12	Added Orderable Part Information tables

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.