

#### 3.5V - 38V / 3A / 0.85V - 6V Output

#### DESCRIPTION

The VDLM series Magl<sup>3</sup>C Power Module provides a fully integrated DC-DC power supply including the switching regulator with integrated MOSFETs, controller and compensation, as well as the shielded inductor in one package.

The 171033801 offers high efficiency and delivers up to 3A of output current. It operates with an input voltage from 3.5V to 38V and is designed for a small solution size.

The module maintains high efficiency throughout the output current range by automatically transitioning between operating modes based on the load demands.

The 171033801 is available in an LGA-12EP package (10 x 6 x 3.1mm).

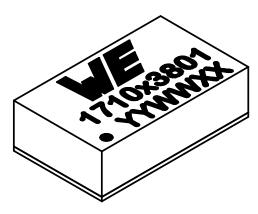
This module has integrated protection circuitry that guards against thermal overstress with thermal shutdown and protects against electrical damage using overcurrent, overvoltage, short circuit and undervoltage protections.

## **TYPICAL APPLICATIONS**

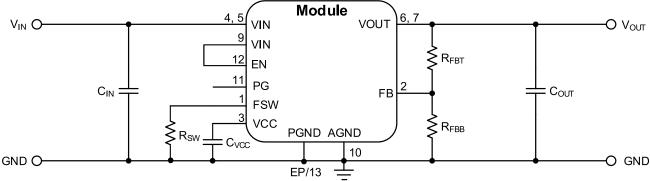
- Point-of-Load DC-DC applications
- Industrial, test and measurement, medical applications
- DSPs, FPGAs, MCUs and MPUs supply
- I/O interface power supply

#### **FEATURES**

- Peak efficiency up to 96%
- Current capability up to 3A
- Input voltage range: 3.5V to 38V
- Output voltage range:
  - 0.85V to 6V at 3A
  - 0.85V to 13V at 2.5A
- 3.5µA typical quiescent current
- Integrated shielded inductor
- Adjustable switching frequency
- Current mode control
- Synchronous operation
- Undervoltage lockout
- Embedded soft-start
- Power good indicator
- Spread spectrum for optimized EMI performance
- Thermal shutdown
- Short circuit, overcurrent, and overvoltage protections
- Cycle-by-cycle current limit
- RoHS and REACh compliant
- Operating ambient temp. range: -40°C to 105°C
- Operating junction temp. range: -40°C to 125°C
- Complies with EN55032 class B conducted and radiated emissions standard



#### TYPICAL CIRCUIT DIAGRAM



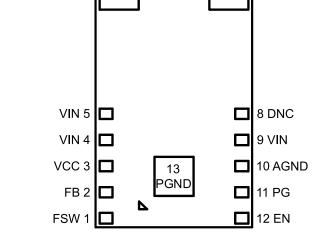
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7 VOUT

## **PINOUT**





VOUT 6

Top View

**Bottom View** 

| SYMBOL | NUMBER  | TYPE   | DESCRIPTION  |
|--------|---------|--------|--|
| FSW    | 1       | Input  | Switching frequency selection pin. Connect an external resistor to select the switching frequency. The resistor can be connected to AGND to disable spread spectrum behavior. The resistor can be connected to VCC to enable spread spectrum behavior. |
| FB     | 2       | Input  | Feedback pin to the internal error amplifier. This pin must be connected to the external resistor divider to adjust the output voltage.  |
| VCC    | 3       | Power  | VCC pin. This pin is attached to the output of the internal LDO. Connect a ceramic capacitor of 1 µF to VCC and AGND. VCC be attached to FSW using a series resistor, R <sub>SW</sub> . It should not be used to power other application functions.    |
| VIN    | 4, 5    | Power  | Input voltage pins. Used for input power supply connection. Place the input capacitor as close as possible to VIN and PGND.  |
| VOUT   | 6, 7    | Power  | Output voltage pins. Place output capacitors as close as possible to VOUT and PGND. For thermal performance use copper plane(s) at this pin.   |
| DNC    | 8       |        | This pin must be left floating.  |
| VIN    | 9       | Power  | Input voltage pin. Internally connected to VIN, can be used to supply PG and EN pin. No need to connect externally to VIN trace (pin 4 and pin 5).   |
| AGND   | 10      | Power  | Analog ground pin. Use this pin as ground for FSW, VCC and PG pins.  |
| PG     | 11      | Output | Power good flag pin. This open drain output asserts low if the output voltage is out of regulation. A pull-up resistor of 1M $\Omega$ is required if this function is used.  |
| EN     | 12      | Input  | Enable pin. This pin has an internal voltage divider that sets the internal UVLO value. Pull this pin down to AGND to disable the module.  |
| PGND   | 13 (EP) | Power  | Exposed Pad. This pin is internally connected to PGND. It is recommended to connect this pin to the ground plane(s) for heat dissipation.  |

# Magl<sup>3</sup>C Power Module

WPME-VDLM - Variable Step Down LGA Module



## **ORDERING INFORMATION**

| ORDER CODE | SPECIFICATIONS             | PACKAGE    | PACKAGING UNIT         |
|------------|----------------------------|------------|------------------------|
| 171033801  | 3A / 0.85V-6V Vout version | LGA-12EP   | 13" Reel (1000 pieces) |
| 178033801  | 3A / 0.85V-6V Vout version | Eval Board | 1 piece                |

#### **PIN COMPATIBLE FAMILY MEMBERS**

| ORDER CODE | SPECIFICATIONS              | PACKAGE  | PACKAGING UNIT         |
|------------|-----------------------------|----------|------------------------|
| 171013801  | 1A / 0.85V-13V Vout version | LGA-12EP | 13" Reel (1000 pieces) |
| 171023801  | 2A / 0.85V-13V Vout version | LGA-12EP | 13" Reel (1000 pieces) |

## **SALES INFORMATION**

## **SALES CONTACT**

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**EMC** and Inductive Solutions

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#### **ABSOLUTE MAXIMUM RATINGS**

#### **Caution:**

Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

| SYMBOL        | PARAMETER  | LIN   | UNIT                  |       |
|---------------|--|---|-----------------------|-------|
| STIVIBOL      | PARAIVIETER  | MIN <sup>(1)</sup>  | MAX <sup>(1)</sup>    | Oluli |
| VIN           | Input Pin Voltage                                    | -0.3  | 42                    | V     |
| VOUT          | Output Pin Voltage                                   | -0.3  | V <sub>IN</sub> + 0.3 | V     |
| FB            | Feedback Pin Voltage                                 | -0.3  | 8                     | V     |
| EN            | Enable Pin Voltage                                   | -0.3  | V <sub>IN</sub> + 0.3 | V     |
| PG            | Power Good Pin Voltage                               | -0.3  | V <sub>IN</sub> + 0.3 | V     |
| VCC           | VCC pin voltage with input voltage from 3.7V to 38V  | -0.3  | 4                     | V     |
| VCC           | VCC pin voltage with input voltage from 3.5V to 3.7V | MIN <sup>(1)</sup> M  -0.3  -0.3 V <sub>IN</sub> -0.3  -0.3 V <sub>IN</sub> -0.3 V <sub>IN</sub> -0.3 V <sub>IN</sub> ut voltage from 3.7V to 38V -0.3  ut voltage from 3.5V to 3.7V -0.3 V <sub>IN</sub> ection pin -0.3 V <sub>CC</sub> ing storage temperature | V <sub>IN</sub> + 0.3 | V     |
| FSW           | Switching frequency selection pin                    | -0.3  | V <sub>CC</sub> + 0.3 | V     |
| $T_{storage}$ | Assembled, non-operating storage temperature         | -40   | 125                   | °C    |
| $V_{ESD}$     | ESD Voltage (HBM), all pins (C=100pF R=1.5kΩ)        | -2  | 2                     | kV    |

#### **OPERATING CONDITIONS**

Operating conditions are conditions under which the device is intended to be functional. All values are referenced to GND. MIN and MAX limits are valid for the recommended ambient temperature range of -40 °C to 105 °C. Typical values represents statistically the utmost probable values at the following conditions:  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 2 \times 4.7 \mu F$  ceramic,  $C_{OUT} = 47 \mu F$  ceramic,  $C_{OUT} = 47$ 

| SYMBOL           | PARAMETER  | MIN <sup>(1)</sup> | TYP <sup>(2)</sup> | MAX <sup>(1)</sup> | UNIT |
|------------------|--|--------------------|--------------------|--------------------|------|
| $V_{IN}$         | Input Voltage                                    | 3.5                | -                  | 38                 | V    |
| V <sub>out</sub> | Output Voltage (Maximum I <sub>OUT</sub> = 2.5A) | 0.85               | -                  | 13                 | V    |
| <b>v</b> 001     | Output Voltage (Maximum I <sub>OUT</sub> = 3A)   | 0.85               | -                  | 6                  | V    |
| Ta               | Ambient temperature range                        | -40                | -                  | 105                | °C   |
| T <sub>jop</sub> | Junction temperature range                       | -40                | -                  | 125                | °C   |
| I <sub>out</sub> | Output current                                   | -                  | -                  | 3                  | А    |

#### THERMAL SPECIFICATIONS

Typical values represents statistically the utmost probable values at the following conditions:  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 2 \times 4.7 \mu F$  ceramic,  $C_{OUT} = 47 \mu F$  ceramic,  $T_A = 25 \, ^{\circ} C$  unless otherwise noted.

| SYMBOL          | PARAMETER  | TYP <sup>(2)</sup> | UNIT |
|-----------------|--|--------------------|------|
| $\Theta_{JA}$   | Junction-to-ambient thermal resistance <sup>(3)</sup>    | 34                 | K/W  |
| $\Theta_{JC}$   | Junction-to-case (top) thermal resistance <sup>(3)</sup> | 17                 | K/W  |
| T <sub>SD</sub> | Thermal shutdown, rising                                 | 165                | °C   |
| TSD             | Thermal shutdown, hysteresis                             | 30                 | °C   |



## **ELECTRICAL SPECIFICATIONS**

 $MIN \ and \ MAX \ limits \ are \ valid \ for \ the \ recommended \ ambient \ temperature \ range \ of \ -40\,^{\circ}C \ to \ 105\,^{\circ}C. \ Typical \ values \ represents$ statistically the utmost probable values at the following conditions:  $V_{IN} = 24V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = 2 \times 4.7 \mu F$  ceramic,  $C_{OUT} = 47 \mu F$ ceramic,  $T_A = 25$ °C unless otherwise noted.

| SYMBOL              | PARAMETER  | TEST CONDITIONS   | MIN <sup>(1)</sup> | TYP <sup>(2)</sup> | MAX <sup>(1)</sup> | UNIT |
|---------------------|--|---|--------------------|--------------------|--------------------|------|
| V <sub>UVLO</sub>   | V <sub>IN</sub> rising threshold                 |   | 2.3                | -                  | 3.3                | V    |
| VUVLO               | V <sub>IN</sub> falling threshold                |   | 2.15               | -                  | 3.15               | V    |
| I <sub>oc</sub>     | Overcurrent limit                                | No slope contribution                                       | -                  | 4.6                | -                  | А    |
| T <sub>ON_MIN</sub> | Minimum on-time                                  |   | -                  | 75                 | -                  | ns   |
|                     |  | Enable  |                    |                    |                    |      |
| $V_{EN}$            | Enable threshold                                 | Rising  | 1.08               | 1.2                | 1.32               | V    |
| VEN                 | Litable tilleshold                               | Hysteresis  | -                  | 0.2                | -                  | V    |
|                     |  | VCC Regulator   |                    |                    |                    |      |
| V <sub>CC</sub>     | LDO output voltage                               |   | 3                  | 3.3                | 3.6                | V    |
|                     | Input Quiesc                                     | ent, No Load and Shutdown Curr                              | ent                |                    |                    |      |
| I <sub>SD</sub>     | Shutdown current from V <sub>IN</sub>            | V <sub>EN</sub> = GND                                       | -                  | 2                  | -                  | μΑ   |
| ΙQ                  | Quiescent current from V <sub>IN</sub>           | $VOUT \leq 3.2V$ , no switching                             | 20                 | 35                 | 60                 | μΑ   |
| l 'Q                | Quiescent current from V <sub>IN</sub>           | VOUT > 3.2V, no switching                                   | 1                  | 3.5                | 6                  | μΑ   |
| I <sub>IN-NL</sub>  | No load input current                            | VOUT = 3.3V   | -                  | 15.3               | -                  | μΑ   |
|                     |  | Output Voltage  |                    |                    |                    |      |
| $V_{FB}$            | Voltage reference                                | $T_J = -40$ °C $\leq T_J \leq 125$ °C                       | 0.842              | 0.85               | 0.858              | V    |
|                     |  | Soft-Start  |                    |                    |                    |      |
| t <sub>SS</sub>     | Soft-start time                                  | Rising edge to V <sub>OUT</sub> (nom.)                      | 1                  | 1.3                | 1.6                | ms   |
|                     |  | Switching Frequency   |                    |                    |                    |      |
| f <sub>SW</sub>     | Switching frequency                              |   | 200                | -                  | 2200               | kHz  |
|                     | •  | Power Good  | •                  |                    |                    |      |
| $V_{PG}$            | Power good V <sub>OUT</sub><br>threshold low     | $T_J = -40^{\circ}\text{C} \le T_J \le 125^{\circ}\text{C}$ | 87                 | 90                 | 93                 | %    |
| $V_{PG}$            | Power good V <sub>OUT_H</sub> threshold          | $T_J = -40$ ° C $\leq T_J \leq 125$ ° C                     | -                  | 120                | -                  | %    |
| V <sub>PG_HYS</sub> | Power good V <sub>OUT</sub> threshold hysteresis |   | -                  | 3                  | -                  | %    |
|                     | •  | Efficiency  | •                  |                    |                    |      |
|                     |  | $V_{IN} = 12V, V_{OUT} = 3.3V,$<br>$I_{OUT} = 3A$           | -                  | 87                 | -                  | %    |
| η                   | Efficiency                                       | $V_{IN} = 12V$ , $V_{OUT} = 5V$ , $I_{OUT} = 3A$            | -                  | 87                 | -                  | %    |
|                     |  | $V_{IN} = 24V$ , $V_{OUT} = 5V$ , $I_{OUT} = 3A$            | -                  | 86                 | -                  | %    |

# Magl<sup>3</sup>C Power Module

WPME-VDLM - Variable Step Down LGA Module



#### RoHS, REACh

RoHS directive

REACh directive



Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACh).

#### **PACKAGE SPECIFICATIONS**

| Part Number | Lead Finish Material | WEIGHT |
|-------------|----------------------|--------|
| 171033801   | ENEPIG               | 0.78g  |

#### **NOTES**

- (1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
- (2) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probable values assuming a Gaussian distribution.
- (3) Measured on the 178033801 evaluation board, a 80 x 80mm four layer board, with 70 µm (2 ounce) copper.



## **TYPICAL PERFORMANCE CURVES**

If not otherwise specified, the following conditions apply:  $V_{IN} = 24V$ ;  $C_{IN} = 2x 4.7 \mu F X7R 50V$  ceramic (885012209048);  $C_{OUT}$ =  $47\mu F$  X5R ceramic;  $T_A = 25$ °C.

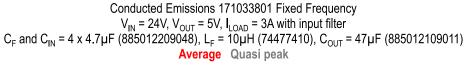
## RADIATED EMISSIONS EN55032 (CISPR-32) CLASS B COMPLIANT TEST SETUP

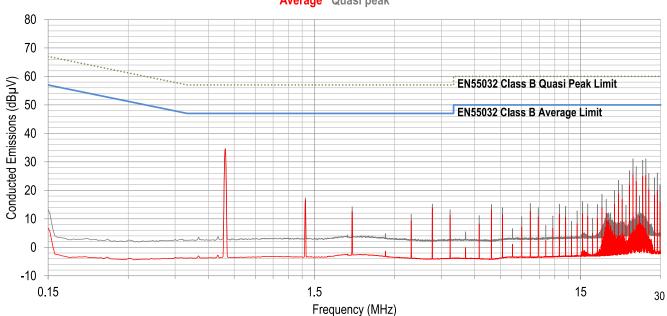
- Measured with module on an Evaluation Board 178033801 in a Fully Anechoic Room (FAR) at 3m antenna distance.
- Measurement input wire length: 160cm (80cm Horizontal + 80cm Vertical)
- Output wire length: 1m
- Resistor as load

#### CONDUCTED EMISSIONS EN55032 (CISPR-32) CLASS B COMPLIANT TEST SETUP

- Measurement input wire length: 80cm
- Output wire length: 1m
- Resistor as load

#### **CONDUCTED EMISSIONS - FIXED FREQUENCY**

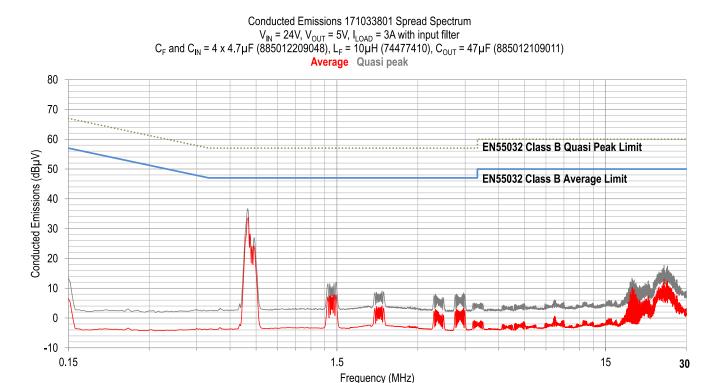




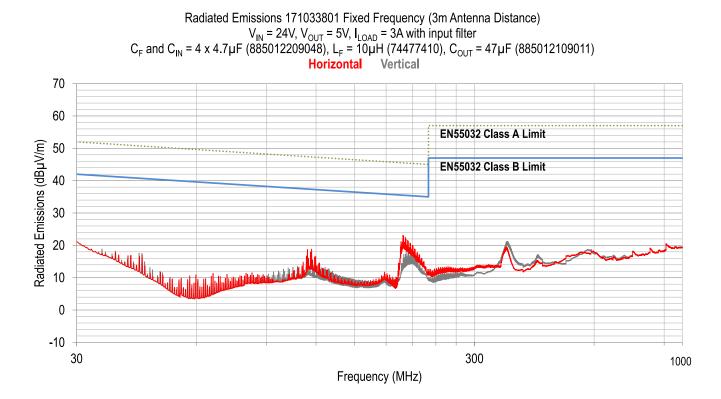
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#### **CONDUCTED EMISSIONS - SPREAD SPECTRUM**

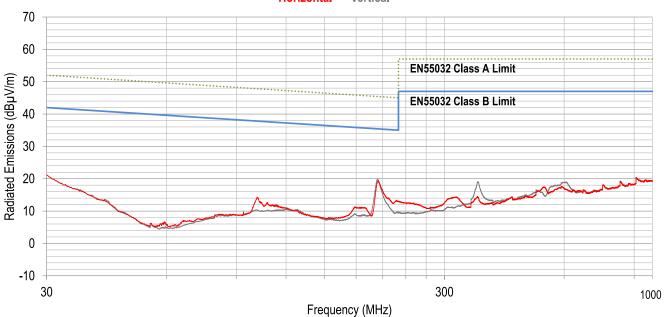


## **RADIATED EMISSIONS - FIXED FREQUENCY**



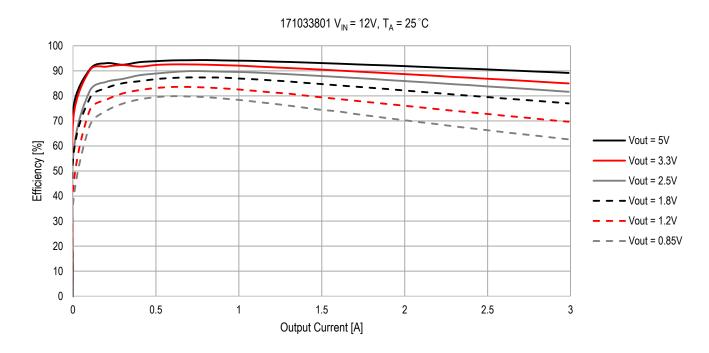


## **RADIATED EMISSIONS - SPREAD SPECTRUM**

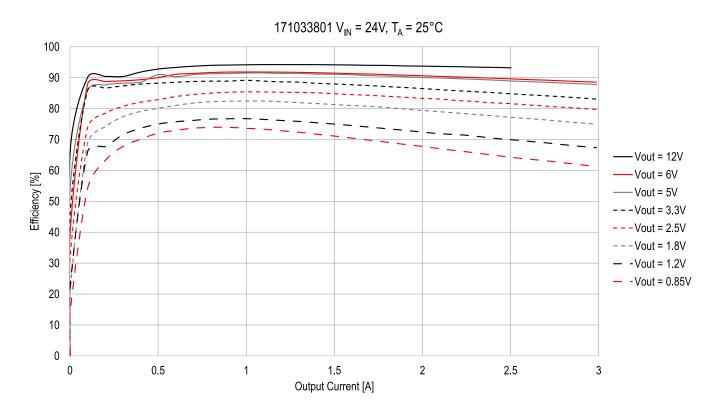




## **EFFICIENCY 12Vin**

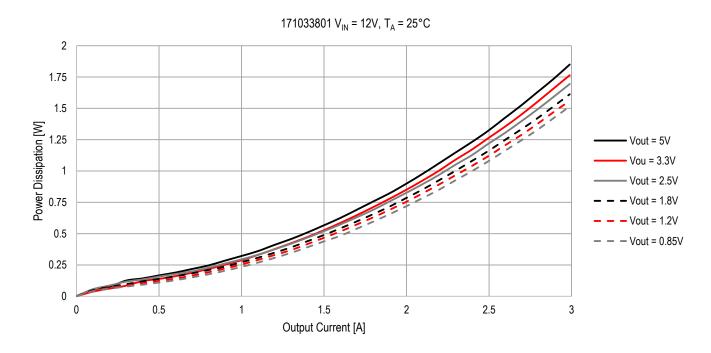


## **EFFICIENCY 24Vin**

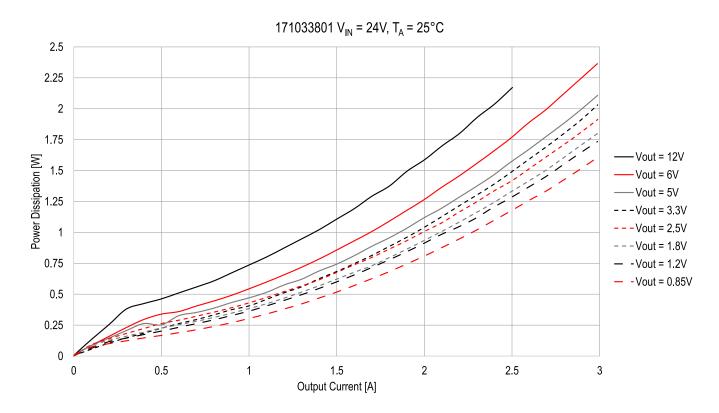




## **POWER DISSIPATION 12Vin**

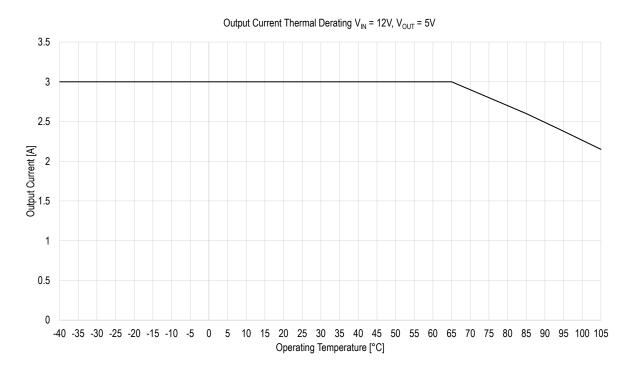


## **POWER DISSIPATION 24Vin**

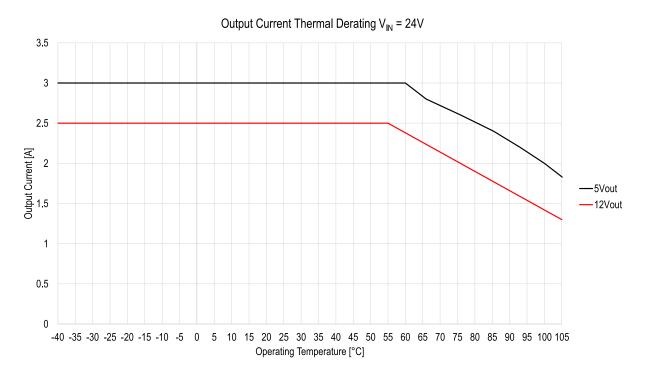




## **THERMAL DERATING 12Vin**



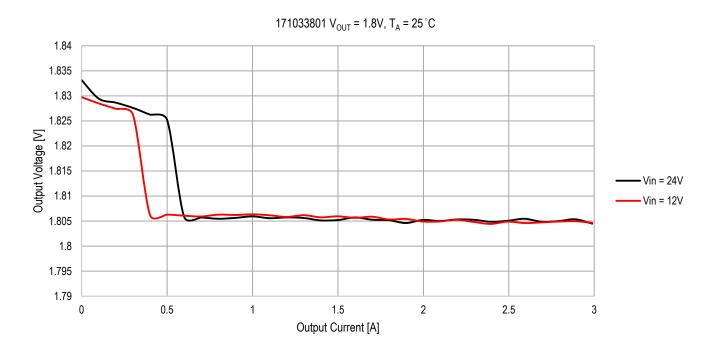
## **THERMAL DERATING 24Vin**



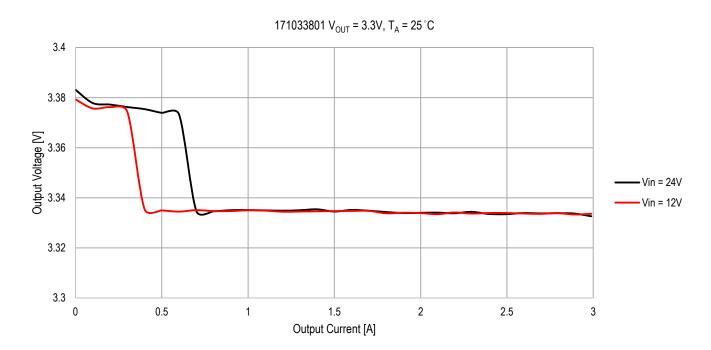
Note: Both thermal derating graphs were measured on the 178033801 Evaluation Board (80 x 80 mm, four layers, 70 µm copper thickness). Please see T<sub>A</sub> limits in Operating Conditions on page 4.



## **LOAD REGULATION 1.8Vout**

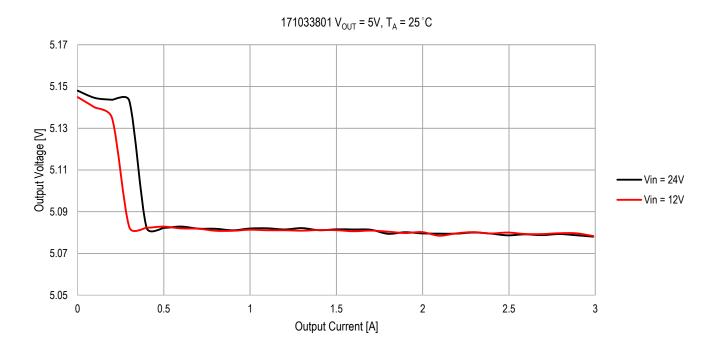


## **LOAD REGULATION 3.3Vout**

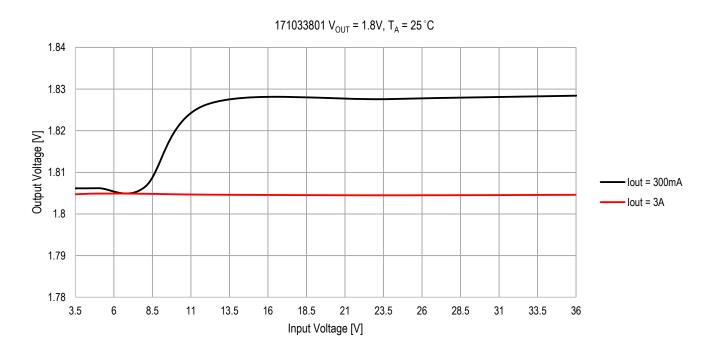




## **LOAD REGULATION 5Vout**

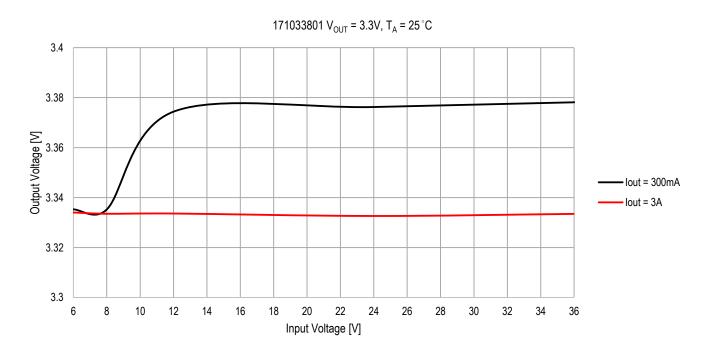


## **LINE REGULATION 1.8Vout**

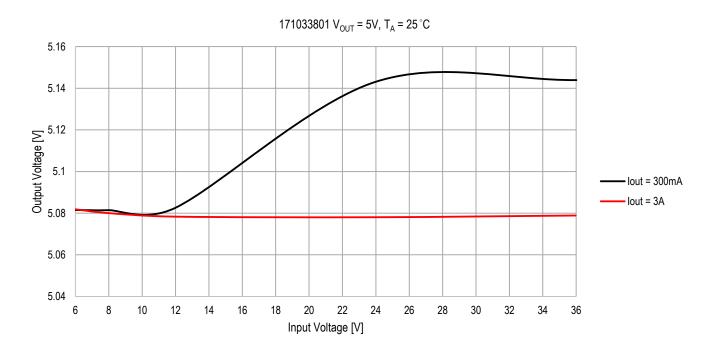




## **LINE REGULATION 3.3Vout**

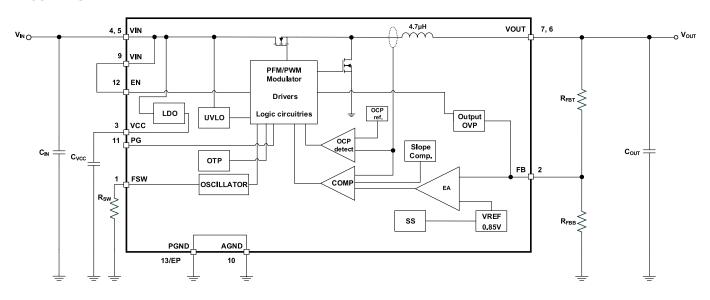


## **LINE REGULATION 5Vout**





#### **BLOCK DIAGRAM**



## **CIRCUIT DESCRIPTION**

The WPME-VDLM 171033801 Magl<sup>3</sup>C Power Module is a DC-DC power supply including the switching regulator with integrated MOSFETs, controller and compensation, as well as the shielded inductor integrated in one package. The control scheme is based on a current mode (CM) regulation loop.

The V<sub>OUT</sub> of the regulator is divided by the feedback resistor network R<sub>FBT</sub> and R<sub>FBB</sub> and fed into the FB pin. The error amplifier compares this signal with the internal 0.85V reference. The error signal is amplified and controls the on-time of a fixed frequency pulse width generator. This signal drives the power MOSFETs.

The current mode architecture features a constant frequency during load steps. Only the on-time is modulated. It is internally compensated and stable with low ESR output capacitors and requires no external compensation network.

This architecture supports fast transient response and very small output voltage ripples (<10m $V_{p-p}$ ) are achieved.

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## **DESIGN FLOW**

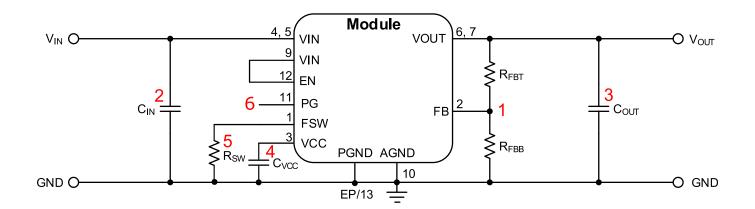
The following simple steps will show how to select the external components to design the 171033801 into an application.

## **Essential Steps**

- 1. Set output voltage
- 2. Select input capacitor
- **3.** Select output capacitor
- **4.** Select V<sub>CC</sub> capacitor
- 5. Set switching frequency

## **Optional Steps**

6. Set power good





## **STEP 1 Setting the Output Voltage (Vout)**

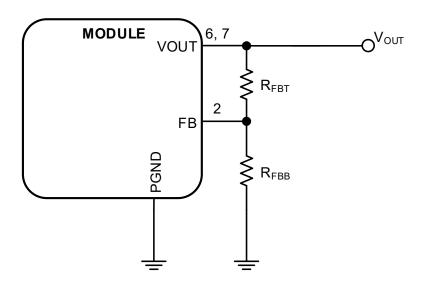
The output voltage is selected with an external resistor divider between  $V_{OUT}$  and GND (see circuit below). The voltage across the lower resistor of the divider is provided to the FB pin and compared with a reference voltage of 0.85V ( $V_{REF}$ ). The output voltage adjustment range is from 0.85V to 6V. The output voltage can be calculated according to the following formula:

$$V_{\rm OUT} = V_{\rm REF} \cdot (\frac{R_{\rm FBT}}{R_{\rm FBB}} + 1) \tag{1}$$

One resistor must be chosen and then the other resistor can be calculated. For example, if  $R_{FBT}$  = 402k $\Omega$  then the resistance value of the lower resistor in the feedback network is indicated in the table below for common output voltages.

| V <sub>OUT</sub> (V)          | 0.85 | 1.2 | 1.8 | 2.5 | 3.3 | 5.0  | 9.0* | 12*  |
|-------------------------------|------|-----|-----|-----|-----|------|------|------|
| $R_{FBB}$ (E96) ( $k\Omega$ ) | Open | 976 | 357 | 205 | 137 | 80.6 | 41.2 | 30.1 |

<sup>\*</sup>Note that for output voltages above 6V, the output current may not exceed 2.5A.



## STEP 2 Select the Input Capacitor (CIN)

The energy at the input of the Module is stored in the input capacitor. An input capacitor (10µF) is required externally to provide cycle-by-cycle switching current and to support load transients. The external input capacitor must be placed directly at the VIN pin. For this Magl<sup>3</sup>C Module it is recommended to use a MLCC (multi-layer ceramic capacitor) of 10µF. Attention must be paid to the voltage, frequency and temperature deratings and thermal class of the selected capacitor.



## STEP 3 Select the Output Capacitor (Cout)

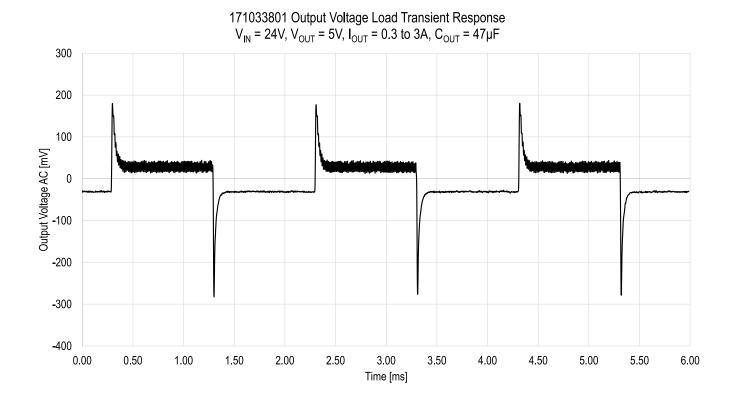
The output capacitor should be selected in order to minimize the output voltage ripple and to provide a stable voltage at the output. It also affects the loop stability. Different output capacitors are recommended depending on the output voltage and switching frequency selected for an application. The external components section provides evaluated recommendations of components for various typical application specifications. Attention must be paid to the voltage, frequency and temperature derating and thermal class of the selected capacitor.

In general, the output voltage ripple can be calculated using the following equation:

$$V_{\text{OUT ripple}} = \Delta I_{\text{L}} \cdot ESR + \Delta I_{\text{L}} \cdot (\frac{1}{8 \cdot f_{\text{SW}} \cdot C_{\text{OUT}}}) \tag{2}$$

where  $\Delta I_L$  is the inductor current ripple and can be calculated with the following equation:

$$\Delta I_{\mathsf{L}} = \frac{V_{\mathsf{OUT}} \cdot (V_{\mathsf{IN}} - V_{\mathsf{OUT}})}{f_{\mathsf{SW}} \cdot L \cdot V_{\mathsf{IN}}} \tag{3}$$



# Magl<sup>3</sup>C Power Module

WPME-VDLM - Variable Step Down LGA Module



#### STEP 4 Select the $V_{CC}$ Capacitor ( $C_{VCC}$ )

The  $171033801 \text{ MagI}^3\text{C}$  Module requires a capacitor,  $C_{VCC}$ , to be placed at the VCC pin to support the internal LDO integrated inside of the module. To ensure stable operation and optimum performance across the entire functional range, a  $1\mu\text{F}$  capacitor is recommended. The Würth Elektronik eiSos capacitors have been experimentally evaluated for performance and is the recommended choice.

## **STEP 5** Select the Switching Frequency (f<sub>SW</sub>)

The switching frequency must be selected according to the input voltage, output voltage and load current for the best performance in loop regulation and transient response. This is done by choosing a resistor value from the table below based on the application conditions. This resistor can either be tied directly to AGND for a fixed switching frequency, indicated in the table below, or it can be tied to VCC allow for spread spectrum operation. Spread spectrum operation will allow for a change in switching frequency typically of  $\pm$  5%. The peaks of the switching spectrum will be reduced and spread, reducing the filter necessary to comply to EN55032 Radiated and Conducted Standards. The difference in EMI behavior can be seen in the EMI section of the data sheet.

| V <sub>OUT</sub> (V)        | 0.85 | 1.2 | 1.8 | 2.5 | 3.3 | 5   |
|-----------------------------|------|-----|-----|-----|-----|-----|
| Switching Frequency (kHz)   | 200  | 400 | 400 | 500 | 700 | 700 |
| $R_{SW}\left(k\Omega ight)$ | 1.8  | 0   | 0   | 3.3 | 5.6 | 5.6 |

When  $R_{SW}$  is indicated as 0  $k\Omega$ , FSW should be tied directly to AGND or VCC.

#### **STEP 6 Set Power Good Resistor**

The PG pin is an open-drain output. Once the output voltage is above 90% (typ.) of the internal reference voltage, the PG pin transitions to a high impedance state. The recommended pull-up resistor value is  $1M\Omega$ , which should be connected to a voltage source such as VIN. The PG pin is pulled low when the output voltage is lower than 90% (typ.) or higher than 120% (typ.) of the internal reference voltage. The PG pin will be pulled low when the UVLO or thermal shutdown activates or when the EN pin is pulled low.

# Magl<sup>3</sup>C Power Module

WPME-VDLM - Variable Step Down LGA Module



#### **MODES OF OPERATION**

The 171033801 Module has two different modes of operation and the transition takes place automatically depending on the load current value. Under light load conditions, the module operates in PFM mode where the Module runs at a lower switching frequency to reduce the current consumption, which leads to achieving a higher efficiency. The PFM control is achieved by creating a single pulse to turn on the high side switch while monitoring the inductor current. The high side switch is kept on until the inductor current hits a preset value of 600mA (typ.).

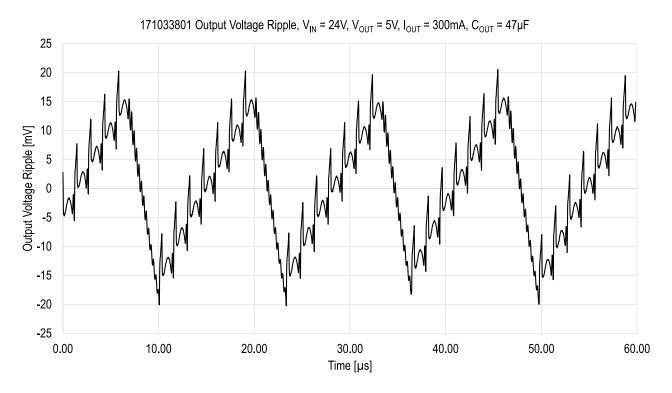
After reaching this value, the high side switch is turned off and the low side switch turns on. The inductor current decreases until it reaches zero. When the inductor current reaches zero, both switches are turned off (idle time) and the output capacitor solely supplies the load with energy. While the energy is supplied to the load, the output voltage starts to drop. The Module monitors the output voltage ripple value and when it hits a certain limit, while the two switches are off, another pulse is initiated and the cycle repeats. When the load current increases, the idle time decreases and the switching frequency increases until the nominal switching frequency is reached and the Module transitions to PWM mode.



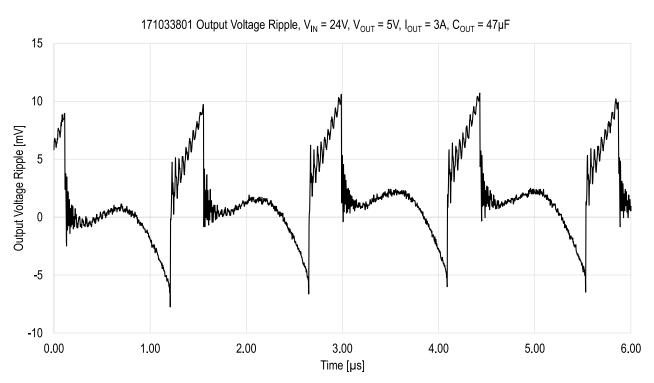
## **OUTPUT VOLTAGE RIPPLE**

If the module is working in PWM mode, the output voltage ripple is very low and is determined by the switching frequency, which is set by the resistor  $R_{SW}$ . If the load current is low enough to be in the PFM mode of operation then the output voltage ripple will be higher with a frequency lower than the nominal switching frequency (see pictures below).

## **PFM Operation**



## **PWM Operation**





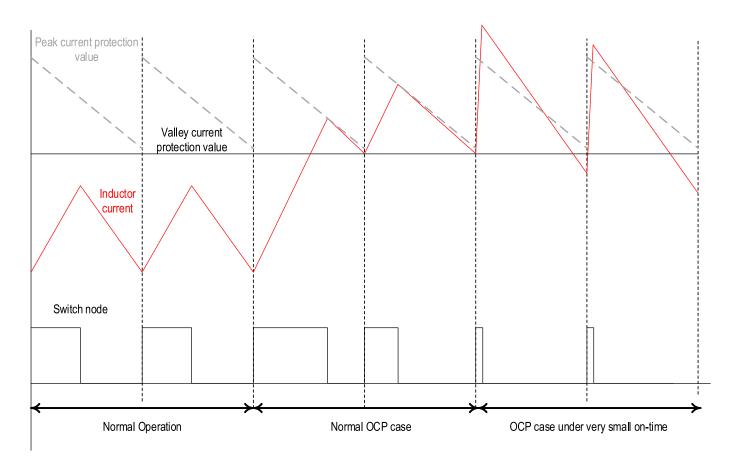
#### **PROTECTION FEATURES**

#### Overcurrent Protection (OCP) and Short Circuit Protection (SCP)

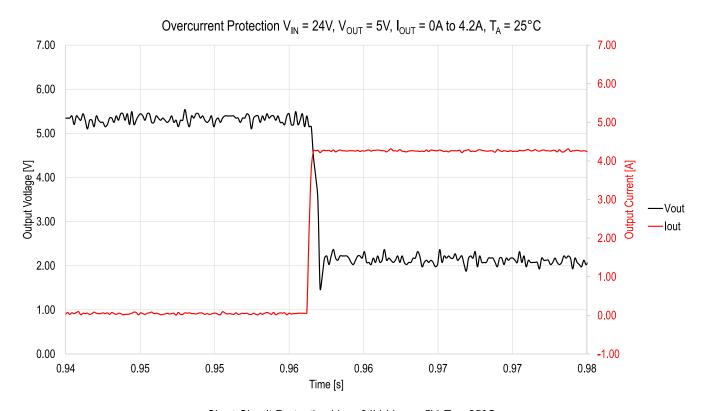
The 171033801 Magl<sup>3</sup>C Module implements a cycle-by-cycle current limit, which is realized through the peak current mode control architecture of the module. The peak current of the high side switch and the valley current of the low side switch are both monitored. Additionally, limiting the valley current during an overcurrent scenario reduces the thermal stresses generated inside of the power module by reducing the rms current value.

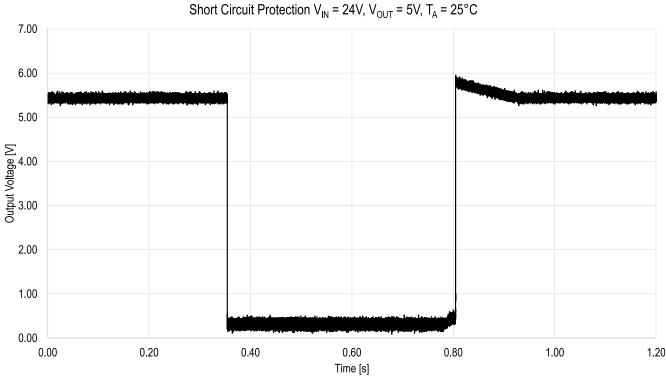
By monitoring both switch currents the user can be confident that the power module will be well protected against overcurrent and short circuit scenarios even in the most extreme conditions of operation, such as very high or low duty cycles. Under very low duty cycle conditions, the peak current can exceed the overcurrent preset value. When this occurs, the low side switch is turned on until the current drops below the preset valley current value. This behavior may result in pulse skipping, temporarily decreasing the effective switching frequency in order to better protect the module during overcurrent scenarios.

The inductor current exceeding the peak protection value will only take place if the minimum on-time stated in the ELECTRICAL SPECIFICATIONS is violated. Even in such a scenario, the power module will still be protected. Following the recommended switching frequencies stated in Step 5 of the DESIGN FLOW will always ensure the minimum on-time is maintained.











#### **Output Overvoltage Protection (OVP)**

The Magl<sup>3</sup>C Module integrates an output overvoltage protection feature. This feature is implemented by monitoring the feedback pin and comparing it to the internal reference. When the feedback pin voltage is 20% higher than the reference voltage, the low side switch is turned on to discharge the output capacitor. There is also a negative current limit set on the low side switch to prevent overcurrent stress when this protection feature activates.

This feature protects the module during specific application scenarios such as when the module is connected to a switching load with long wires or backfeeding from other loads sharing the same voltage node occurs.

## **Over Temperature Protection (OTP)**

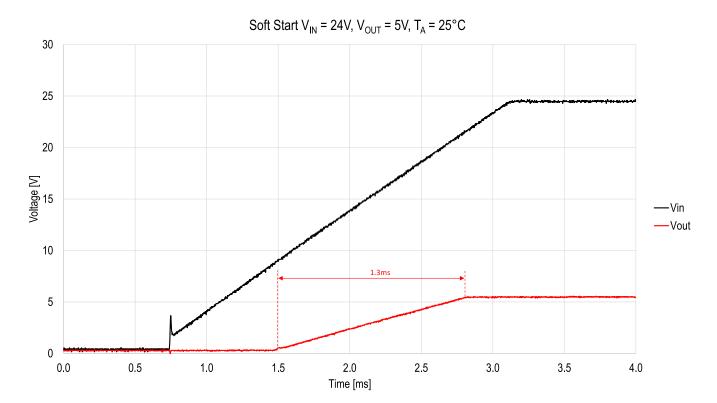
Thermal protection helps prevent catastrophic failures due to accidental device overheating. The junction temperature of the Magl<sup>3</sup>C Module should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit, which activates when the junction temperature reaches  $165^{\circ}$ C (typ). Under the thermal shutdown condition both MOSFETs remain off, causing the output voltage to drop. When the junction temperature falls below  $135^{\circ}$ C (typ) the internal soft start is released,  $V_{OUT}$  rises smoothly, and normal operation resumes.

## Input Undervoltage Lockout (UVLO)

The device incorporates input undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the UVLO are indicated in the ELECTRICAL SPECIFICATIONS.

#### **Soft Start**

The Magl<sup>3</sup>C Module implements an internal soft start in order to limit the inrush current and avoid output voltage overshoot during start-up. The typical duration of the soft start is around 1.3ms (see figure below).



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## Enable/Adjustable UVLO

The Magl<sup>3</sup>C Module is enabled by setting the EN pin high. When the EN voltage reaches 1.2V the module begins switching and the internal soft start regulates the output voltage rise until the desired output voltage is met, allowing normal operation to take place.

The UVLO threshold of the power module can be externally set by adding a resistor between VIN and EN and a second resistor between EN and GND. This voltage divider should be chosen so that the desired minimum input voltage corresponds to 1.2V at EN.

The two resistors should be chosen based on the following ratio:

$$\frac{R_{\text{ENT}}}{R_{\text{FNR}}} = \frac{V_{\text{UVLO (EXT.)}}}{1.2} - 1 \tag{4}$$

V<sub>UVLO (EXT.)</sub> = User programmable input voltage threshold to enable and disable the module

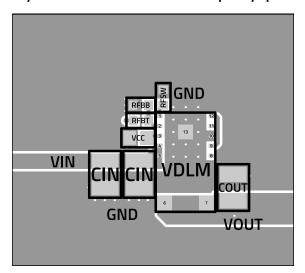
This is often used in battery-powered systems to prevent deep discharge of the system battery. It is also useful in system designs with output rail sequencing or to prevent early turn-on of the supply as the main input voltage rail rises at power-up. Most systems will benefit by using the precision Enable threshold to establish a system undervoltage lockout based on specific application parameters.

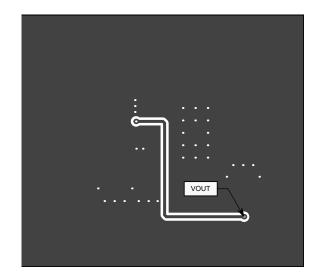
In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the Magl<sup>3</sup>C Module output rail. The recommended approach is to choose an input UVLO level that is higher than the target regulated output voltage for the stage.



## LAYOUT RECOMMENDATION

## Layout recommedation for fixed frequency operation





The images above show the top and bottom routed outer layers for a recommended four layer layout. There are two internal GND layers that are not pictured above. These are necessary for optimal thermal performance.

The pictures above show a possible layout for the 171033801 Magi<sup>3</sup>C Module. Nevertheless, some recommendations

The pictures above show a possible layout for the 171033801 Magl<sup>3</sup>C Module. Nevertheless, some recommendations should be followed when designing the layout:

- 1. The input and output capacitors should be placed as close as possible to the VIN and VOUT pins of the device.
- 2. The feedback resistor divider should be placed as close as possible to the FB pin.
- 3. Avoid placing vias in any of the pads for the module.



## RECOMMENDED EXTERNAL COMPONENTS

| V <sub>OUT</sub> (V) | F <sub>SW</sub> *<br>(kHz) | $\mathbf{R}_{FBT}$ (k $\Omega$ ) | $\mathbf{R}_{FBB}$ (k $\Omega$ ) | $R_{PG}$ (M $\Omega$ ) | $\mathbf{R}_{SW}$ (k $\Omega$ ) | C <sub>IN</sub> (µF) | С <sub>оит</sub> (µF) | C <sub>vcc</sub> (µF) |
|----------------------|----------------------------|----------------------------------|----------------------------------|------------------------|---------------------------------|----------------------|-----------------------|-----------------------|
| 0.85                 | 200                        | 402                              | Open                             | 1                      | 1.8                             | 2x 4.7μF, 50V        | 440µF, 6.3V           | 1μF, 16V              |
| 1.2                  | 400                        | 402                              | 976                              | 1                      | 0                               | 2x 4.7μF, 50V        | 200µF, 6.3V           | 1μF, 16V              |
| 1.8                  | 400                        | 402                              | 357                              | 1                      | 0                               | 2x 4.7μF, 50V        | 200μF, 6.3V           | 1μF, 16V              |
| 2.5                  | 500                        | 402                              | 205                              | 1                      | 3.3                             | 2x 4.7μF, 50V        | 100µF, 6.3V           | 1μF, 16V              |
| 3.3                  | 700                        | 402                              | 137                              | 1                      | 5.6                             | 2x 4.7μF, 50V        | 47μF, 6.3V            | 1μF, 16V              |
| 5                    | 700                        | 402                              | 80.6                             | 1                      | 5.6                             | 2x 4.7μF, 50V        | 47μF, 10V             | 1μF, 16V              |
|                      | Würth Ele                  | ktronik P                        | art Numb                         | er/Family              |                                 | 885012209048         | 885012207051          |                       |

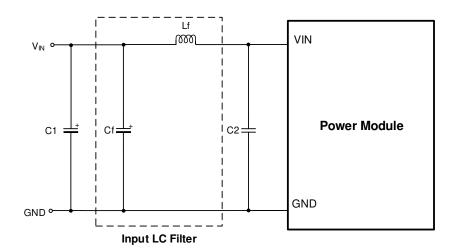
<sup>\*</sup>Recommended switching frequency values for optimum module operation. Stable module operation can also be achieved with different switching frequencies; however, a reduction of the module performance is possible.

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## **FILTER SUGGESTION**

The input filter shown in the schematic below is recommended to achieve conducted and radiated compliance according to EN55032 Class B (see also RADIATED AND CONDUCTED TYPICAL PERFORMANCE CURVES).



| Designator     | Description  | Order Code   | Manufacturer |
|----------------|--|--------------|--------------|
| C <sub>f</sub> | 2x Filter ceramic capacitor 4.7μF, X7R, 50V                              | 885012209048 | WE           |
| L <sub>f</sub> | Filter inductor 10 $\mu$ H, PD2 family, $I_{SAT}$ = 2.5A, $I_{R}$ = 2.2A | 74477410     | WE           |

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#### HANDLING RECOMMENDATIONS

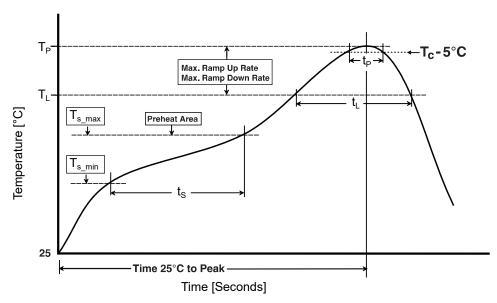
- 1. The power module is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
- 2. The parts are delivered in a sealed bag (Moisture Barrier Bags = MBB) and should be processed within one year.
- 3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
- 4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
- 5. Maximum number of solder cycles is two.
- 6. For minimum risk, solder the module in the last solder cycle of the PCB production.
- 7. For soldering process please consider lead material copper (Cu) and lead finish tin (Sn).
- 8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
- 9. The profile below is valid for convection reflow only.
- 10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

#### **SOLDER PROFILE**

Table 1: Reflow Solder Profile

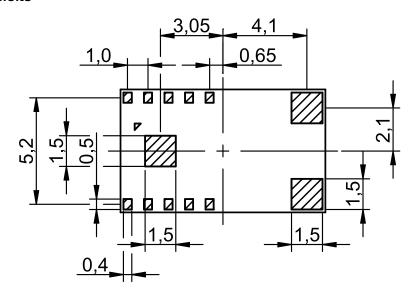
| Profile Feature  | Symbol             | Value                           |  |  |
|--|--------------------|---------------------------------|--|--|
| Preheat temperature minimum                                | T <sub>s_min</sub> | 150°C                           |  |  |
| Preheat temperature maximum                                | T <sub>s_max</sub> | 200°C                           |  |  |
| Preheat time from T <sub>s_min</sub> to T <sub>s_max</sub> | t <sub>s</sub>     | 60-120 seconds                  |  |  |
| Liquidous temperature                                      | TL                 | 217°C                           |  |  |
| Time maintained above $T_{L}$                              | t∟                 | 60-150 seconds                  |  |  |
| Peak package body temperature                              | T <sub>P</sub>     | $T_P \leq 250 ^{\circ} C$       |  |  |
| Time within 5°C of actual peak<br>temperature              | t <sub>P</sub>     | $t_P \leq 30 \; \text{seconds}$ |  |  |
| Ramp-up Rate (T <sub>L</sub> to T <sub>p</sub> )           |                    | 3°C/second maximum              |  |  |
| Ramp-down rate (T <sub>p</sub> to T <sub>L</sub> )         |                    | 6°C/second maximum              |  |  |
| Time 25°C to peak temperature                              |                    | 8 minutes maximum               |  |  |

Please refer to JEDEC J-STD020E for further information pertaining to reflow soldering of electronic components.

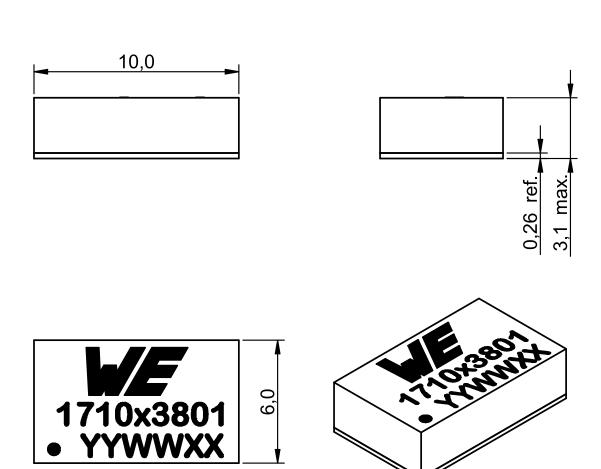




## **PHYSICAL DIMENSIONS**



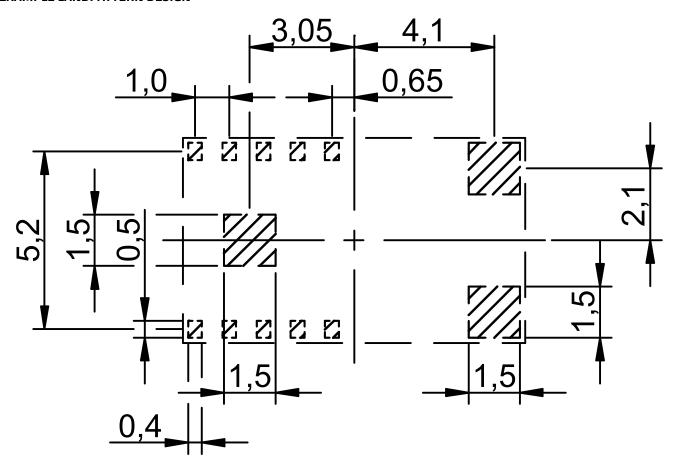
Bottom view



All dimensions in mm Tolerances ±0,1mm unless otherwise specified



## **EXAMPLE LANDPATTERN DESIGN**

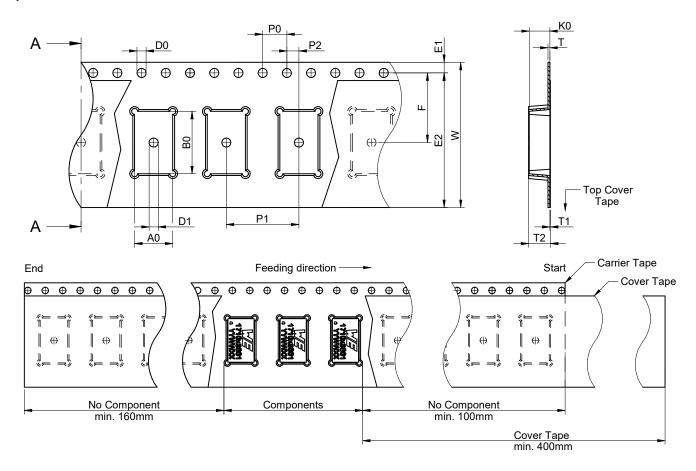


All dimensions in mm Stencil thickness of 100µm.



## **PACKAGING**

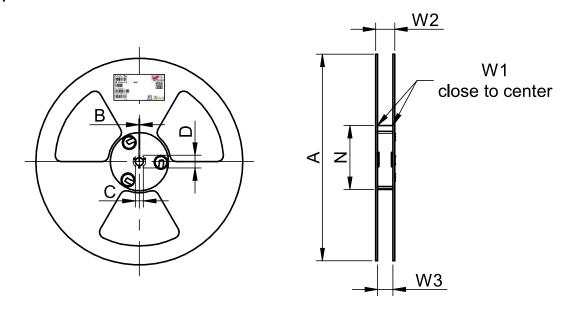
## Tape (mm)

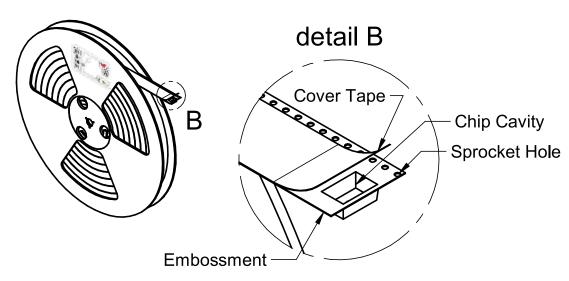


| Tape<br>Type | AO   | ВО   | W    | Т     | T1 | T2 | КО   | P0   | P1   | P2   | D0   | D1   | E1   | E2    | F     | Material    |
|--------------|------|------|------|-------|----|----|------|------|------|------|------|------|------|-------|-------|-------------|
|              | ±0.1 | ±0.1 | ±0.3 | ±0.05 |    |    | ±0.1 | ±0.1 | ±0.1 | ±0.1 | +0.1 | Min. | ±0.1 | ±0.4  | ±0.1  |             |
| 2a           | 6.3  | 10.3 | 24   | 0.3   |    |    | 3.4  | 4    | 12   | 2    | 1.5  | 1    | 1.75 | 22.25 | 11.50 | Polystyrene |



# Reel (mm)





| Α      | В    | С     | D     | N      | W1   | W2   | W3   | Material    |
|--------|------|-------|-------|--------|------|------|------|-------------|
| ±1.0   | ±0.5 | ±0.5  | Min.  | ±0.5   | Тур. | Тур. | Тур. |             |
| 330.00 | 2.0  | 13.00 | 12.50 | 102.00 | 30.2 | 30.2 | 24.8 | Polystyrene |

# Magl<sup>3</sup>C Power Module

**WPME-VDLM** - Variable Step Down LGA Module



## **DOCUMENT HISTORY**

| Revision | Date          | Description                            | Comment  |  |  |  |
|----------|---------------|--|--|--|--|--|
| 1.0      | February 2022 | Initial data sheet release             |  |  |  |  |
| 1.1      | March 2022    | Correction of component values         | Feedback resistor value for 5Vo corrected      Cff removed from EMI conditions |  |  |  |
| 1.2      | October 2022  | Updated design example layout pictures |  |  |  |  |



#### **CAUTIONS AND WARNINGS**

The following conditions apply to all goods within the product series of Magl<sup>3</sup>C of Würth Elektronik eiSos GmbH & Co. KG:

#### General:

- All recommendations according to the general technical specifications of the data-sheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

## **Product specific:**

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

#### Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

WPME-VDLM - Variable Step Down LGA Module



#### **IMPORTANT NOTES**

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Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not. Accordingly, the customer is cautioned to verify that the datasheet is current before placing orders.

#### Customer Responsibility Related to Specific, in Particular Safety-Relevant, Applications

It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

#### **Best Care and Attention**

Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

#### **Customer Support for Product Specifications**

Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

#### **Product R&D**

Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

#### **Product Life Cycle**

Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered. The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

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