MPQ7230



42V, 1.2A, Synchronous Buck-Boost or 3A Buck Automotive Infrared LED Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ7230 is a fixed-frequency, constant current buck-boost LED driver with integrated power MOSFETs. The device offers a very compact solution to achieve 1.2A of continuous output current, with excellent load and line regulation across a wide input supply range. The MPQ7230 can also be configured to buck mode to provide up to 3A of constant load current.

The MPQ7230 can support PWM dimming frequencies as low as 10Hz to adjust infrared radiation (IR) in LED driver applications. It is also compatible with 30FPS, 60FPS, and 120FPS dimming.

Constant frequency hysteretic control mode provides extremely fast transient response without loop compensation.

Full protection features include over-current protection (OCP), thermal derating (TD), and thermal shutdown (TSD).

The MPQ7230 requires a minimal number of readily available, standard external components. It is available in a space-saving QFN-19 (3mmx4mm) package.

FEATURES

Built for a Wide Range of IR LED Applications:

- Wide 6V to 42V Operating Input Range
- 10Hz to 2kHz PWM Dimming Frequency
- Compatible with 30FPS, 60FPS, and 120FPS Dimming

High Performance for Improved Thermals:

- Configurable LED Current without Sensing Resistor
- \circ 44mΩ/40mΩ Low R_{DS(ON)} Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation

Optimized for EMC/EMI:

- Default 410kHz f_{SW} with Spread Spectrum
- o EMI Reduction Technique

Full Protection Features:

- LED Short (to GND and Battery), LED Open, Output OVP with Fault Indication
- OCP with Latch-Off Mode
- Configurable Thermal Derating via NTC Remote Temperature Sense
- Thermal Shutdown

Additional Features:

- Configurable 1.2A Current in Buck-Boost Mode or 3A in Buck Mode
- 5% LED Current Accuracy (700mA–
 1.2A for Buck-Boost or 1A–2A for Buck)
- Available in QFN-19 (3mmx4mm) Package
- Available in Wettable Flank
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Infrared (IR) LED Drivers for Driver Monitoring Systems (DMS)
- Infrared (IR) Illumination for Automotive Cameras
- Surveillance Systems

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TYPICAL APPLICATION

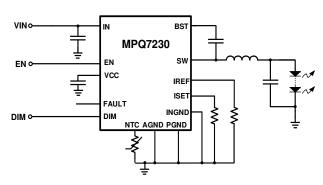
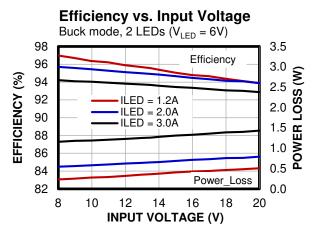


Figure 1: Buck Topology (≥14.7kΩ R_{IREF})



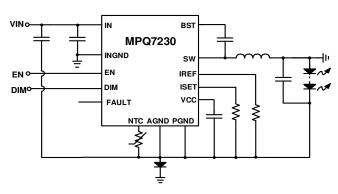
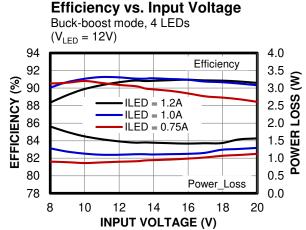


Figure 2: Buck-Boost Topology (≤9.09kΩ R_{IREF})



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7230GLE-AEC1***	QFN-19 (3mmx4mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MPQ7230GLE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

TOP MARKING

MPYW

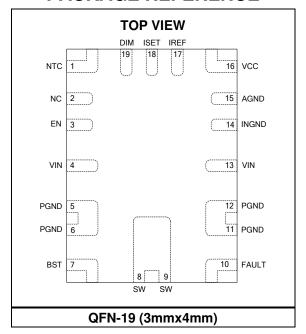
7230

LLL

Е

MP: MPS prefix Y: Year code W: Week code 7230: Part number LLL: Lot number E: Wettable lead flank

PACKAGE REFERENCE





PIN FUNCTIONS

Pin #	Name	Description
PIN#	name	·
1	NTC	Remote temperature sense. Connect NTC to a resistor, or connect a resistor network from NTC to AGND, to configure the temperature derating starting point. The device provides protections for NTC to PGND, AGND, or INGND shorts.
2	NC	Not connection. Externally connect NC to PGND on the board.
3	EN	Enable. Pull EN above 1.2V to enable the chip; pull EN below 0.6V to shut down the chip. The part starts to sense the different pin configurations at the first positive edge of EN. The EN pin can be connected to VIN through a resistor below $100k\Omega$. EN is pulled low with an internal resistor. When EN is floating, the device is off by default.
4, 13	VIN	Supply voltage. The MPQ7230 operates from a 6V to 42V input rail. An input capacitor (C_{IN}) is required to decouple the input rail. Connect VIN to the input rail using a wide PCB trace.
5, 6, 11, 12	PGND	Power ground. PGND is the reference ground of the power device (including the configuration pins), so PGND requires careful consideration during PCB layout. Generally, PGND is used to dissipate thermal heat.
7	BST	Bootstrap. Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET driver. A resistor can also be placed between SW and the capacitor to reduce the SW spike voltage and improve EMI performance.
8, 9	SW	Switch output. SW is the middle point of the high-side and low-side MOSFETs. It is recommended to keep the SW node small. Use a wide SW trace to reduce noise coupling and improve EMI.
10	FAULT	Fault indicator. FAULT is an open-drain output with an internal $300k\Omega$ pull-up resistor connected to VIN, and a $4M\Omega$ pull-down resistor connected to INGND. FAULT is pulled low if one of the following occurs: an LED short or open fault, over-temperature protection (OTP), false mode detection, and over-current protection (OCP). FAULT can be continuously connected to VIN through a pull-up resistor.
14	INGND	VIN, EN, DIM, and FAULT ground for a buck-boost topology. For a buck topology, connect INGND to PGND or AGND.
15	AGND	Analog ground. AGND is the reference ground of the logic circuit. Connect AGND to PGND with an external trace.
16	VCC	Internal bias supply. VCC supplies power to the internal control circuit and gate drivers. A $\ge 3\mu F$ decoupling capacitor should be connected from VCC to ground, and placed close to VCC. Considering the capacitance derating, a $10\mu F/10V$ or $16V$ capacitor with X7R dielectrics is strongly recommended.
17	IREF	Mode selection and NTC reference current setting. Connect a ≤9.09kΩ resistor to IREF to select buck-boost mode, or connect a ≥14.7kΩ resistor to select buck mode. The voltage on IREF is 0.57V after mode detection finishes. Connect a resistor (R _{IREF}) from IREF to GND to get a reference current (0.57V / R _{IREF}). If the IREF pin is shorted to ground or has an open fault, the device latches off and asserts FAULT. The current on the NTC pin is 50 (buck mode) or 5 (buck-boost mode) times the reference current.
18	ISET	LED current set. Connect an external resistor from ISET to ground to set the LED average current. If the ISET pin experiences a short or open fault, the part latches off and asserts FAULT.
19	DIM	Dimming control. Apply an external clock to the DIM pin for PWM dimming. Drive DIM above 1.6V to turn dimming on; drive DIM below 0.7V to turn dimming off. Ensure that the dimming on time is at least 100µs to avoid mistriggering FAULT. The dimming off time can be as long as 100ms. This means that the MPQ7230 can support a dimming frequency as low as 10Hz to handle 30Hz infrared LED driver applications.



ABSOLUTE MAXIMUM RATINGS (1) V_{IN} - $V_{\text{PGND/AGND}}$ -0.3V to +50V V_{IN} - V_{INGND} -0.3V to +50V V_{FAULT} - V_{INGND}-0.3V to +50V V_{EN}, V_{DIM} - V_{INGND}--0.3V to +5.5V V_{DIM} - V_{PGND/AGND} -0.3V to +50V V_{SW} - V_{PGND/AGND}.....-0.3V to V_{IN} - $V_{PGND/AGND}$ + 0.3V V_{BST} $V_{SW} + 5.5V$ All other pins - $V_{\text{PGND/AGND}}.....$ -0.3V to 5.5VContinuous power dissipation ($T_A = 25^{\circ}C$) (2) (6) QFN-19 (3mmx4mm)......3.9W Junction temperature 150°C Lead temperature260°C Storage temperature.....-65°C to +150°C Electrostatic Discharge (ESD) Ratings Human body model (HBM) Class 2 (3) Charged device model (CDM) Class C2b (4) **Recommended Operating Conditions** Supply voltage (V_{IN} - V_{PGND}) 6V to 42V LED current (I_{LED}) buck-boost mode.. Up to 1.2A LED current (I_{LED}) buck mode............................... Up to 3A Operating junction temp (T_J) -40°C to +150°C

Thermal Resistance	Ө ЈА	Ө JС	
QFN-19 (3mmx4mm)			
JESD51-7 (5)	48	11.	°C/W
EVQ7230-L-00A (6)	32	6	°C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Per AEC-Q100-002.
- Per AEC-Q100-011.
- 5) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
- S) Measured on MPS standard EVB of MPQ7230, 4-layer PCB,

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ELECTRICAL CHARACTERISTICS

Buck mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Supply current (shutdown)	I _{SD}	$V_{EN} = 0V$		30	80	μA
Supply current (quiescent)	ΙQ	V _{EN} = 2V, no switching, I _{IREF} float (exclude I _{IREF} and NTC current)		1.2	2	mA
		FAULT latch			2	mA
HS switch on resistance	HS _{RDS-ON}	$V_{BST-SW} = 5V$, $R_{ISET} = 13.3k\Omega$		44	85	mΩ
no switch on resistance	nords-on	$V_{BST-SW} = 5V$, $R_{ISET} = 40.2k\Omega$		85	160	mΩ
LC quitab an registance	LS _{RDS-ON}	$V_{CC} = 5.2V$, $R_{ISET} = 13.3k\Omega$		40	80	mΩ
LS switch on resistance	LORDS-ON	$V_{CC} = 5.2V$, $R_{ISET} = 40.2k\Omega$		80	150	mΩ
Switch leakage	SWLKG	V _{EN} = 0V, V _{SW} =13.5V, T _J = 25°C			1	μΑ
Switch leakage	SVVLKG	$V_{EN} = 0V, V_{SW} = 13.5V$			5	μA mA mA mΩ mΩ mΩ mΩ
Peak current limit (7)	1	$R_{ISET} = 40.2k\Omega$	2.65	3.15	3.65	Α
reak current iimit (7)	ILIMIT_PEAK	$R_{ISET} = 13.3k\Omega$	5.3	6.3	7.3	Α
ZCD (7)				50		mA
Oscillator frequency	fsw	FSS activated	330	410	490	kHz
Minimum on time (7)	ton_min			55	80	ns
Minimum off time (7)	toff_min			75	100	ns
Maximum duty cycle (7)	D _{MAX}	Low dropout	95	98		%
Spread spectrum frequency (7)				15		kHz
Spread spectrum frequency range (7)				±10%		f _{SW}
LED current	I _{LED}	$R_{ISET} = 13.3k\Omega$, $T_J = 25$ °C to 100 °C	1.14	1.2	1.26	^
LED current	ILED	$R_{ISET} = 13.3k\Omega$	1.02	1.2	1.38	_ ^
LED current threshold for MOSFET (half off)	ILED_CUT			600	700	mA
ISET voltage	VISET	I _{ISET} = 45µA	0.573	0.592	0.606	V
ISET current threshold for		ILED < ILED_CUT	80	120	160	μA
short fault		ILED > ILED_CUT	180	220	260	μΑ
ISET current threshold for open fault			0.5	1.4	5	μA
EN rising threshold	V _{EN_RISING}	VEN - VINGND		1	1.6	V
EN falling threshold	V _{EN_FALLING}	VEN - VINGND	0.6	0.9		V
EN threshold hysteresis	V _{EN_HYS}	V _{EN} - V _{INGND}		100		mV
EN inner to a constant		V _{EN} - V _{INGND} = 2V		2	8	μA
EN input current	I _{EN}	V _{EN} - V _{INGND} = 0V		0	0.2	μA



Buck mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
DIM rising threshold	V _{DIM_RISING}	V _{DIM} - V _{INGND}		1	1.6	V
DIM falling threshold	V _{DIM_} FALLING	V _{DIM} - V _{INGND}	0.7	0.9		V
DIM threshold hysteresis	V _{DIM_HYS}	V _{DIM} - V _{INGND}		100		mV
DIM input current	I _{DIM}	V _{DIM} - V _{INGND} = 2V		2		μA
Diw input current	IDIM	V _{DIM} - V _{INGND} = 0V		0	0.2	μΑ
Maximum DIM off time	tdim_off		100			ms
V _{IN} under-voltage lockout rising threshold	INUV _{VTH_R}	VIN - VINGND	5.75	6	6.25	V
V _{IN} under-voltage lockout falling threshold	INUV _{VTH_F}	V _{IN} - V _{INGND}	4.4	4.9	5.2	V
V _{IN} under-voltage lockout threshold hysteresis	INUV _{HYS}	VIN - VINGND		1.1		V
V _{CC} under-voltage lockout rising threshold	V cc_vтн	Vcc - Vagnd	4.4	4.7	5	V
V _{CC} under-voltage lockout falling threshold		Vcc - Vagnd	3.4	4.05	4.7	V
V _{CC} under-voltage lockout threshold hysteresis	V _{CC_HYS}	Vcc - Vagnd		650		mV
VCC regulator	Vcc	Icc = 0mA	4.9	5.1	5.3	V
VCC load regulation		Icc = 20mA	4.7			V
VCC maximum current ability		Vcc = Vcc uvlo + 100mV, no switching	50	80	120	mA
VCC source current ability (7)		Vcc = Vcc uvlo + 100mV, switching		25		mA
Output under-voltage threshold	UV _{VTH}		0.6	1.1	1.7	V
LED low current threshold			45	60	75	mA
LED low current threshold			100	120	150	mA
FAULT assertion delay time when startup	tft-d-start		20	35	45	ms
FAULT assertion deglitch time after start-up (7)	t _{FT-D}			20		μs
FAULT assertion low sink current ability	IFAULT_SINK	VFAULT = 12V VFAULT = 0.2V	10 5	30 12	50	mA mA
FAULT pull-up resistor		VPAULT - 0.2 V	100	300	500	kΩ
FAULT pull-down resistor				4000	6000	kΩ
<u>'</u>			2000	4000	0000	K12
IREF current for mode detection			200	240	280	μA
VIREF threshold for mode detection			2.6	2.7	2.8	V



Buck mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
IREF voltage	VIREF	Irref = 20µA	0.51	0.57	0.63	V
IREF current threshold for pin short detection			60	85	120	μΑ
IREF current threshold for pin open detection				3	6	μA
NTC source current	Into	$V_{NTC} = 1.25V$, $I_{REF} = 20\mu A$	950	1020	1090	μΑ
		ILED = 98% of nominal	-2.5%	1.25	+2.5%	V
NTC voltage for current derating		I _{LED} = 74% of nominal	-2.5%	0.89	+2.5%	V
		ILED = 50% of nominal	-2.5%	0.53	+2.5%	V
VNTC threshold for OTP				0.37		V
VNTC deglitch time for OTP		V _{NTC} = 0.3V	180	256	320	μs
V _{NTC} recovery threshold for OTP				0.48		V
Thermal shutdown (7)			155	170	185	ô

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Buck-boost mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Supply current (shutdown)	I _{SD}	V _{EN} = 0V		30	80	μA
Supply current (quiescent)	ΙQ	V _{EN} = 2V, no switching, l _{IREF} float (exclude l _{IREF} and NTC current)		1.2	2	mA
,		FAULT latch			2	mA
HS switch on resistance	HS _{RDS-ON}	$V_{BST-SW} = 5V, R_{ISET} = 13.3k\Omega$		44	85	mΩ
LS switch on resistance	LS _{RDS-ON}	$V_{CC} = 5.2V$, $R_{ISET} = 13.3k\Omega$		40	80	mΩ
Switch leakage	SWLKG	V _{EN} = 0V, V _{SW} = 13.5V, T _J = 25°C			1	μA
- 1		V _{EN} = 0V, V _{SW} = 13.5V			5	μA
Peak current limit (7)	ILIMIT_PEAK		5.3	6.3	7.3	A
ZCD ⁽⁷⁾				50		mA
Oscillator frequency	f _{SW}	FSS activated	330	410	490	kHz
Minimum on time (7)	t _{ON_MIN}			55	80	ns
Minimum off time (7)	t _{OFF_MIN}			75	100	ns
Maximum duty cycle (7)	D _{MAX}	Low dropout	95	98		%
Spread spectrum frequency (7)				15		kHz
Spread spectrum frequency range (7)				±10%		fsw
		$R_{ISET} = 21.5k\Omega$, $T_J = 25$ °C to 100 °C	0.7125	0.75	0.7875	Α
LED current	I _{LED}	$R_{ISET} = 21.5k\Omega$	0.6375	0.75	0.8625	_ ^
LED current		$R_{ISET} = 13.3k\Omega$, $T_J = 25$ °C to 100 °C	1.14	1.2	1.26	A
		$R_{ISET} = 13.3k\Omega$	1.02	1.2	1.38	
ISET voltage	VISET	I _{ISET} = 45µA	0.573	0.592	0.606	V
Demon denstina natio		V _{IN} = 6.6V, V _{ISET} respect to nominal		95		%
Power derating ratio		V _{IN} = 5.3V, V _{ISET} respect to nominal		75		%
ISET current threshold for pin short			80	120	160	μΑ
ISET current threshold for pin open			0.5	1.4	5	μΑ
EN rising threshold	V _{EN_RISING}	Ven - Vingnd		1	1.6	٧
EN falling threshold	VEN_FALLING	V _{EN} - V _{INGND}	0.6	0.9		٧
EN threshold hysteresis	V _{EN_HYS}	V _{EN} - V _{INGND}		100		mV
ENI:	,	V _{EN} = 2V		2	8	μA
EN input current	I _{EN}	$V_{EN} = 0V$		0	0.2	μA
		•			•	



Buck-boost mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
DIM rising threshold	V _{DIM_RISING}	VDIM - VINGND		1	1.6	V
DIM falling threshold	VDIM_FALLING	V _{DIM} - V _{INGND}	0.7	0.9		V
DIM threshold hysteresis	V _{DIM_HYS}	V _{DIM} - V _{INGND}		100		mV
DIM input accordant	1	V _{DIM} - V _{INGND} = 2V		2		μΑ
DIM input current	I _{DIM}	V _{DIM} - V _{INGND} = 0V		0	0.2	μΑ
Maximum DIM off time	t _{DIM_OFF}		100			ms
V _{IN} under-voltage lockout rising threshold	INUV _{VTH_R}	Vin - Vingnd	5.75	6	6.25	V
V _{IN} under-voltage lockout falling threshold	INUV _{VTH_F}	VIN - VINGND	4.4	4.9	5.2	V
V _{IN} under-voltage lockout threshold hysteresis	INUV _{HYS}	Vin - Vingnd		1.1		V
Vcc under-voltage lockout rising threshold	V _{CC_} VTH	Vcc - Vagnd	4.4	4.7	5	٧
Vcc under-voltage lockout falling threshold		Vcc - Vagnd	3.4	4.05	4.7	V
V _{CC} under-voltage lockout threshold hysteresis	V _{CC_HYS}	Vcc - Vagnd		650		mV
VCC regulator	Vcc	Icc = 0mA	4.9	5.1	5.3	V
VCC load regulation		I _{CC} = 20mA	4.7			V
VCC max current ability		Vcc = Vcc_uvlo + 100mV, no switching	50	80	120	mA
VCC source current ability		$V_{CC} = V_{CC_UVLO} + 100 \text{mV}$, switching		25		mA
Output over voltage threshold	OV_{VTH}	Vingnd - Vagnd	17	18	19	٧
Output Under voltage threshold	UV _{VTH}	Vingnd - Vagnd	1	1.35	1.7	V
VIN load dump protection threshold			38	40	42	٧
VIN load dump protection falling threshold			37	39	41	V
VIN load dump protection hysteresis				1		V
Output discharge current		V _{INGND} - V _{PGND} > 5V	40	100	180	mA
for load dump protection		VINGND - VPGND = 1V	20	45	90	mA



Buck-boost mode, V_{IN} = 13.5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
FAULT assertion delay time when startup	tft-d-start		20	35	45	ms
FAULT assertion deglitch time after startup	t _{FT-D}			20		μs
FAULT assertion low sink	Jewy z owy	VFAULT = 12V	10	30	50	mA
current ability	IFAULT_SINK	VFAULT = 0.2V	5	12		mA
FAULT pull-up resistor			100	300	500	kΩ
FAULT pull-down resistor			2000	4000	6000	kΩ
IREF current for mode detection			200	240	280	μΑ
VIREF threshold for mode detection			2.6	2.7	2.8	٧
IREF voltage	V _{IREF}	$I_{REF} = 20\mu A$	0.51	0.57	0.63	V
IREF current threshold for pin short detection			650	800	950	μA
IREF current threshold for pin open detection				40	55	μA
NTC source current	Intc	V _{NTC} = 1.25V, I _{IREF} = 200µA	950	1020	1090	μΑ
NITO III (ILED = 98% of nominal	-2.5%	1.25	+2.5%	V
NTC voltage for current derating		I _{LED} = 74% of nominal	-2.5%	0.89	+2.5%	V
derating		I _{LED} = 50% of nominal	-2.5%	0.53	+2.5%	V
VNTC threshold for OTP				0.37		V
VNTC deglitch time for OTP		V _{NTC} = 0.3V	180	256	320	μs
V _{NTC} recovery threshold for OTP				0.48		V
Thermal shutdown (7)			155	170	185	°C

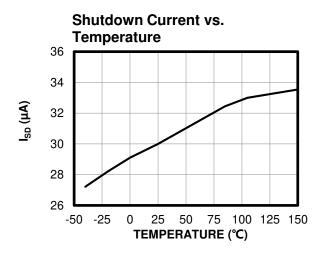
Note:

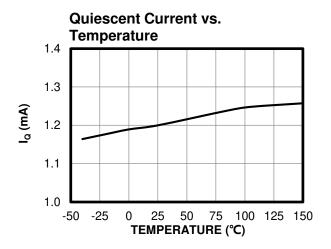
⁷⁾ Not tested in production and guaranteed by design and characterization.

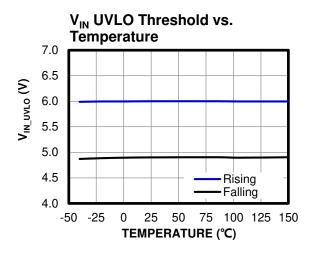


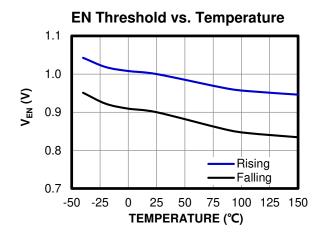
TYPICAL CHARACTERISTICS

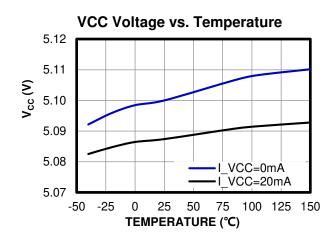
 $V_{IN} = 12V$, $T_J = -40$ °C to +150°C, unless otherwise noted.

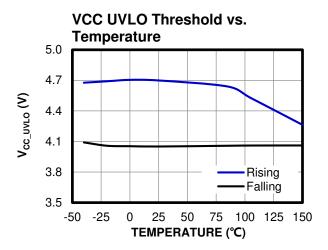








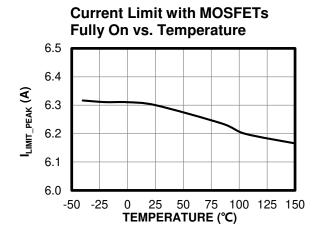


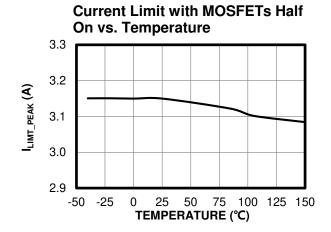


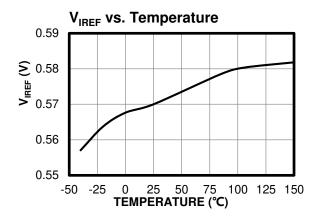
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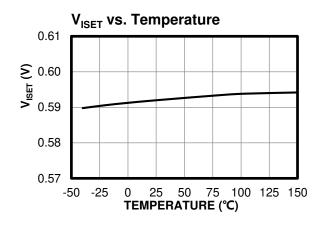


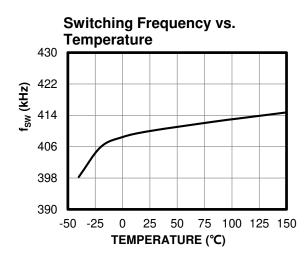
 $V_{IN} = 12V$, $T_J = -40$ °C to +150°C, unless otherwise noted.

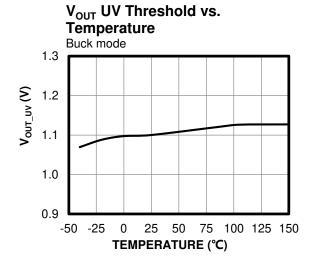






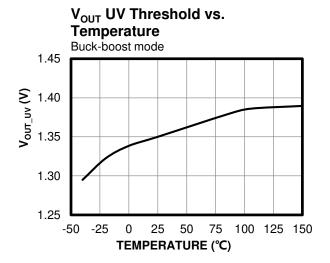


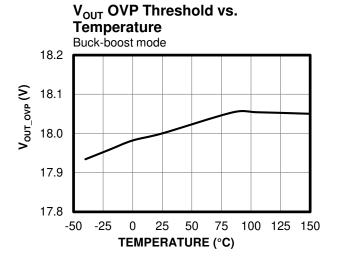






 $V_{IN} = 12V$, $T_J = -40$ °C to +150°C, unless otherwise noted.

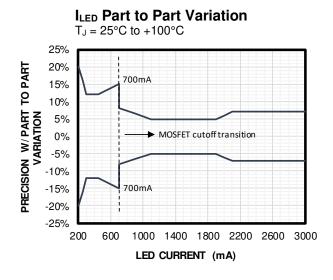


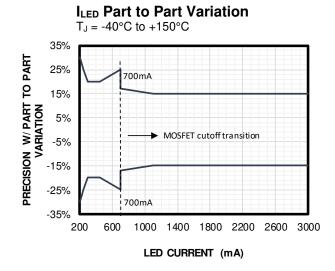


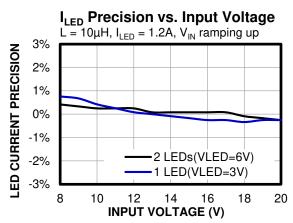
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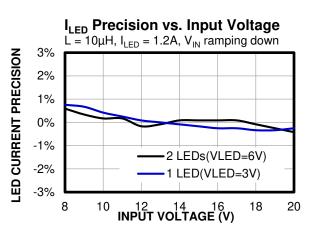


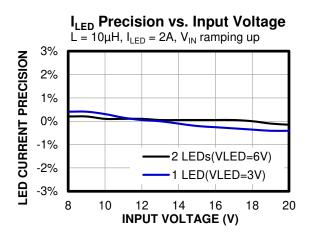
TYPICAL PERFORMANCE CHARACTERISTICS

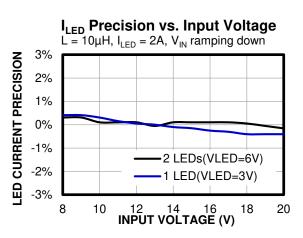




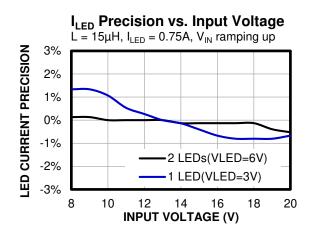


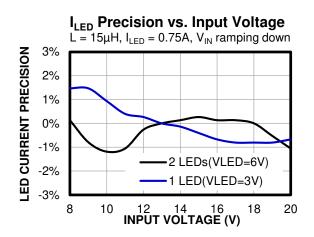


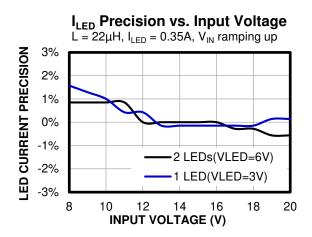


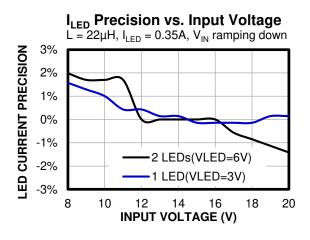


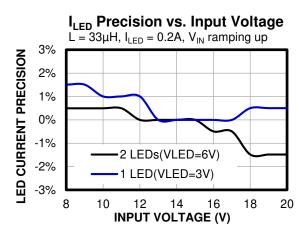


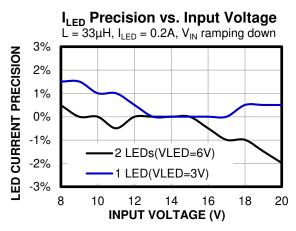














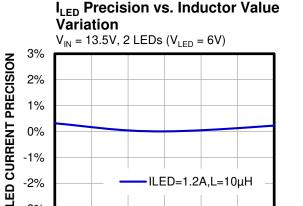
-3%

0.7

8.0

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Buck mode, 2 LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 410kHz, L = 10 μ H, T_A = 25°C, unless otherwise noted.



RATIO TO NORMALIZED INDUCTOR

1.0

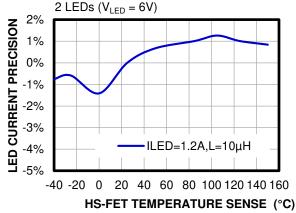
1.1

1.2

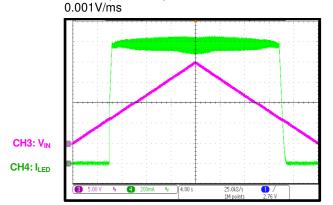
1.3

I_{LED} Precision vs. HS-FET **Temperature Sense**

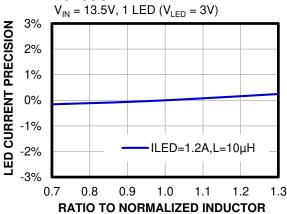
0.9



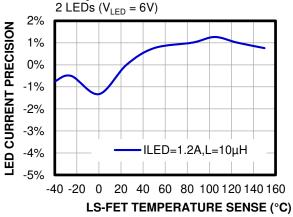
VIN Slowly Ramps Up and Down 2 LEDs (V_{LED} = 6V), I_{LED} = 1.2A, V_{IN} = 0V to 20V,



I_{LED} Precision vs. Inductor Value Variation

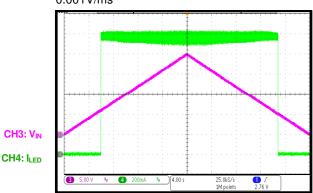


I_{LED} Precision vs. LS-FET **Temperature Sense**



V_{IN} Slowly Ramps Up and Down

1 LED (VLED = 3V), ILED = 1.2A, VIN = 0V to 20V, 0.001V/ms



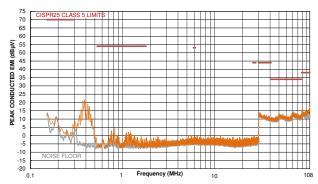
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Buck mode, 2 LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 410kHz, L = 10 μ H, PWM dimming: 30Hz/5ms, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

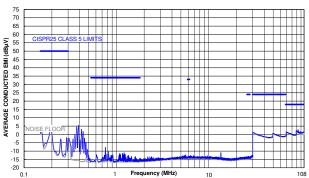
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



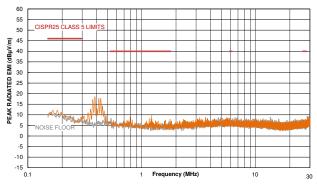
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



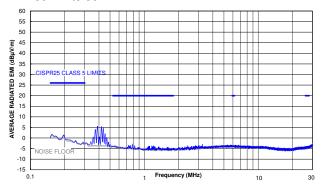
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



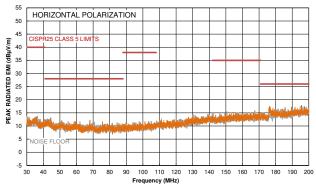
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



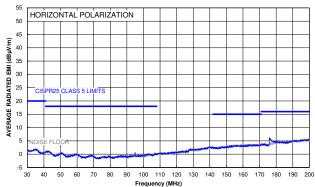
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

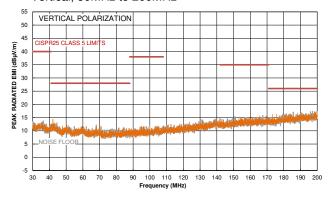




Buck mode, 2 LEDs in series (VLED = 6V), V_{IN} = 13.5V, f_{SW} = 410kHz, L = 10 μ H, PWM dimming: 30Hz/5ms, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

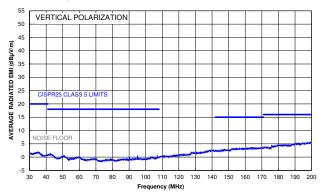
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



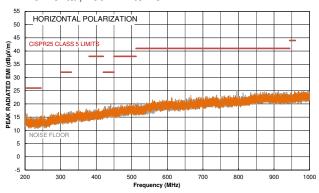
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



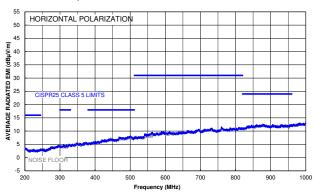
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



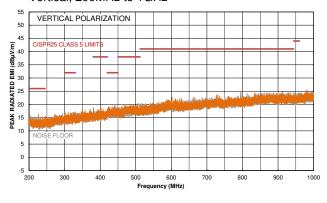
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



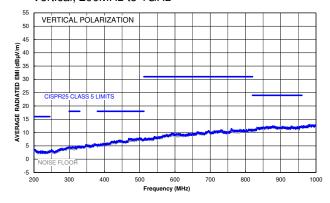
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

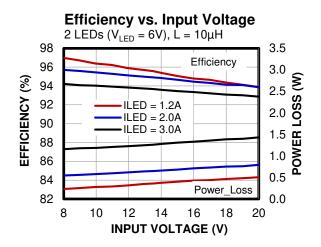
Vertical, 200MHz to 1GHz

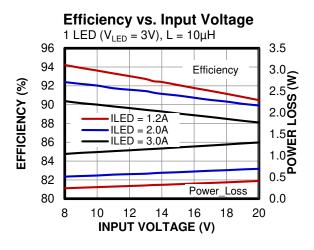


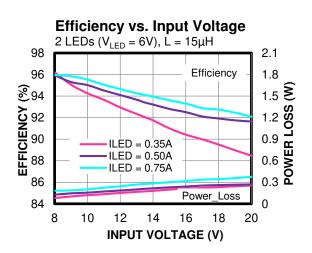
Note:

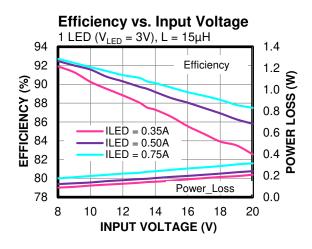
8) The MPQ7230 buck mode EMC test results are based on the application circuit with EMI filters in Figure 9 on page 50.

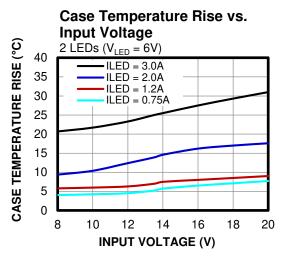


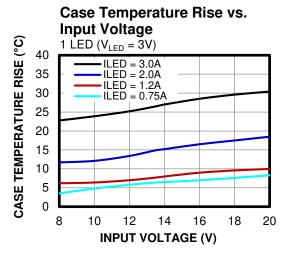




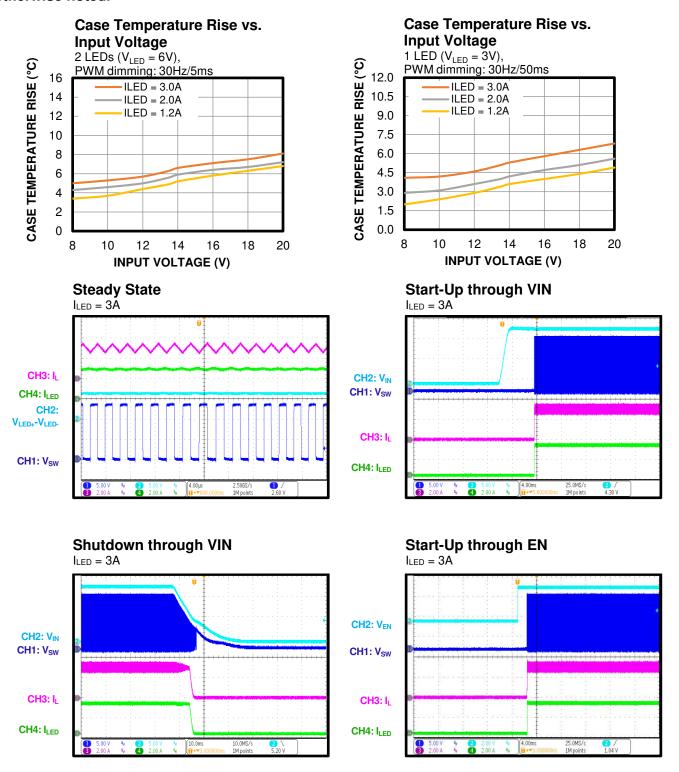




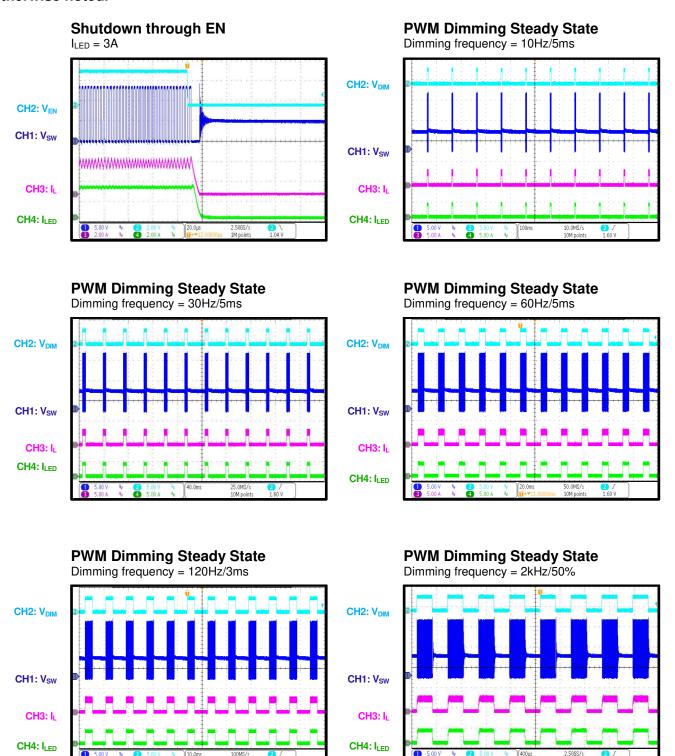




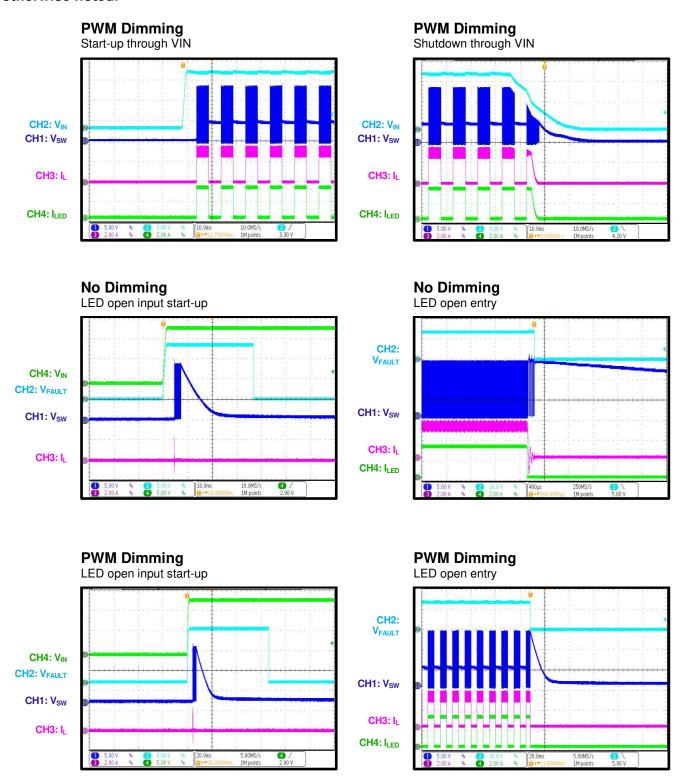




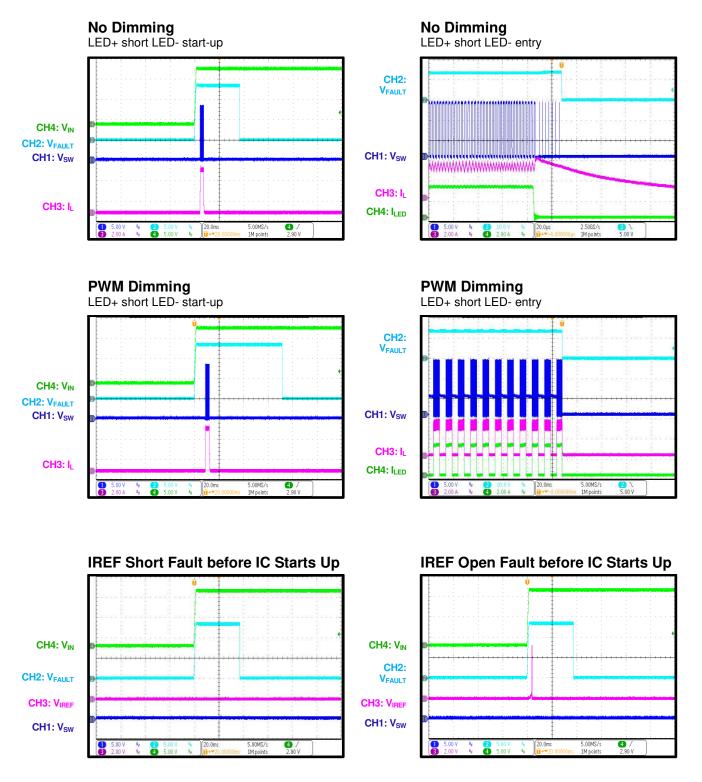




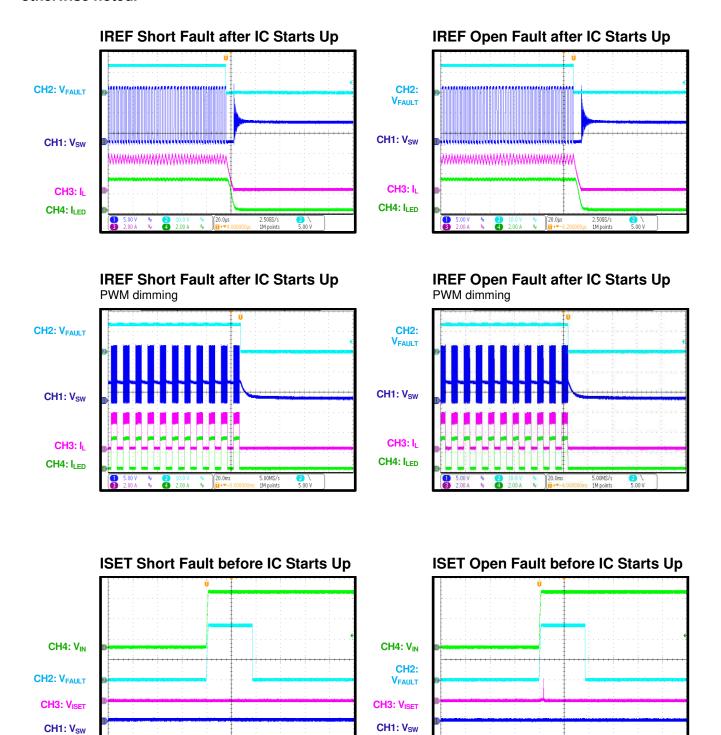












CH2:

V_{FAULT}

CH1: V_{SW}

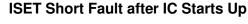
CH3: IL

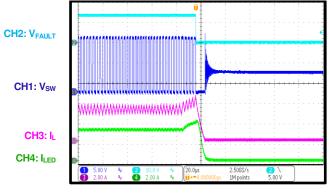
CH4: I_{LED}



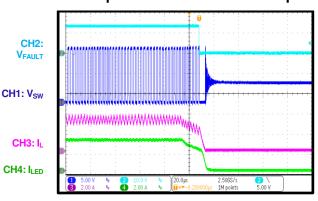
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Buck mode, 2 LEDs in series (V_{LED} = 6V), V_{IN} = 13.5V, f_{SW} = 410kHz, L = 10 μ H, T_A = 25°C, unless otherwise noted.

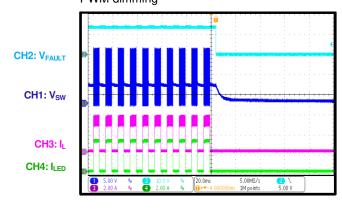




ISET Open Fault after IC Starts Up



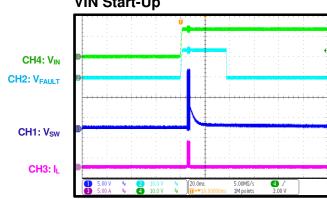
ISET Short Fault after IC Starts Up PWM dimming



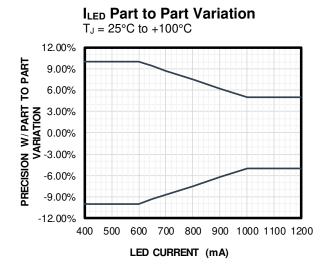
ISET Open Fault after IC Starts Up PWM dimming

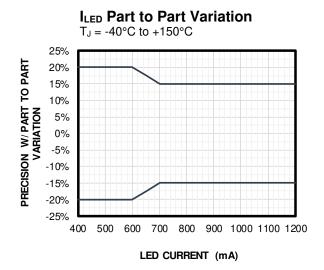


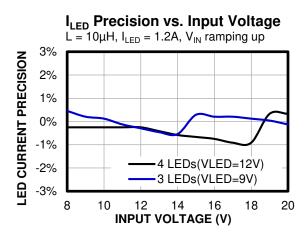
Incorrect Mode Detection during VIN Start-Up

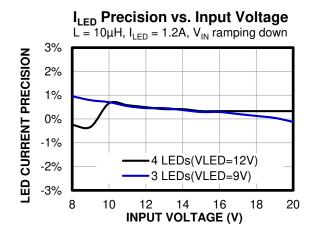


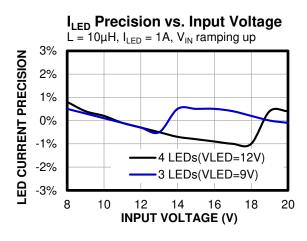


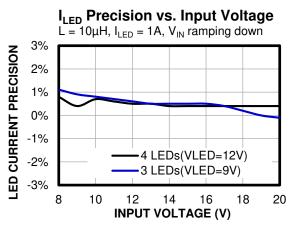




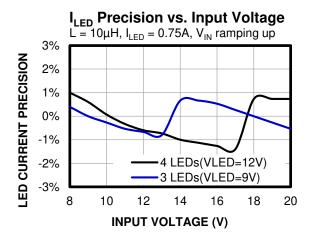


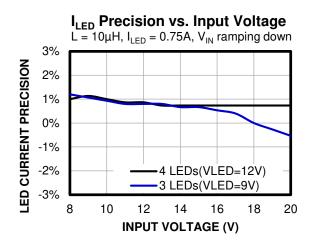


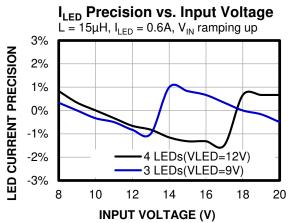


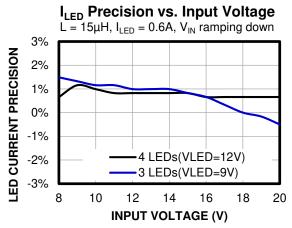


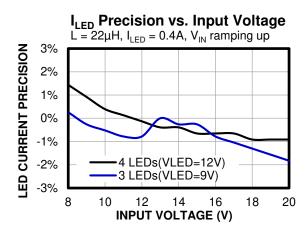


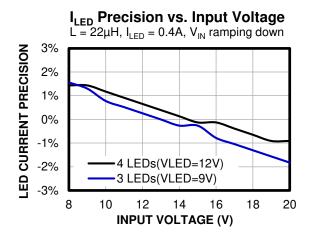






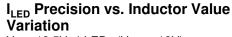


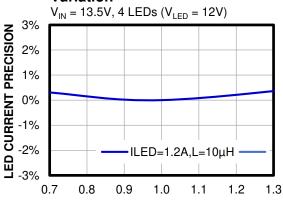






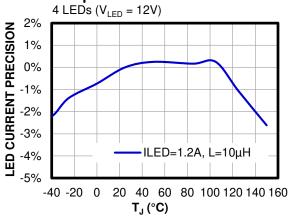
Buck-boost mode, 4 LEDs in series ($V_{LED} = 12V$), $V_{IN} = 13.5V$, $I_{LED} = 1.2A$, $f_{SW} = 410kHz$, $L = 10\mu H$, $T_A = 25$ °C, unless otherwise noted.





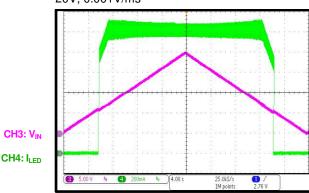
RATIO TO NORMALIZED INDUCTOR

I_{LED} Precision vs. Junction **Temperature**

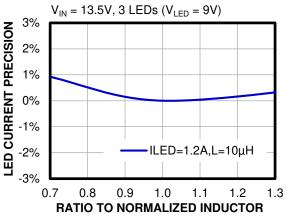


V_{IN} Slowly Ramps Up and Down

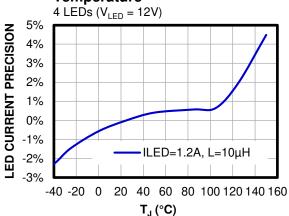
4 LEDs (VLED = 12V), ILED = 1.2A, VIN = 0V to 20V, 0.001V/ms



I_{LED} Precision vs. Inductor Value Variation

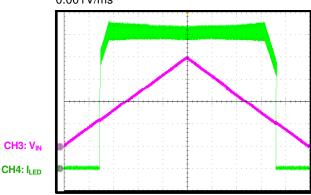


I_{LED} Precision vs. Junction **Temperature**



VIN Slowly Ramps Up and Down

 $3 \text{ LEDs } (V_{LED} = 9V), I_{LED} = 1.2A, V_{IN} = 0V \text{ to } 20V,$ 0.001V/ms

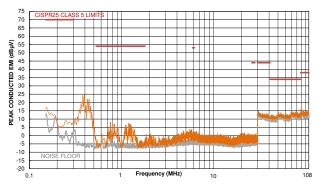




Buck-boost mode, 4 LEDs in series ($V_{LED} = 12V$), $V_{IN} = 13.5V$, $I_{LED} = 1.2A$, $f_{SW} = 410kHz$, $L = 10\mu H$, PWM dimming: 30Hz/5ms, with EMI filters, $T_A = 25^{\circ}C$, unless otherwise noted. (9)

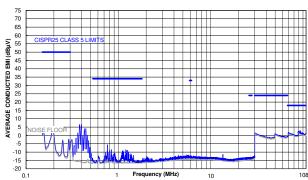
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



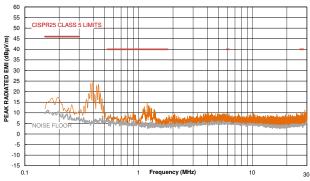
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



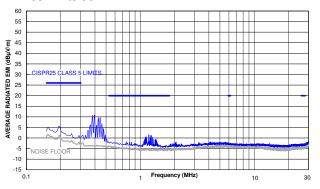
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



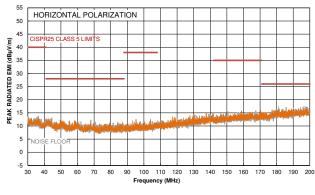
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



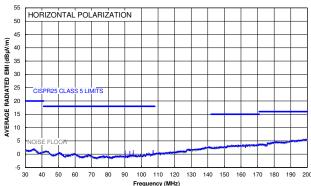
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

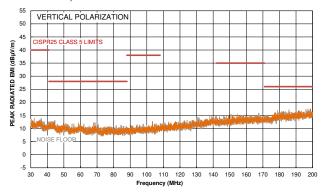




Buck-boost mode, 4 LEDs in series ($V_{LED} = 12V$), $V_{IN} = 13.5V$, $I_{LED} = 1.2A$, $f_{SW} = 410kHz$, $L = 10\mu H$, PWM dimming: 30Hz/5ms, with EMI filters, $T_A = 25^{\circ}C$, unless otherwise noted. (9)

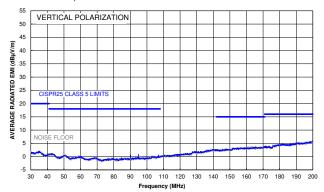
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



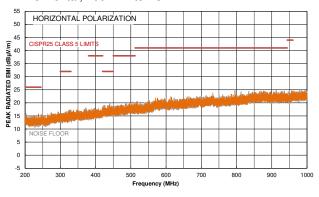
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



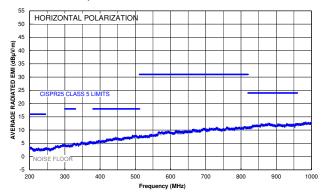
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



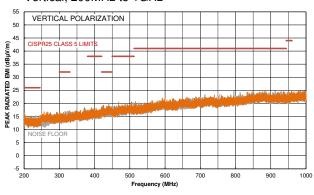
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



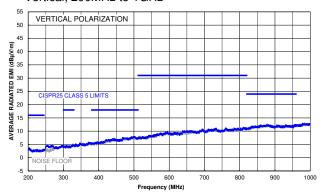
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

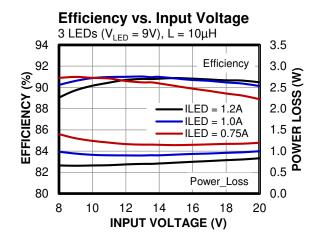
Vertical, 200MHz to 1GHz

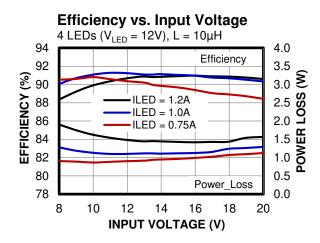


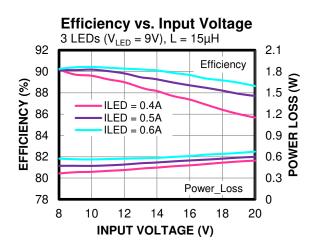
Note:

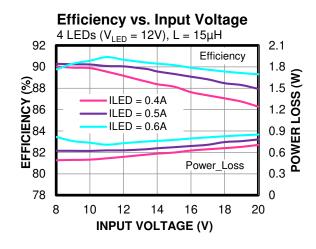
9) The MPQ7230 buck-boost mode EMC test results are based on the application circuit with EMI filters in Figure 10 on page 50.

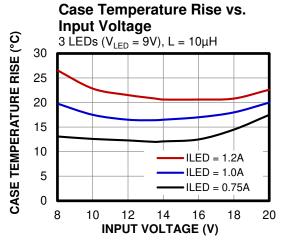


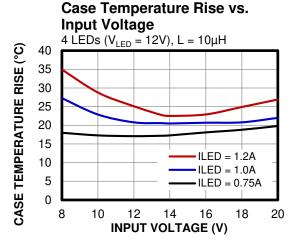




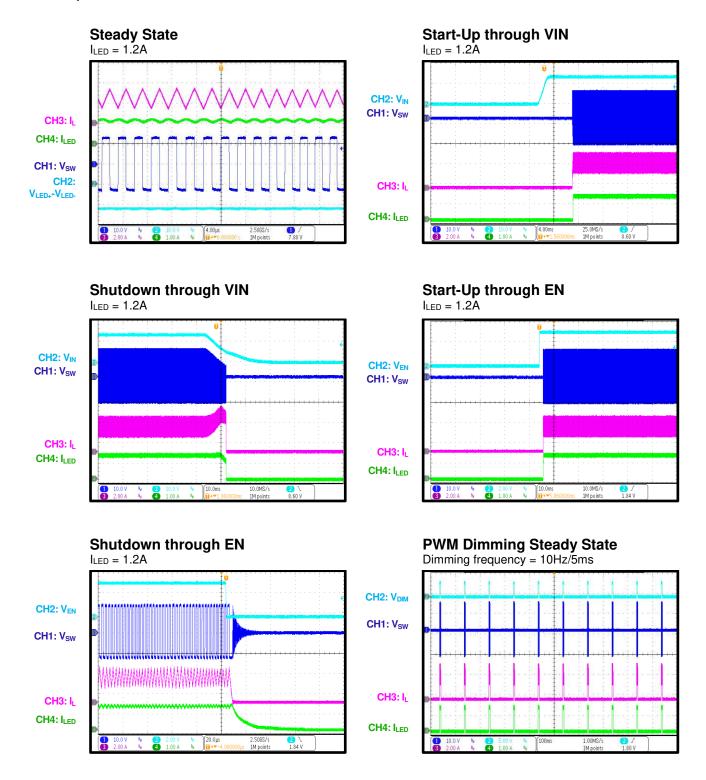




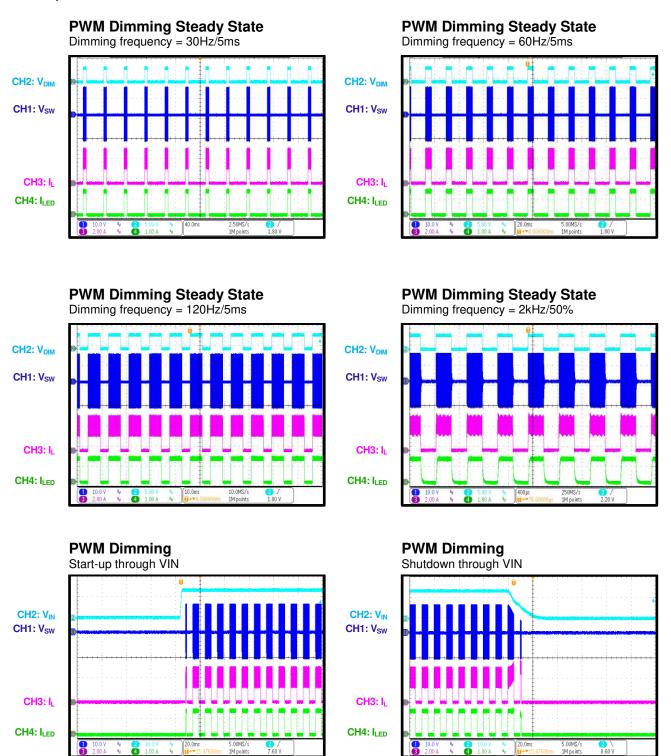




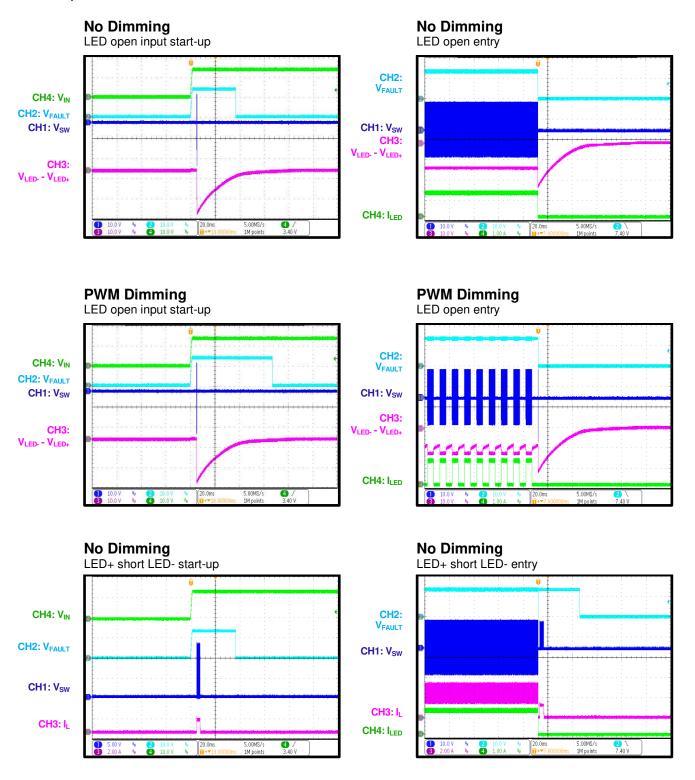




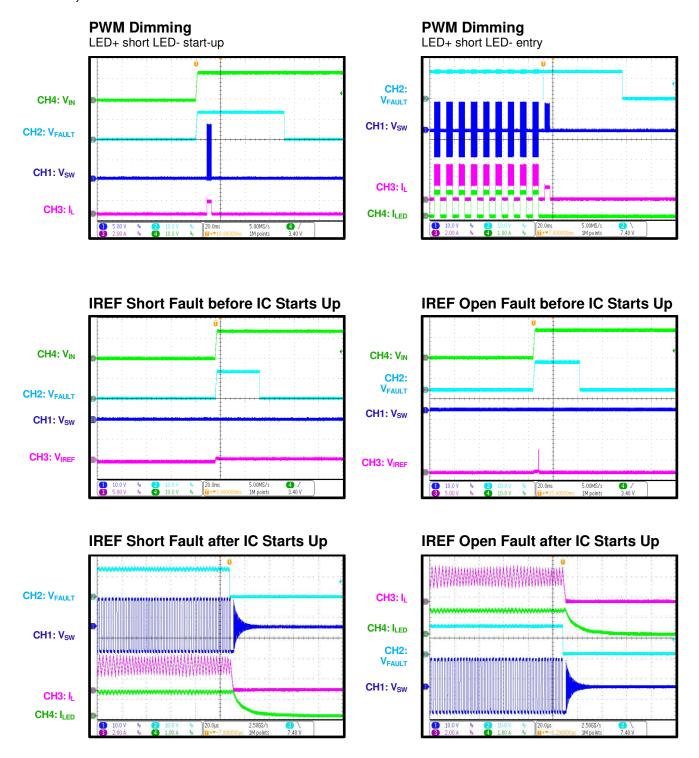








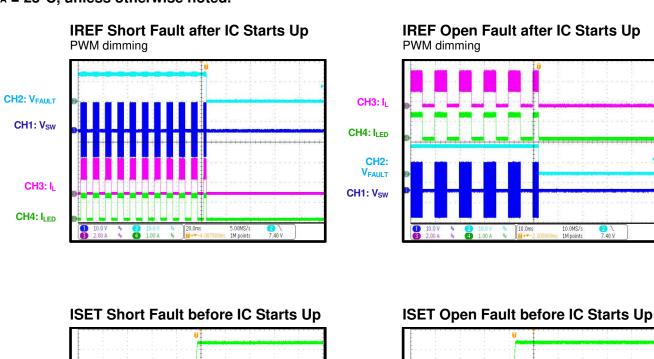


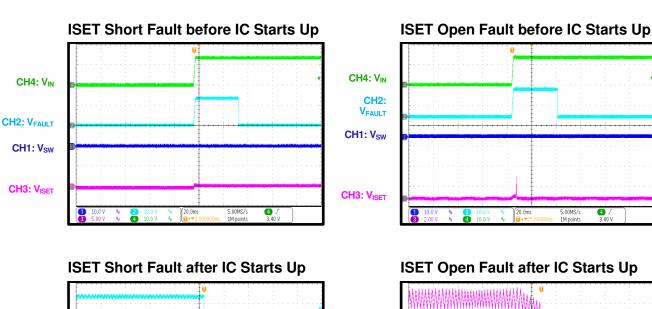


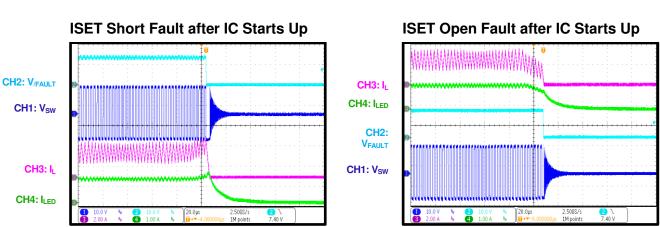


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Buck-boost mode, 4 LEDs in series (V_{LED} = 12V), V_{IN} = 13.5V, I_{LED} = 1.2A, f_{SW} = 410kHz, L = 10 μ H, T_A = 25°C, unless otherwise noted.







CH3: IL

CH2: **V**FAULT

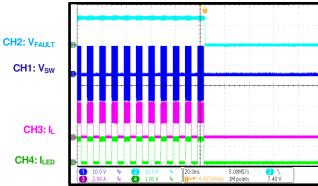
CH1: V_{SW}



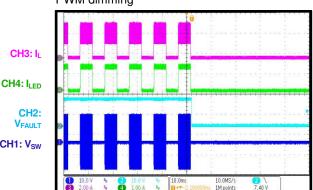
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Buck-boost mode, 4 LEDs in series ($V_{LED} = 12V$), $V_{IN} = 13.5V$, $I_{LED} = 1.2A$, $f_{SW} = 410kHz$, $L = 10\mu H$, $T_A = 25$ °C, unless otherwise noted.

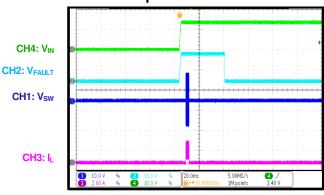
ISET Short Fault after IC Starts Up PWM dimming



ISET Open Fault after IC Starts Up PWM dimming



Incorrect Mode Detection during VIN Start-Up





FUNCTIONAL BLOCK DIAGRAM

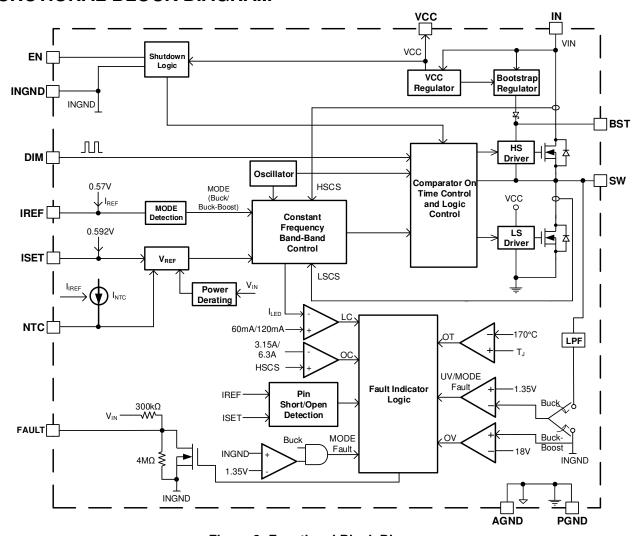


Figure 3: Functional Block Diagram



OPERATION

The MPQ7230 is a fixed-frequency, synchronous, rectified, buck or buck-boost, switch-mode LED driver with built-in power MOSFETs. The device offers a very compact solution to achieve 1.2A of continuous output current in a buck-boost topology and 3A in a buck topology. It also provides excellent load and line regulation across the 6V to 42V input supply range.

Fixed Frequency Band-Band Control

The MPQ7230 use fixed frequency band-band control with a spread spectrum technique to reduce EMC noise. When compared to fixed-frequency PWM control, band-band control offers the advantages of simpler control loop and faster transient response. Even without an output capacitor, the loop is stable. Band-band control compares the inductor current to two internal thresholds: IBANDPEAK and IBANDVALLEY.

When the inductor current exceeds $I_{BANDPEAK}$, the high-side MOSFET (HS-FET) turns off. When the inductor current drops below $I_{BANDVALLEY}$, the HS-FET turns on. ($I_{BANDPEAK}$ + $I_{BANDVALLEY}$) / 2 is controlled by a PID loop to regulate the LED current (I_{LED}). $I_{BANDPEAK}$ - $I_{BANDVALLEY}$ is controlled by a PLL loop to regulate the switching frequency to be about 410kHz. If the minimum on time (I_{CON_MIN}) or minimum off time (I_{CON_MIN}) is triggered, the switching frequency drops, and the switching frequency can be calculated with (D / I_{CON_MIN}) or [(1 - D) / I_{CON_MIN}], where D is the required duty cycle. and I_{CON_MIN} and I_{CON_MIN} are both 80ns maximum.

The additional spread spectrum uses a 15kHz modulation frequency with a triangular profile to spread the internal oscillator frequency across a ±10% nominal switching frequency window.

Middle Point Inductor Current Sense

The MPQ7230 senses I_{LED} by sensing the middle point of the inductor current (I_{LMID}). I_{LMID} is sensed through the HS-FET or low-side MOSFET (LS-FET) depending on the duty cycle. I_{LMID} is sensed through the HS-FET when the duty exceeds D_{TH_H} (55% in buck mode or 60% in buck-boost mode), or it is sensed through LS-FET when the duty cycle is below D_{TH_L} (45% in buck mode or 40% in buck-boost mode). A duty cycle hysteresis (D_{TH_HYS} , 10% in buck or 20% in buck-

boost) prevents the current sense from switching between HS-FET and LS-FET at critical duty cycles (see Figure 4).

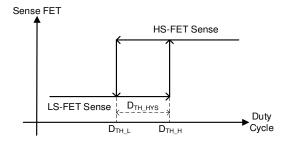


Figure 4: Current-Sense MOSFET vs. Duty Cycle

 I_{LED} is equal to I_{LMID} in buck topologies. The LED current is equal to I_{LMID} x V_{IN} / $(V_{IN}$ + $V_{OUT})$ in buck-boost topologies.

Selecting Buck Mode or Buck-Boost Mode

The MPQ7230 can be configured to a buck or buck-boost topology by connecting a different resistor (R_{IREF}) at the IREF pin. I_{LMID} is sensed through the sensing FET. I_{LED} is equal to I_{LMID} in buck topologies, while it is equal to I_{LMID} x V_{IN} / (V_{IN} + V_{OUT}) in buck-boost topologies.

Mode detection starts when V_{CC} reaches its under-voltage lockout (UVLO) threshold (about 4.7V). A 240μA current source (I_{IREF_DET}) flows from the IREF pin to detect the resistor's voltage value during start-up. If the voltage generated by I_{IREF_DET} x R_{IREF} < 2.6V, buck-boost mode is selected. Buck mode is selected when I_{IREF_DET} x R_{IREF} > 2.8V. This means that the corresponding R_{IREF} for buck-boost mode is ≤9.09kΩ, or ≥14.7kΩ for buck mode. To avoid an IREF short fault in buck-boost mode, set the resistor between 1.05kΩ and 9.09kΩ. To avoid an IREF open fault in buck mode, set the resistor between 14.7kΩ and 80.6kΩ.

Once detection finishes, the mode is latched, and I_{IREF} (0.57V / R_{IREF}) becomes the reference for the NTC pin current. The latched mode signal is reset by V_{CC} UVLO, but it cannot be reset by pulling EN low. An internal 1MHz filter works with the 250 μ s deglitch time to protect the part from false mode detection, which can be caused by noise coupling at the pin. To ensure that the detected mode is consistent with the real topology connection, the V_{INGND} - V_{PGND} voltage



is monitored. If the mode is detected as buck mode while V_{INGND} - V_{PGND} exceeds 1.35V, the part latches off and FAULT asserts low. If the mode is detected as buck-boost mode while V_{INGND} - V_{PGND} is below 1.35V (detected as an output under-voltage (UV) condition), the part latches off and FAULT asserts low.

Internal Regulator

The 5.1V internal regulator (VCC) powers most of the internal circuitries. VCC rises after V_{IN} reaches its rising UVLO threshold, regardless of whether EN is high or low. VCC is a reference to PGND/AGND, but not INGND. This means that INGND is not the reference ground for VCC in buck-boost mode.

A lower-value VCC capacitor can cause VCC voltage ringing and lead to unstable switching. It is recommended to place a ≥3µF decoupling ceramic capacitor at the VCC pin. When capacitor, consider choosing the capacitance derating to ensure that the capacitance exceeds or is equal to 3µF. A 10µF capacitor with X7R dielectrics and a ≥10V DC voltage rating is recommended. V_{CC} has its own UVLO threshold, with a 4.7V rising threshold and a 4.05V falling threshold. Besides powering internal circuitries. VCC can also power external circuitries in the system with a current capability of 25mA.

Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM)

The MPQ7230 uses continuous conduction mode (CCM) to ensure that the part works with a fixed frequency from the minimum load to full-load range. The advantages of CCM are its controllable frequency and lower output ripple under light loads. When IBANDVALLEY = 0A, the MPQ7230 enters discontinuous conduction mode (DCM). In DCM, the LS-FET acts as an ideal diode. Ensure that the part does not enter DCM mode, even during start-up or power derating, by selecting an appropriate inductor. Otherwise, LED current precision cannot be guaranteed.

Enable Control (EN)

EN is a control pin that turns the LED driver on and off. Drive V_{EN} - V_{INGND} above 1.6V to turn on the regulator; drive it below 0.6V to turn the part off and reset FAULT.

Connect EN to VIN through a resistor in both buck and buck-boost mode. If the enable function is not required in buck mode, connect EN to VCC. EN can be floated to shut down the chip due to the internal $1M\Omega$ resistor connected from EN to INGND. An integrated Zener diode is placed in parallel with the EN pin to clamp its voltage to about 7V. This internal Zener diode can handle a 1mA current for load dump voltages up to 100V when a $100k\Omega$ resistor is connected between the car battery (VBAT) and EN.

ISET

The LED average current can be configured by a resistor (R_{ISET}) connected at the ISET pin. The LED current (I_{LED}) can be calculated with Equation (1):

$$I_{LED}(A) = 16 / R_{ISET}(k\Omega)$$
 (1)

The nominal voltage ($V_{\rm ISET}$) of the ISET pin is about 0.592V. $V_{\rm ISET}$ can be adjusted below 0.592V to decrease the LED current in power derating or thermal derating.

During the mode detection period at start-up in buck mode, the ISET current is monitored to detect if I_{LED} is above or below 600mA. If I_{ISET} > 22.2µA during this period, ILED is detected to be >600mA, and the MOSFETs fully turn on. If I_{LED} is detected to be <600mA, half of the LS-FETs and HS-FETs turn off to improve currentsense accuracy. When the MOSFETs cut off by half, the current limit drops from 6.3A to 3.15A. The signal that indicates if ILED is above or below 600mA is latched once the detection finishes. This signal can only be reset by V_{CC} UVLO. After LED current detection, the MOSFET's R_{DS(ON)} does not change, even if ILED rises above or falls below 600mA. The MOSFET is fully on in buckboost mode, and the current limit stays at 6.3A.

During normal operation, the ISET pin is continuously monitored to detect open or short to GND conditions. If the ISET rises above this threshold, the device detects a short to ground condition.

If I_{LED} is set below 600mA, the ISET current threshold for short detection is 120 μ A (corresponding to a 4.9 $k\Omega$ resistor or 3.24A I_{LED}). If the LED current is set above 600mA, the threshold is 220 μ A (corresponding to a 2.7 $k\Omega$ resistor or 5.9A I_{LED}).

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When ISET current is lower than $1.4\mu A$ (corresponding to $428k\Omega$ resistor or 37.3mA ILED), pin open will be detected.

The part latches off once the ISET pin detects a short or open fault, regardless of whether FAULT asserts or not. FAULT asserts low immediately if an ISET short or open condition is detected after start-up. There is a 20ms to 45ms delay for FAULT assertion if a short or open condition is detected during start-up.

IREF

The IREF pin configures the device for buck mode or buck-boost mode, then it sets the current in the external NTC. After mode detection finishes, the voltage on the IREF pin (V_{IREF}) is set to 0.57V with a 10.5% tolerance. Connect a resistor between IREF and GND to obtain a current (I_{IREF}) equal to 0.57V / R_{IREF} . This current is used as a reference current for the NTC's current source. Note that the NTC current is 50 x I_{IREF} in buck mode and 5 x I_{IREF} in buck-boost mode.

The IREF pin is continuously monitored to detect open and short to GND conditions. If the IREF current exceeds $85\mu A$ in buck mode (corresponding to a $6.7k\Omega$ resistor) or $800\mu A$ in buck-boost mode (corresponding to a $0.71k\Omega$ resistor), the pin detects a short to GND condition. If the IREF current is below $3\mu A$ in buck mode (corresponding to a $190k\Omega$ resistor) or $40\mu A$ in buck-boost mode (corresponding to a $14.7k\Omega$ resistor), the pin detects an open fault.

The part latches off once the IREF pin detects a short or open condition, regardless of whether FAULT asserts. FAULT asserts low immediately if a short or open fault occurs after start-up. There is a 20ms to 45ms delay for FAULT assertion if a short or open condition is detected during start-up.

PWM Dimming

An external 10Hz to 2kHz PWM waveform can be applied to the DIM pin to implement PWM dimming. The part stops switching when DIM drops below 0.7V and I_{LED} is zero. The device resumes normal operation with the nominal LED current when DIM exceeds 1.6V. The average LED current is proportional to the PWM duty.

Note that DIM should be high for longer than $100\mu s$. Otherwise, the part may stop switching

and latch due to an LED open condition. To avoid this, the DIM voltage should not be low for longer than 100ms.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. Both (V_{IN} - V_{INGND}) and V_{CC} have UVLO thresholds. V_{IN} - V_{INGND} UVLO has a 6V rising threshold with a 1.1V hysteresis. V_{CC} UVLO has a 4.7V rising threshold with a 0.65V hysteresis. V_{IN} and V_{CC} UVLO do not trigger FAULT.

Fault Detection and Indicator

The MPQ7230 has fault indication. The FAULT pin is the open drain of a MOSFET. FAULT is pulled to VIN through a $300k\Omega$ resistor, and it is pulled to INGND with a $4M\Omega$ pull-down resistor. FAULT is pulled high during normal operation. FAULT pulls low if one of the following occurs: LED short, LED open, thermal shutdown, false mode detection, and over-current protection (OCP). FAULT also asserts if the ISET or IREF pins experience a short or open fault during startup.

The MPQ7230 senses the output voltage (V_{OUT}) by monitoring SW's average voltage in buck mode, or INGND's voltage in buck-boost mode. If an LED+ short to LED- or LED+ short to GND occurs, V_{OUT} drops below the under voltage (UV) threshold. Then a short circuit is detected, and FAULT indicates the fault.

FAULT asserts in buck-boost mode if one of the following occurs: LED+ short to battery, LED open, and output over-voltage (OV) condition. FAULT also asserts if HS-FET's current is low. This low current threshold is 60mA when I_{LED} is below 600mA; otherwise, the threshold is 120mA.

In buck mode, low current detection is disabled when V_{IN} drops below 7.5V to keep the part from latching under cold-crank conditions. In buckboost mode, FAULT does not assert under the following conditions: if LED+ (or INGND) short to battery occurs, or V_{IN} - V_{INGND} drops below its UV. If LED- (or PGND) is shorted to INGND, or V_{INGND} falls below its UV threshold, FAULT asserts. If there is an LED open condition, V_{INGND} exceeds its OV threshold, and FAULT asserts.

In case of higher temperatures, the part operates with a reduced current. The device only stops operating when the internal temperature reaches



the over-temperature protection (OTP) threshold (about 170°C), then FAULT asserts.

If a fault occurs, the part stops switching, and the FAULT output asserts after $20\mu s$. Then the part latches. During the latch, VCC is still present, and the part consumes <2mA of current.

The FAULT pin can only can be reset by $V_{\rm CC}$ UVLO. At start-up, the FAULT pin is not activated, and it remains inactive to 20ms. FAULT activates within 45ms to avoid any false functions when multiple FAULT pins are connected to one another and share the same EN signal. Individual parts are self-protected and latch off immediately if a fault condition is detected, regardless of whether FAULT asserts.

The FAULT pin can withstand 30mA of current, and it protects itself even if it experiences a short or a high voltage. At lower voltages (typically <1.6V), the FAULT sink current increases to enhance the pull-down capability. Figure 5 shows the detailed FAULT sink current when the pin is pulled low at different voltages.

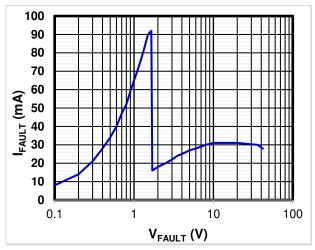


Figure 5: FAULT Sink Current vs. FAULT Voltage

In PWM dimming, fault conditions will not be detected correctly when the dimming ON time is below 100µs. So make sure that the dimming ON time is always higher than 100µs to ensure that the fault detection operates correctly.

Table 1: Fault Detection (10)

Table III and Detection						
Fault Canditions	Detection					
Fault Conditions	Buck	Buck-Boost				
LED+ short to LED-	Vout UV (Vout < 1.1V)	INGND UV (VINGND - VPGND < 1.35V) (12)				
LED+ short to PGND	Vоит UV (Vоит < 1.1V)	INGND UV (V_{INGND} - V_{PGND} < 1.35V) (12)				
LED+ short to INGND	Vоит UV (Vоит < 1.1V)	Normal Condition				
LED+ short to battery	Low LED current (I _{HS} < 60mA when I _{LED_SETTING} < 600mA; I _{HS} < 120mA when I _{LED_SETTING} > 600mA)	FAULT does not assert (V _{IN} - V _{INGND} UVLO)				
LED- short to INGND	Normal conditions	INGND UV (VINGND - VPGND < 1.35V) (12)				
LED- short to battery	FAULT does not assert (Vin - Vingnd UVLO)	FAULT does not assert (Vin - Vingnd UVLO)				
LED open	Low LED current (IHS < 60mA when ILED_SETTING < 600mA, IHS < 120mA when ILED_SETTING > 600mA)	INGND OV (VINGND - VPGND > 18V)				
Incorrect mode detection	VINGND - VPGND > 1.35V	INGND UV (V _{INGND} - V _{PGND} < 1.35V)				
OTP	T _J > 170°C or V _{NTC}	< 0.37V for >256µs				
ISET short (12)	liset > 120µA when lled_setting < 600mA; liset > 220µA when lled_setting > 600mA	I _{ISET} > 120µA				
ISET open (12)	I _{ISET} < 1.4µA					
IREF short (12)	liref > 85µA	IIREF > 800µA				
IREF open (12)	I _{IREF} < 3µA	I _{IREF} < 40µA				
OCP	Current limit triggered 3 times continuously					

Notes:

- 10) Once a fault in the table is detected, the part latches and FAULT is asserted, unless otherwise noted.
- 11) FAULT may glitch if INGND PGND is pulled below -0.3V when an LED+ short to LED- fault occurs with a long cable.
- 12) The part latches when the ISET or IREF pins experience a short or open fault before or after start-up when FAULT is pulled low.



Over-Current Protection (OCP)

The MPQ7230 has cycle-by-cycle peak currentlimit protection. The inductor current is monitored while the HS-FET is on. If the inductor current exceeds the current limit value (about 6.3A when I_{LED} is set above 600mA, or 3.15A when I_{LED} is below 600mA), **HS-FET** the turns immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor current reaches the zero current detection (ZCD) threshold. Then another HS-FET on cycle begins. If the over-current condition remains after three cycles, the part latches off and reports a failure with FAULT.

Load Dump Protection

The MPQ7230's internal MOSFETs have a 50V absolute maximum rating, and the operating voltage can be up to 42V. In buck mode, the maximum voltage can handle load dump conditions up to 42V. In buck-boost mode, the voltage difference between VIN and PGND is equal to the car battery's voltage plus the LED voltage.

Under load dumps, the voltage can rise above the maximum value. To protect the device from load dumps in buck-boost mode, the MPQ7230 stops switching when V_{IN} - V_{PGND} rises above 40V. Then a 100mA sink current at INGND is activated to discharge the output voltage, so that the MOSFET only supports V_{IN} voltage stress. The device automatically restarts when V_{IN} - V_{PGND} drops back to 39V. Load dump protection does not trigger faults, and this protection is not active in buck mode. Load dump protection can reset FAULT after another fault occurs, but it cannot the reset a latch-off state.

Power Derating

When V_{IN} falls below a threshold (about 7V) in buck-boost mode, the power derating starts, and I_{LED} linearly drops with V_{IN} , similar to analog dimming. The derating continues until V_{IN} UVLO occurs, with a -29% derating ratio at UVLO. During start-up, power derating is activated in buck-boost mode, but it is disabled in buck mode.

Thermal Derating through NTC

Connecting a NTC resistor network (R_{NTC}) to the NTC pin drops the output current via analog dimming when the sensed temperature rises above a configured value. The current source

 (I_{NTC}) is 50 x I_{IREF} in buck mode, or 5 x I_{IREF} in buck-boost mode. I_{IREF} flows out the NTC pin and generates a voltage (V_{NTC}) that is equal to I_{NTC} x R_{NTC}). V_{NTC} is sensed to indicate the real temperature and determine the dimming ratio.

When V_{NTC} exceeds 1.25V, there is no dimming. To avoid activating the NTC function, pull the NTC pin above 1.25V, or pull it to VCC. When V_{NTC} is lower than 1.2V, dimming is activated and the dimming ratio decreases as V_{NTC} decreases. The dimming ratio drops by a step of 2% when V_{NTC} drops by 30mV. When V_{NTC} drops from 1.25V to 0.5V, the dimming ratio drops to 50%, and the LED average current drops to 50% of the set value accordingly. The LED current does not drop below 50%, even if V_{NTC} is below 0.5V. The device triggers OTP if V_{NTC} drops below 0.4V for longer than 256 μ s. The device stops switching and does not recover until V_{NTC} rises back to 0.5V. FAULT does not assert for this event.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 170°C, the entire chip shuts down and FAULT is asserted. Restart the device with a power-on restart, or by resetting EN.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The bootstrap capacitor voltage is charged to about 5V from VCC through the pass transistor when the LSFET is on. This floating driver has its own UVLO protection, with a rising threshold of 2.5V and a hysteresis of 700mV. When the BST-to-SW voltage drops to 2.2V, the LS-FET is forced on to refresh the BST voltage.

A 22nF to 220nF ceramic capacitor is recommended for the bootstrap capacitor. The capacitance should have a derating for the DC voltage and temperature. Consider this derating when choosing the capacitor to ensure that the real capacitance is between 22nF and 200nF. A maximum 22Ω resistor can be placed in series with the bootstrap capacitor to reduce the SW spike voltage.



APPLICATION INFORMATION

Buck and Buck-Boost Mode Selection

The operation mode can be configured by connecting a different resistor (R_{IREF}) at the IREF pin. Select a $1.05k\Omega \le R_{IREF} \le 9.09k\Omega$ for buckboost mode, or a $80.6k\Omega \ge R_{IREF} \ge 14.7k\Omega$ for buck mode.

Setting the LED Current

The external resistor (R_3) connected to the ISET pin sets the LED current (I_{LED}) . R_3 can be calculated with Equation (2):

$$R_3 = \frac{16}{I_{LED}(A)}(k\Omega)$$
 (2)

Table 2 shows the recommended values for R₃.

Table 2: Resistor Selection for Common LED Currents

I _{LED} (A)	R ₃ (kΩ)		
3	5.36		
2	8		
1.2	13.3		
0.75	21.1		

If I_{LED} is below 0.7A in buck-boost mode, certain resistors are recommended (see Table 3).

Table 3: Resistor Selection when I_{LED} ≤ 700mA in Buck-Boost Mode

I _{LED} (A)	R ₃ (kΩ)
0.7	22.6
0.65	24.4
0.6	26.3
0.55	28.6
0.5	31.5
0.45	34.9
0.4	39.1

Figure 6 shows the relationship between I_{LED} and R_{ISET} in buck-boost mode.

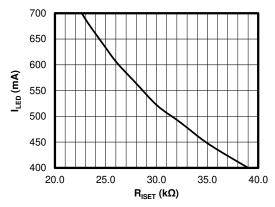


Figure 6: I_{LED} vs. R_{ISET} when I_{LED} ≤ 700mA in Buck-Boost Mode

Selecting the Inductor

For most applications, use an inductor ranging between $4.7\mu H$ and $33\mu H$ with a DC current rating higher than the maximum inductor current. Consider the inductor's DC resistance when estimating the output current and the inductor's power consumption.

For buck converter designs, estimate the required inductance value with Equation (3):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_{I} \times f_{SW}}$$
(3)

Choose the inductor ripple current to be higher than 20% of the LED current. The inductor peak current can be calculated with Equation (4):

$$I_{L_PEAK} = I_{L_AVG} + \frac{\Delta I_L}{2}$$
 (4)

Where I_{L_AVG} is the average current through the inductor, which is equal to the output load current (LED current) in buck applications. Under lightload conditions, use a larger-value inductor to improve efficiency and current precision. Table 4 shows the recommended inductor values in buck mode with common LED currents.

Table 4: Buck Mode Inductor Value for Common LED Currents

I _{LED} (A)	Recommended Inductor Value (µH)				
(1A, 3A]	10				
(0.5A, 1A]	15				
(0.3A,0.5A]	22				
[0.2A, 0.3A]	33				



For buck-boost converter designs, estimate the required inductance value with Equation (5):

$$L = \frac{V_{OUT} \times V_{IN}}{(V_{OUT} + V_{IN}) \times \Delta I_{L} \times f_{SW}}$$
 (5)

Where ΔI_L is the inductor peak-to-peak current ripple. Set ΔI_L to be over 25% of the inductor average current when $I_{LED} > 0.7A$, and set it to be over 20% of the inductor average current when $I_{LED} < 0.7A$. I_{L_AVG} can be calculated with Equation (6):

$$I_{L_{AVG}} = I_{LED} \times (1 + \frac{V_{OUT}}{V_{IN}})$$
 (6)

The inductor's peak current can be calculated with Equation (7):

$$I_{L_PEAK} = I_{L_AVG} + \frac{1}{2} \times \Delta I_{L}$$
 (7)

Under light-load conditions, use a larger-value inductor to improve efficiency and current precision. Table 5 shows the recommended inductor values in buck-boost mode with common LED currents.

Table 5: Buck-Boost Mode Inductor Value for Common LED Currents

I _{LED} (A)	Recommended Inductor Value (µH)			
(0.75A, 1.2A]	10			
(0.5A, 0.75A]	15			
(0.3A, 0.5A]	22			
[0.2A, 0.3A]	33			

Selecting the Input Capacitor

The input current in buck and buck-boost mode is discontinuous, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a $4.7\mu\text{F}$ to $22\mu\text{F}$ capacitor. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, it is recommended to use another lower-value capacitor (e.g. $0.1\mu\text{F}$) with a small package size (0603) to absorb high-

frequency switching noise. Place the smaller capacitor as close to VIN and GND (INGND is connected to PGND in buck mode, but the capacitor should be close to both INGND and PGND in buck-boost mode) as possible.

Since C_{IN} absorbs the input switching current in buck mode, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (8):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$
 (8)

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (9):

$$I_{CIN} = \frac{I_{LOAD}}{2} \tag{9}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input voltage ripple caused by the capacitance can be estimated with Equation (10):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

At buck-boost mode, if the $I_{BANDVALLEY} \ge I_{LED}$, the capacitance can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{I_{LED} \times V_{OUT}}{(V_{IN} + V_{OUT}) \times f_{SW} \times C_{IN}}$$
(11)

In buck-boost mode, the capacitor between VIN and PGND must consider VCC regulator stability. When $(V_{INGND} - V_{PGND}) > 5.1V$, the input of the VCC regulator switches to V_{INGND} to reduce power loss. A 2.2 μ F to 10μ F/50V X7R ceramic capacitor should be placed between VIN to PGND to keep VCC stable when the VCC charging source changes from VIN to INGND. Place a symmetric 4.7 μ F/50V, X7R ceramic capacitor between VIN and PGND.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. For the best results, use low-ESR capacitors to keep the output voltage ripple low.



In buck mode, the output voltage ripple can be estimated with Equation (12):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times (R_{\text{ESR}} + \frac{1}{8 \times f_{\text{sw}} \times C_{\text{OUT}}}) \ (12)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (13):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{8 \times f_{\text{SW}}^2 \times L \times C_{\text{OUT}}} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \quad (13)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (14):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{f_{\text{SW}} \times L} \times (1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}) \times R_{\text{ESR}} \qquad (14)$$

For buck-boost applications, if the I_{BandValley} ≥the I_{LED}, the output capacitor can be selected using Equation (15):

$$\Delta V_{\text{OUT}} = I_{\text{LED}} \times (R_{\text{ESR}} + \frac{V_{\text{OUT}}}{f_{\text{sw}} \times C_{\text{OUT}} \times (V_{\text{IN}} + V_{\text{OUT}})}) \text{ (15)}$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (16):

$$\Delta V_{OLIT} = I_{LED} \times R_{ESB} \tag{16}$$

A 2.2 μ F to 10 μ F ceramic capacitor is sufficient for most applications.

Selecting the Diode from PGND to INGND in Buck-Boost Mode

In buck-boost mode, place a Schottky diode between INGND and PGND to handle the charge current for the VIN to PGND capacitor, especially when V_{IN} has a high slew rate. When $(V_{INGND} - V_{PGND}) < 5.1V$, VCC is powered from VIN. In this scenario, the VCC charge current flows from the VCC capacitor to PGND, then back to INGND and the car battery. A Schottky diode with a low forward voltage (V_F) (about 0.32V), a minimum 1A current rating, and a

VRRM voltage exceeding 20V is sufficient. It is recommended to use the PMEG2010EPAS Schottky diode.

Selecting VCC Capacitor

A smaller-value VCC capacitor causes VCC voltage ringing and leads to unstable switching. It is recommended to place a ≥3µF decoupling ceramic capacitor at the VCC pin. When choosing the capacitor, consider capacitance derating to ensure that the real capacitance is ≥3µF. A 10µF capacitor with X7R dielectrics and a ≥10V DC rated voltage is recommended. VCC is referenced PGND/AGND.

BST Resistor and Capacitor

It is recommended to place a resistor in series with the BST capacitor to reduce the SW spike voltage. A higher resistance improves SW spike reduction but compromises efficiency. The recommended external BST capacitor value is a 22nF to 220nF ceramic capacitor with a 10V/16V DC derating. A maximum 22 Ω resistor with a 0603/0402 package is recommended. It is not necessary to use a large resistor package.

In normal operation, the average current flowing through the bootstrap resistor is about 20mA in buck mode and 10mA in buck-boost mode. If the capacitor is short-circuited, the current inside the resistor is limited by the internal LDO. Then the device quickly detects that the LED current is below the low limit, and a failure is detected. Then the part latches off and no more current is sourced to the resistor. A 0402 package can handle the power dissipation on the bootstrap resistor.

Low Dimming Frequency Application

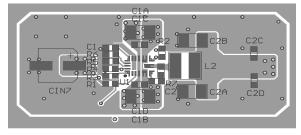
For applications with low PWM dimming frequencies at small dimming duty cycles, the error amplifier's output voltage (V_{COMP}) may be discharged by the leakage if the dimming off time is too long. The minimum dimming frequency should not be below 10Hz.



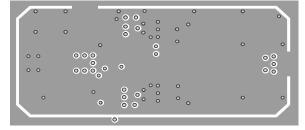
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially for input capacitor placement. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 7 and Figure 8 (on page 49) and follow the guidelines below:

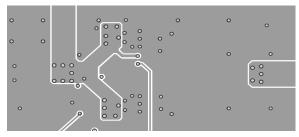
- Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
- 2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
- Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize high-frequency noise. Keep the connection between the input capacitor and VIN as short and wide as possible.
- 4. Place the VCC capacitor as close as possible to the VCC and GND pins.
- 5. Route SW and BST away from sensitive analog areas, such as FB.
- 6. Place the feedback resistors close to chip to ensure that the trace connected to the FB pin is as short as possible.
- 7. Use multiple vias to connect the power planes to the internal layers.



Top Layer



Mid-Layer 1



Mid-Layer 2

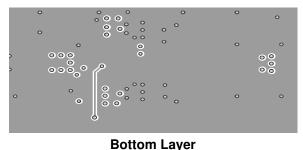
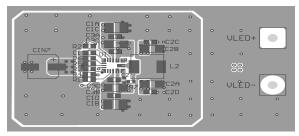
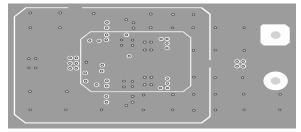


Figure 7: Recommended PCB Layout for Buck Mode (13)

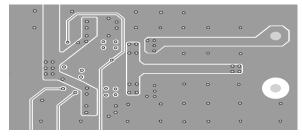




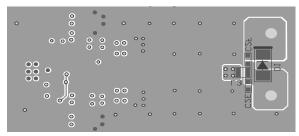
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout for Buck-Boost Mode (14)

Notes:

- 13) The recommended layout is based on Figure 9 on page 50.14) The recommended layout is based on Figure 10 on page 50.



TYPICAL APPLICATION CIRCUITS

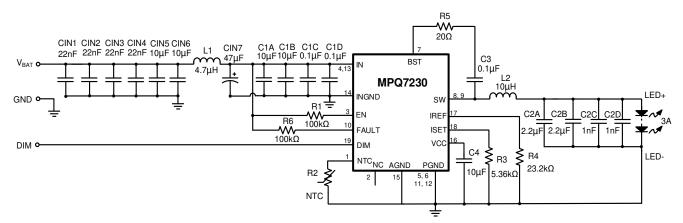


Figure 9: Buck Application Circuit (I_{LED} = 3A)

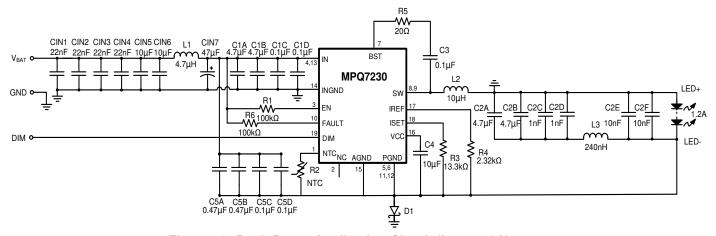
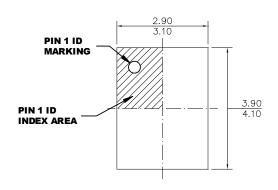


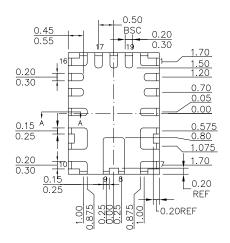
Figure 10: Buck-Boost Application Circuit (I_{LED} = 1.2A)



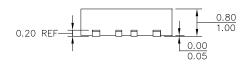
PACKAGE INFORMATION

QFN-19 (3mmx4mm) Wettable Flank



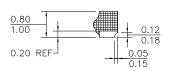


TOP VIEW

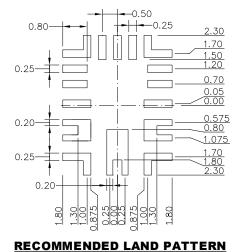


SIDE VIEW

BOTTOM VIEW



SECTION A-A

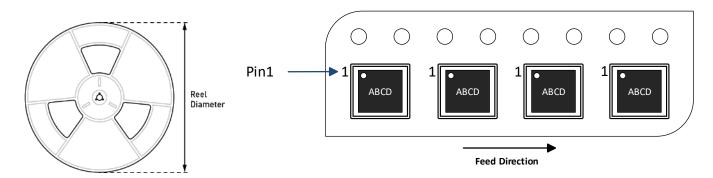


NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7230GLE- AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/18/2021	Initial Release	-

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