

MC74VHCT126A

Quad Bus Buffer with 3-State Control Inputs

The MC74VHCT126A is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT126A requires the 3-state control input (OE) to be set Low to place the output into high impedance.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

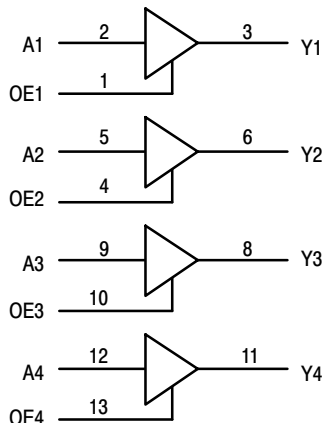
The VHCT126A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0V$. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 3.8ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^\circ C$
- TTL-Compatible Inputs: $V_{IL} = 0.8V$; $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM

Active-High Output Enables



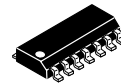
FUNCTION TABLE

VHCT126A		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

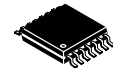


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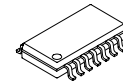
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14-LEAD SOIC
D SUFFIX
CASE 751A

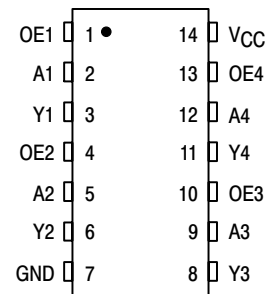


14-LEAD TSSOP
DT SUFFIX
CASE 948G



14-LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 107 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT126AD	SOIC	55 Units/Rail
MC74VHCT126ADT	TSSOP	96 Units/Rail
MC74VHCT126AM	SOIC EIAJ	50 Units/Rail

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage	- 0.5 to + 7.0	V
V _{out}	DC Output Voltage	- 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	- 20	mA
I _{OK}	Output Diode Current	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 40	+ 85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 5.0V ± 0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0	1.2			1.2		1.2		V
			4.5	2.0		2.0		2.0			
			5.5	2.0		2.0		2.0			
V _{IL}	Maximum Low-Level Input Voltage		3.0			0.53		0.53		0.53	V
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = - 50μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = - 4mA I _{OH} = - 8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μA
I _{CC(T)}	Quiescent Supply Current	Input: V _{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I _{OZ}	Maximum 3-State Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5			± 0.25		± 2.5		± 2.5	μA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5V	0.0			0.5		5.0		10	μA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.6	8.0	1.0	9.5		12.0	ns
		$C_L = 50\text{pF}$		8.1	11.5	1.0	13.0		16.0	
		$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$		3.8	5.5	1.0	6.5		8.5	
		$C_L = 50\text{pF}$		5.3	7.5	1.0	8.5		10.5	
t_{PZL} , t_{PZH}	Maximum Output Enable Time, $\overline{\text{OE}}$ to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 15\text{pF}$		5.4	8.0	1.0	9.5		11.5	ns
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		7.9	11.5	1.0	13.0		15.0	
		$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 15\text{pF}$		3.6	5.1	1.0	6.0		7.5	
		$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$		5.1	7.1	1.0	8.0		9.5	
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time, $\overline{\text{OE}}$ to Y	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$		9.5	13.2	1.0	15.0		18.0	ns
		$R_L = 1\text{k}\Omega$								
		$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 50\text{pF}$		6.1	8.8	1.0	10.0		12.0	
		$R_L = 1\text{k}\Omega$								
t_{OSLH} , t_{OSHL}	Output-to-Output Skew	$V_{CC} = 3.3 \pm 0.3\text{V}$ $C_L = 50\text{pF}$			1.5		1.5		2.0	ns
		(Note 1.)								
		$V_{CC} = 5.0 \pm 0.5\text{V}$ $C_L = 50\text{pF}$			1.0		1.0		1.5	
		(Note 1.)								
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)			6						pF

Symbol	Parameter	Typical @ 25°C , $V_{CC} = 5.0\text{V}$		Unit
		Min	Max	
C_{PD}	Power Dissipation Capacitance (Note 2.)		15	pF

- Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0\text{ns}$, $C_L = 50\text{pF}$, $V_{CC} = 5.0\text{V}$)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

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SWITCHING WAVEFORMS

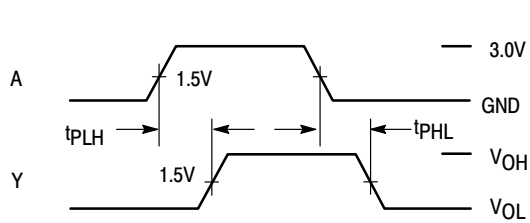


Figure 1.

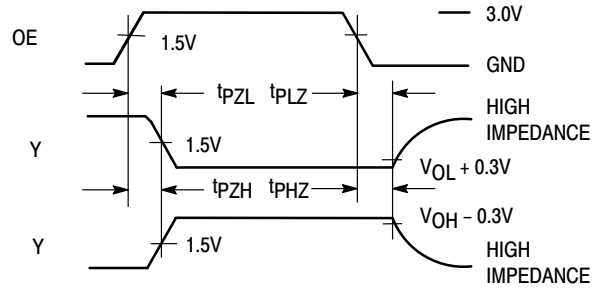
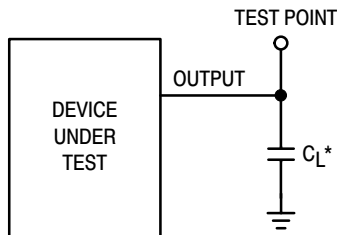
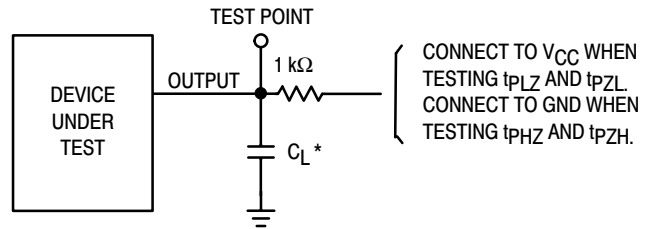


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit

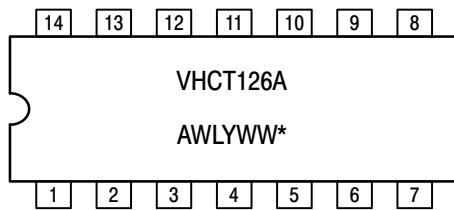


*Includes all probe and jig capacitance

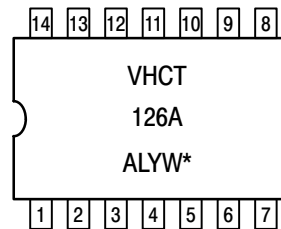
Figure 4. Test Circuit

MARKING DIAGRAMS

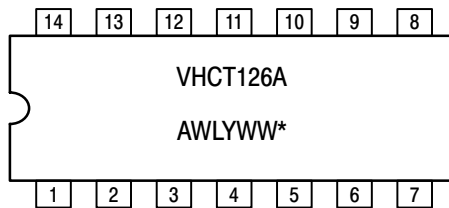
(Top View)



14-LEAD SOIC
D SUFFIX
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14-LEAD TSSOP
DT SUFFIX
CASE 948G



14-LEAD SOIC EIAJ
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*See Applications Note #AND8004/D for date code and traceability information.