HARRIS SEMICONDUCTOR

ICL7660S
Super Voltage Converter

GENERAL DESCRIPTION

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry-standard ICL7660 offering an ***extended*** operating supply voltage range up to 12V, with ***lower*** supply current. ***No external diode*** is needed for the ICL7660S. In addition, a ***Frequency Boost pin*** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of −1.5V to −12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

FEATURES

- ***Guaranteed Lower*** **Max Supply Current for** ***All*** **Temperature Ranges**
- ***Guaranteed Wider*** **Operating Voltage Range —1.5V to 12V**
- ***No External Diode*** **Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- ***Guaranteed*** **Minimum Power Efficiency of 96%**
- ***Improved*** **Minimum Open Circuit Voltage Conversion Efficiency of 99%**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use—Requires Only 2 External Non-Critical Passive Components**
- ***Improved*** **Direct Replacement for Industry-Standard ICL7660 and Other Second-Source Devices**

APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems & Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7660SCBA	0°C to +70°C	8-Pin SOIC
ICL7660SCPA	0°C to +70°C	8-Pin Minidip
ICL7660SIBA	−25°C to +85°C	8-Pin SOIC
ICL7660SCTV	0°C to +70°C	TO-99
ICL7660SIPA	−25°C to +85°C	8-Pin Minidip
ICL7660SITV	−25°C to +85°C	TO-99
ICL7660SMTV*	−55°C to +125°C	TO-99

*Add /883B to part number if 883B processing is required.

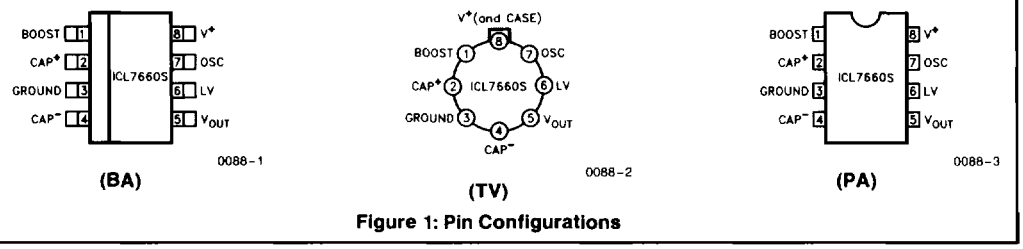


Figure 1: Pin Configurations

302163-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 13.0V

LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V+ + 0.3V) for V+ <5.5V
..... (V+ − 5.5V) to (V+ + 0.3V) for V+ >5.5V

Current into LV (Note 1) ..... 20 μA for V+ > 3.5V

Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous

Power Dissipation (Note 2)
ICL7660SCTV ..... 500 mW
ICL7660SCPA ..... 300 mW
ICL7660SCBA ..... 300 mW
ICL7660SITV ..... 500 mW
ICL7660SIPA ..... 300 mW
ICL7660SIBA ..... 300 mW
ICL7660SMTV ..... 500 mW

Operating Temperature Range
ICL7660SM ..... −55°C to +125°C
ICL7660SI ..... −25°C to +85°C
ICL7660SC ..... 0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature
(Soldering, 10 sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

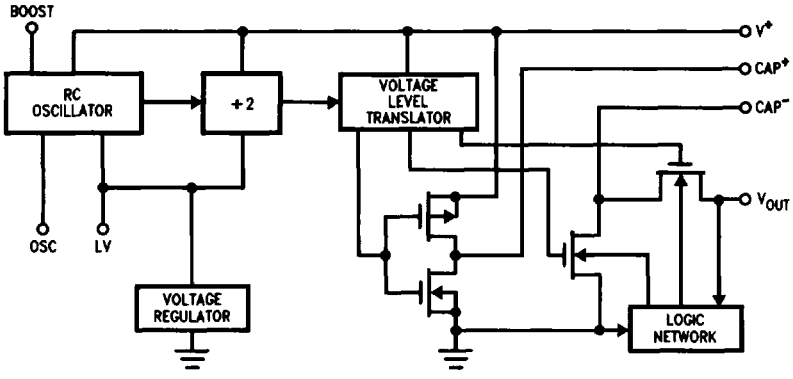


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, OSC = Free running, Test Circuit Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I^+	***Supply Current*** (Note 3)	$R_L = \infty$, 25°C		***80***	***160***	μA
		$0°C < T_A < +70°C$			***180***	
		$-25°C < T_A < +85°C$			***180***	
		$-55°C < T_A < +125°C$			***200***	
V_H^+	***Supply Voltage Range—HI*** (Note 4)	$R_L = 10K$, LV Open $T_{min} < T_A < T_{max}$	3.0		***12***	V
V_L^+	Supply Voltage Range—Lo	$R_L = 10K$, LV to GROUND $T_{min} < T_A < T_{max}$	1.5		3.5	V
R_{OUT}	***Output Source Resistance***	$I_{OUT} = 20$ mA, $T_A = 25°C$		60	100	Ω
		$I_{OUT} = 20$ mA, $0°C < T_A < +70°C$			120	
		$I_{OUT} = 20$ mA, $-25°C < T_A < +85°C$			120	
		$I_{OUT} = 20$ mA, $-55°C < T_A < +125°C$			150	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $0°C < T_A < +70°C$			***250***	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $-25°C < T_A < +85°C$			***300***	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $-55°C < T_A < +125°C$			400	
f_{OSC}	***Oscillator Frequency***	$C_{OSC} = 0$, Pin 1 Open or GND	***5***	10		kHz
		Pin 1 = V^+		***35***		
PEff	***Power Efficiency***	$R_L = 5$ kΩ	***96***	98		%
		$T_{min} < T_A < T_{max}$	***95***	***97***		
V_{OUT} ***Eff***	***Voltage Conversion Efficiency***	$R_L = \infty$	***99***	99.9		%
Z_{OSC}	Oscillator Impedance	$V^+ = 2V$		1		MΩ
		$V^+ = 5V$		100		kΩ

NOTE 1: Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.

2: Derate linearly above 50°C by 5.5 mW/°C.

3: In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5 pF.

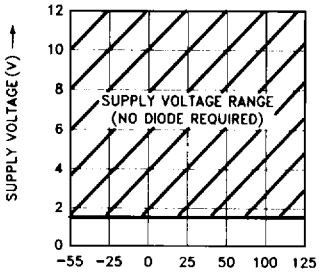
4: The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

5: All significant improvements over the industry-standard ICL7660 are highlighted in ***bold italics.***

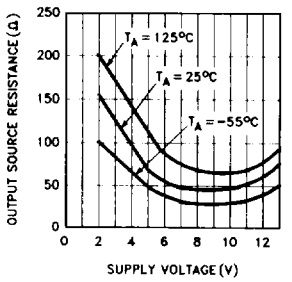
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

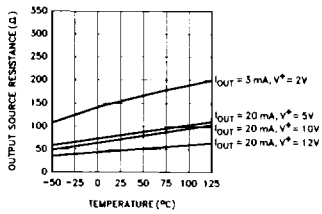
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



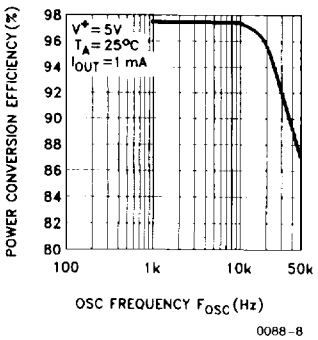
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



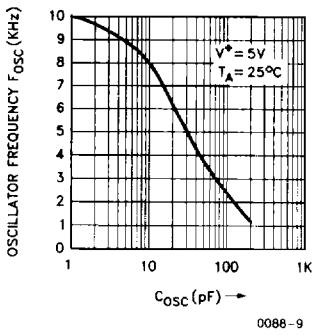
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



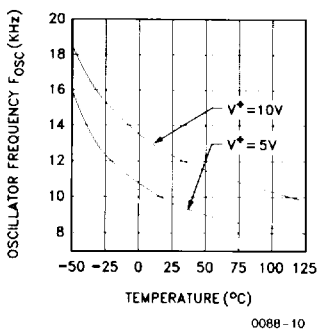
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



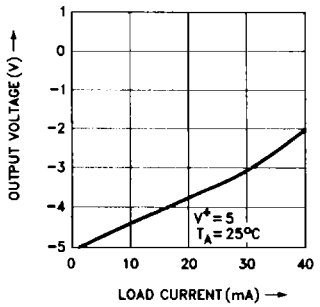
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



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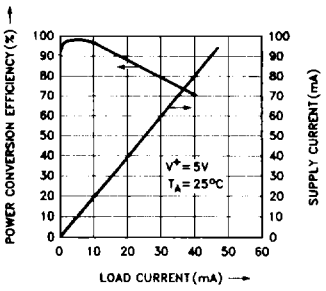
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



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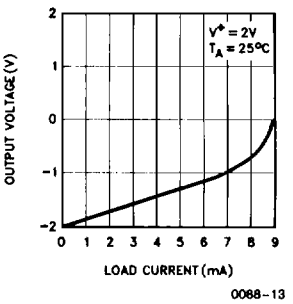
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



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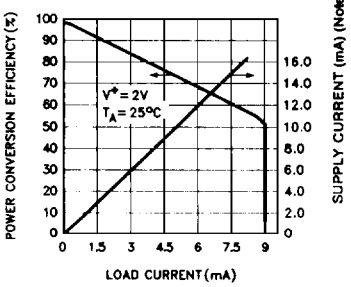
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



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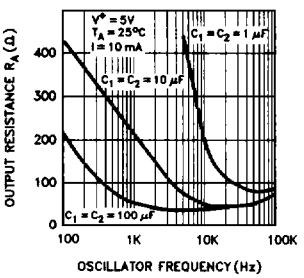
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



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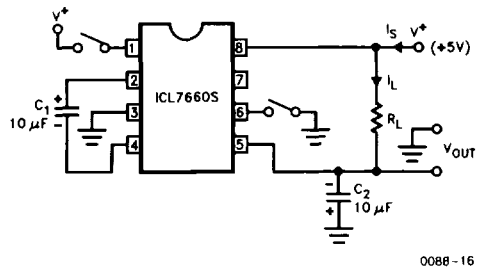
NOTE 6: These curves include in the supply current that current fed directly into the load R_L from V+ (see Figure 3). Thus approximately half the supply current goes directly to the positive side of the load, and the other half, throught the ICL7660S, to the negative side of the load. Ideally, $V_{OUT} \approx 2\ V_{IN}$, $I_S \approx 2\ I_L$, so $V_{IN} \times I_S \approx V_{OUT} \times I_L$.

NOTE: All typical values have been characterized but are not tested.



NOTE 1: For large values of C_{OSC} (> 1000pF) the values of C_1 and C_2 should be increased to 100μF.

Figure 3: ICL7660S Test Circuit

DETAILED DESCRIPTION

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660S, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

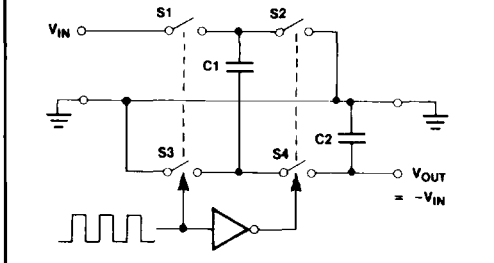


Figure 4: Idealized Negative Voltage Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \tfrac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the 7660S has a large source impedance (25 - 30 ohms), then a 2.2μF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/μs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.
   A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).

NOTE: All typical values have been characterized but are not tested.

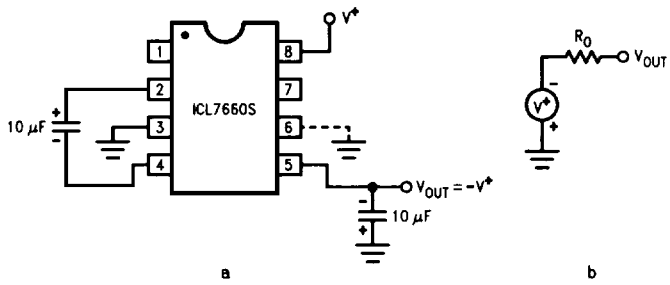


Figure 5: Simple Negative Converter and its Output Equivalent

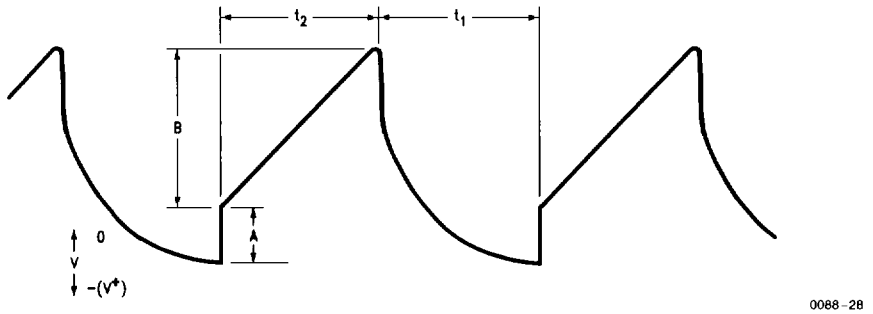


Figure 6: Output Ripple

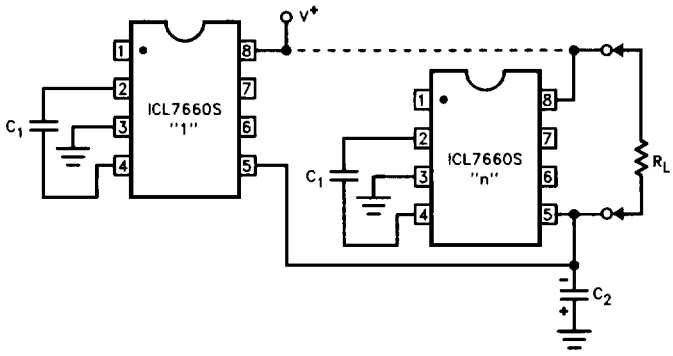
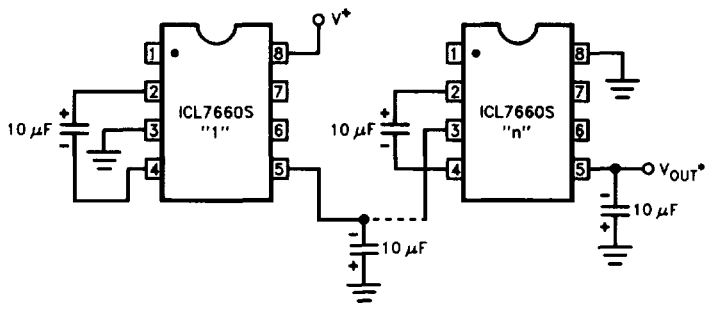


Figure 7: Paralleling Devices

NOTE: All typical values have been characterized but are not tested



*NOTE 1: $V_{OUT} = -nV^+$ for $1.5V \leq V^+ \leq 12V$.

Figure 8: Cascading Devices for Increased Output Voltage

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of −(V+). The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_o \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_o \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C1} + 4 \times ESR_{C1} + ESR_{C2}\ \Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω @ 25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C1)$ term, but may have the side effect of a net increase in output impedance when C1 > 10 μF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10 kHz and C = C1 = C2 = 10 μF:

$$R_o \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_o \cong 46 + 20 + 5 \times ESR_C\ \Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 6. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flowing into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is $2 \times I_{OUT}$, hence the total drop is $2 \times I_{OUT} \times ESR_{C2}$ volts. Segment B is the voltage change across C2 during time t_2, the half of the cycle when C2 supplies current to the load. The drop at B is $I_{OUT} \times t_2/C2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left(\frac{1}{2 \times f_{PUMP} \times C2} + 2 \times ESR_{C2}\right) \times I_{OUT}$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660S})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

NOTE: All typical values have been characterized but are not tested.

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S R_{OUT} values.

Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to V^+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately 3½ times. The result is a decrease in the output impedance and ripple. This is of major importance for surface-mount applications where capacitor size and cost are critical. Smaller capacitors, e.g. 0.1 μF, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 10$ μF or 100 μF. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent device latchup, a 100 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

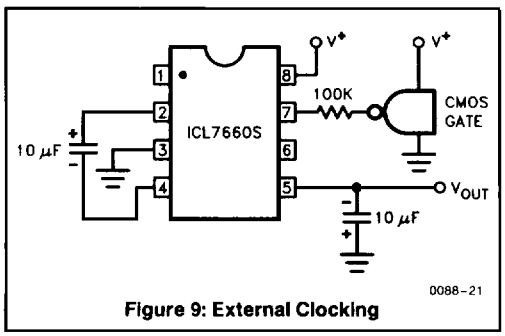


Figure 9: External Clocking

It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

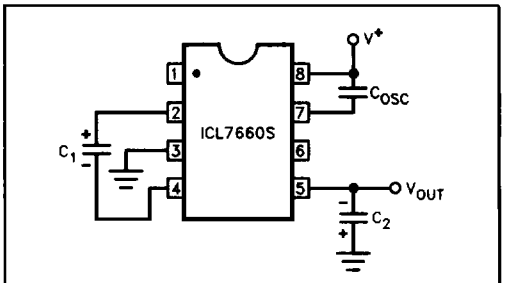
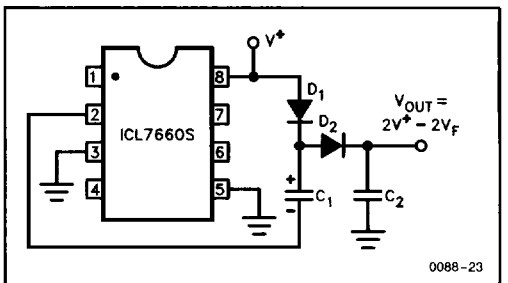


Figure 10: Lowering Oscillator Frequency



NOTE: D_1 & D_2 can be any suitable diode.

Figure 11: Positive Voltage Doubler

Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7660S are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

NOTE: All typical values have been characterized but are not tested.

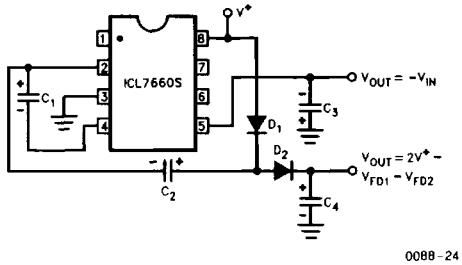


Figure 12: Combined Negative Voltage Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, although with rather high series output resistance (~250Ω).

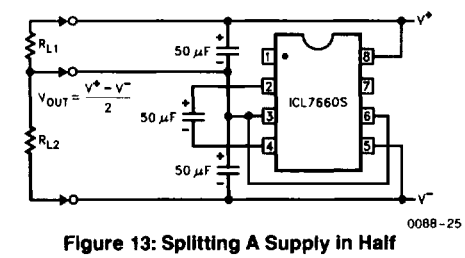


Figure 13: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660S may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

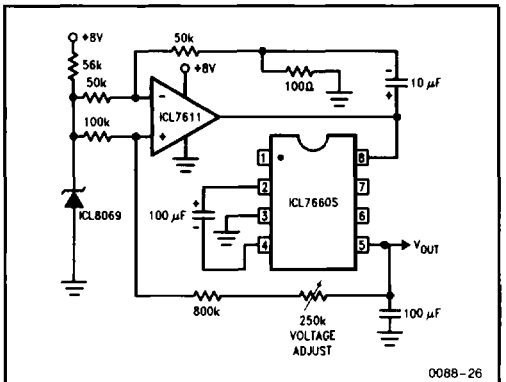


Figure 14: Regulating the Output Voltage

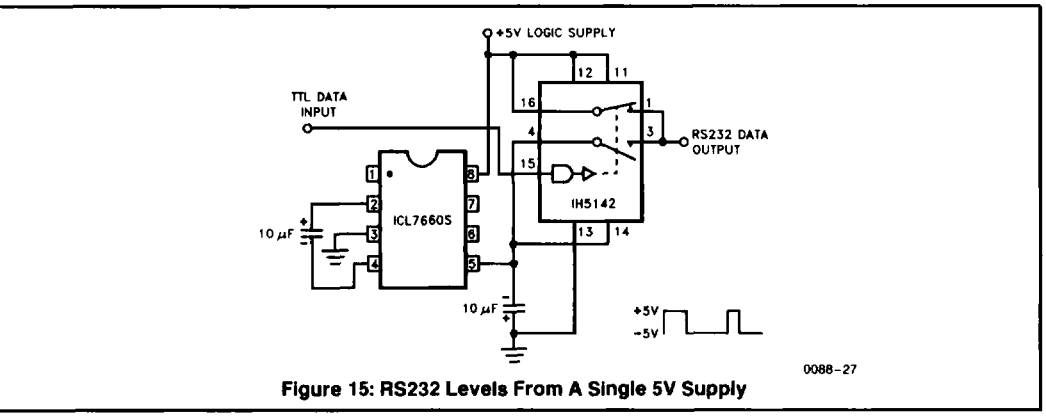


Figure 15: RS232 Levels From A Single 5V Supply

NOTE: All typical values have been characterized but are not tested.