



28 GBPS, D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

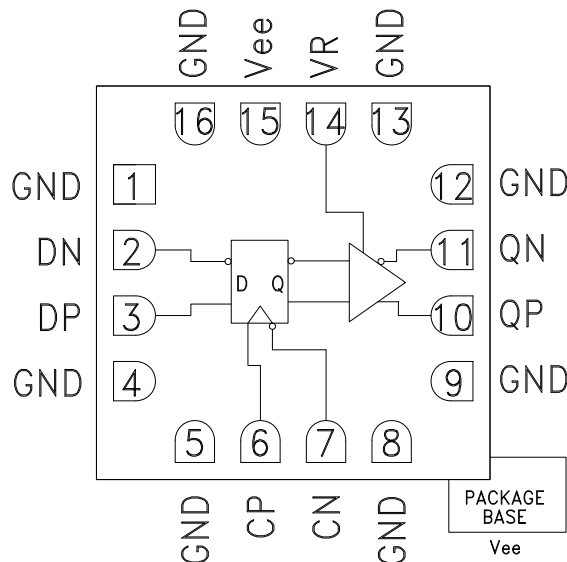
The HMC853LC3 is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 28 Gbps
- Digital Logic Systems up to 28 GHz

Features

- Differential & Single-Ended Operation
- Fast Rise and Fall Times: 15/14 ps
- Low Power Consumption: 240 mW typ.
- Programmable Differential Output Voltage Swing: 700 - 1300 mVp-p
- Single Supply: -3.3 V
- 16 Lead Ceramic 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC853LC3 is a D-Type Flip-Flop designed to support data transmission rates of up to 28 Gbps, and clock frequencies as high as 28 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications.

All differential inputs to the HMC853LC3 are CML and terminated on-chip with 50 Ohms to the positive supply, Vcc, and may be AC or DC coupled. The differential CML outputs are source terminated to 50 Ohms and may also be AC or DC coupled. Outputs can be connected directly to a 50 Ohm Vcc-terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to ground. The HMC853LC3 also features an output level control pin, VR, which allows for loss compensation or signal-level optimization. The HMC853LC3 operates from a single 3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, $T_A = 25^\circ\text{C}$, $V_{ee} = -3.3\text{ V}$, $VR = 0\text{ V}$

| Parameter | Conditions | Min. | Typ. | Max | Units |
|---------------------------------------|----------------------------|------|------|------|-------|
| Power Supply Voltage | | -3.6 | -3.3 | -3.0 | V |
| Power Supply Current | | | 73 | | mA |
| Maximum Data Rate | | | 28 | | Gbps |
| Maximum Clock Rate | | | 28 | | GHz |
| Input Voltage Range | | -1.5 | | 0.5 | V |
| Input Differential Voltage | | 0.1 | | 2.0 | Vp-p |
| Input Return Loss, Output Return Loss | Frequency <24 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 550 | | mVp-p |
| | Differential, peak-to-peak | | 1100 | | mVp-p |
| Output High Voltage | | | -10 | | mV |

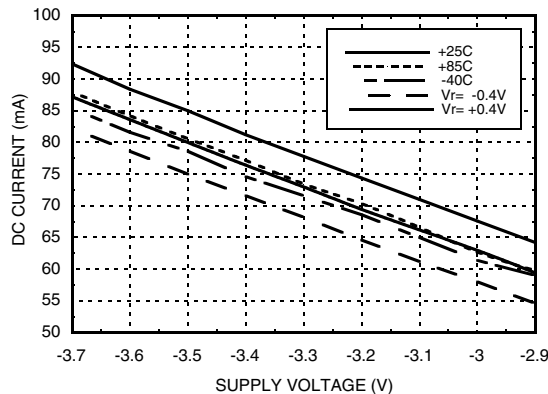


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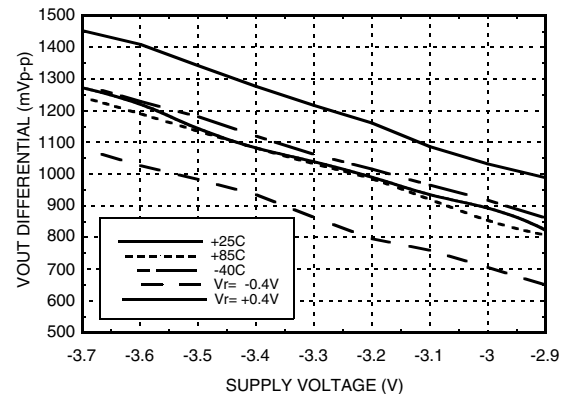
Electrical Specifications (continued)

| Parameter | Conditions | Min. | Typ. | Max | Units |
|-------------------------------------|---|------|---------|-----|---------|
| Output Low Voltage | | | -560 | | mV |
| Output Rise / Fall Time | Differential, 20% - 80% | | 15 / 14 | | ps |
| Output Return Loss | Frequency <24 GHz | | 10 | | dB |
| Random Jitter Jr | rms | | | 0.2 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, 2 ¹⁵ -1 PRBS input [1] | | 2 | | ps, p-p |
| Propagation Delay Clock to Data, td | | | 101 | | ps |
| Clock Phase Margin | 28 GHz | | 300 | | deg |
| Set Up Time, t _s | | | 4 | | ps |
| Hold Time, t _h | | | 3 | | ps |
| VR Pin Current | VR = 0.0 V | | 2.5 | | mA |
| VR Pin Current | VR = 0.4 V | | | 4 | mA |

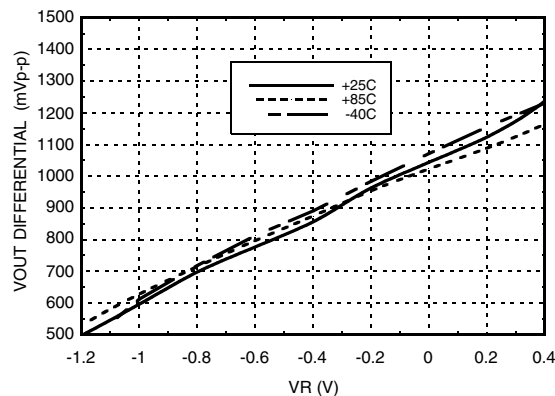
DC Current vs. Supply Voltage [1][2]



Output Differential Voltage vs. Supply Voltage [1][2]



Output Differential Voltage vs. VR [2][3]



[1] VR = 0.0 V

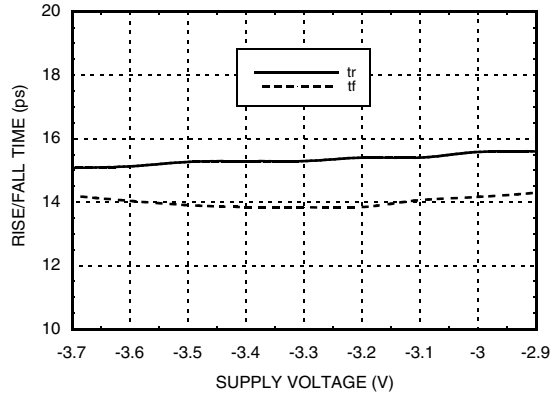
[2] Frequency = 13 GHz

[3] Vee = -3.3 V

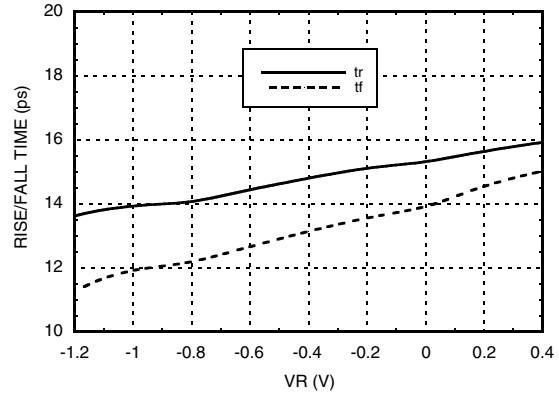


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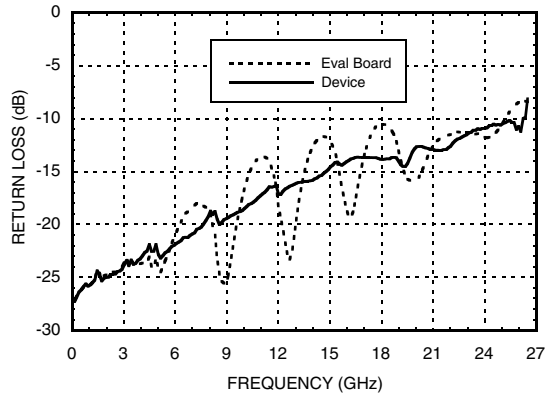
Rise / Fall Time vs. Supply Voltage [1][2]



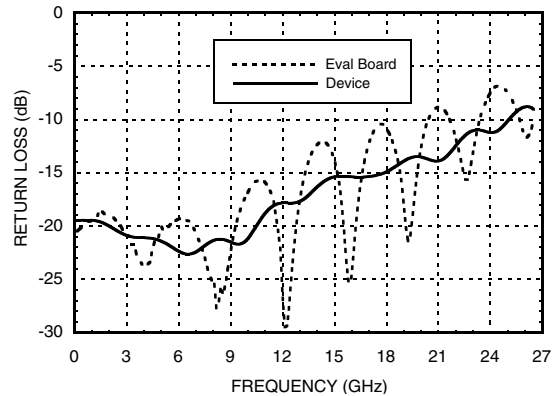
Rise / Fall Time vs. VR [2][4]



Input Return Loss vs. Frequency [1][3][4]



Output Return Loss vs. Frequency [1][3][4]



[1] VR = 0.0 V
[4] Vee = -3.3 V

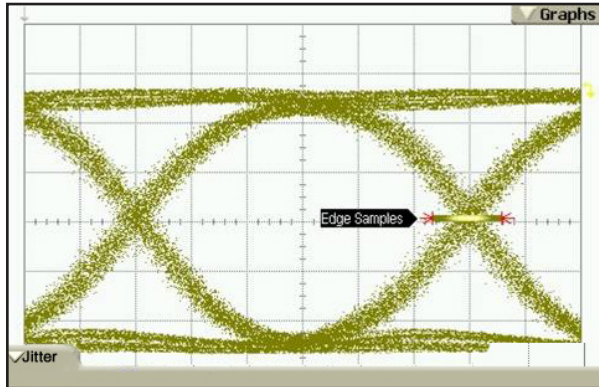
[2] Frequency = 13 GHz

[3] Device measured on evaluation board with single-ended time domain gating.



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Eye Diagram @ 25 Gbps

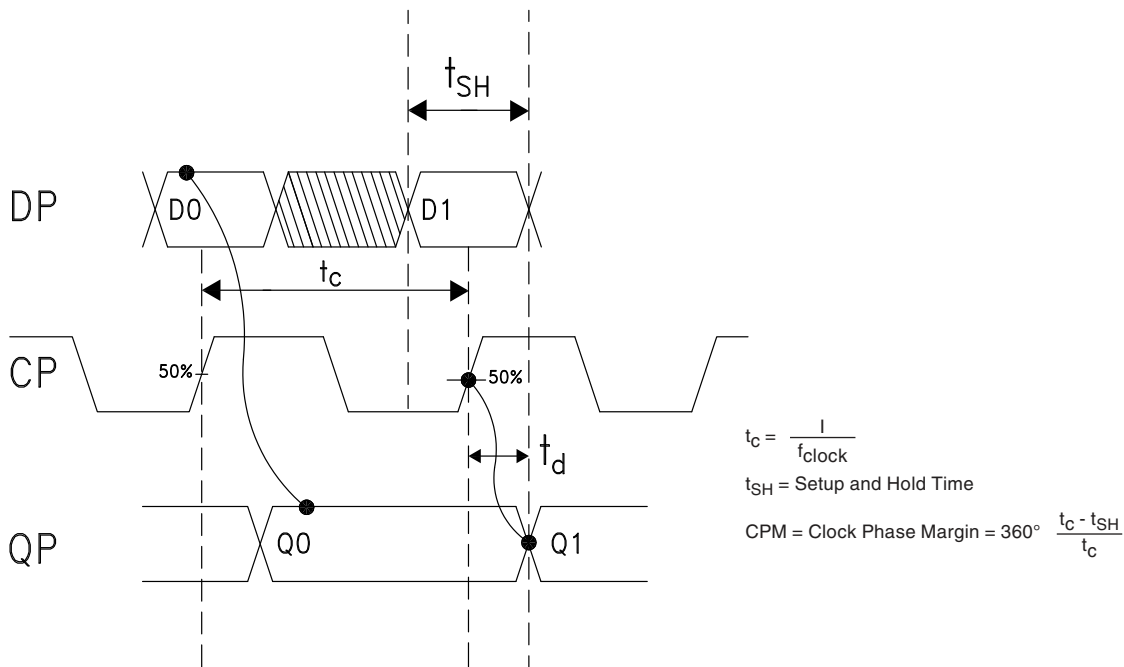


| Parameter | Conditions |
|----------------|--------------|
| Bit Rate | 24.9900 Gbps |
| Pattern Length | 127 Bits |
| DJ (d-d) | 2.0 ps |
| Vertical Scale | 100 mV / div |
| Time Scale | 6.7 ps / div |

Test Conditions:

Pattern generated with a 2⁷-1 PN generator at 25 GHz. Measured using an Agilent 86100C 33 GHz DCA. Single-ended 550 mV data and 400 mV clock inputs.

Timing Diagram



Truth Table

| Input | | Outputs |
|-------|--------|---------|
| D | C | Q |
| L | L -> H | L |
| H | L -> H | H |

Notes:
 D = DP - DN
 C = CP - CN
 Q = QP - QN
 H - Positive Difference Voltage
 L - Negative Difference Voltage



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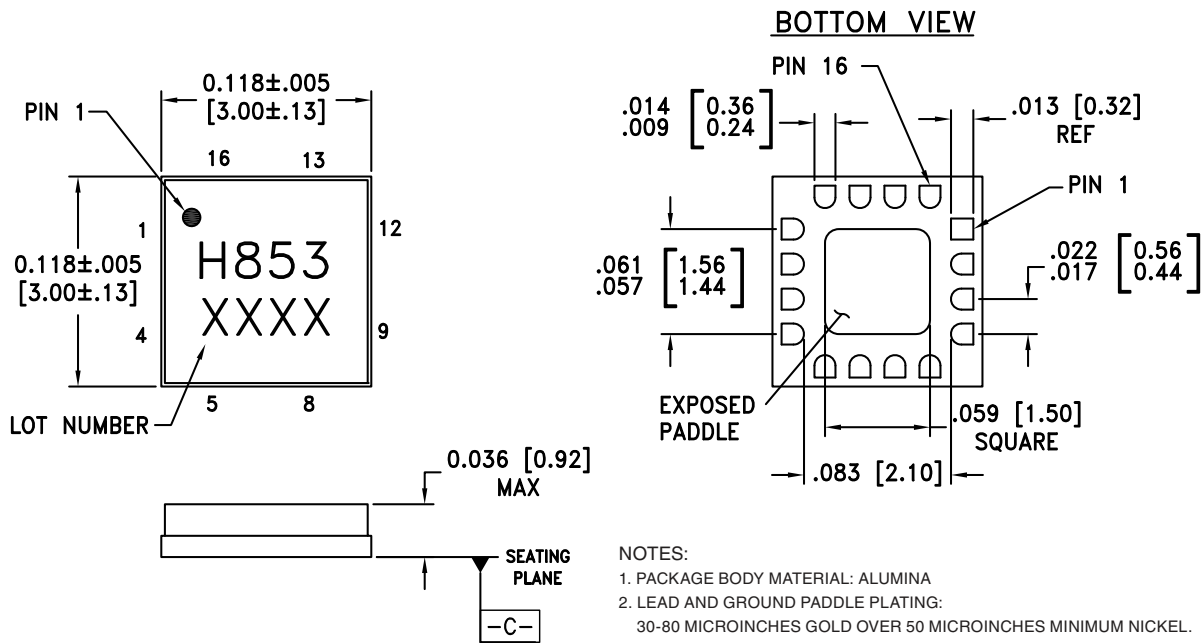
Absolute Maximum Ratings

| | |
|---|-------------------|
| Power Supply Voltage (Vee) | -3.75 V to +0.5 V |
| Input Signals | -2 V to +0.5 V |
| Output Signals | -1.5 V to +1 V |
| Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C) | 0.68 W |
| Thermal Resistance (R _{th(j-p)}) Worst Case Junction to Package Paddle | 59 °C/W |
| Maximum Junction Temperature | 125 °C |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 °C to +85 °C |
| ESD Sensitivity (HBM) | Class 1C |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



- NOTES:
- PACKAGE BODY MATERIAL: ALUMINA
 - LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
 - DIMENSIONS ARE IN INCHES [MILLIMETERS].
 - LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
 - PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
 - ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
 - PADDLE MUST BE SOLDERED TO Vee.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[2] |
|-------------|-----------------------|------------------|---------------------|--------------------------------|
| HMC853LC3 | Alumina, White | Gold over Nickel | MSL3 ^[1] | H853 XXXX |


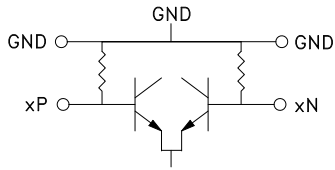
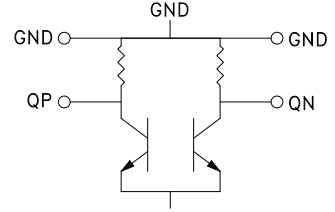

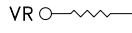
[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX



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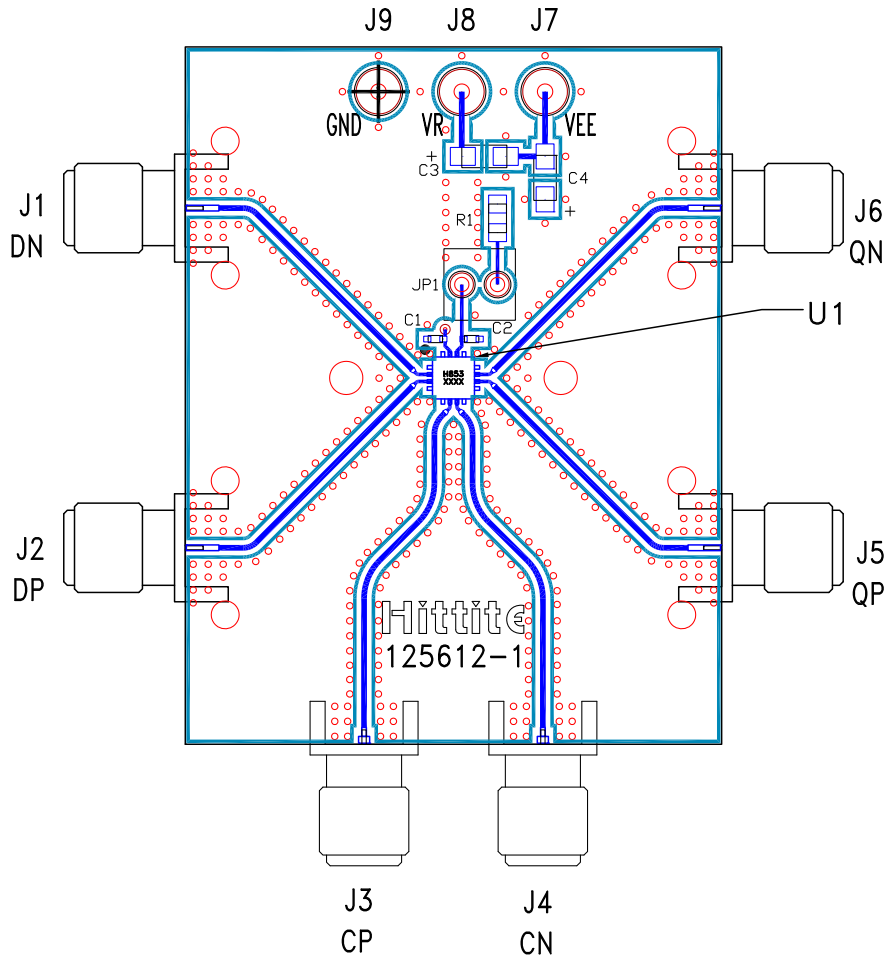
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|-------------------|------------------|---|---|
| 1, 4, 5, 8, 9, 12 | GND | Signal Grounds |  |
| 2, 3 6, 7 | DN, DP CP, CN | Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply |  |
| 10, 11 | QP, QN | Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply. |  |
| 13, 16 | GND | Supply Ground |  |
| 14 | VR | Output level control. Output level may be increased or decreased by applying a voltage to VR per "Output Differential vs. VR" plot. |  |
| 15, Package Base | Vee | This pin and the exposed paddle must be connected to the negative voltage supply. | |



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Evaluation PCB



List of Materials for Evaluation PCB 125614 [1]

| Item | Description |
|---------|--|
| J1 - J6 | PCB Mount K RF Connectors |
| J7 - J9 | DC Pin |
| C1, C2 | 100 pF Capacitor, 0402 Pkg. |
| C3, C4 | 4.7 μF Capacitor, Tantalum |
| R1 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC853LC3 High Speed Logic, D-Type Flip-Flop |
| PCB [2] | 125612 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.



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Application Circuit

