MC34151, MC33151

High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual−in−line and surface mount packages.

Features

- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026
- These are Pb−Free and Halide−Free Devices

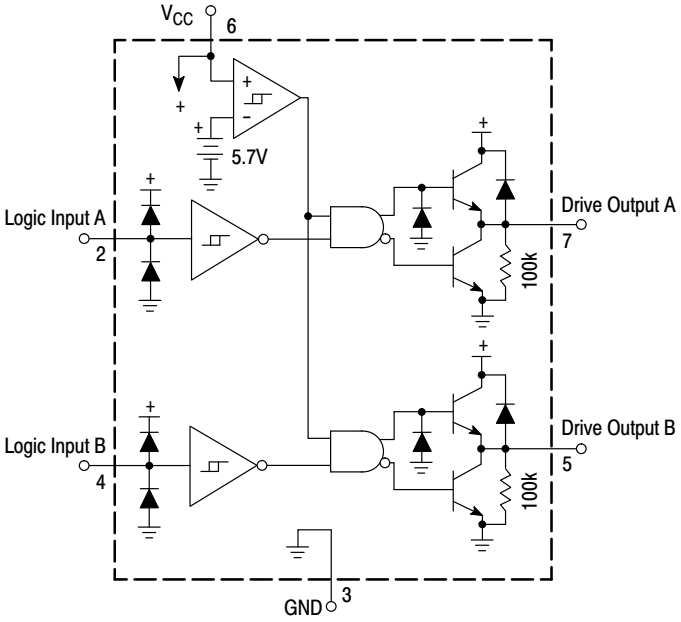
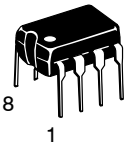


Figure 1. Representative Block Diagram

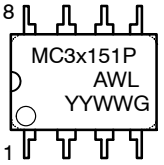
ON Semiconductor®

http://onsemi.com

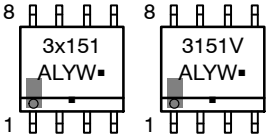
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626



SOIC−8
D SUFFIX
CASE 751

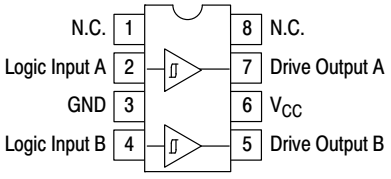


MC3x151 **MC33151V**

x	= 3 or 4
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	−0.3 to V_{CC}	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	 I_O $I_{O(clamp)}$	 1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix SOIC−8 Package Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air P Suffix 8−Pin Package Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34151 MC33151 MC33151V	T_A	 0 to +70 −40 to +85 −40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Electrostatic Discharge Sensitivity (ESD) (Note 3) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	 2000 200 1500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. ESD protection per JEDEC Standard JESD22−A114−F for HBM
   per JEDEC Standard JESD22−A115−A for MM
   per JEDEC Standard JESD22−C101D for CDM.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage – Output Transition High to Low State	V_{IH}	–	1.75	2.6	V
Output Transition Low to High State	V_{IL}	0.8	1.58	–	
Input Current – High State (V_{IH} = 2.6 V)	I_{IH}	–	200	500	μA
– Low State (V_{IL} = 0.8 V)	I_{IL}	–	20	100	
DRIVE OUTPUT					
Output Voltage – Low State (I_{Sink} = 10 mA)	V_{OL}	–	0.8	1.2	V
(I_{Sink} = 50 mA)		–	1.1	1.5	
(I_{Sink} = 400 mA)		–	1.7	2.5	
– High State (I_{Source} = 10 mA)	V_{OH}	10.5	11.2	–	
(I_{Source} = 50 mA)		10.4	11.1	–	
(I_{Source} = 400 mA)		9.5	10.9	–	
Output Pulldown Resistor	R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	–	35	100	
Logic Input to Drive Output Fall	$t_{PHL(in/out)}$	–	36	100	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	14	30	ns
C_L = 2.5 nF		–	31	–	
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	16	30	ns
C_L = 2.5 nF		–	32	–	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		–	6.0	10	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)		–	10.5	15	
Operating Voltage	V_{CC}	6.5	–	18	V

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151 T_{high} = +70°C for MC34151
   −40°C for MC33151 +85°C for MC33151

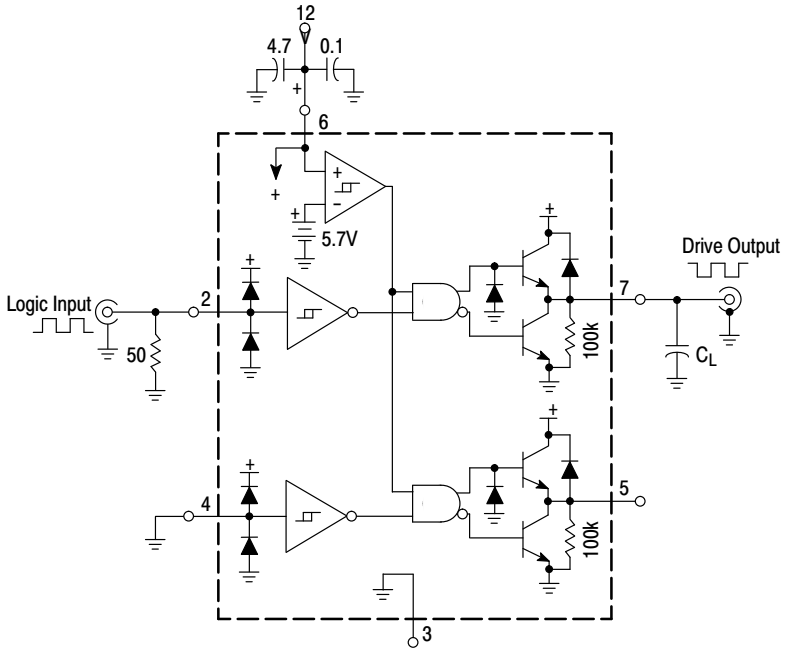


Figure 2. Switching Characteristics Test Circuit

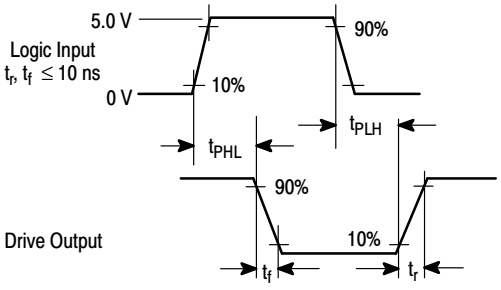


Figure 3. Switching Waveform Definitions

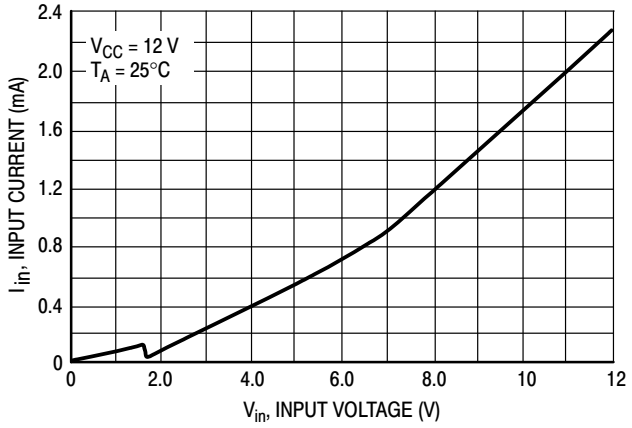


Figure 4. Logic Input Current versus Input Voltage

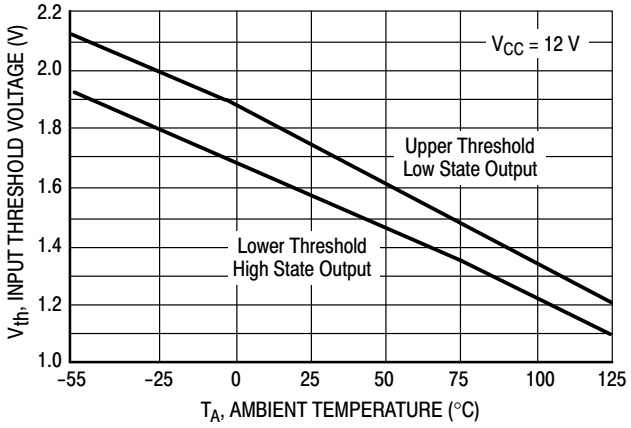


Figure 5. Logic Input Threshold Voltage versus Temperature

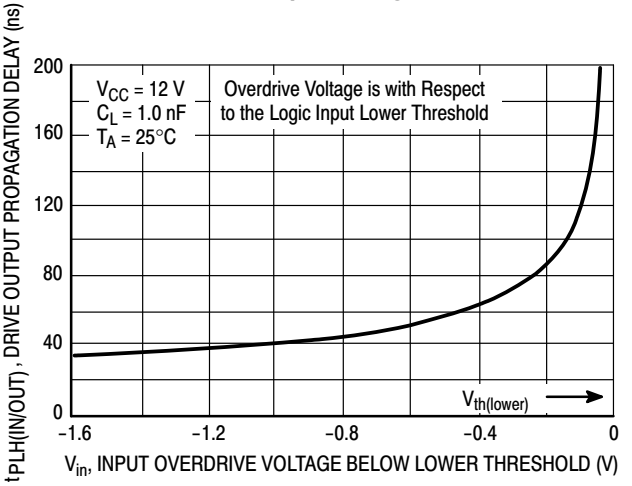


Figure 6. Drive Output Low−to−High Propagation Delay versus Logic Overdrive Voltage

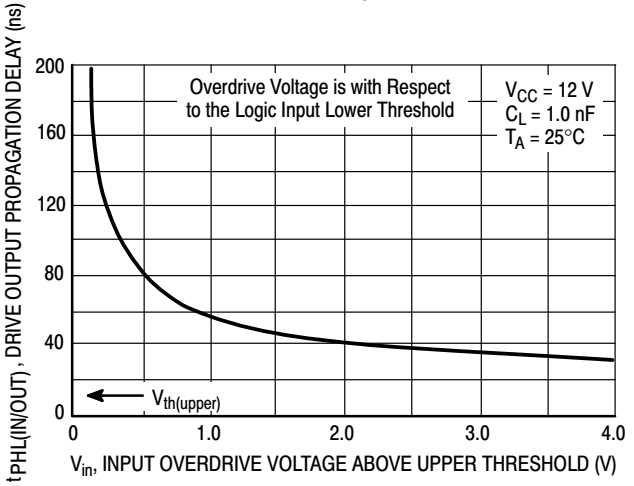


Figure 7. Drive Output High−to−Low Propagation Delay versus Logic Input Overdrive Voltage

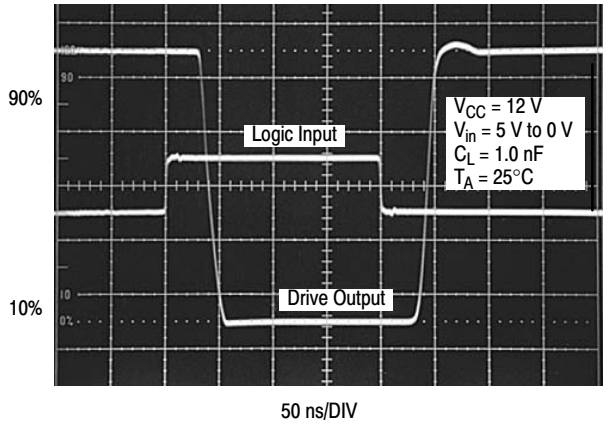


Figure 8. Propagation Delay

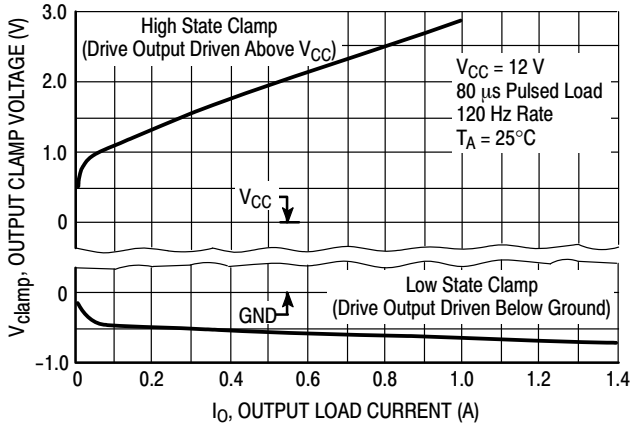


Figure 9. Drive Output Clamp Voltage versus Clamp Current

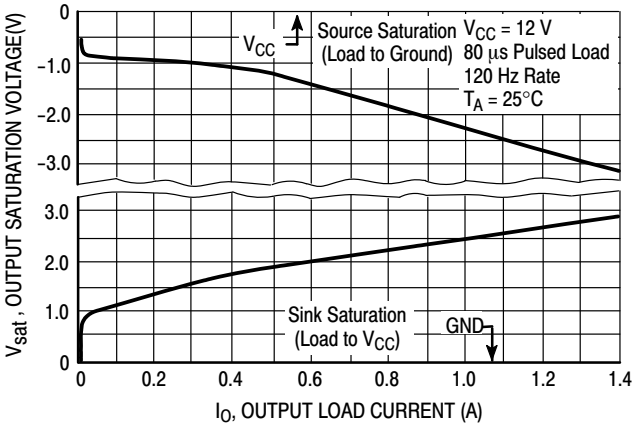


Figure 10. Drive Output Saturation Voltage versus Load Current

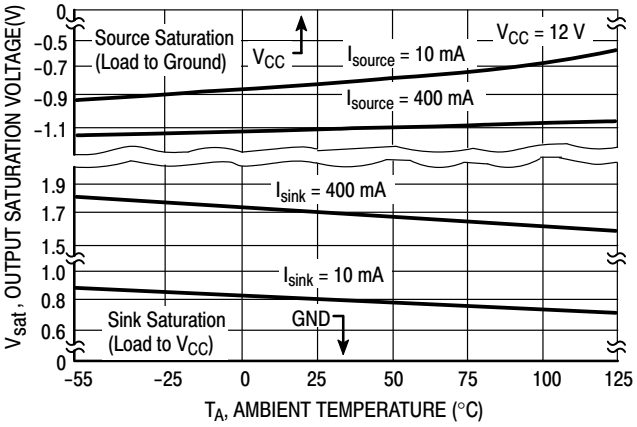


Figure 11. Drive Output Saturation Voltage versus Temperature

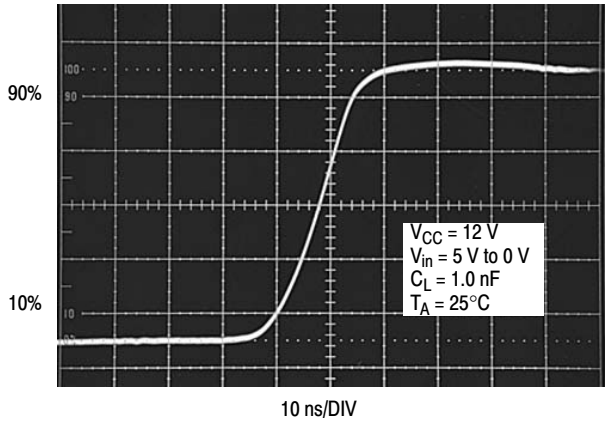


Figure 12. Drive Output Rise Time

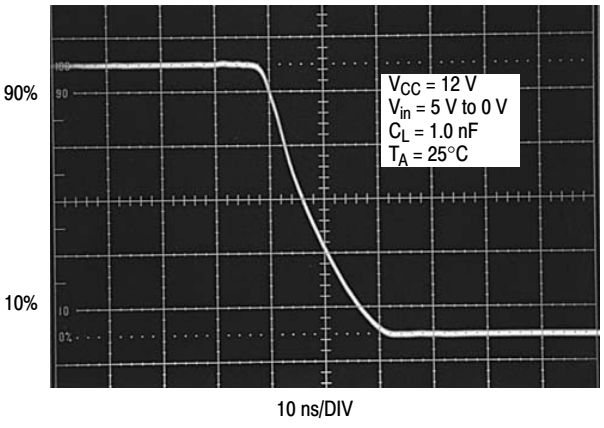


Figure 13. Drive Output Fall Time

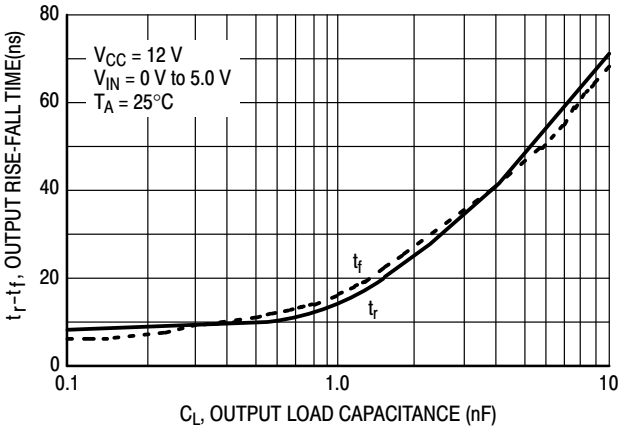


Figure 14. Drive Output Rise and Fall Time versus Load Capacitance

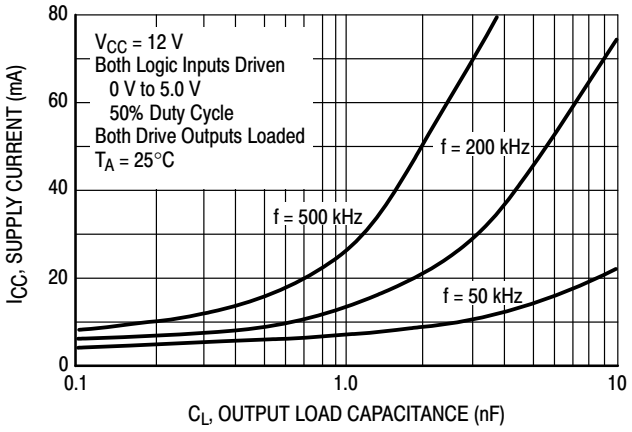


Figure 15. Supply Current versus Drive Output Load Capacitance

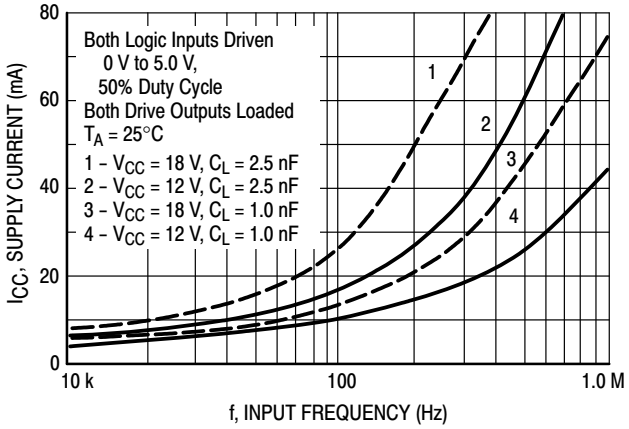


Figure 16. Supply Current versus Input Frequency

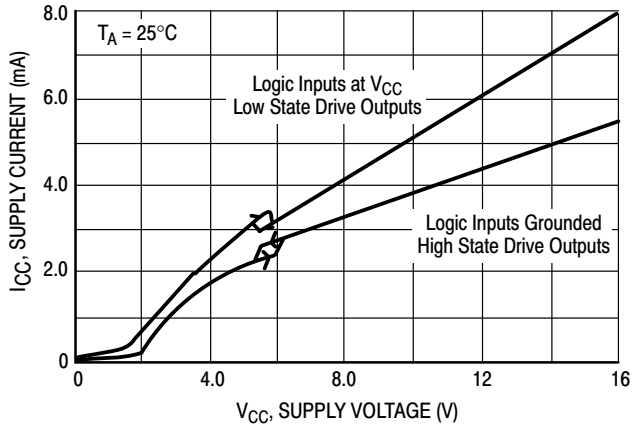


Figure 17. Supply Current versus Supply Voltage

APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master−slave operation. Each input has a 30 kΩ pulldown resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical ‘on’ resistance of 2.4 Ω at 1.0 A. The low ‘on’ resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pulldown resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn−on transition, and below ground during the turn−off transition. With CMOS drivers, this mode of operation can cause a destructive output latchup condition. The MC34151 is immune to output latchup. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pullup transistor. Since full supply voltage is applied across

the NPN pullup during the negative output transient, power dissipation at high frequencies can become excessive. Figures 20, 21, and 22 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where:
T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where:
P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 17. The device's quiescent power dissipation is:

$$P_Q = V_{CC} \left(I_{CCL} (1-D) + I_{CCH} (D) \right)$$

where:
I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where:
V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 18 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

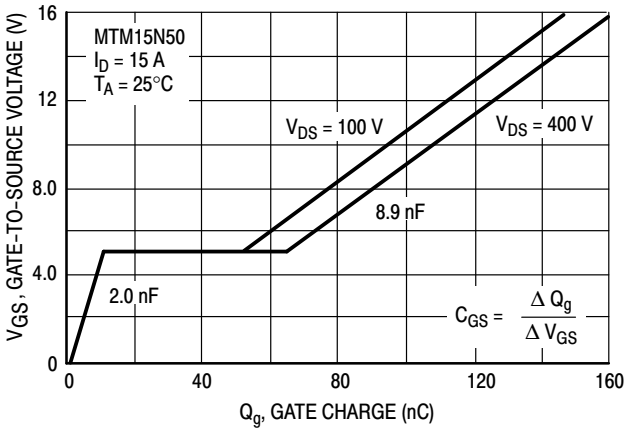


Figure 18. Gate−To−Source Voltage versus Gate Charge

The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_C Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain−to−gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T = V_{CC} (1.08 V_{CC} C_L f - 8 \text{ y } 10^{-4})$$

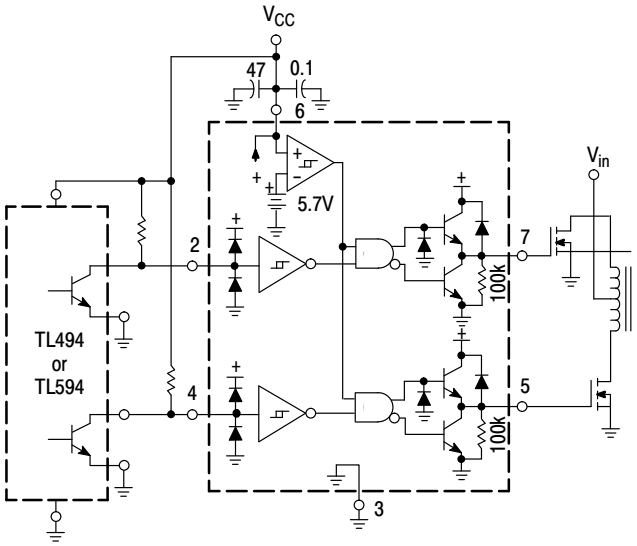
P_T must be greater than zero.

Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 14 shows that for small capacitance loads, the switching speed is limited by transistor turn−on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

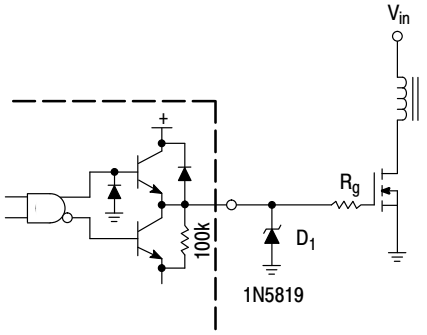
High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.



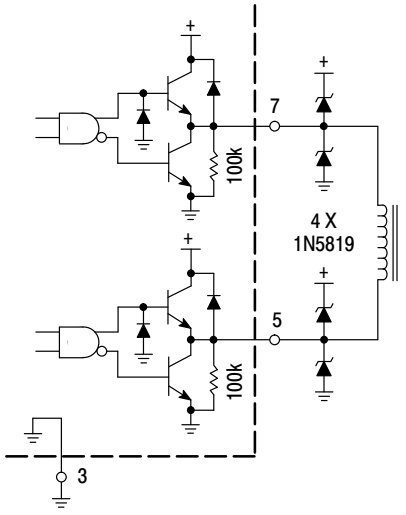
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. Enhanced System Performance with Common Switching Regulators



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. MOSFET Parasitic Oscillations



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Direct Transformer Drive

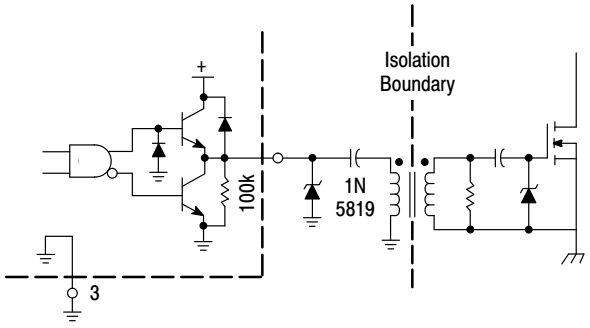
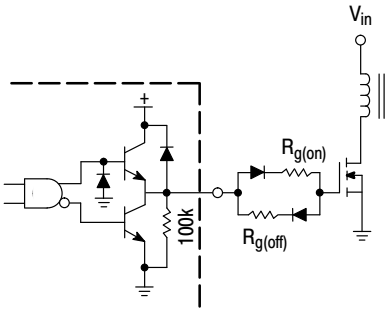
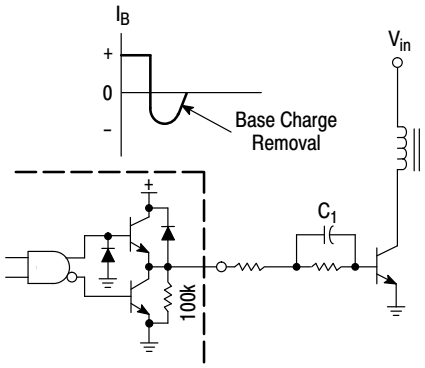


Figure 22. Isolated MOSFET Drive



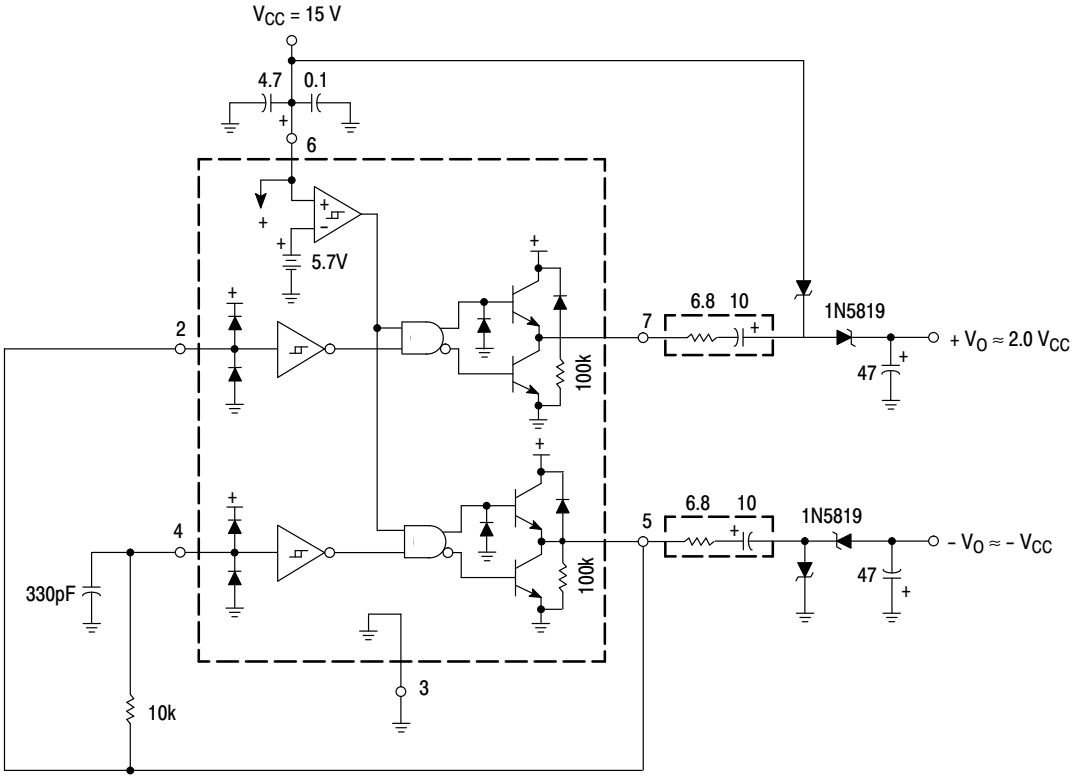
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn−on and turn−off times.

Figure 23. Controlled MOSFET Drive



The totem−pole outputs can furnish negative base current for enhanced transistor turn−off, with the addition of capacitor C_1.

Figure 24. Bipolar Transistor Drive



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figure 25. Dual Charge Pump Converter

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	−13.3
1.0	27.4	−12.9
10	26.4	−11.9
20	25.5	−11.2
30	24.6	−10.5
50	22.6	−9.4

ORDERING INFORMATION

Device	Package	Shipping†
MC34151DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC34151DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MC34151PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33151DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33151DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
MC33151PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33151VDR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

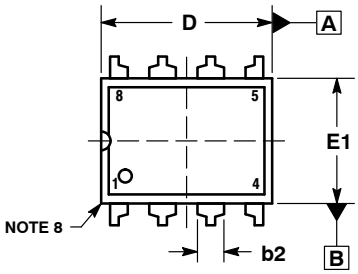
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

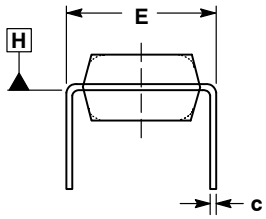
PDIP–8
CASE 626–05
ISSUE P

DATE 22 APR 2015

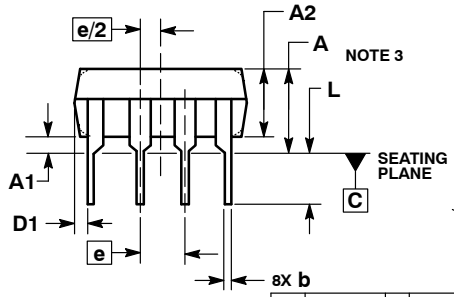
SCALE 1:1



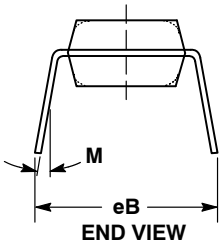
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



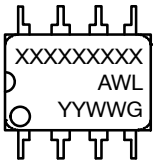
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98ASB42420B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**PDIP–8**	**PAGE 1 OF 1**

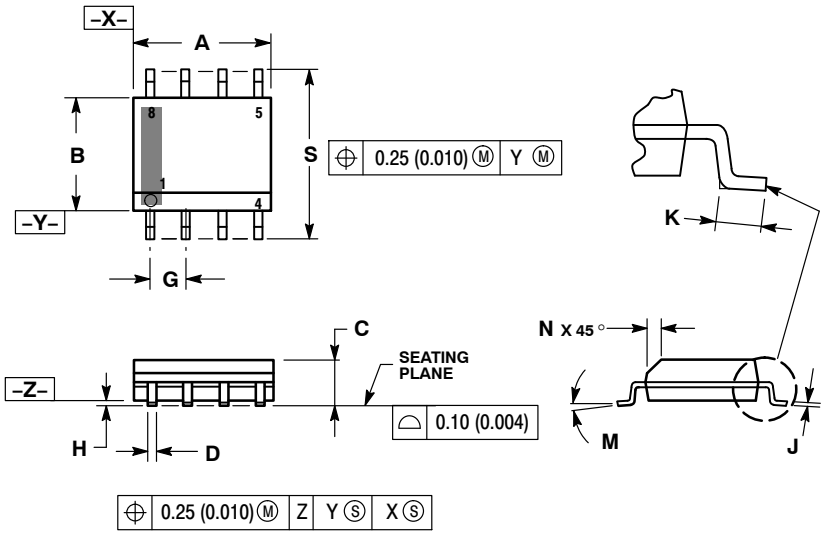
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

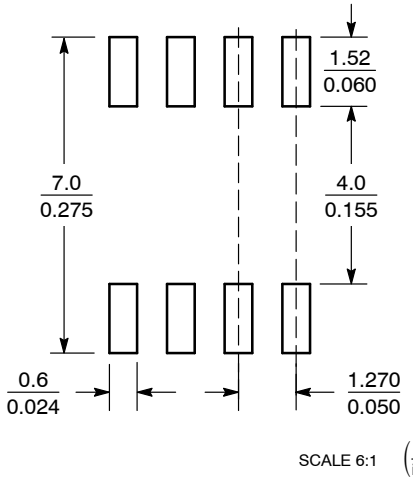
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

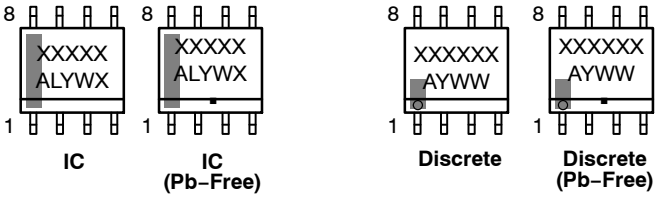
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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