1A, Single-Input, Single Cell Li-Ion Battery Charger with 50-mA LDO, External Power Path Control, and Single Input Interface

Check for Samples: bq25050

FEATURES

- **30V input Rating, With 10.5V Over-Voltage Protection (OVP)**
- **FET Controller for External Battery FET for External Power Path Control (BGATE)**
- **Input Voltage Dynamic Power Management**
- **50mA integrated Low Dropout Linear Regulator (LDO)**
- **Programmable Charge Current Through Single Input Interface (CTRL)**
- **0.5% Battery Voltage Regulation Accuracy**
- **7% Charge Current Regulation Accuracy**
- **Thermal Regulation and Protection**
- **Battery NTC Monitoring During Charge and Discharge**
- **Status Indication – Charging/Done and Temperature Faults**
- **Available in small 2mm × 3mm 10 Pin SON Package**

APPLICATIONS

- **Smart Phones**
- **Mobile Phones**
- **Portable Media Players**
- **Low Power Handheld Devices**
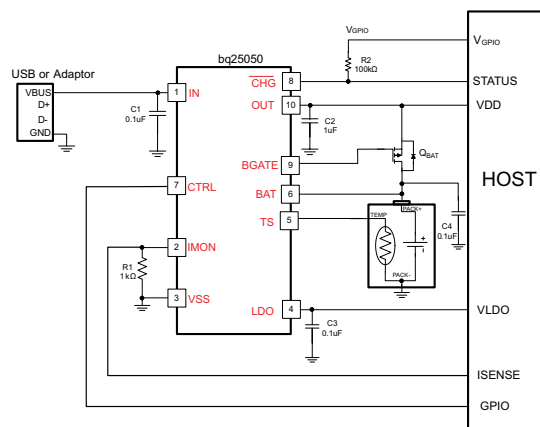
DESCRIPTION

The bq25050 is a highly integrated Li-Ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell Li-Ion battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The bq25050 has a single power output that charges the battery. The system load is connected to OUT. The low-battery system startup circuitry maintains OUT greater than 3.4V whenever an input source is connected. This allows the system to start-up and run whenever an input source is connected regardless of the battery voltage. The charge current is programmable up to 1A using the CTRL input. Additionally, a 4.9V 50mA LDO is integrated into the IC for supplying low power external circuitry.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination.

TYPICAL APPLICATION CIRCUIT

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NO.	MARKING	MEDIUM	QUANTITY
bq25050DQCR	DAM	Tape and Reel	3000
bq25050DQCT	DAM	Tape and Reel	250

PACKAGE DISSIPATION RATINGS TABLE

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	$T_A < 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$
10 Pin 2mm × 3mm SON[1]	58.7°C/W[2]	3.9°C/W	1.70W	0.017W/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = $[T_{J(max)} - T_A]/R_{\theta JA}$.
(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2×3 via matrix.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
Input Voltage	IN (with respect to VSS)	−0.3 to 30 V
	CTRL, TS, $\overline{CHG}$, BGATE (with respect to VSS)	−0.3 to 7 V
Output Voltage	BAT, OUT, LDO, $\overline{CHG}$, BGATE, IMON (with respect to VSS)	−0.3 to 7 V
Input Current (Continuous)	IN	1.2 A
Output Current (Continuous)	BAT	1.2 A
Output Current (Continuous)	LDO	100 mA
Output Sink Current	$\overline{CHG}$	5 mA
Junction temperature, T_J		−40°C to 150°C
Storage temperature, T_{STG}		−65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	3.55	28	V
	IN operating voltage range	4.4	10.2	
I_{IN}	Input current, IN		1	A
I_{OUT}	Ouput Current in charge mode, OUT		1	A
T_J	Junction Temperature	0	125	°C

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{UVLO}	Under-voltage lock-out	V_{IN}: 0V → 4V	3.25	3.30	3.55	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{IN}: 4V → 0V		250		mV

Product Folder Link(s): *bq25050*

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T$_J$ ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V$_{BATUVLO}$	Battery UVLO	V$_{BAT}$ rising	1.95	2.05	2.15	V
V$_{HYS-BUVLO}$	Hysteresis on BAT UVLO	V$_{BAT}$ falling		125		mV
V$_{IN-SLP}$	Valid input source threshold V$_{IN-SLP}$ above V$_{BAT}$	Input power good if V$_{IN}$ > V$_{BAT}$ + V$_{IN–SLP}$ V$_{BAT}$ = 3.6V, V$_{IN}$: 3.5V → 4V	30	75	150	mV
V$_{HYS-INSLP}$	Hysteresis on V$_{IN-SLP}$	V$_{BAT}$ = 3.6V, V$_{IN}$: 4V → 3.5V		32		mV
t$_{DGL(NO-IN)}$	Deglitch time, input power loss to charger turn-off	Time measured from V$_{IN}$: 5V → 2.5V 1μs fall-time		32		ms
V$_{OVP}$	Input over-voltage protection threshold	V$_{IN}$: 5 V → 11 V	10.2	10.5	10.8	V
V$_{HYS-OVP}$	Hysteresis on OVP	V$_{IN}$: 11 V → 5 V		100		mV
t$_{DGL(OVP)}$	Input over-voltage deglitch time			100		μs
t$_{REC(OVP)}$	Input over-voltage recovery time	Time measured from V$_{IN}$: 11V → 5V 1μs fall-time to LDO = HI, V$_{BAT}$ = 3.5V		100		μs
V$_{IN\_DPM}$	Input DPM threshold	V$_{IN}$ Falling, V$_{IN}$-DPM enabled with CTRL	4.2	4.30	4.4	V
QUIESCENT CURRENT						
I$_{BAT(PDWN)}$	Battery current into BAT, No input connected	V$_{IN}$ = 0V, V$_{\overline{CHG}}$ = High, TS Enabled		120	150	μA
		V$_{IN}$ = 0V, V$_{\overline{CHG}}$ = Low, TS Disabled, T$_J$ = 85°C			6	μA
I$_{BAT(DONE)}$	BAT current, charging terminated	V$_{IN}$ = 6V, V$_{BAT}$ > V$_{BAT(REG)}$			10	μA
I$_{IN(STDBY)}$	Standby current into IN pin	CTRL = HI, V$_{IN}$ < VOVP			0.5	mA
		CTRL = HI, V$_{IN}$ ≥ VOVP			2	
I$_{CC}$	Active supply current, IN pin	V$_{IN}$ = 6V, no load on OUT pin, V$_{BAT}$ > V$_{BAT(REG)}$, IC enabled			3	mA
BATTERY CHARGER FAST-CHARGE						
V$_{BAT(REG)}$	Battery charge regulation voltage	T$_A$ = 0°C to 125°C, I$_{OUT}$ = 50 mA	4.16	4.20	4.23	V
		T$_A$ = 25°C	4.179	4.200	4.221	
I$_{IN(LIM)}$	Input current limit (selected by CTRL interface)	4 pulses on CTRL	87	93	100	mA
		5 pulses on CTRL	174	187	200	
		6 pulses on CTRL	261	280	300	
		7 pulses on CTRL	348	374	400	
		8 pulses on CTRL	435	467	500	
		9 pulses on CTRL	608	654	700	
		10 pulses on CTRL	739	794	850	
		11 pulses on CTRL	864	935	1000	
V$_{DO(IN-OUT)}$	V$_{IN}$ − V$_{OUT}$	V$_{IN}$ = 4.2V, I$_{OUT}$ = 0.75 A		500	900	mV
K$_{IMON}$	Input current monitor ratio	K$_{IMON}$ = I$_{IMON}$ / I$_{CHG}$, R$_{IMON}$ = 1kΩ, Current programmed using CTRL		1		mA/A
V$_{IMON(MAX)}$	Maximum IMON voltage	IMON open		1.2	1.25	V
	IMON Accuracy	25 mA < I$_{IN}$ < 100 mA	−25%		25%	
		I$_{IN}$ = 100 mA to 1 A	−8.5%		5%	
PRE-CHARGE AND CHARGE DONE						
V$_{LOWV}$	Pre-charge to fast-charge transition threshold	External power path control disabled, BGATE = VSS	2.4	2.5	2.6	V
		External power path control enabled	2.8	2.9	3.0	
t$_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
t$_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I$_{PRECHARGE}$	Precharge current to BAT during precharge mode	V$_{BAT}$ = 0V to 2.9V, Battery FET connected	28	37	45	mA
		V$_{BAT}$ = 0V to 2.5V, BGATE = VSS, Input current limit regulated to I$_{PRECHARGE}$	41.5	45	48.5	
I$_{TERM}$	Default termination current threshold	V$_{IN}$ = 5V, I$_{CHARGE}$ = 100 mA to 1 A	7.5	10.5	13.5	%I$_{CHG}$
RECHARGE OR REFRESH						
V$_{RCH}$	Recharge detection threshold	V$_{BAT}$ falling	V$_{BAT(REG)}$ −0.13V	V$_{BAT(REG)}$ −0.1V	V$_{BAT(REG)}$ −0.065V	V

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			25		ms
EXTERNAL POWER PATH CONTROL						
$V_{OUT(REG)}$	Output regulation voltage	V_{BAT} ≤ 2.9 V	3.4	3.5	3.6	V
		2.9 V < V_{BAT} ≤ 3.6V	3.44	3.59	3.75	V
		V_{BAT} > 3.6 V		V_{BAT} + $V_{drop(QBAT)}$		V
V_{SUPP1}	Enter supplement mode threshold	V_{BAT} = 3.4 V, V_{OUT} Falling		V_{OUT} ≤ V_{BAT} -60mV		V
V_{SUPP2}	Exit supplement mode threshold	V_{BAT} = 3.4 V, V_{OUT} Rising		V_{OUT} ≥ V_{BAT}-20mV		V
LDO						
V_{LDO}	LDO Output Voltage	V_{IN} = 5.5V, I_{LDO} = 0mA to 50mA	4.	4.9	5.1	V
I_{LDO}	Maximum LDO Output Current		60			mA
V_{DO}	Dropout Voltage	V_{IN} = 4.5V, I_{LDO} = 50mA		200	300	mV
CTRL INTERFACE						
$t_{CTRL-DGL}$	CTRL Deglitch timer		5			ms
$t_{CTRL-LATCH}$	CTRL Latch timer		2			ms
$t_{CTRL-HIGH}$	High Duration on CTRL		50		1000	µs
$t_{CTRL-LOW}$	Low Time Duration on CTRL		50		1000	µs
$R_{PULLDOWN}$	CTRL Pulldown Resistor			260		kΩ
LOGIC LEVELS ON CTRL, $\overline{CHG}$, BGATE						
V_{IL}	Logic LOW input voltage				0.4	V
V_{IH}	Logic HIGH input voltage		1.4			V
BATTERY-PACK NTC MONITOR (TS)						
V_{TS_CLAMP}	Maximum TS Voltage				1.5	V
I_{TS-0C}	Current source for 0°C TS sensing		3.75	4	4.25	µA
I_{TS}	Current source for 45°C and 60°C TS sensing		19	20	21	µA
V_{COLD}	TS Cold Threshold, when BGATE is disabled	V_{TS} < V_{COLD} to begin charge (Corresponds to 0°C, 2°C, 4°C[1] [2])	0.55	0.575	0.600	V
V_{CUTOFF_0}	TS Cold Cutoff Threshold	Temp falling (Corresponds to −1°C, 1°C, 3°C[1] [2])	0.575	0.600	0.625	V
V_{HOT_45}	TS Hot Threshold (0°C to 45°C), when BGATE is disabled	V_{TS} > V_{HOT_45} to begin charge, 0°C to 45°C thresholds selected. (Corresponds to 40°C, 42°C, 44°C[1] [2])	0.44	0.45	0.46	V
V_{CUTOFF_45}	TS Hot Cutoff Threshold (0°C to 45°C)	Temp rising (Corresponds to 45°C, 47°C, 49°C[1] [2])	0.365	0.375	0.385	V
V_{HOT_60}	TS Hot Threshold (0°C to 60°C), when BGATE is disabled	V_{TS} > V_{HOT_60} to begin charge, 0°C to 60°C thresholds selected, Temp rising (Corresponds to 54.5°C, 57°C, 60°C[1] [2])	0.240	0.250	0.258	V
V_{CUTOFF_60}	TS Hot Cutoff Threshold (0°C to 60°C)	Temp rising. (Corresponds to 58.5°C, 61.5°C, 64°C[1] [2])	0.204	0.213	0.223	V
V_{-20}	−20°C TS Voltage	See [1]		0.968		V
V_{80}	+80°C TS Voltage	See [1]		0.110		V
$t_{dgl(TS)}$	Deglitch for TS Fault	Fault detected on TS to stop charge		25		ms
$\overline{CHG}$ OUTPUT						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.45	V
I_{IH}	Leakage current	$V_{/CHG}$ = 5 V			1	µA
$t_{FLSH(TS)}$	TS fault flash period	50% Duty Cycle, TS out of valid range		100		ms
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit	T_J rising		125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C

(1) Information is based on using the NCP15WB473F NTC thermistor.
(2) Temperature references give design guidance only, actual absolute temperatures are **not** guaranteed.
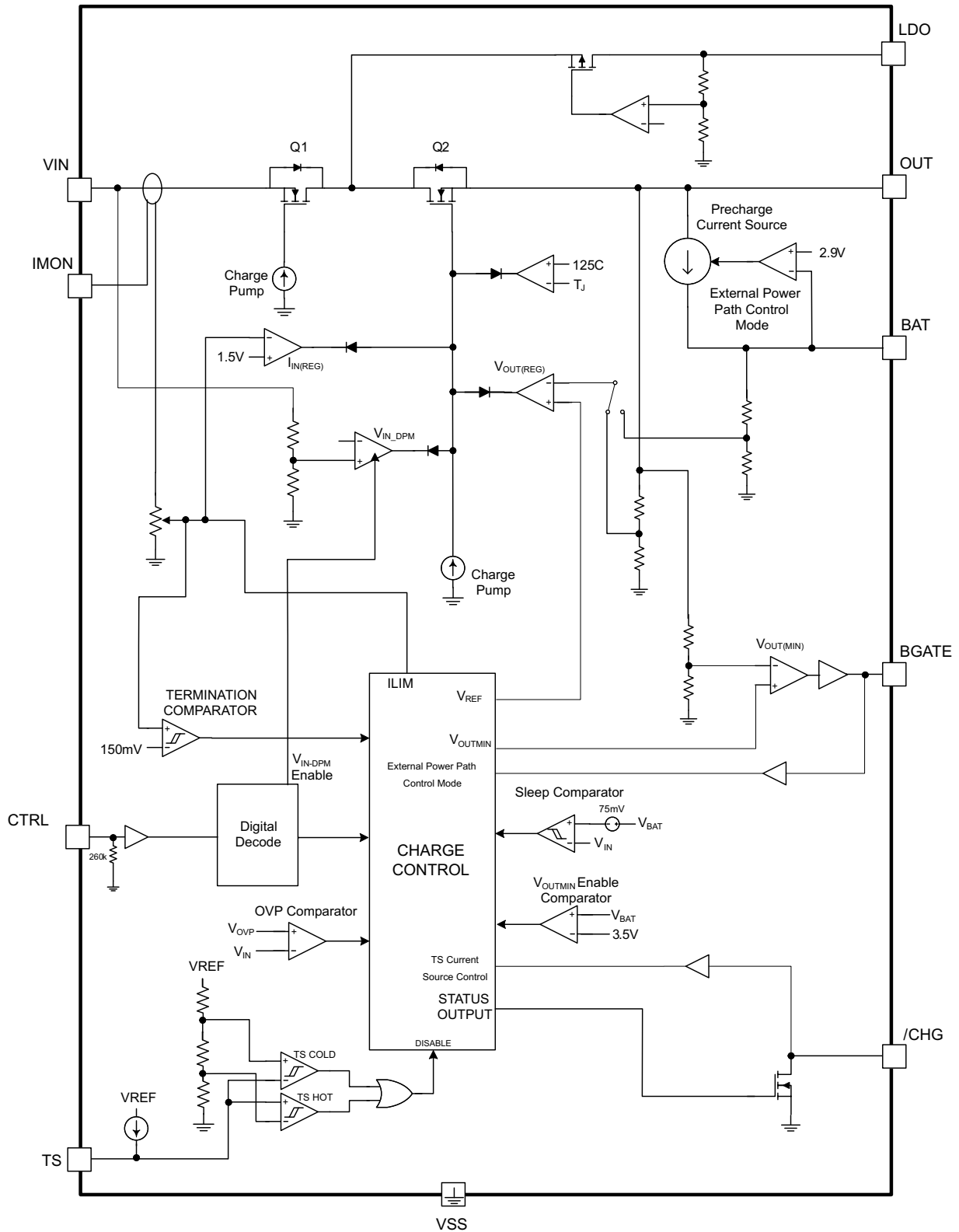
ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	T_J falling		20		°C

DEVICE INFORMATION

SIMPLIFIED BLOCK DIAGRAM

PIN CONFIGURATION

```
                    ┌─────────────────────┐
              IN ──┤ 1               10 ├── OUT
            IMON ──┤ 2                9 ├── BGATE
             VSS ──┤ 3                8 ├── CHG
                   │     bq25050          │
             LDO ──┤ 4                7 ├── CTRL
              TS ──┤ 5                6 ├── BAT
                    └─────────────────────┘
```

10-pin 2mm x 3mm SON

PIN FUNCTIONS

PIN NAME	NO.	I/O	DESCRIPTION
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to VSS with at least a 0.1µF ceramic capacitor.
IMON	2	O	Current monitoring output. Connect a 1kΩ resistor from IMON to VSS to monitor the input current. The voltage at IMON ranges from 0V to 1V which corresponds to an input current from 0A to 1A.
VSS	3	–	Ground terminal. Connect to the thermal pad and the ground plane of the circuit.
LDO	4	O	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO to VSS with a 0.1µF ceramic capacitor. LDO is enabled when $V_{UVLO} < V_{IN} < V_{OVP}$.
TS	5	I	Battery pack NTC monitoring input. Connect the battery pack 47-kΩ NTC from TS to VSS to monitor battery pack temperature. The default pack temperature range is 0°C to 45°C thresholds.
CTRL	7	I	Single-input interface Input. Drive CTRL with pulses to enable/disable the device, enable/disable V_{IN}-DPM, select battery temperature range and select current limits. See the interface section for details on using the CTRL interface.
CHG	8	I/O	Charge status indicator open-drain output. CHG is pulled low while the device is charging the battery. CHG goes high impedance when the battery is fully charged and does not indicate subsequent recharge cycles. CHG pulses to indicate TS faults.
BAT	6	O	Battery connection output. BAT is the sense input for the battery as well as the precharge current output. Connect BAT to the battery and bypass BAT to VSS with a 0.1µF ceramic capacitor.
BGATE	9	I/O	Battery P-Channel FET gate drive output. Connect BGATE to the gate of the external P-Channel FET that connects the battery to OUT. Connect BGATE to VSS if the external FET is not used. No external capacitor is recommended from BGATE to GND.
OUT	10	O	System output connection. OUT supplies the system with a minimum voltage of 3.4V (min.) to ensure system operation whenever an input adapter is connected regardless of the battery voltage. Bypass OUT to VSS with a 1µF ceramic capacitor.
Thermal PAD	Pad	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

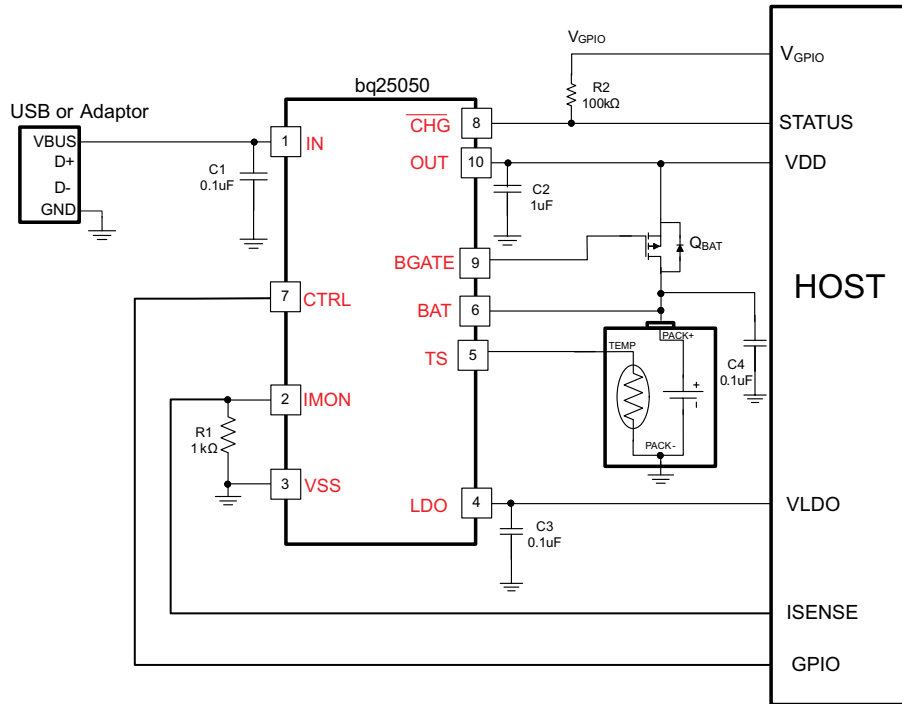## APPLICATION CIRCUITS

Figure 1. Typical Application Circuit Using the External Power Path Control Feature
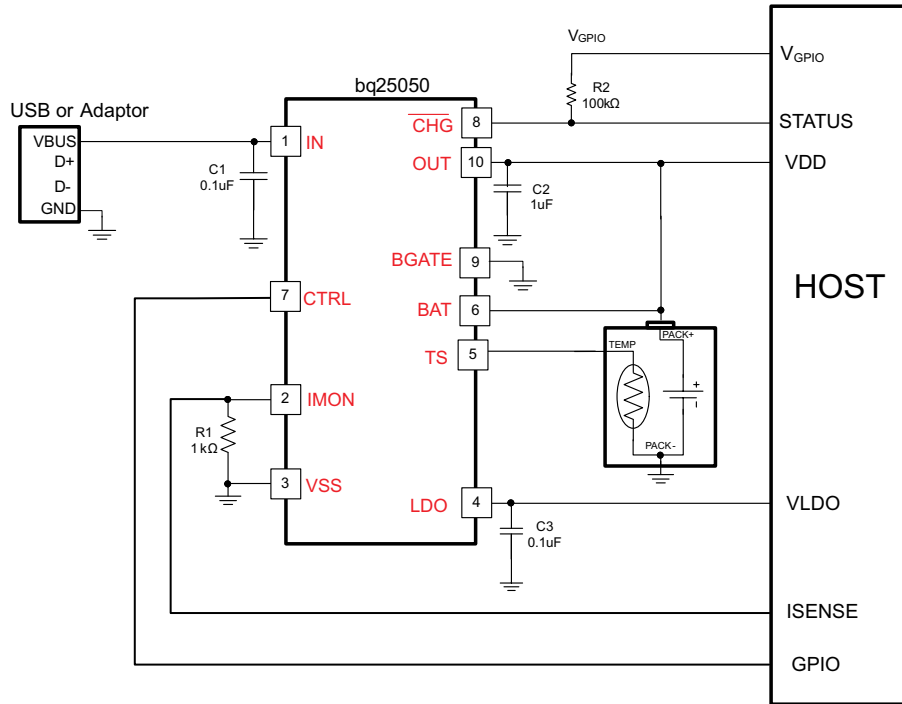

Figure 2. Typical Application Circuit Disabling the External Power Path Control Feature

TYPICAL CHARACTERISTICS

Using circuit in Figure 1, T$_A$ = 25°C, unless otherwise specified

ADAPTER INSERTION

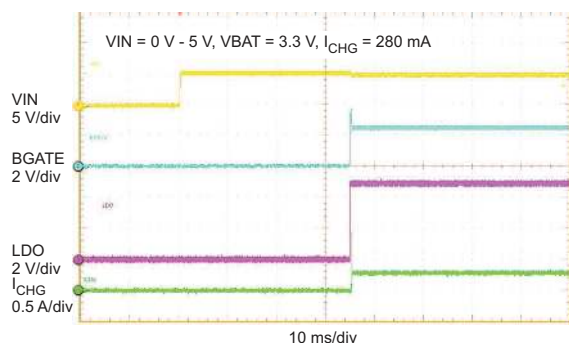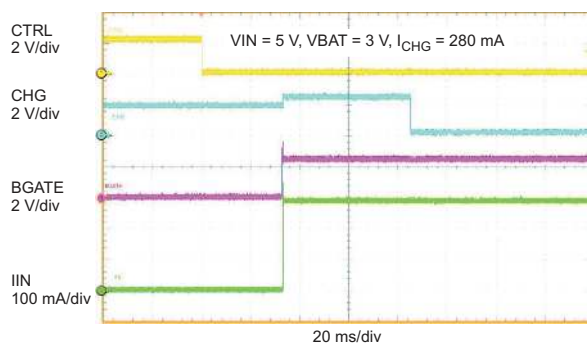

Figure 3.

ENABLE USING CTRL
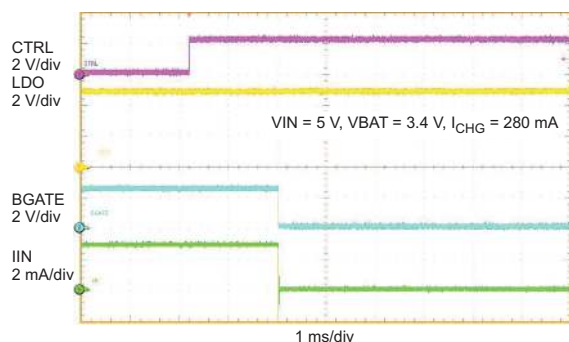

Figure 4.

DISABLE USING CTRL

Figure 5.

CONTROL CURRENT LIMIT - STEP UP
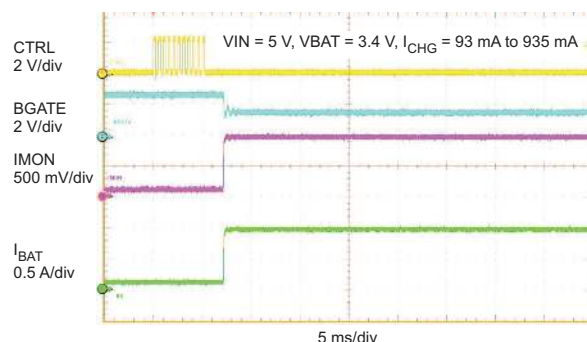
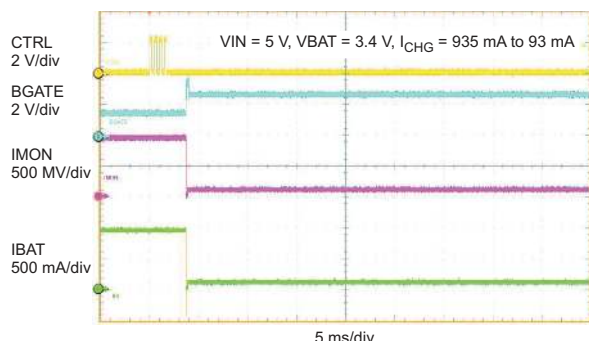**Figure 6.**

CONTROL CURRENT LIMIT - STEP DOWN

Figure 7.

BGATE FORCED ON

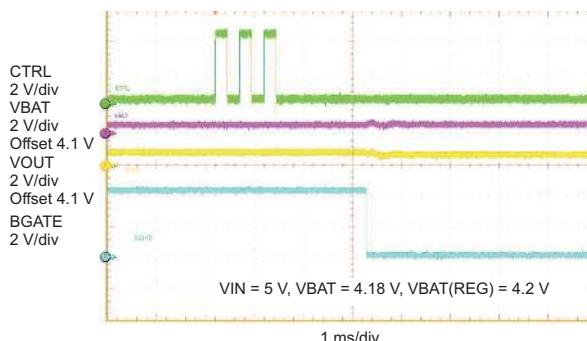**Figure 8.**

TYPICAL CHARACTERISTICS (continued)

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

CANCEL BGATE FORCED ON

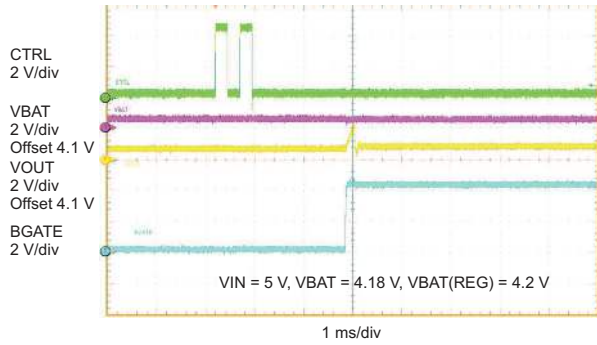VIN = 5 V, VBAT = 4.18 V, VBAT(REG) = 4.2 V

CTRL 2 V/div
VBAT 2 V/div Offset 4.1 V
VOUT 2 V/div Offset 4.1 V
BGATE 2 V/div

1 ms/div

Figure 9.

INPUT OVP

VIN = 5 V to 29 V, VBAT = 3.8 V

VIN 10 V/div
VBAT 2V/div
LDO 2 V/div
IBAT 0.5 A/div

50 µs/div
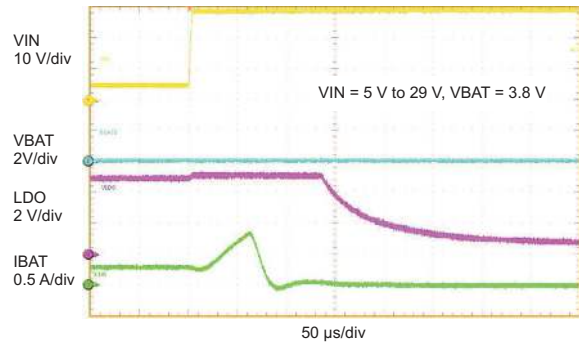
Figure 10.

PRE-CHARGE MODE TO MINIMUM OUTPUT REGULATION MODE

VIN = 5 V, VBAT = 1.8 V to 3.45 V, ICHG = 467 mA

VBAT 500 V/div
IMON 500 mV/div
BGATE 2 V/div
IBAT 500 mA/div

20 ms/div
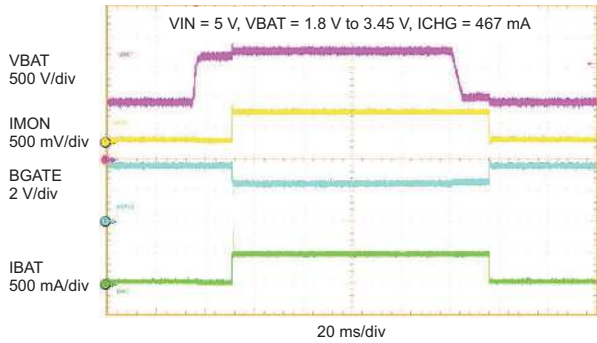
Figure 11.

MINIMUM OUTPUT REGULATION MODE TO CONSTANT CURRENT (CC) MODE

VIN = 5 V, VBAT = 2.4 V to 3.6 V, ICHG = 467 mA

VBAT 500 V/div
IMON 500 mV/div
BGATE 2 V/div
IBAT 500 mA/div

20 ms/div
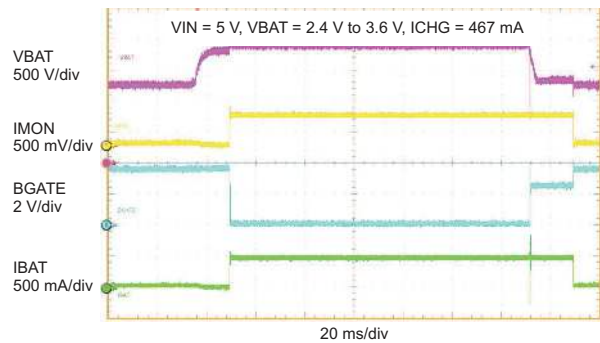
Figure 12.

PRE-CHARGE TO CONSTANT VOLTAGE (CV) MODE
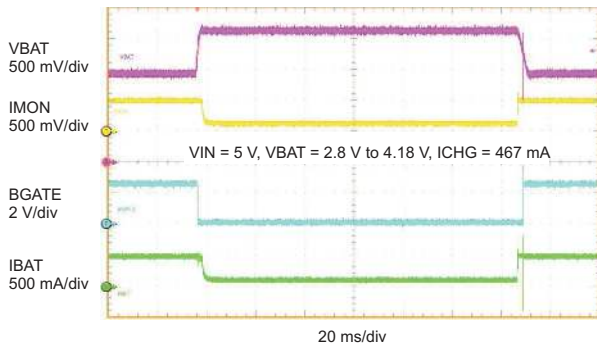
VIN = 5 V, VBAT = 2.8 V to 4.18 V, ICHG = 467 mA

VBAT 500 mV/div
IMON 500 mV/div
BGATE 2 V/div
IBAT 500 mA/div

20 ms/div

Figure 13.

VIN-DPM

VIN = 5 V with current limit of 600 mA, VBAT = 3.2 V, ICHG = 93 mA to 935 mA

VIN 2 V/div
IIN 500 mA/div
IMON 500 mV/div
BGATE 2 V/div

200 µs/div

Figure 14.

Product Folder Link(s): *bq25050*

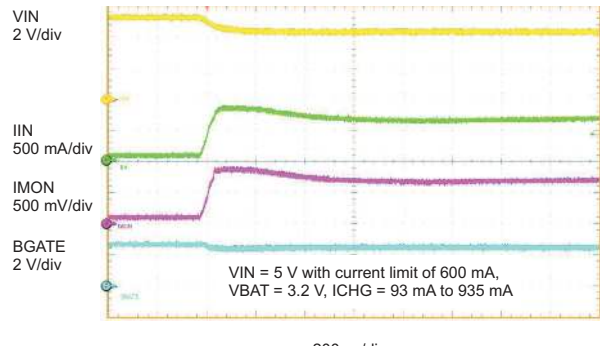## TYPICAL CHARACTERISTICS (continued)

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

SUPPLEMENT MODE

VIN = 5 V, VBAT = 3.2 V,
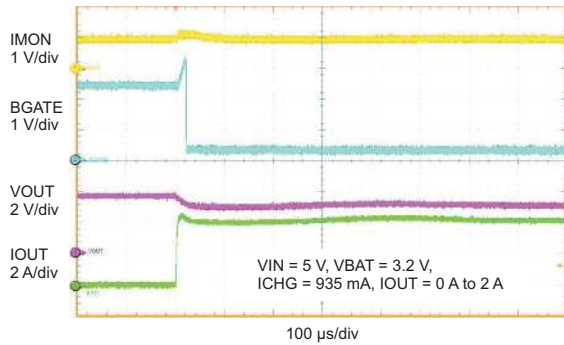ICHG = 935 mA, IOUT = 0 A to 2 A

IMON
1 V/div

BGATE
1 V/div

VOUT
2 V/div

IOUT
2 A/div

100 µs/div

Figure 15.

CHARGE CYCLE DEMO

VIN = 5 V, ICHG = 280 mA,
BGATE =Enabled, CBAT = 2000 µF,
No battery connected,
RDSon from IN to OUT

VOUT
2 V/div

VBAT
2 V/div

IIN
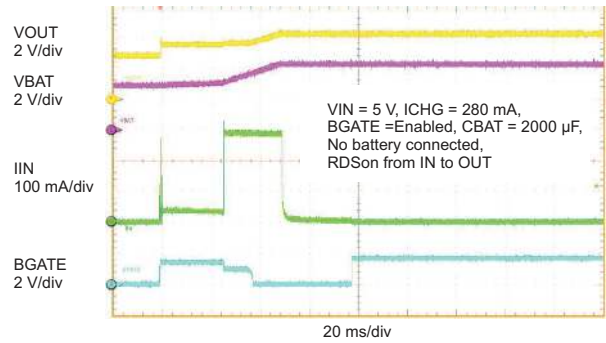100 mA/div

BGATE
2 V/div

20 ms/div

Figure 16.

**BATTERY VOLTAGE
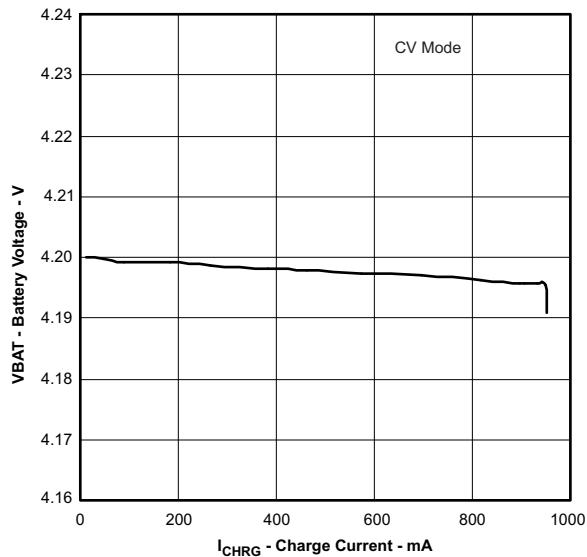vs
CHARGE CURRENT**

Figure 17.

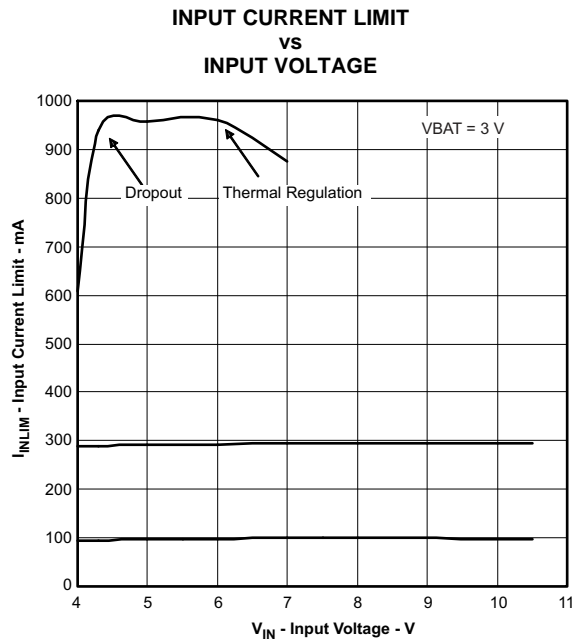**R$_{DSON}$ (From IN to OUT)
vs
JUNCTION TEMPERATURE**
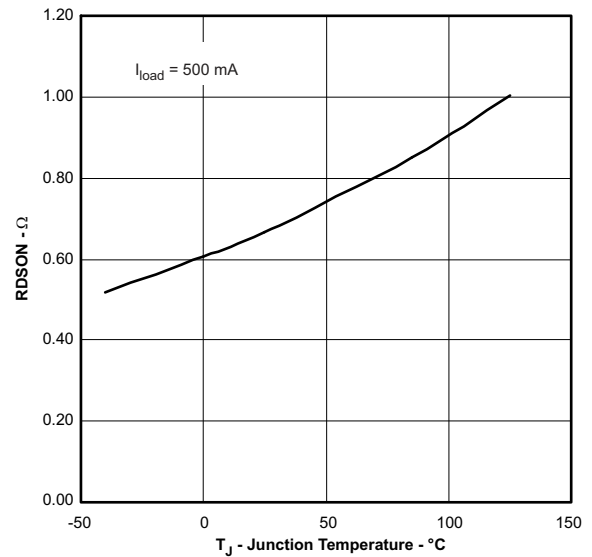
Figure 18.

Product Folder Link(s): bq25050

TYPICAL CHARACTERISTICS (continued)

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

INPUT CURRENT LIMIT
vs
INPUT VOLTAGE

Figure 19.

OUTPUT VOLTAGE
vs
CHARGE CURRENT

Figure 20.
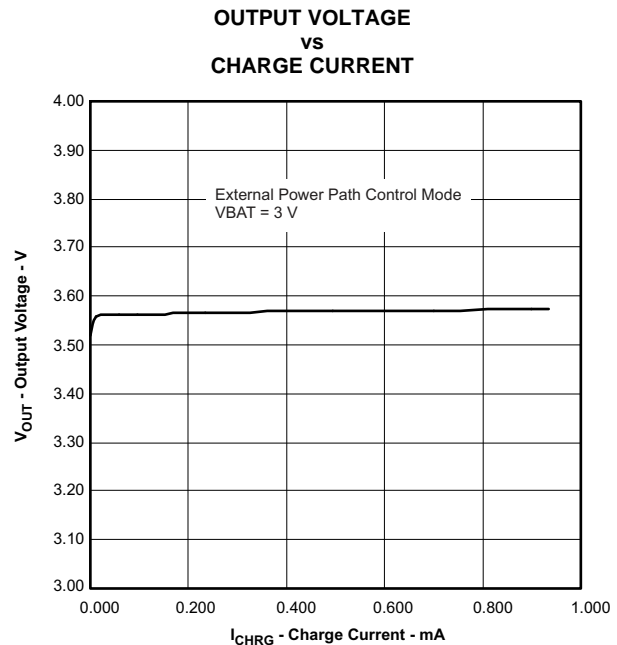
DETAILED FUNCTIONAL DESCRIPTION

The bq25050 is a highly integrated Li-Ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell Li-Ion battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The bq25050 has a single power output that charges the battery. The system load is connected to OUT. The low-battery system startup circuitry maintains OUT pin voltage at $V_{OUT(REG)}$ whenever an input source is connected. This allows the system to start-up and run whenever an input source is connected regardless of the battery voltage. The charge current is programmable up to 1A using the CTRL input. Additionally, a 4.9V 50mA LDO is integrated into the IC for supplying low power external circuitry.

External FET Controller (BGATE)

The External Power Path Control feature is implemented using the BGATE output. BGATE is also used to enable/ disable the External Power Path Control feature. When power is first applied to either V_{BAT} or V_{IN} on the bq25050, the BGATE output is tested. If the BGATE pin is connected to VSS, the External Power Path Control feature is disabled. In order to enable the External Power Path Control feature after it has been disabled, the battery and the input source must be removed and reconnected and BGATE must NOT be connected to VSS.

With External Power Path Control enabled, BGATE is used to drive an external P-channel MOSFET that connects the battery to the system output. This state of this MOSFET is dependant on the battery voltage and the IC status. In discharge mode, BGATE is pulled to GND to turn the MOSFET on fully. During discharge mode, the output is connected directly to the battery. Discharge mode is entered under the following conditions:

1. IC disabled or no input power
2. Supplement mode
3. "Force On" – enabled through CTRL

When not in one of these conditions, the BGATE output is controlled by the bq25050 and changes depending on which mode is required. See the *Charging Operation* section for more details.

Enable/ Disable External Power Path Control

When power is first applied to the bq25050, either at the IN or BAT input, the bq25050 checks the BGATE output. The device sources a small current out of BGATE for 32ms and monitors the voltage. If VBGATE is connected to ground and the voltage does not rise above logic High, the External Power Path Control feature is disabled and VLOWV is set to 2.5V. If the BGATE voltage rises above logic High, the External Power Path Control feature is enabled and V_{LOWV} is set to 2.9V. The bq25050 only does this check when power is initially applied. Power must removed from IN and BAT and then reapplied to initiate another check. Figure 21 illustrates the startup check procedure.
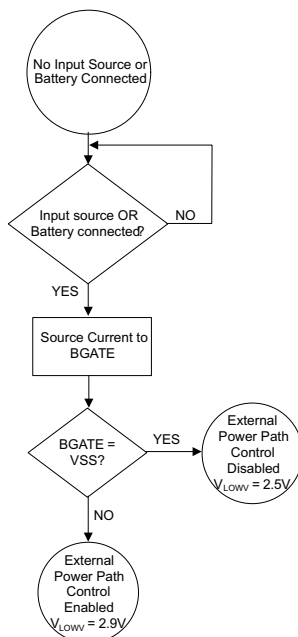

Figure 21. BGATE Monitor Sequence

Charging Operation

The bq25050 charges a battery in 3 stages while maintaining a minimum system output. When the bq25050 is enabled by CTRL, the battery voltage is monitored to verify which stage of charging must be used. The bq25050 charges in precharge mode, minimum output regulation mode, or normal CC/CV mode based on the battery voltage.

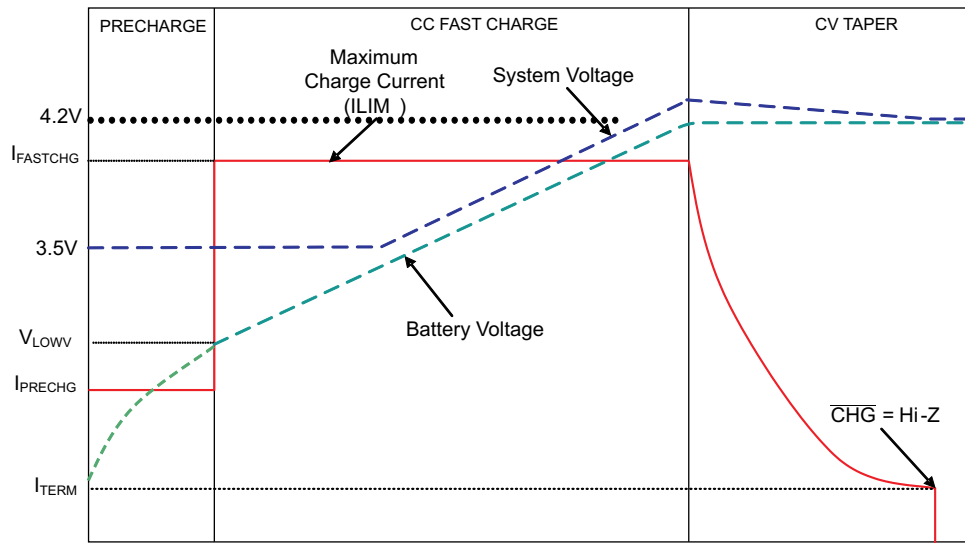**Charger Operation with External Power Path Control Mode Enabled**

Figure 22. Typical Charging Cycle with External Power Path Control Enabled

Precharge Mode ($V_{BAT} \leq V_{LOWV}$)

The bq25050 enters precharge mode when $V_{BAT} \leq V_{LOWV}$. Upon entering precharge mode, the battery is charged with a 40mA current source and /CHG goes low. During precharge mode, V_{OUT} is regulated to 3.5V and the battery is charged from the internal fixed 40mA current source connected to the BAT output. With BGATE connected to GND, the system output is connected to the battery and therefore the system voltage is equal to the battery voltage.

Minimum Output Regulation Mode ($2.9V < V_{BAT} < 3.6V$)

Once VBAT exceeds 2.9V, the bq25050 enters Minimum Output Regulation Mode. While $2.9V < V_{BAT} < 3.6V$, V_{OUT} is regulated to $V_{OUT(REG)}$ by the external FET (QBAT) while the internal FETs between IN and OUT is used to regulate the fast charge current. The total current is shared between the output load and the battery. As the system current increases, the battery charge current decreases. In order to maintain the minimum output regulation voltage $V_{OUT(REG)}$, the system load must be less than the input current limit.

Normal CC/CV Mode

Once $V_{BAT} > 3.6V$, QBAT is fully turned on and $V_{OUT} = V_{BAT} + V_{drop(Q1)}$. At this point, the bq25050 is in constant current (CC) mode where charge current is regulated using the internal FETs between IN and OUT. The V_{OUT} voltage is not regulated. The total current is shared between the output load and the battery. Once the battery voltage charges up to $V_{BAT(REG)}$, the bq25050 enters constant voltage (CV) mode where V_{BAT} is regulated to VBAT(REG) and the current is reduced. Once the input current falls below the termination threshold (I_{TERM}) BGATE is turned off and $\overline{CHG}$ goes high impedance. The system output is regulated to 4.2V and the battery is disconnected from OUT, however supplement mode is still available.

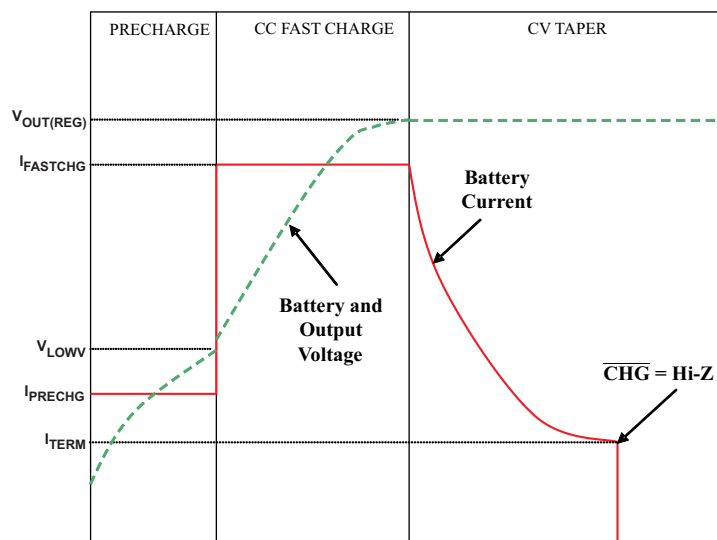**Charger Operation With External Power Path Control Mode Disabled (BGATE = VSS)**

Figure 23. Charging Cycle with External Power Path Control Disabled (BGATE = VSS)

Precharge Mode (V_{BAT} ≤ V_{LOWV})

The bq25050 enters precharge mode when V_{BAT} ≤ V_{LOWV}. Upon entering precharge mode, $\overline{CHG}$ goes low and the input current limit is set to $I_{PRECHARGE}$. With BGATE connected to GND, the system output is connected to the battery and therefore the system voltage is equal to the battery voltage. During precharge mode, the input current is regulated to 50mA and as such, only loads up to 50mA are supported.

Normal CC/CV Mode

Once V_{BAT} > V_{LOWV}, the bq25050 enters constant current (CC) mode where charge current is regulated using the internal MOSFETs between IN and OUT. The total current is shared between the output load and the battery. Once the battery voltage charges up to VBAT(REG), the bq25050 enters constant voltage (CV) mode where V_{BAT} is regulated to VBAT(REG) and the current is reduced. Once the input current falls below the termination threshold (I_{TERM}), $\overline{CHG}$ goes high impedance but the system remains charging and regulates the output to $V_{BAT(REG)}$.

Charge Current Translator (IMON)

When the charger is enabled, internal circuits generate a current proportional to the charge current at the IMON input. The current out of IMON is 1/1000 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R1 (see Figure 1), generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT. Connect a 1kΩ resistor from IMON to VSS. The voltage at IMON is calculated as:

$$V_{IMON} = 1_{IN} \times 1 \text{ V/A}$$

Using this output allows for the host to calculate the actual charging current and therefore perform more accurate termination. The input current to the system must be monitored and subtracted from the current into the bq25050 which is show by V_{IMON}.

Input Over Voltage Protection

The bq25050 contains an input over voltage protection circuit that disables the LDO output and charging when the input voltage rises above V_{OVP}. This prevents damage from faulty adapters. The OVP circuitry contains an deglitch that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than V_{OVP} is plugged in, the IC completes power up and then shuts down if the voltage remains above V_{OVP} after the deglitch. The LDO remains off and charging remains disabled until the input voltage falls below V_{OVP}.

Under-Voltage Lockout (UVLO)

The bq25050 remains in power down mode when the input voltage is below the under-voltage lockout threshold (VUVLO). During this mode, the control input (CTRL) is ignored. The LDO, the charge FET connected between IN and OUT are off and the status output (CHG) is high impedance. Once the input voltage rises above V_{UVLO}, the internal circuitry is turned on and the normal operating procedures are followed.

Input DPM Mode (VIN-DPM)

The input current into the bq25050 includes all load currents, i.e. the system load, LDO load, and battery charge current. The total input current is regulated by the input current limit of the bq25050. The bq25050 utilizes the V_{IN}-DPM mode for operation from current-limited input sources. V_{IN}-DPM is enabled at startup and active until disabled by the CTRL interface. See the *Single Input Interface (CTRL)* section for more details.

When $_{VIN}$-DPM is enabled, the input voltage is monitored. If V_{IN} falls to V_{IN-DPM}, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq25050 from crashing poorly designed or incorrectly configured USB sources. Figure 24 shows the V_{IN}-DPM behavior to a current limited source. In this figure the input source has a 200mA current limit and the device has started up with the 285mA current limit.
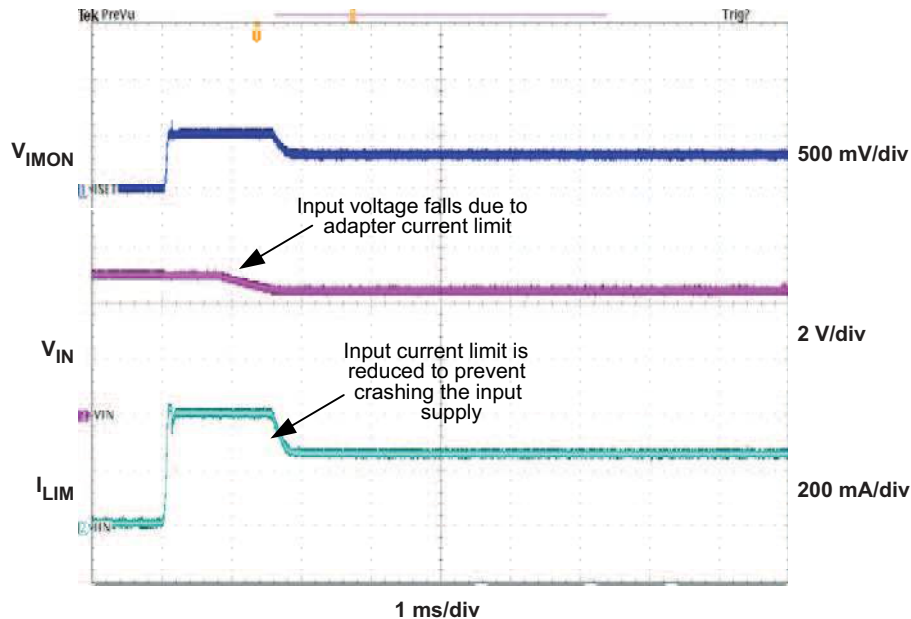

Figure 24. bq25050 V_IN-DPM

External NTC Monitoring (TS)

The bq25050 provides a TS input for monitoring an external 47kΩ NTC thermistor. There are 2 temperature thresholds that are monitored; the cold battery threshold (T_{COLD}) and the hot battery threshold (T_{HOT}). The TS input is monitored at all times and disables charge if the temperature of the NTC falls outside of the operating range. The operating range by default is 0°C to 45°C. An extended range of 0°C to 60°C is selectable using the CTRL input. V_{TS} is also used to monitor the battery temperature. The temperature range is based on the NTC thermistor #NCP15WB473F.

The TS function remains on during battery discharge to enable the host to monitor the battery temperature. The VTS reflects the battery temperature the same as when the battery is charged. The bq25050 does not monitor this voltage, only the current source is active. Table 1 shows important temperatures and the corresponding voltage. This table can be used by the host to determine proper operation limits. The TS function is disabled if the CHG voltage falls below logic low while in battery discharge mode.

Table 1. V$_{TS}$ vs Temperature
(47kΩ Thermistor, β=4050, NCP15WB473F)

TEMPERATURE	VTS
−20°C	0.968 V
0°C	0.600 V
45°C	0.450 V
60°C	0.250 V
80°C	0.110 V

50mA LDO (LDO)

The LDO output of the bq25050 is a low dropout linear regulator (LDO) that supplies up to 50mA while regulating to V$_{LDO}$. The LDO is active whenever the input voltage is above V$_{UVLO}$ and below V$_{OVP}$. It is not affected by the CTRL input. The LDO output is used to power circuitry such as USB transceivers in dead battery conditions. This allows the user to operate the product immediately after plugging the adapter in, instead of waiting for the battery to charge to useable levels.

Charge Status Indicator ($\overline{\text{CHG}}$)

The bq25050 contains an open drain $\overline{\text{CHG}}$ output that indicates when charge cycles and faults. When charging a battery in precharge, fastcharge or CV mode, the $\overline{\text{CHG}}$ output is pulled to VSS. Once the BAT output reaches regulation and the charge current falls below the termination threshold, $\overline{\text{CHG}}$ goes high impedance to signal the battery is fully charged. The $\overline{\text{CHG}}$ output goes low during battery recharge cycles to signal the host to monitor for termination.

Additionally, $\overline{\text{CHG}}$ notifies the host if a NTC temperature fault has occurred. $\overline{\text{CHG}}$ pulses with a period of 100ms and a 50% duty cycle if a TS faults occurs. Connect $\overline{\text{CHG}}$ to the required logic level voltage through a resistor to use the signal with a microprocessor. The sink current I$_{\overline{\text{CHG}}}$ must be below 5mA.

The IC monitors the $\overline{\text{CHG}}$ pin when no input is connected to verify if the phone circuitry is active. If the voltage at $\overline{\text{CHG}}$ is logic low when no driven low, the TS current source is turned off for a low quiescent current state. Once the voltage at $\overline{\text{CHG}}$ increases above logic high, the current source is turned on to allow the host to sense battery temperature.

Single Input Interface (CTRL)

CTRL is used to enable/disable the device as well as select the input current limit, enable/disable charge, extend the TS operation range and disable V$_{IN}$-DPM mode. CTRL is pulled low to enable the device. After the deglitch t$_{CTRL\_DGL}$ expires, the IC enters the 32ms WAIT state. CTRL may be used to program the bq25050 during this time. Once t$_{WAIT}$ expires, the IC starts up. If no command is sent to CTRL during t$_{WAIT}$, the IC starts up with a default 285mA current limit, termination enabled and V$_{IN}$-DPM enabled.

Programming the different modes is done by pulsing the CTRL input. See Table 2 for a map of the different modes. The width of the CTRL pulses is unimportant as long as they are between 50µs and 1000µs long. The time between pulses must be between 50µs and 1000µs to be properly read. Once CTRL is held low for 2ms, the number of pulses is passed to the control logic and decoded and then the mode changes. To ensure proper operation, more than 16 pulses are not recommended. See Figure 26 for a flow diagram of the CTRL interface.

Table 2. Pulse Counting Map for CTRL Interface

# OF PULSES	BGATE CONTROL	CURRENT LIMIT	TS RANGE	V$_{IN}$-DPM
1	Force Termination	No Change	No Change	No Change
2	Force On Disable	No Change	No Change	No Change
3	Force On Enable	No Change	No Change	No Change
4	No Change	93 mA	No Change	No Change
5	No Change	187 mA	No Change	No Change
6	No Change	280 mA	No Change	No Change
7	No Change	374 mA	No Change	No Change
8	No Change	467 mA	No Change	No Change

Table 2. Pulse Counting Map for CTRL Interface (continued)

# OF PULSES	BGATE CONTROL	CURRENT LIMIT	TS RANGE	V_{IN}-DPM
9	No Change	654 mA	No Change	No Change
10	No Change	794 mA	No Change	No Change
11	No Change	935 mA	No Change	No Change
12	No Change	No Change	0°C to 60°C	No Change
13-16	No Change	No Change	No Change	Disabled

If, at any time, the CTRL input is held high for more than 2ms, the IC is disabled. When disabled, charging is suspended and the bq25050 input quiescent current is reduced.
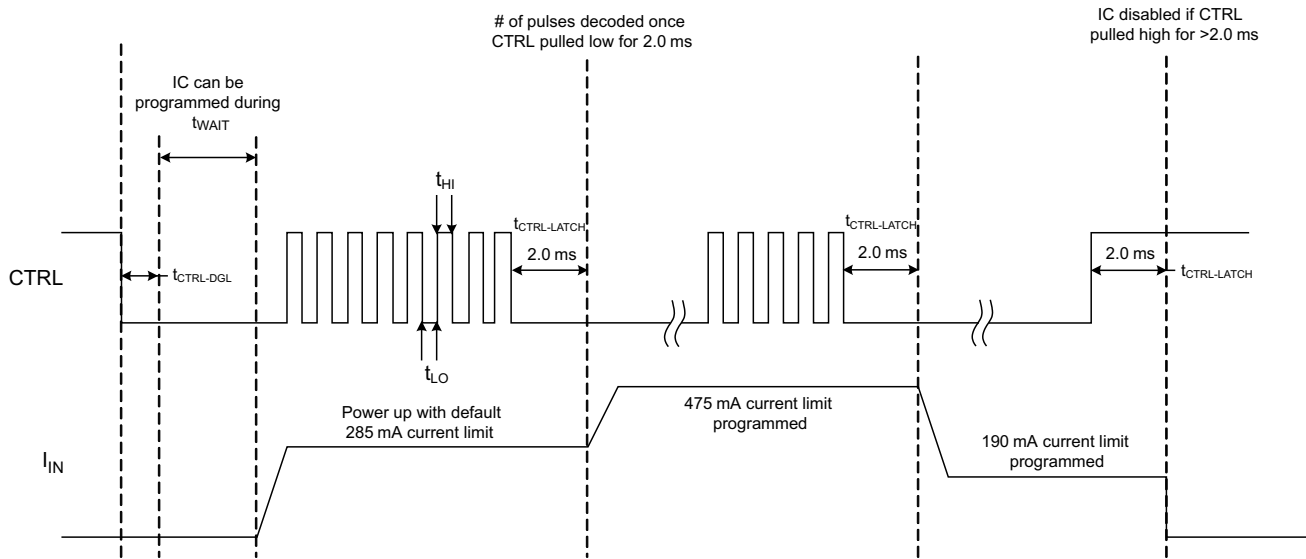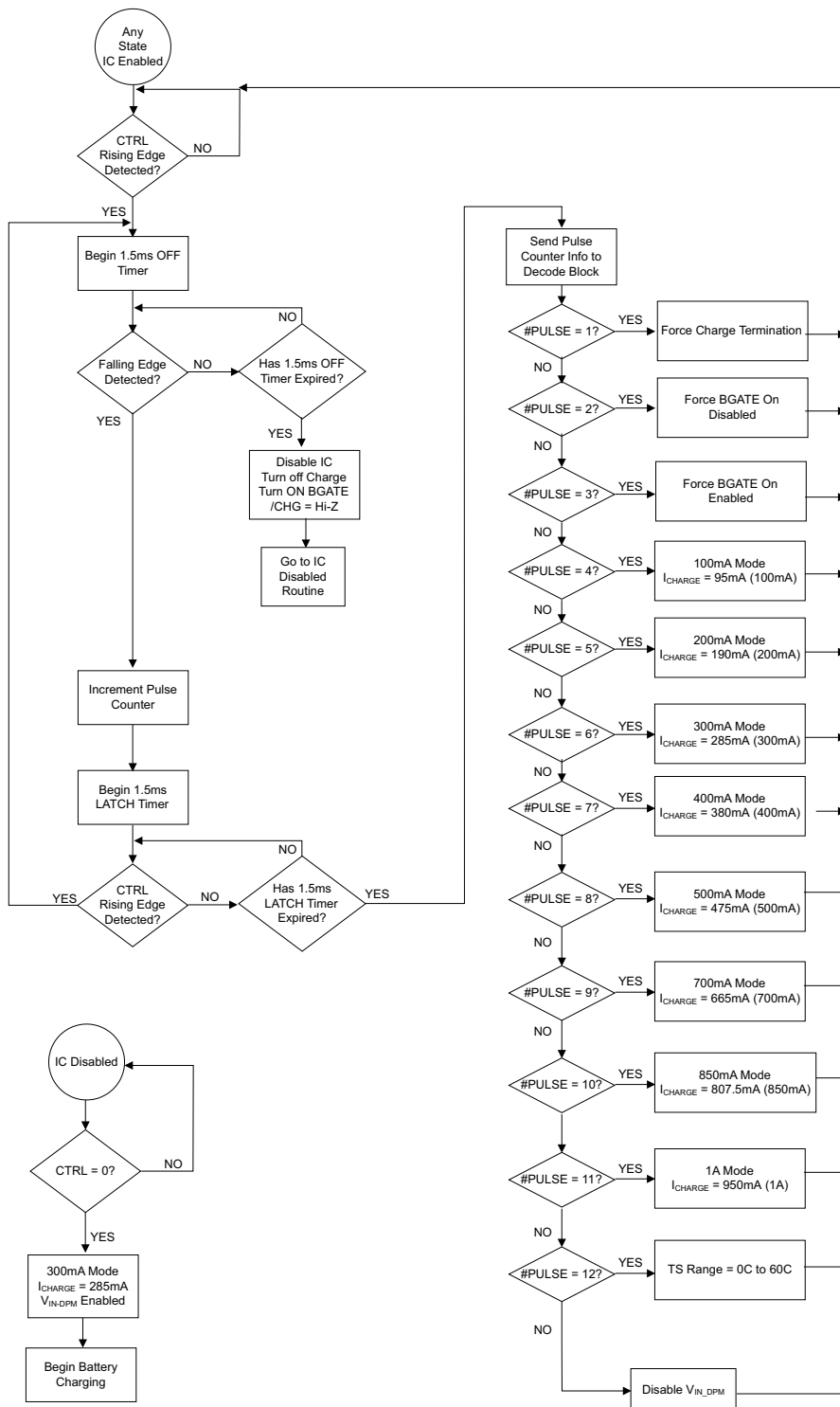

Figure 25. CTRL Timing Diagram

Product Folder Link(s): *bq25050*

Figure 26. CTRL Flow Diagram

Thermal Regulation and Thermal Shutdown

The bq25050 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25050. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm.

Product Folder Link(s): *bq25050*

APPLICATION INFORMATION

Selection of Input/ Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 0.1µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25050 requires a capacitor from OUT to GND for loop stability. Connect a 1µF ceramic capacitor from OUT to GND close to the pins for best results. More output capacitance may be required to minimize the output droop during large load transients. Connect a 0.1µF ceramic capacitor from BAT to GND to eliminate the potential ESD strike.

The LDO also requires an output capacitor for loop stability. Connect a 0.1µF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

bq25050 Charger Design Example

The following sections provide an example for determining the component values for use with the bq25050.

Requirements Refer to Figure 1 and Figure 2 for Schematics of the Design Example
- Supply voltage = 4.35~10.2V
- Fast charge current is set by CTRL - pin 7
- Input current monitoring output - pin 2
- Set 0°C~45°C operating range

Calculations

Program the Fast Charge Current (CTRL): Programming the different input currents, BGATE option, temperature operating range, and VIN-DPM is done by pulsing the CTRL input. See table 2 for details. If, at any time, the CTRL input is held high for more than 2ms, the IC is disabled. After CTRL is pulled low for more than 2ms, the charger resumes. See Figure 26 for details.

Program the input current monitoring output (IMON): Connect a resistor from IMON to VSS to monitor the input current. The voltage of IMON pin is determined by:

$V_{IMON} = K_{IMON} \times R_{IMON} \times I_{CHG}$

The maximum IMON pin voltage is typically 1.2V. If the V_{IMON} is programmed to be higher than $V_{IMON(MAX)}$, the V_{IMON} will be clamped on $V_{IMON(MAX)}$. But, I_{CHG} is controlled by the CTRL pin separately and is not affected by V_{IMON}.

Set charger operating temperature range (TS): The operating range is 0°C to 45°C by a default NTC thermistor NCP15WB473F (47kΩ Thermistor, β=4050). 12 qualified CTRL pulses can set V_{HOT_60} as TS hot threshold and set 0°C to 60°C as the operating range. The following conditions will reset temperature operating range back to 0°C to 45°C.
- Input voltage is lower than UVLO
- The CTRL input is held high for more than 2ms

In battery discharge mode, the TS function is disabled if the $\overline{CHG}$ voltage falls below logic low.

External FET Controller (BGATE): On Figure 1, BGATE drives an external P-channel FET that connects the battery to the system output. When power is first applied to either V_{BAT} or V_{IN}, the device sources a typical 50µA small current out of BGATE and monitors the voltage. If BGATE voltage is higher than logic high in first 1ms and stays high for at least 2ms, the external power path control feature is enabled and V_{LOWV} is set to 2.9V. The OUT pin maintains voltage at $V_{OUT(REG)}$.

In Figure 2, BGATE is connected to Vss. The external power path control feature is disabled and V_{LOWV} is set to 2.5V. The OUT pin shorts to BAT.

Status Indicators ($\overline{CHG}$): The $\overline{CHG}$ pin is open drain output. If used, $\overline{CHG}$ pin should be pulled up via a resistor and possibly a LED to a power source. If monitored by a host, the host pull-up power source should be used.

Thermal Considerations

The bq25050 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

(1)

Where:

   T_J = chip junction temperature
   T_A = ambient temperature
   P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

(2)

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 22. If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25050, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25050 is packaged in a thermally enhanced SON package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25050DQCR	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAM	Samples
BQ25050DQCT	ACTIVE	WSON	DQC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
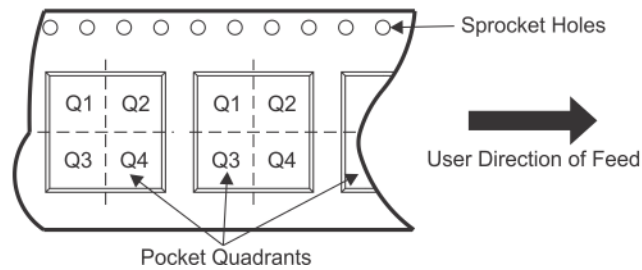
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25050DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ25050DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25050DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
BQ25050DQCT	WSON	DQC	10	250	210.0	185.0	35.0
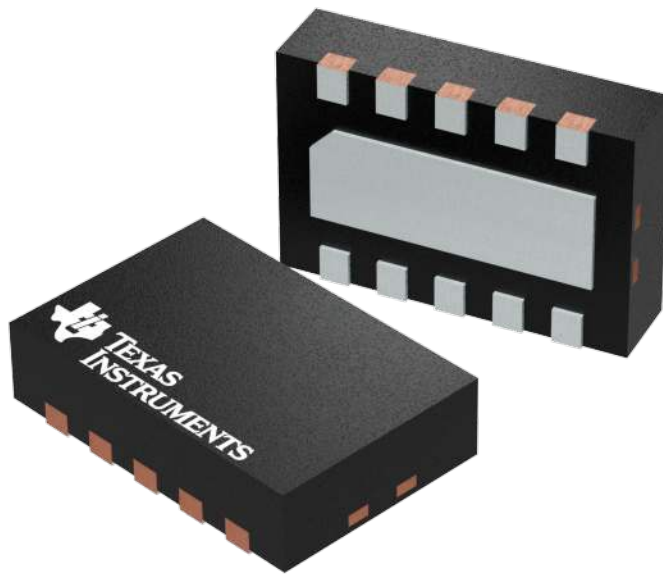
Images above are just a representation of the package family, actual package may vary.
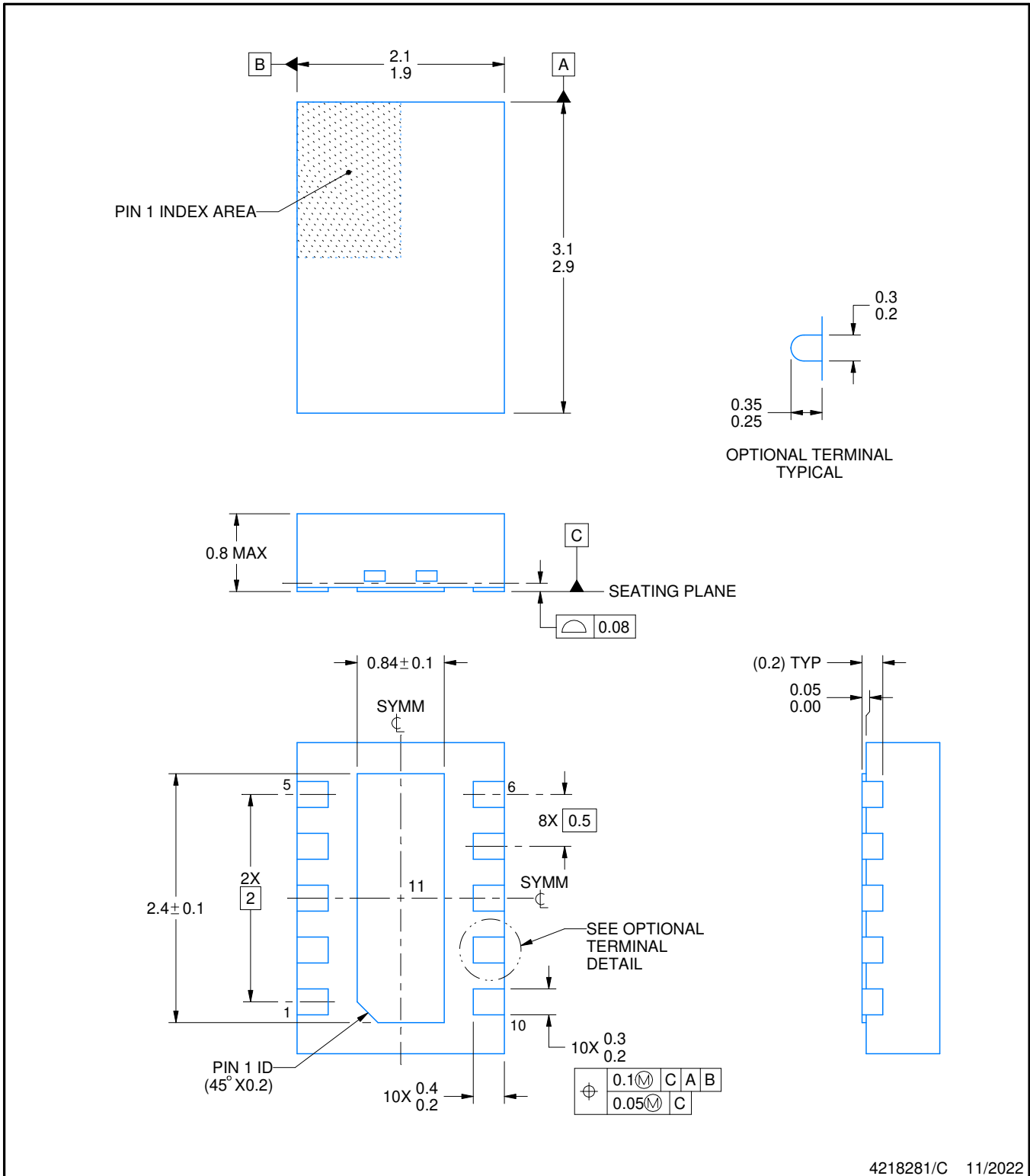Refer to the product data sheet for package details.

4209674/B

B

2.1
1.9

A

PIN 1 INDEX AREA

3.1
2.9

0.3
0.2

0.35
0.25

OPTIONAL TERMINAL
TYPICAL

0.8 MAX

C

SEATING PLANE

⌒ 0.08

0.84±0.1

SYMM
℄

(0.2) TYP

0.05
0.00

5

6

8X 0.5

2X
2

11

SYMM
℄

2.4±0.1

SEE OPTIONAL
TERMINAL
DETAIL

1

10

PIN 1 ID
(45° X0.2)

10X 0.3
0.2

10X 0.4
0.2

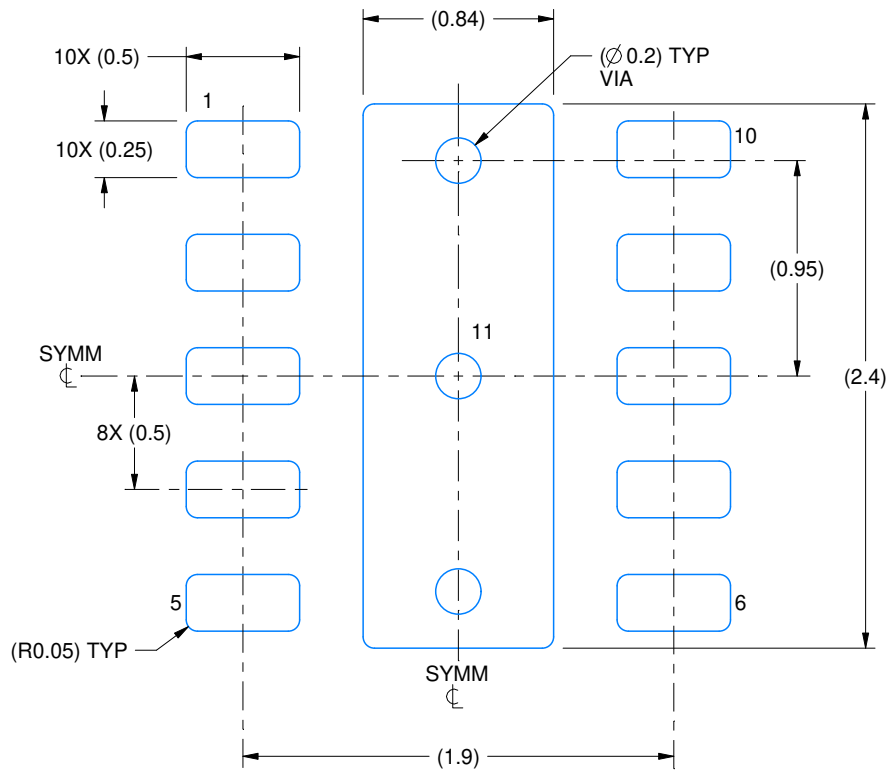| ⊕	0.1Ⓜ	C	A	B
	0.05Ⓜ	C		

4218281/C   11/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
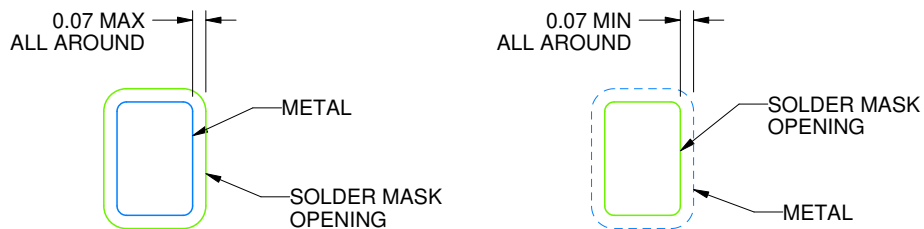
10X (0.5)

1

10X (0.25)

(0.84)

(⌀ 0.2) TYP
VIA

10

(0.95)

SYMM
℄

8X (0.5)

11

(2.4)

5

6

(R0.05) TYP

SYMM
℄

(1.9)

LAND PATTERN EXAMPLE
SCALE: 30X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218281/C   11/2022
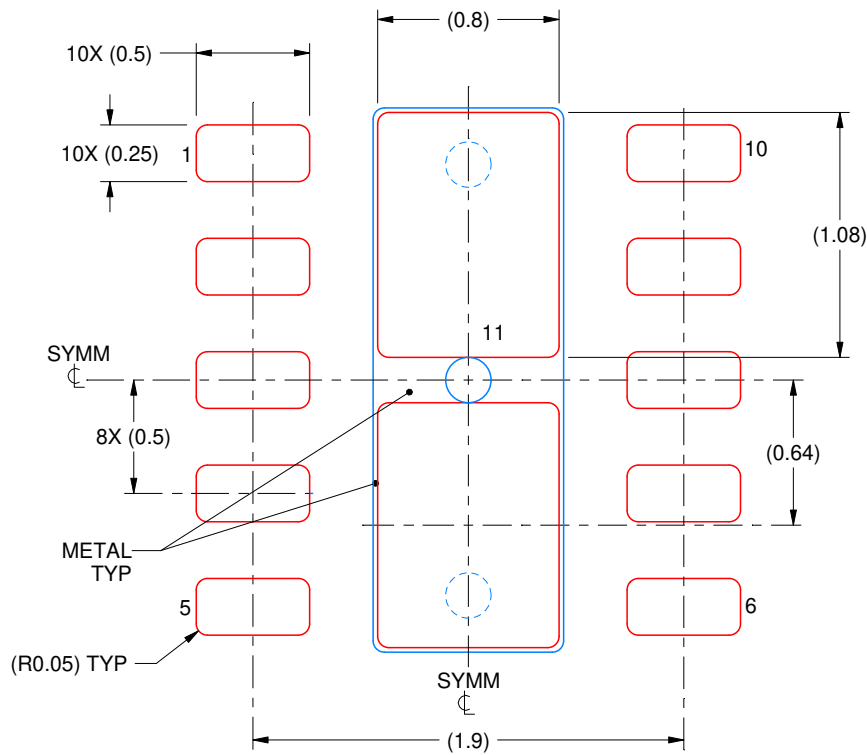
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

10X (0.5)

10X (0.25) 1

(0.8)

10

(1.08)

SYMM

11

8X (0.5)

(0.64)

METAL
TYP

5

6

(R0.05) TYP

SYMM

(1.9)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

4218281/C   11/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.