

IRLR7807ZPbF
IRLU7807ZPbF

Applications

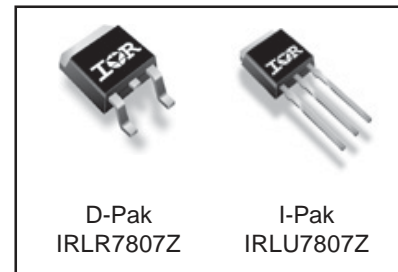
- High Frequency Synchronous Buck Converters for Computer Processor Power
- Lead-Free

HEXFET® Power MOSFET

| V_{DSS} | $R_{DS(on)}$ max | Qg (typ.) |
|------------|------------------|--------------|
| 30V | 13.8mΩ | 7.0nC |

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|---|-----------------------|-------|
| V_{DS} | Drain-to-Source Voltage | 30 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | |
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 43 ^④ | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 30 ^④ | |
| I_{DM} | Pulsed Drain Current ^① | 170 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Maximum Power Dissipation ^⑤ | 40 | W |
| $P_D @ T_C = 100^\circ\text{C}$ | Maximum Power Dissipation ^⑤ | 20 | |
| | Linear Derating Factor | 0.27 | W/°C |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|--|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.75 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ^⑥ | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 110 | |

Notes ^① through ^⑥ are on page 11

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IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--------------------------------|--|------|------|------|-------|--|
| BV_{DSS} | Drain-to-Source Breakdown Voltage | 30 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 23 | — | mV/°C | Reference to 25°C , $I_D = 1mA$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 11 | 13.8 | mΩ | $V_{GS} = 10V, I_D = 15A$ ③ |
| | | — | 14.5 | 18.2 | | $V_{GS} = 4.5V, I_D = 12A$ ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.35 | 1.8 | 2.25 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | — | -4.5 | — | mV/°C | |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 1.0 | μA | $V_{DS} = 24V, V_{GS} = 0V$ |
| | | — | — | 150 | | $V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| g_{fs} | Forward Transconductance | 51 | — | — | S | $V_{DS} = 15V, I_D = 12A$ |
| Q_g | Total Gate Charge | — | 7.0 | 11 | nC | $V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 12A$ See Fig. 16 |
| Q_{gs1} | Pre-V _{th} Gate-to-Source Charge | — | 1.8 | — | | |
| Q_{gs2} | Post-V _{th} Gate-to-Source Charge | — | 0.7 | — | | |
| Q_{gd} | Gate-to-Drain Charge | — | 2.7 | — | | |
| Q_{godr} | Gate Charge Overdrive | — | 1.8 | — | | |
| Q_{sw} | Switch Charge ($Q_{gs2} + Q_{gd}$) | — | 3.4 | — | | |
| Q_{oss} | Output Charge | — | 4.0 | — | nC | $V_{DS} = 15V, V_{GS} = 0V$ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 7.1 | — | ns | $V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 12A$ Clamped Inductive Load |
| t_r | Rise Time | — | 28 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 9.8 | — | | |
| t_f | Fall Time | — | 3.5 | — | | |
| C_{iss} | Input Capacitance | — | 780 | — | pF | $V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$ |
| C_{oss} | Output Capacitance | — | 180 | — | | |
| C_{riss} | Reverse Transfer Capacitance | — | 100 | — | | |

Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|----------|---------------------------------|------|------|-------|
| E_{AS} | Single Pulse Avalanche Energy ② | — | 28 | mJ |
| I_{AR} | Avalanche Current ① | — | 12 | A |
| E_{AR} | Repetitive Avalanche Energy ① | — | 4.0 | mJ |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|--|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 43 ③ | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 170 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.0 | V | $T_J = 25^\circ\text{C}, I_S = 12A, V_{GS} = 0V$ ③ |
| t_{rr} | Reverse Recovery Time | — | 23 | 35 | ns | $T_J = 25^\circ\text{C}, I_F = 12A, V_{DD} = 15V$ |
| Q_{rr} | Reverse Recovery Charge | — | 14 | 21 | nC | $di/dt = 100A/\mu s$ ③ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

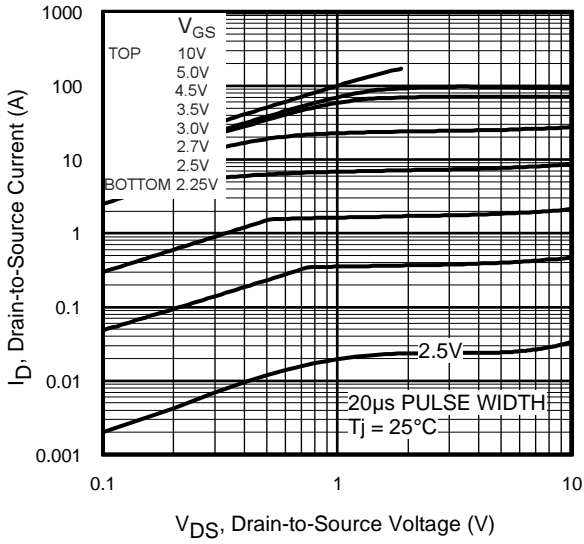


Fig 1. Typical Output Characteristics

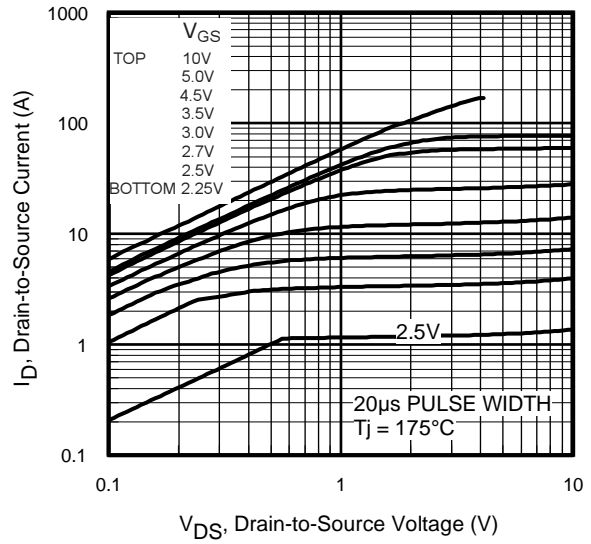


Fig 2. Typical Output Characteristics

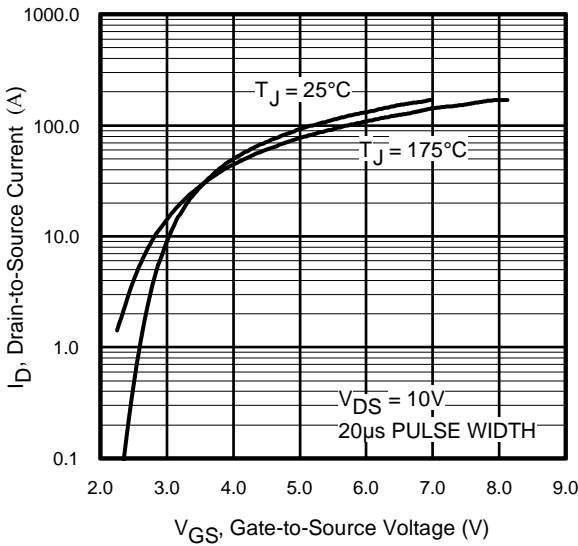


Fig 3. Typical Transfer Characteristics

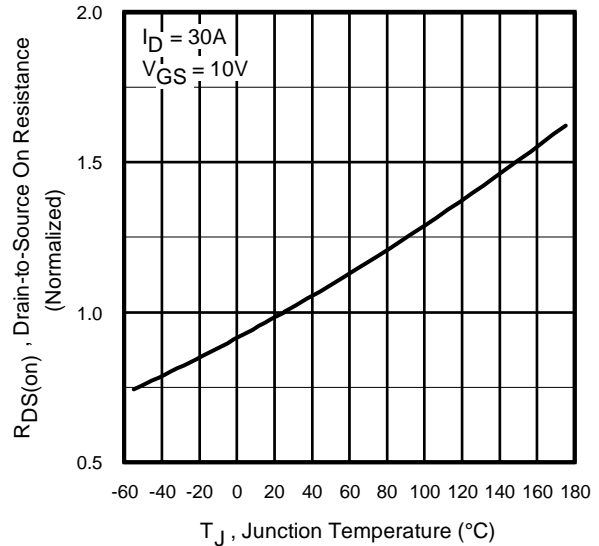


Fig 4. Normalized On-Resistance vs. Temperature

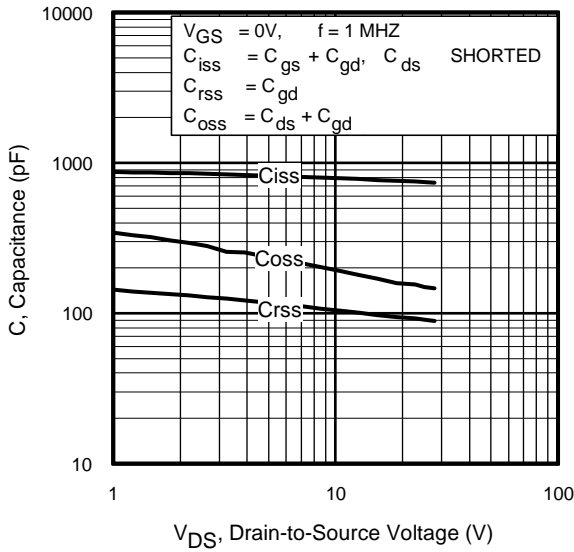


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

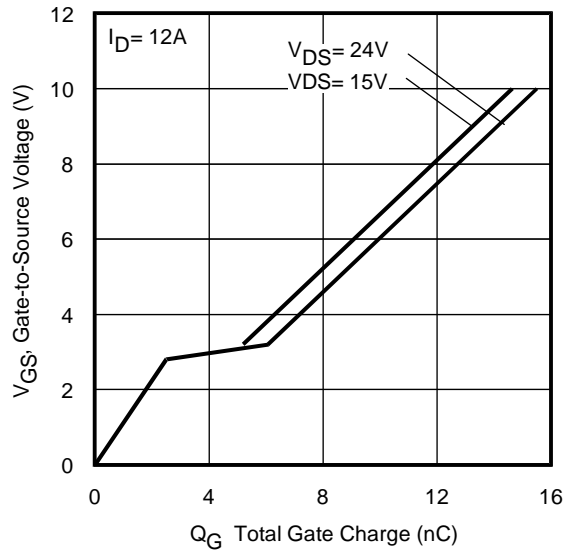


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

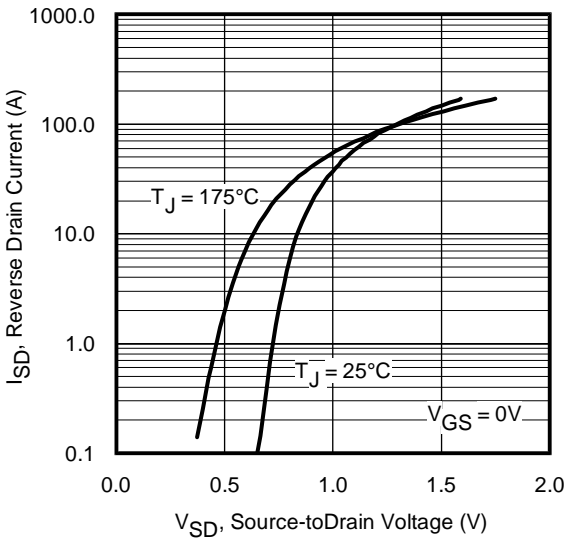


Fig 7. Typical Source-Drain Diode Forward Voltage

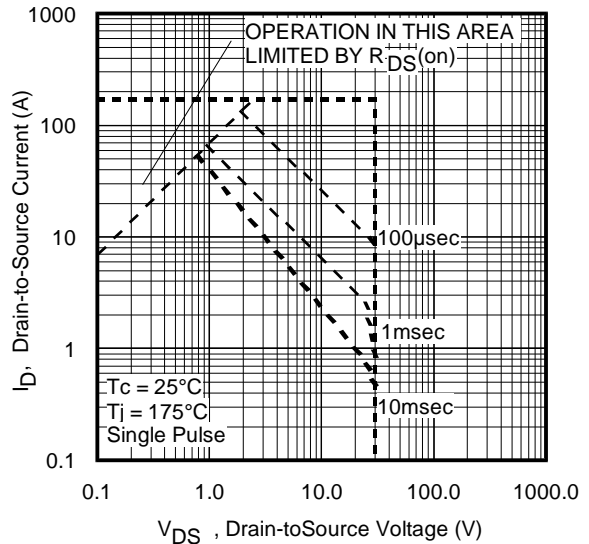


Fig 8. Maximum Safe Operating Area

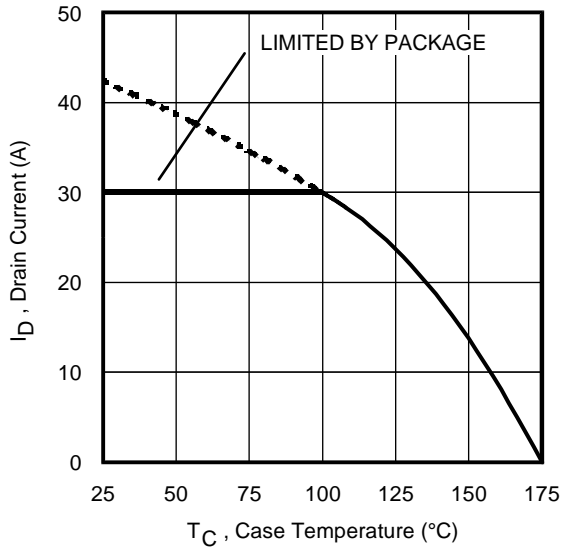


Fig 9. Maximum Drain Current vs. Case Temperature

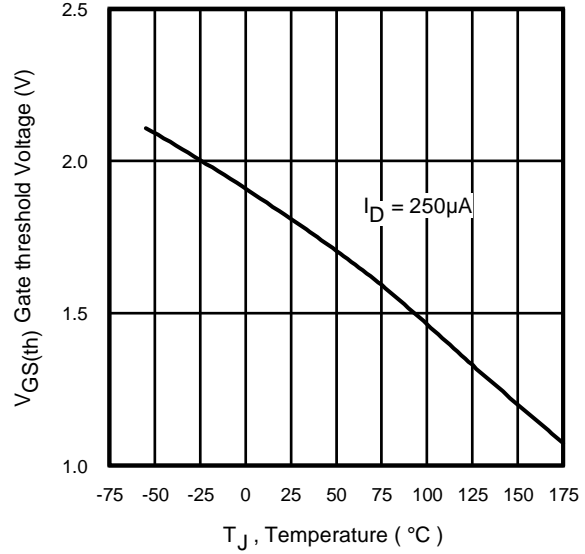


Fig 10. Threshold Voltage vs. Temperature

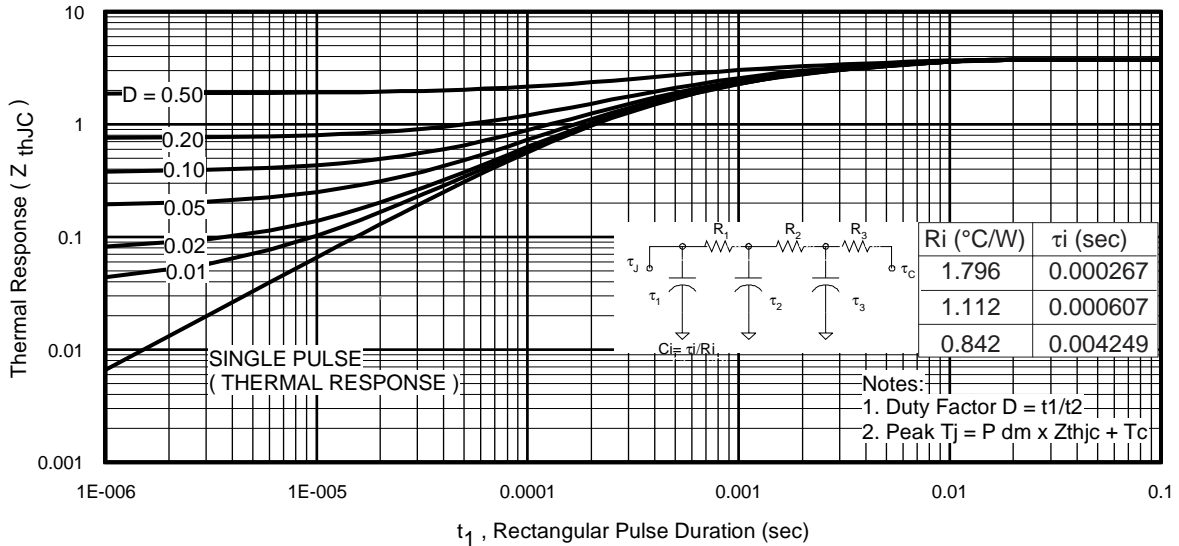


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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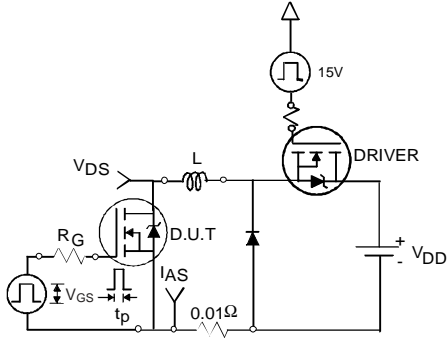


Fig 12a. Unclamped Inductive Test Circuit

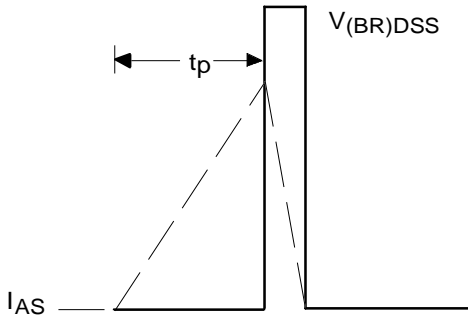


Fig 12b. Unclamped Inductive Waveforms

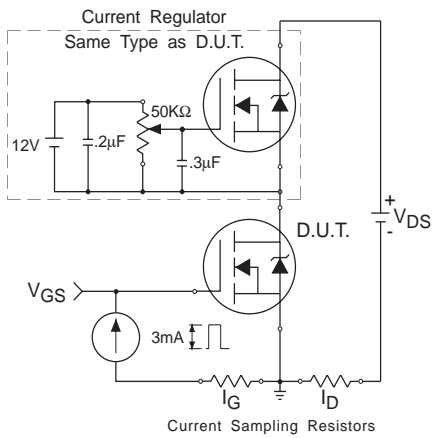


Fig 13. Gate Charge Test Circuit

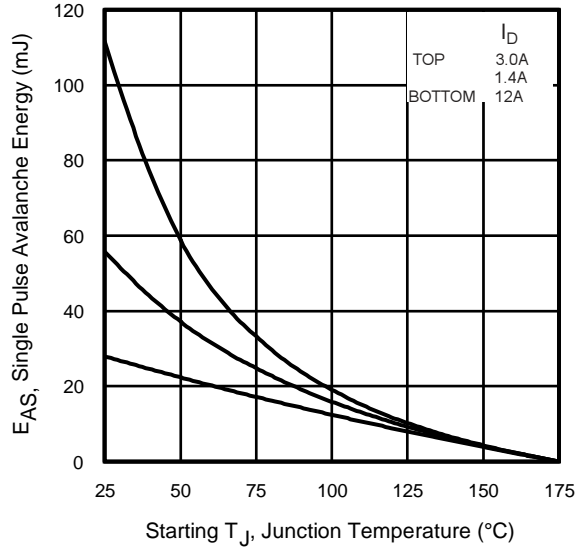


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

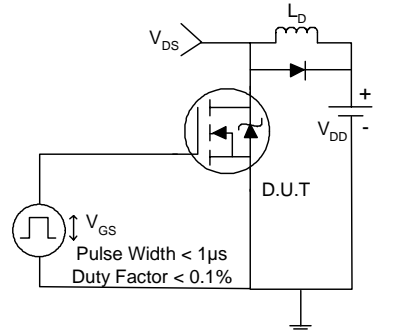


Fig 14a. Switching Time Test Circuit

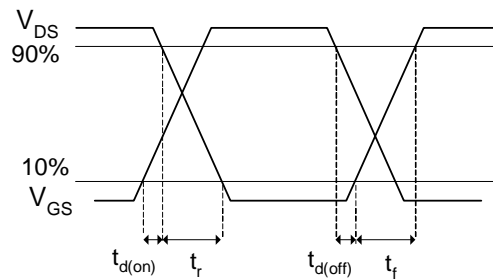


Fig 14b. Switching Time Waveforms

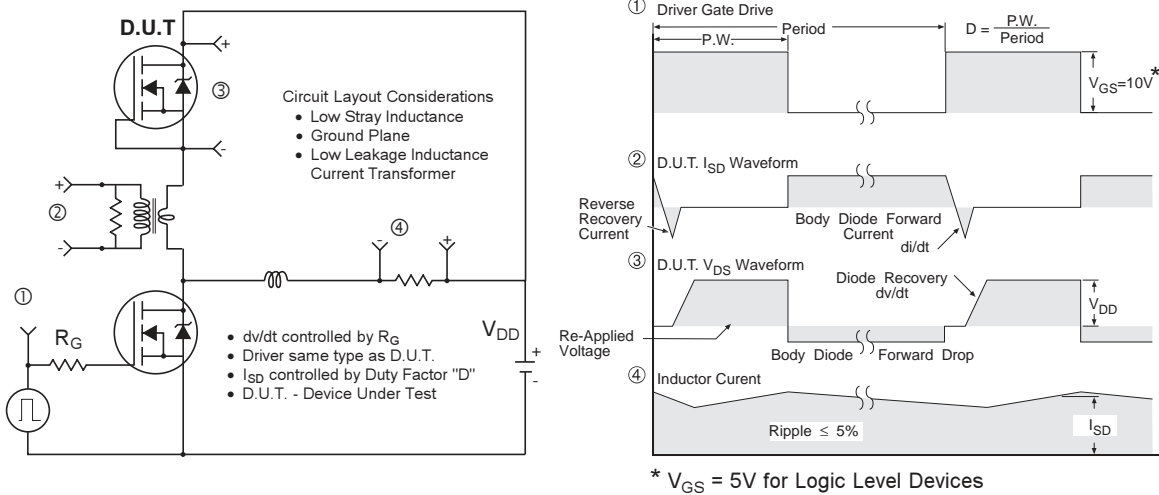


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

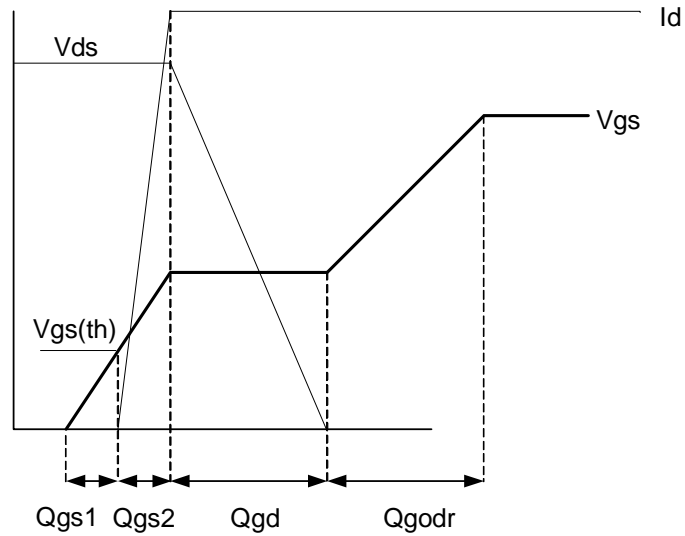


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^2 \times R_{ds(on)} \right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + \left(Q_g \times V_g \times f \right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = \left(I_{rms}^2 \times R_{ds(on)} \right) + \left(Q_g \times V_g \times f \right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

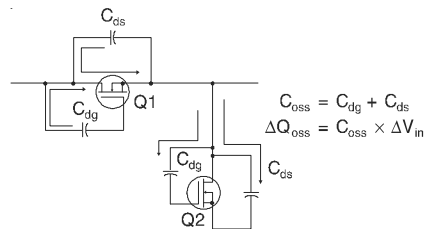
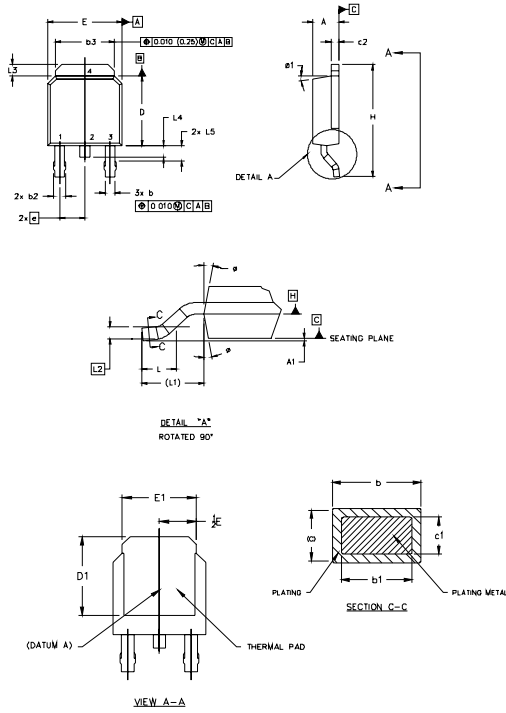


Figure A: Q_{oss} Characteristic

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
 - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
 - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

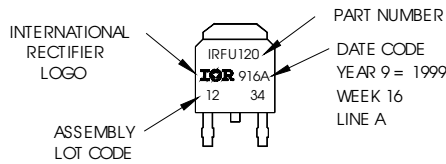
| SYMBOL | MILLIMETERS | | INCHES | | NOTES |
|--------|-------------|-------|-----------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | | 0.13 | | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | 5 |
| b1 | 0.64 | 0.79 | .025 | 0.031 | 5 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | |
| c | 0.46 | 0.61 | .018 | .024 | 5 |
| c1 | 0.41 | 0.56 | .016 | .022 | 5 |
| c2 | .046 | 0.89 | .018 | .035 | 5 |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 | | .090 BSC | | |
| H | 9.40 | 10.41 | .370 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 REF. | | .108 REF. | | |
| L2 | .051 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | |
| L4 | | 1.02 | | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| ø | 0" | 10" | 0" | 10" | |
| ø1 | 0" | 15" | 0" | 15" | |

- LEAD ASSIGNMENTS**
- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN
- IGBTs, CoPACK**
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
 - 4.- COLLECTOR

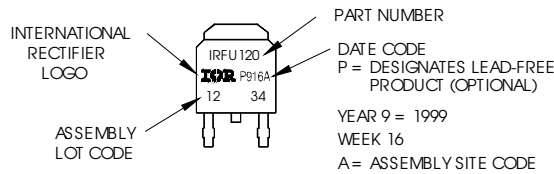
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON VW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"



OR



IRLR/U7807ZPbF

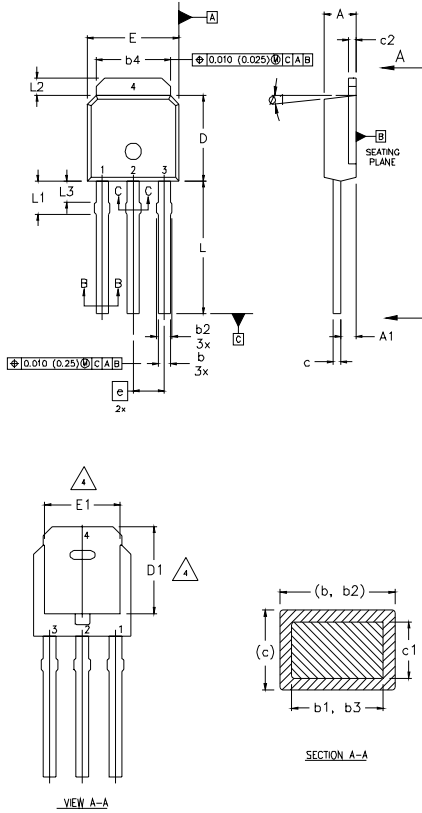
International
IR Rectifier

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.



| SYMBOL | DIMENSIONS | | | | NOTES |
|----------|-------------|------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | 0.086 | .094 | |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 | |
| b | 0.64 | 0.89 | 0.025 | 0.035 | |
| b1 | 0.64 | 0.79 | 0.025 | 0.031 | 4 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 | |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 | |
| b4 | 5.00 | 5.46 | 0.195 | 0.215 | 4 |
| c | 0.46 | 0.61 | 0.018 | 0.024 | |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 | |
| c2 | .046 | 0.86 | 0.018 | 0.035 | |
| D | 5.97 | 6.22 | 0.235 | 0.245 | 3, 4 |
| D1 | 5.21 | - | 0.205 | - | 4 |
| E | 6.35 | 6.73 | 0.250 | 0.265 | 3, 4 |
| E1 | 4.32 | - | 0.170 | - | 4 |
| e | 2.29 | | 0.090 BSC | | |
| L | 8.89 | 9.60 | 0.350 | 0.380 | |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 | |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 | 4 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 | 5 |
| $\phi 1$ | 0 | 15 | 0 | 15 | |

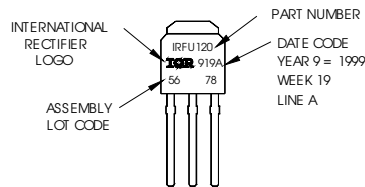
LEAD ASSIGNMENTS

HEXFET

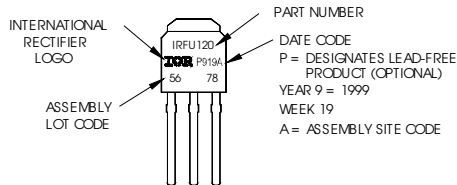
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 1999 IN THE ASSEMBLY LINE "A"
Note: "P" in assembly line position indicates "Lead-Free"

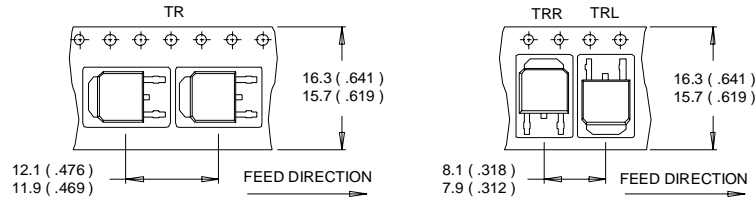


OR

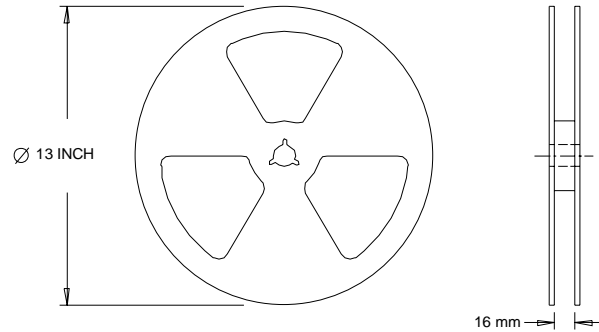


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.39\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 12\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>