MACHLV210-12/15/20

Lattice Semiconductor

High Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3-V JEDEC compatible**
  - V_{CC} = +3.0 V to +3.6 V
- **< 5 mA standby current**
- **Patented design allows minimal standby current without speed degradation**
- **Exclusively designed for 3.3-V applications**
- **44 Pins**
- **64 Macrocells**
- **12 ns t_{PD} Commercial**
  18 ns t_{PD} Industrial
- **83.3 MHz f_{CNT}**
- **38 Bus-Friendly Inputs**
- **32 Outputs**
- **64 Flip-flops; 2 clock choices**
- **4 "PAL22V16" blocks with buried macrocells**
- **Pin-, function-, and JEDEC-compatible with MACH210**
- **Pin-compatible with MACH110, MACH111, MACH210, MACH211, and MACH215**

GENERAL DESCRIPTION

The MACHLV210 is a member of the high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell. It is architecturally identical to the MACH210, with the addition of I/O pull-up/pull-down resistors and low-voltage, low-power operation.

The MACHLV210 provides 3.3-V operation with low-power CMOS technology. The patented design allows for minimal standby current without speed degradation by limiting the leakage current when signals are not switching. At less than 5 mA maximum standby current, the MACHLV210 is ideal for low-power applications.

The MACHLV210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACHLV210 has two kinds of macrocell: output and buried. The MACHLV210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACHLV210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

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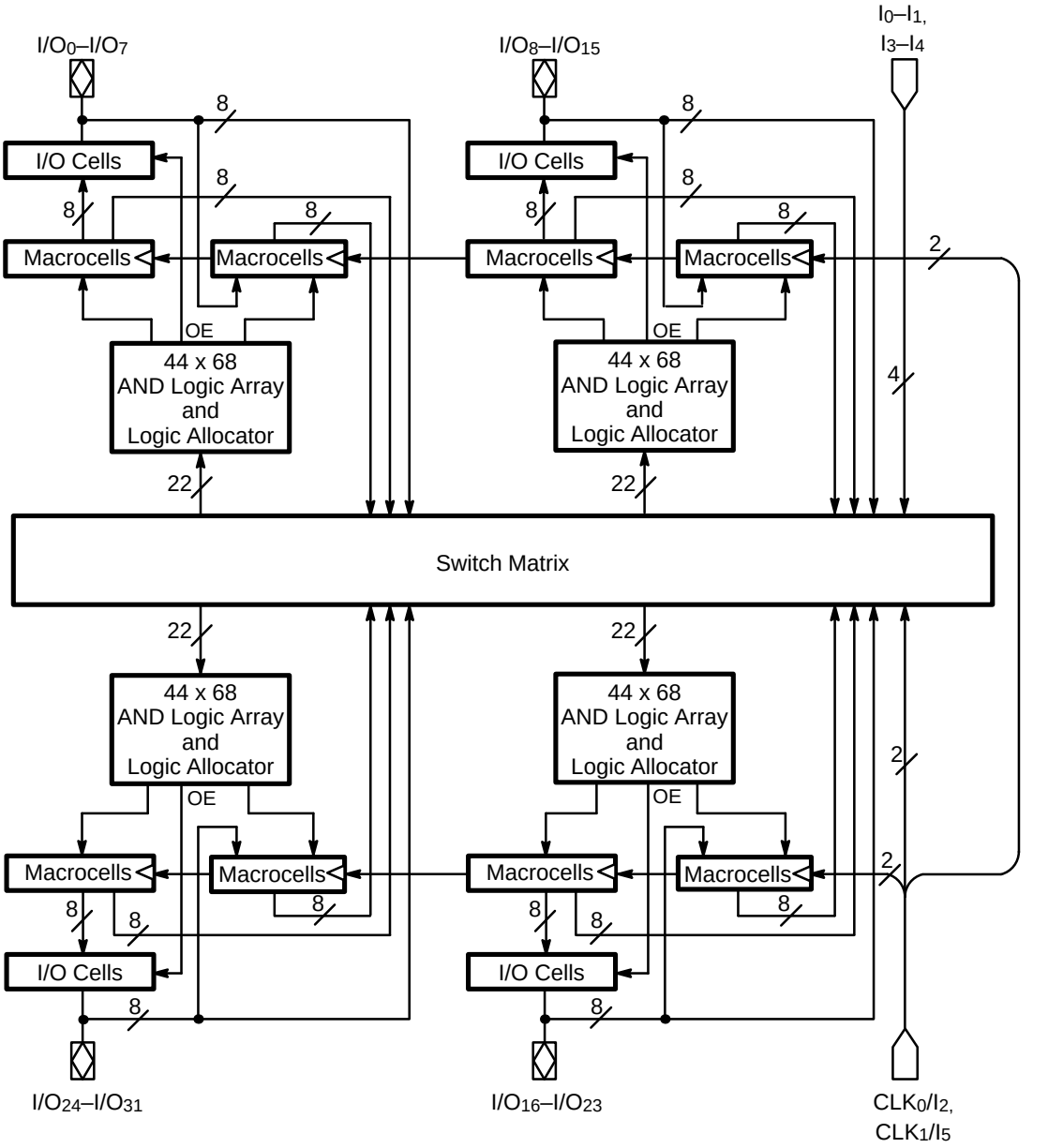
BLOCK DIAGRAM



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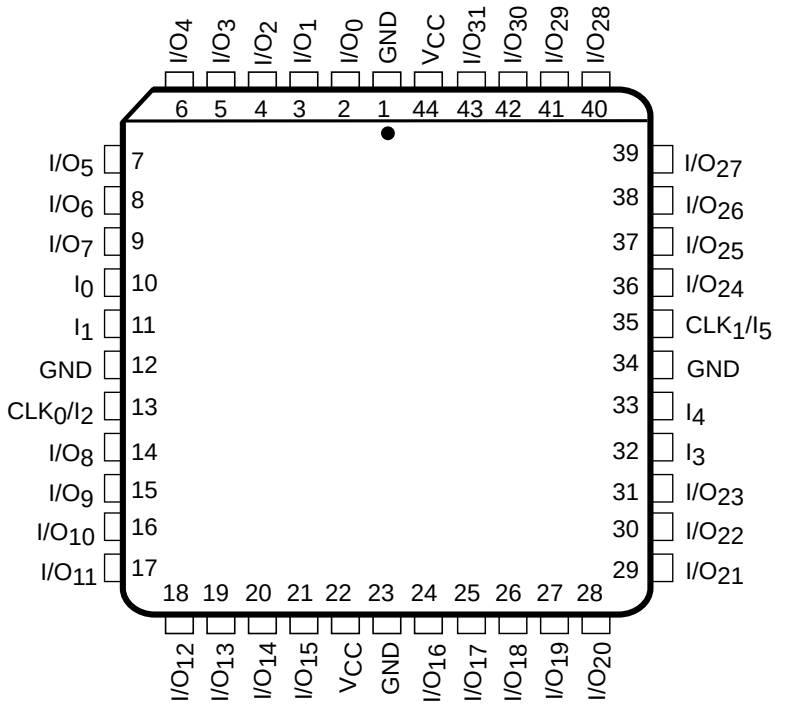
CONNECTION DIAGRAM
Top View

PLCC



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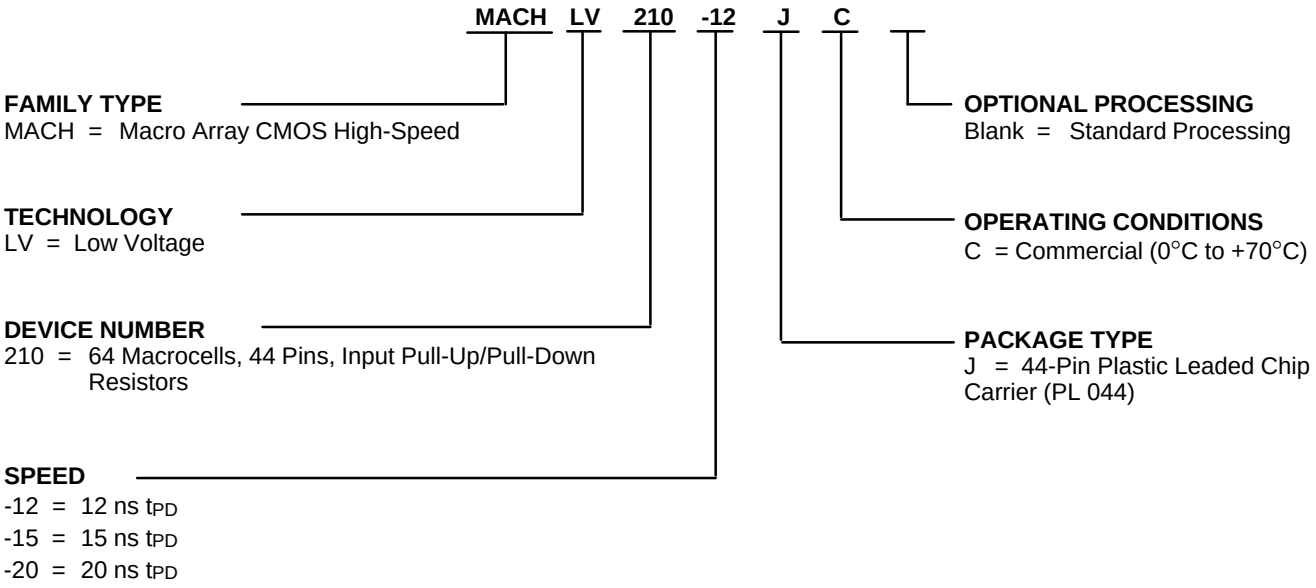
Note:
Pin-compatible with MACH110, MACH111, MACH210, MACH211, and MACH215.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



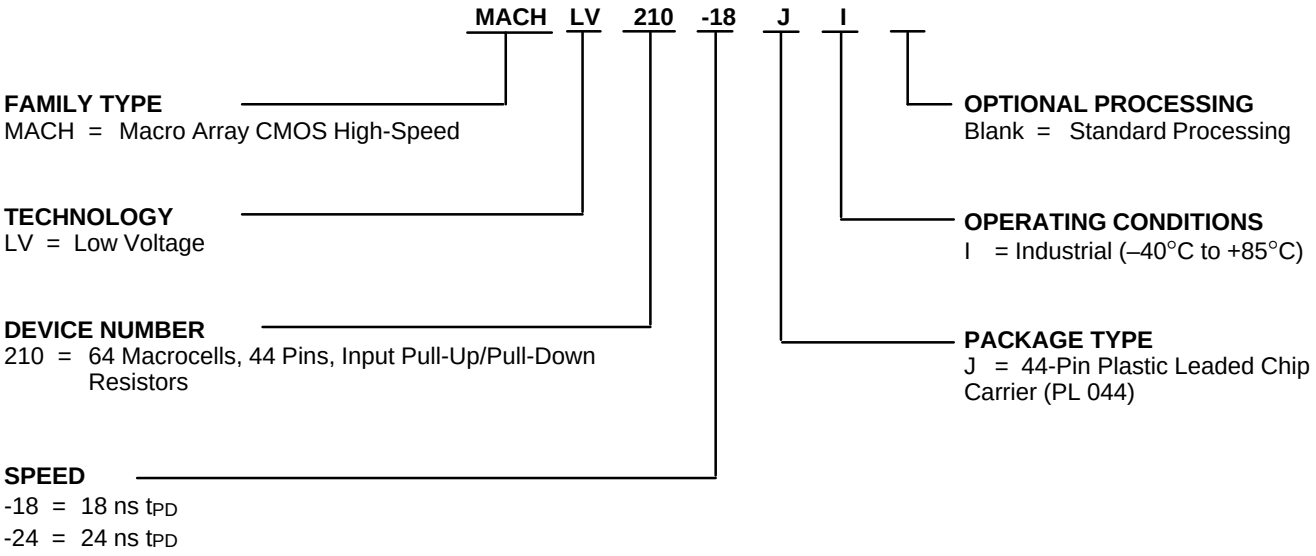
Valid Combinations	
MACHLV210-12	JC
MACHLV210-15	
MACHLV210-20	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

Programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACHLV210-18	JI
MACHLV210-24	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACHLV210 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The MACHLV210 inputs and I/O pins have advanced pull-up/pull-down resistors that enable the inputs to be pulled to the last driven state. While it is always a good design practice to tie unused pins high or low, the MACHLV210 pull-up/pull-down resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACHLV210 (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent “PAL22V16” with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACHLV210 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACHLV210 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACHLV210 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		C_9, C_{10}, C_{11}, C_{12}
	M_{11}	C_{10}, C_{11}, C_{12}, C_{13}
M_{12}		C_{11}, C_{12}, C_{13}, C_{14}
	M_{13}	C_{12}, C_{13}, C_{14}, C_{15}
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACHLV210 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACHLV210 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

Benefits of Lower Operating Voltage

The MACHLV210 has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for portable applications.

Because power is proportional to the square of the voltage, reduction of the supply voltge from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications.

Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3-V designs facilitate a reduction in the form factor.

The MACHLV210 is not designed to interface between 3.3-V and 5.0-V logic. Latch-up may occur if V_{OH} for the MACHLV210 is greater than V_{IH} for the 5.0-V device. Although this scenario is unlikely, interfacing the MACHLV210 with 5.0-V devices is not encouraged without necessary latch-up design precautions.

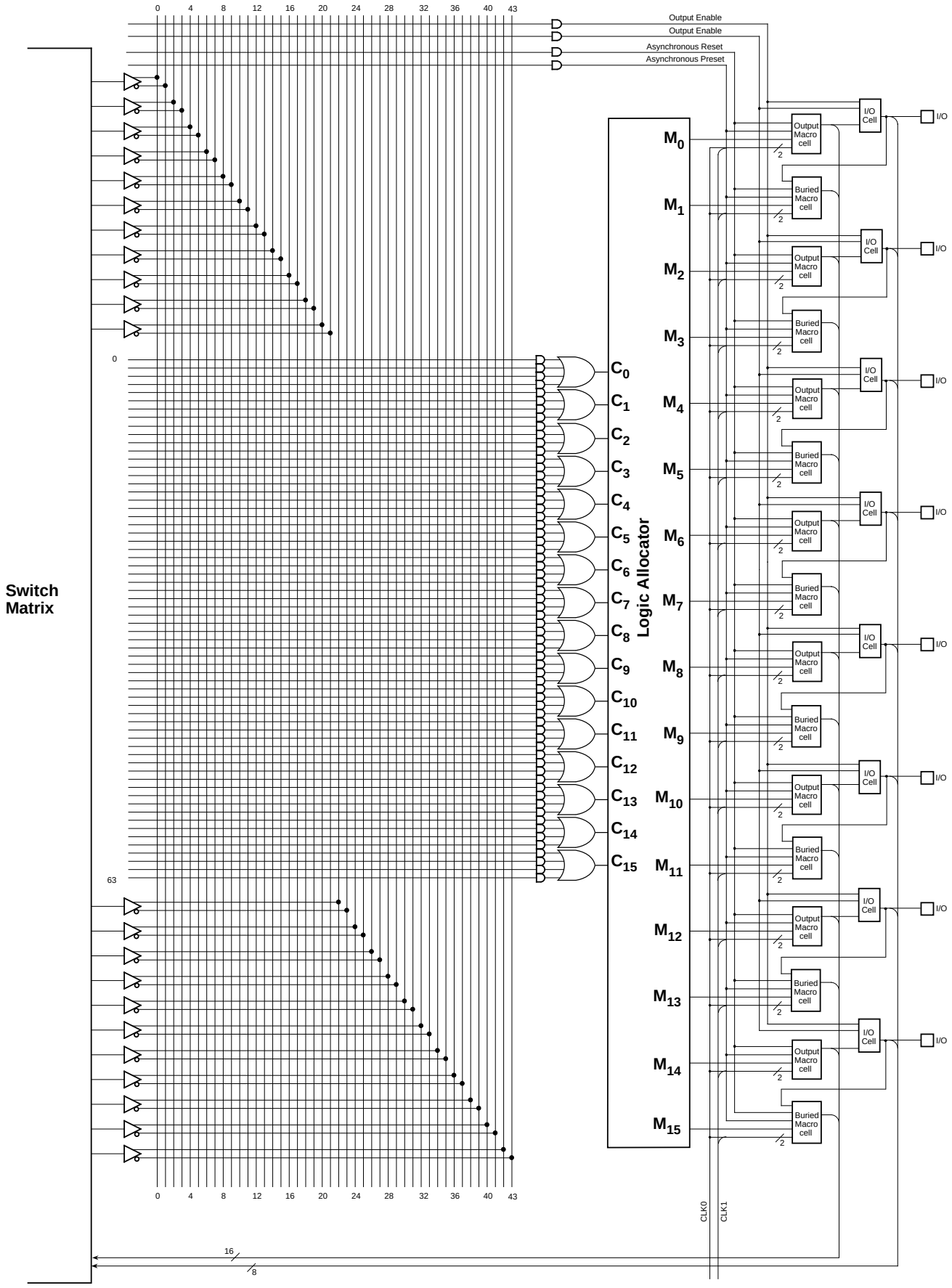


Figure 1. MACHLV210 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +5.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C, (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-12 Min	-12 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	9		ns
			T-type	10		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				8	ns
t_{WL}	Clock Width		LOW	5		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	58.8		MHz
			T-type	55.6		MHz
		Internal Feedback (f_{CNT})	D-type	83.3		MHz
			T-type	76.9		MHz
		No Feedback (f_{CNT})		90.9		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			9		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				9	ns
t_{GWL}	Gate Width LOW			5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				15	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			1.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output				15	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	12		ns
			T-type	13		ns
t_{WICL}	Input Register Clock Width		LOW	5		ns
t_{WICH}			HIGH	6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$		90.9		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			1.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				19	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			10		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			13		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		17	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		12	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		12	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +5.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		14		ns
				T-type	11		15		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	5		7		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		38.5		MHz
				T-type	47.6		37		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		90.9		66.7		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		14		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					11		15	ns
t_{GWL}	Gate Width LOW				5		7		ns
t_{PDL}	Input, I/O, or Feedback to Output Through					17		23	ns
t_{SIR}	Input Register Setup Time				2.5		3		ns
t_{HIR}	Input Register Hold Time				1.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		24	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	13		27		ns
				T-type	14		20		ns
t_{WICL}	Input Register Clock Width			LOW	5		7		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			90.9		66.7		MHz
t_{SIL}	Input Latch Setup Time				2.5		3		ns
t_{HIL}	Input Latch Hold Time				1.5		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					19		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					22		29	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		16		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				14		18		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	5		7		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		21		28	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		26	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		26	ns
t_{APW}	Asynchronous Preset Width (Note 1)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +5.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Temperature (T_A) Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}				0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)				0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)				–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 3.3 V, T_A = 25°C (Note 4)	f = 0 MHz		2		mA
			f = 25 MHz		60		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-18 Min	-18 Max	-24 Min	-24 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	12		17		ns
				T-type	13.5		18		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					12		14.5	ns
t_{WL}	Clock Width			LOW	6		8.5		ns
t_{WH}				HIGH	7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		30.5		MHz
				T-type	38		29.5		MHz
		Internal Feedback (f_{CNT})		D-type	53		40		MHz
				T-type	50		38		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		72.5		53		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				12		17		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					13.5		18	ns
t_{GWL}	Gate Width LOW				6		8.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Latch					20.5		28	ns
t_{SIR}	Input Register Setup Time				3		4		ns
t_{HIR}	Input Register Hold Time				2.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22		29	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	16		32.5		ns
				T-type	17		24		ns
t_{WICL}	Input Register Clock Width			LOW	6		8.5		ns
t_{WICH}				HIGH	7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		72.5		53		MHz
t_{SIL}	Input Latch Setup Time				3		4		ns
t_{HIL}	Input Latch Hold Time				2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					23		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					26.5		34.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				14.5		19.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				17		22		ns

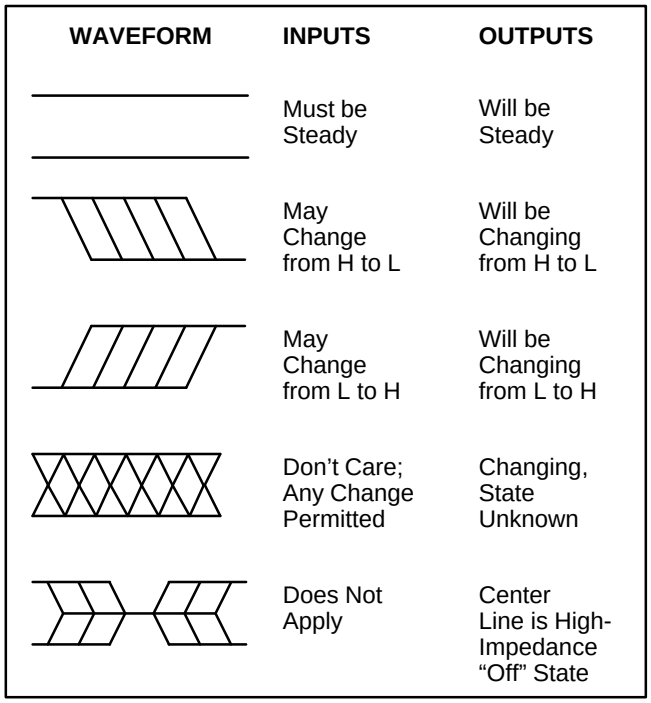
SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-18		-24		Unit
		Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		8.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25.5		34	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		24		31.5	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	18		24		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		24		31.5	ns
t_{APW}	Asynchronous Preset Width (Note 1)	18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	18		24		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		18		24	ns

Notes:

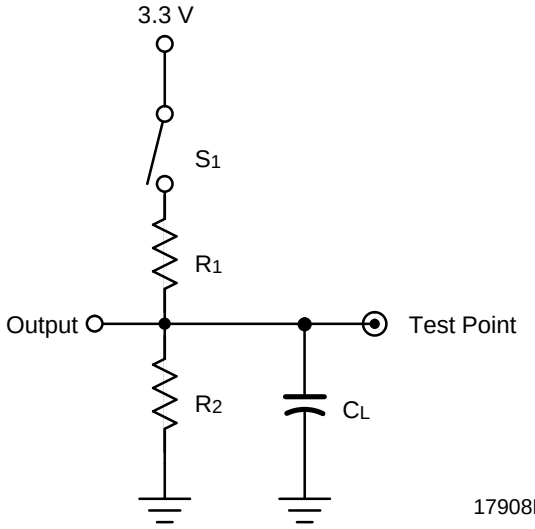
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit at the back of this Data Sheet for test conditions.*
3. *Parameters measured with 16 outputs switching.*

KEYS TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT*



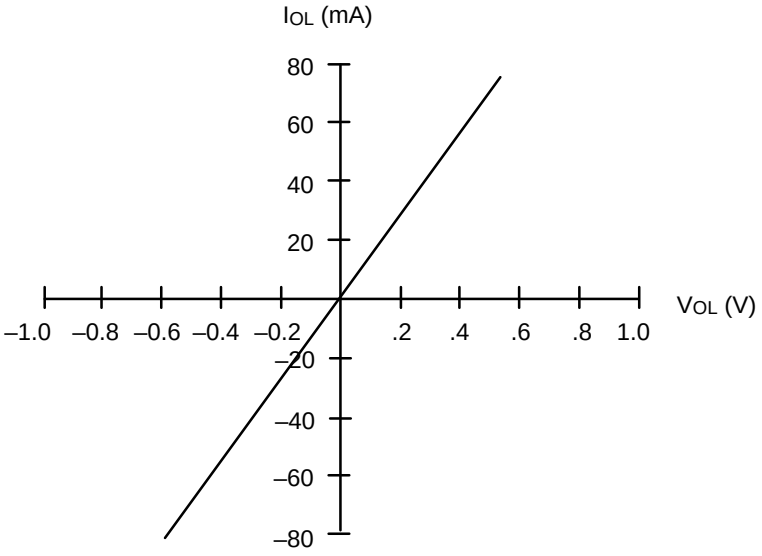
17908D-4

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	30 pF	1.6 K	1.6 K	1.5 V
t_{EA}	$Z \rightarrow H$: Open $Z \rightarrow L$: Closed				1.5 V
t_{ER}	$H \rightarrow Z$: Open $L \rightarrow Z$: Closed	5 pF			$H \rightarrow Z$: V_{OH} – 0.5 V $L \rightarrow Z$: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

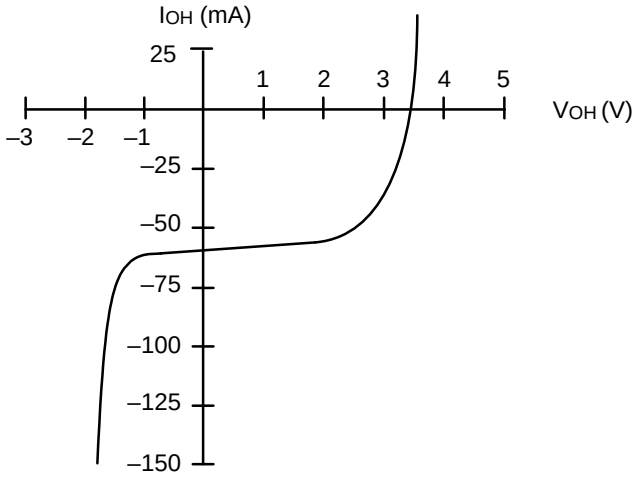
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



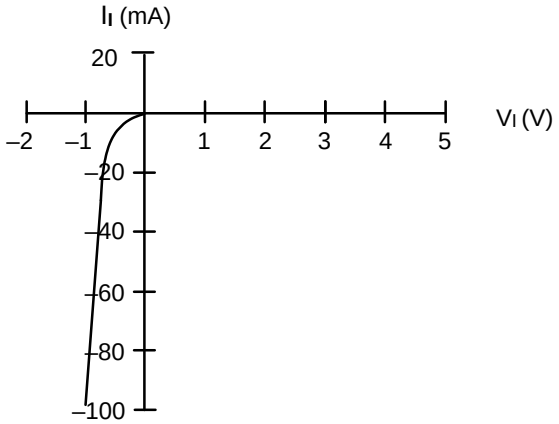
17908D-5

Output, LOW



17908D-6

Output, HIGH

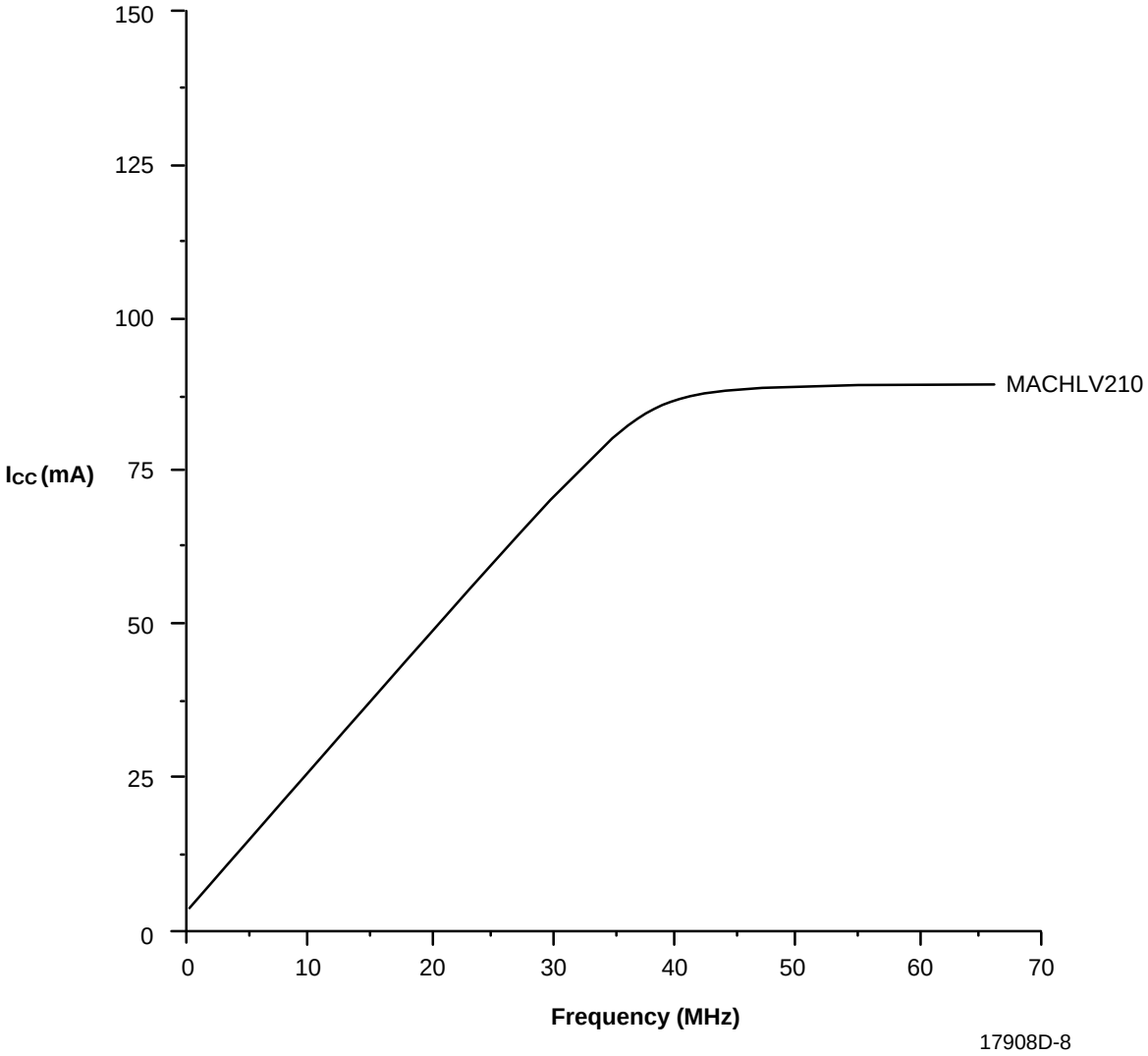


17908D-7

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

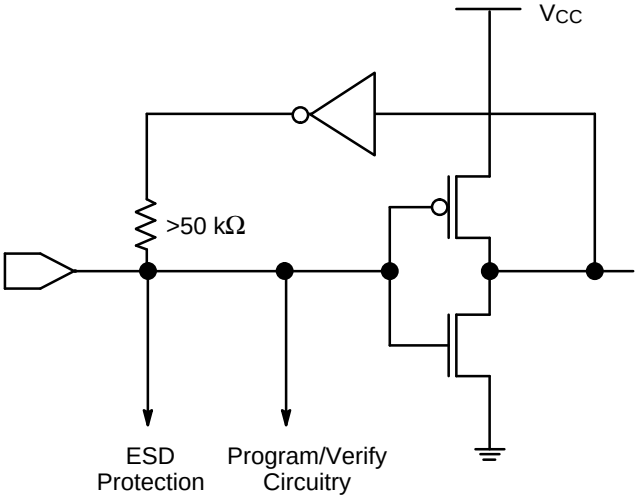
Maximum frequency shown uses internal feedback and a D-type register.

ENDURANCE CHARACTERISTICS

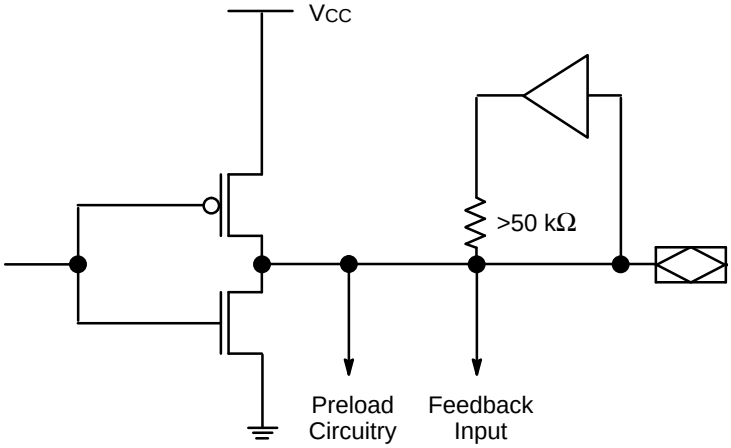
The MACHLV210 is manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Parameter Symbol	Parameter Description	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Max Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

17908D-9

TYPICAL THERMAL CHARACTERISTICS

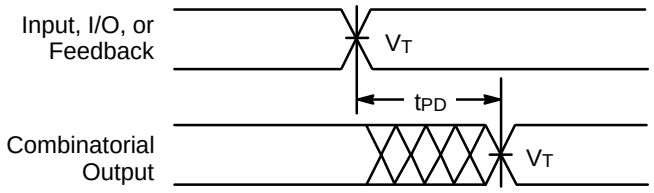
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	°C/W
		400 lfpm air	33	°C/W
		600 lfpm air	31	°C/W
		800 lfpm air	29	°C/W

Plastic θjc Considerations

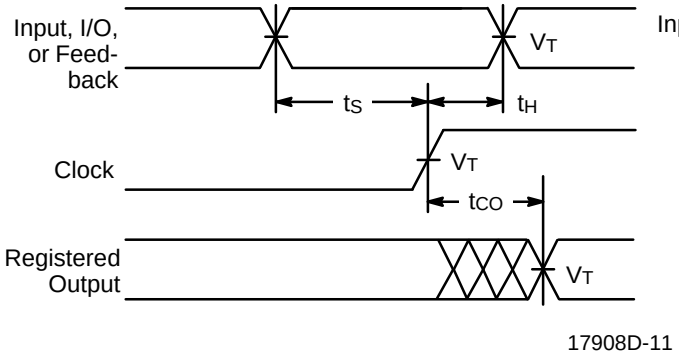
The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

SWITCHING WAVEFORMS



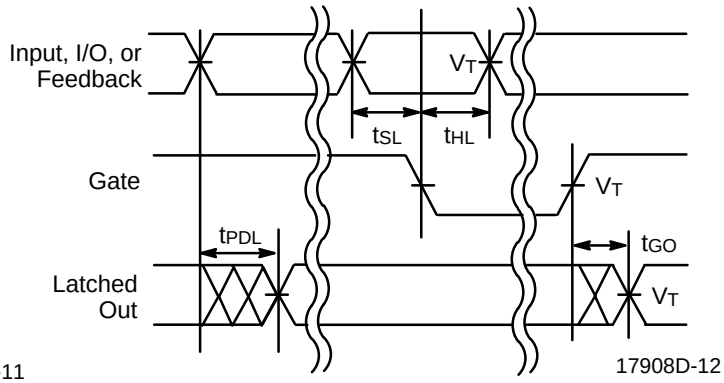
17908D-10

Combinatorial Output



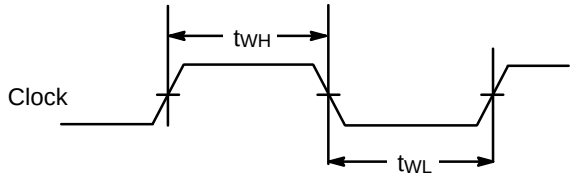
17908D-11

Registered Output



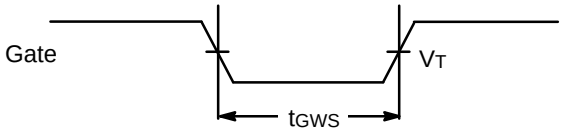
17908D-12

Latched Output (MACH 2, 3, and 4)



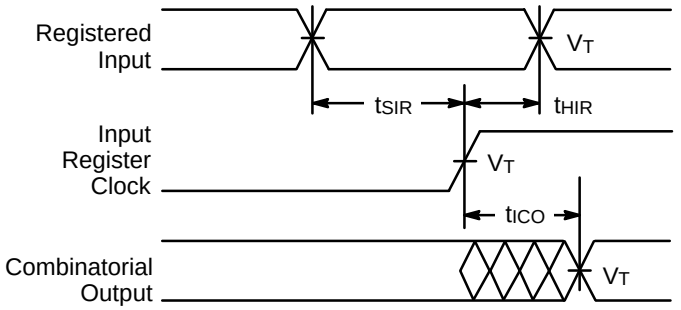
17908D-13

Clock Width



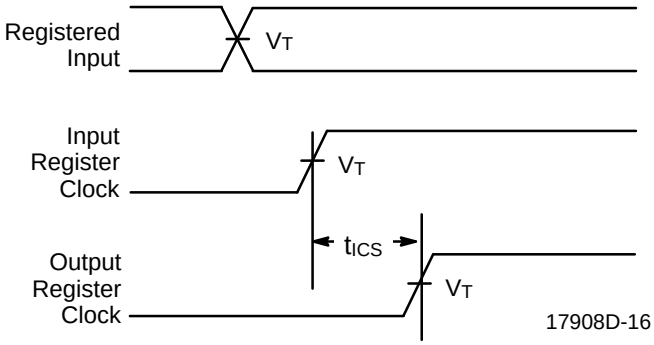
17908D-14

Gate Width (MACH 2, 3, and 4)



17908D-15

Registered Input (MACH 2 and 4)



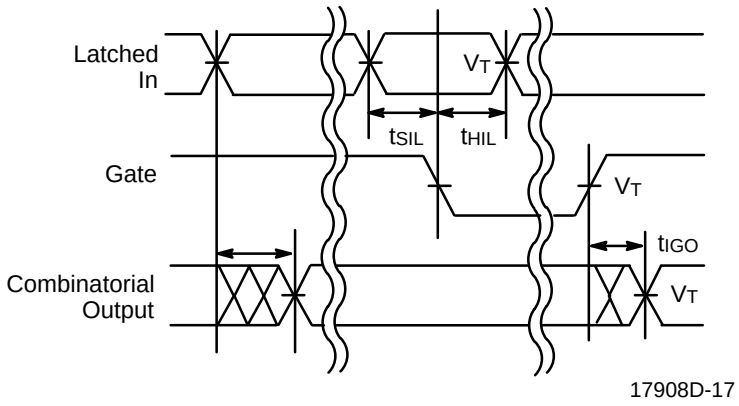
17908D-16

Input Register to Output Register Setup (MACH 2 and 4)

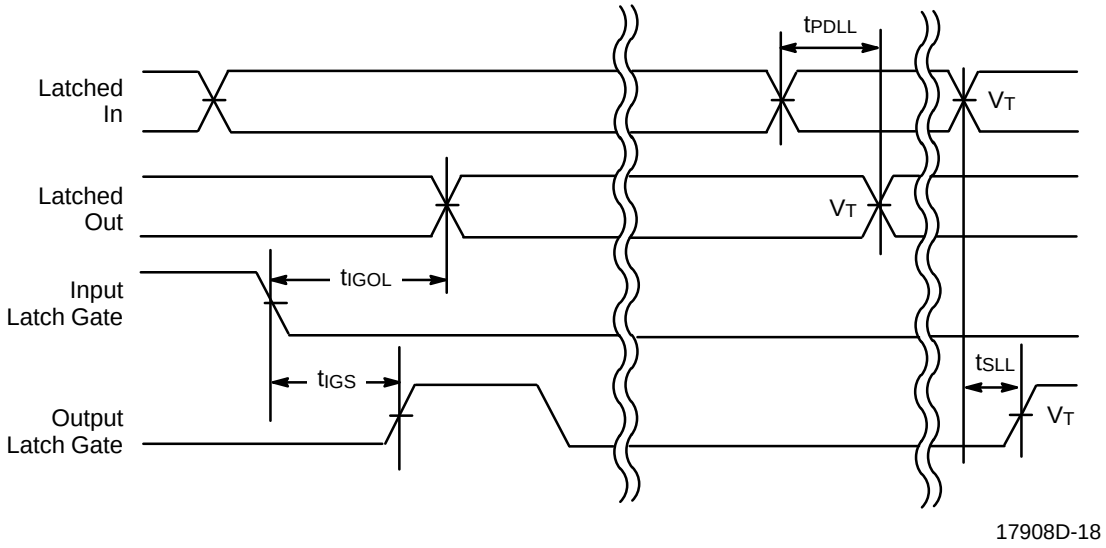
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



Latched Input (MACH 2 and 4)

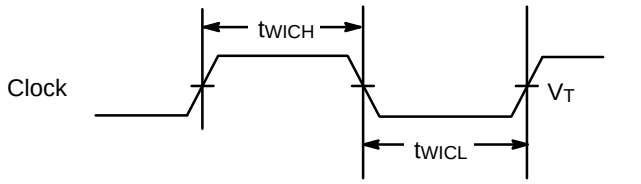


Latched Input and Output
(MACH 2, 3, and 4)

Notes:

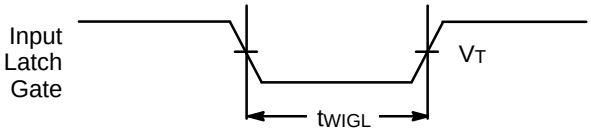
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



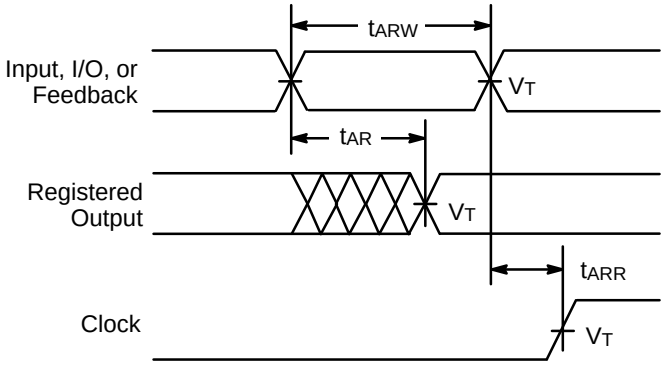
17908D-19

Input Register Clock Width (MACH 2 and 4)



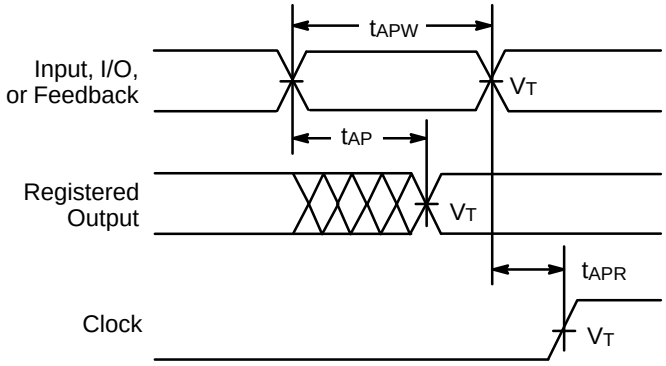
17908D-20

Input Latch Gate Width (MACH 2 and 4)



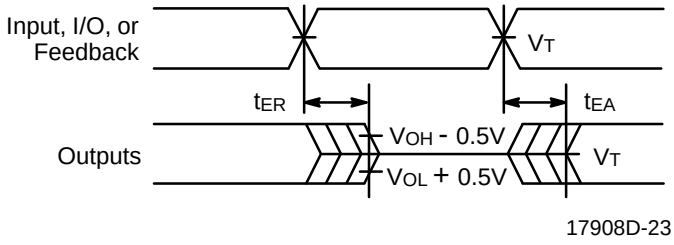
17908D-21

Asynchronous Reset



17908D-22

Asynchronous Preset



17908D-23

Output Disable/Enable

Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

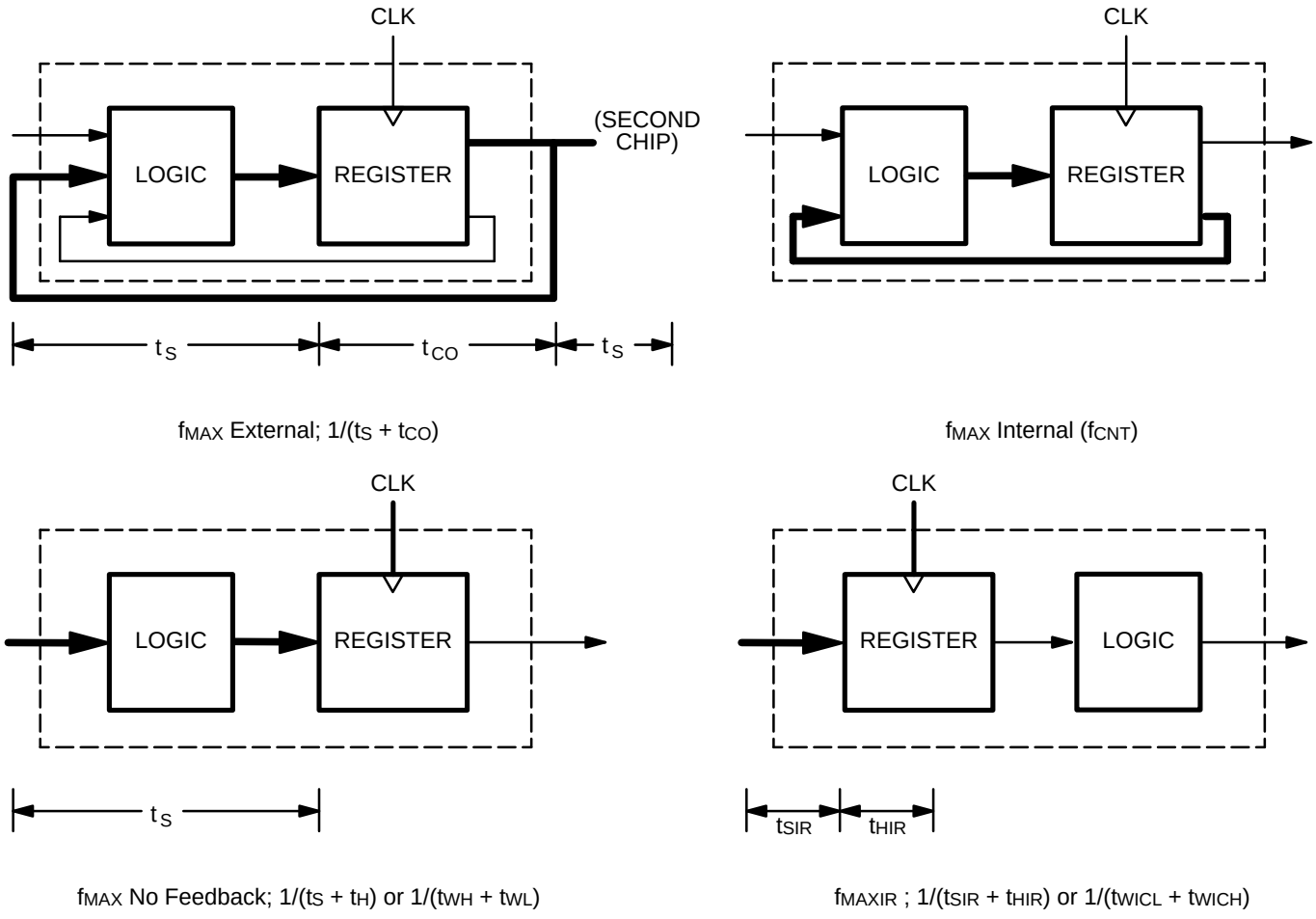
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



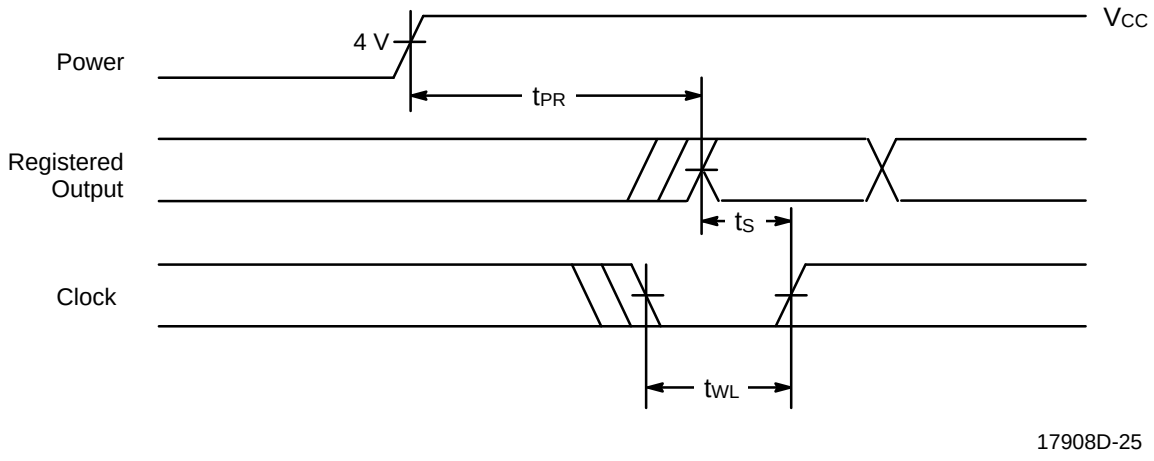
17908D-24

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

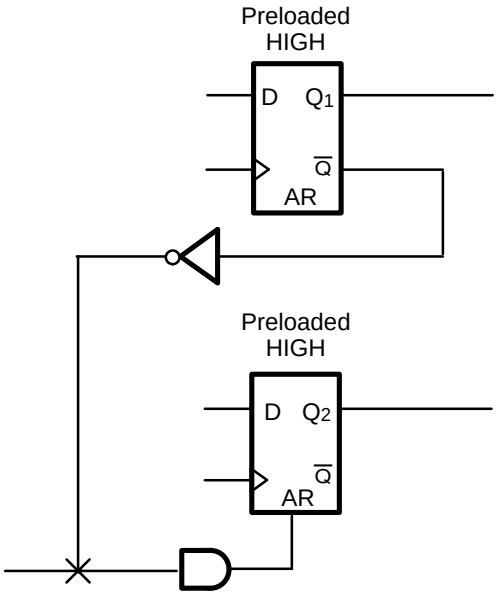
While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 2. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 3. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.



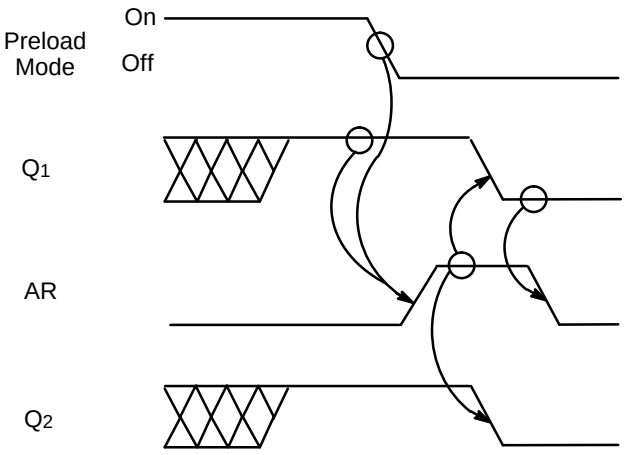


Figure 2. Preload/Reset Conflict

17908D-26

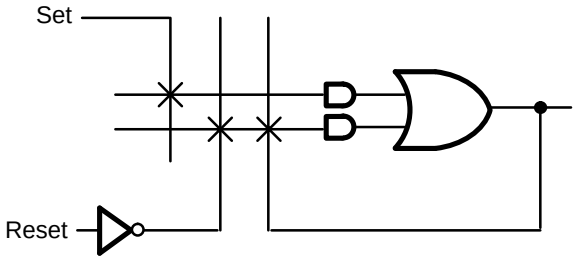
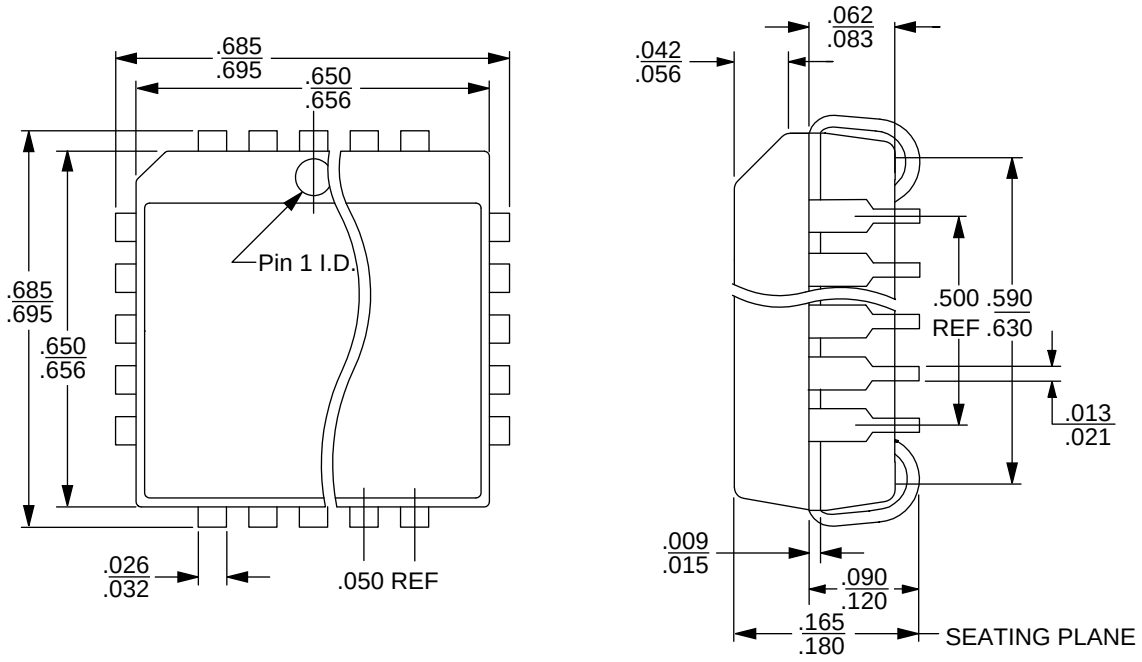


Figure 3. Combinatorial Latch

17908D-27

PHYSICAL DIMENSIONS*

PL 044
44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

SIDE VIEW

16-038-SQ
PL 044
DA78
6-28-94 ae

**For reference only. BSC is an ANSI standard for Basic Space Centering.*