300MHz to 4GHz Active Downconverting Mixer with Wideband IF

FEATURES

- **High IIP3: +26.9dBm at 1950MHz**
- **1.9dB Conversion Gain**
- **Low Noise Figure: 11.8dB at 1950MHz**
- **16.5dB NF Under 5dBm Blocking**
- **Low Power: 294mW**
- **Wide IF Frequency Range Up to 2.5GHz**
- LO Input 50Ω Matched when Shutdown
- –40°C to 105°C Operation (T_C)
- Very Small Solution Size
- Pin Compatible with LT5557
- 16-Lead (4mm × 4mm) QFN package

APPLICATIONS

- Wireless Infrastructure Receivers
- DPD Observation Receivers
- CATV Infrastructure

DESCRIPTION

The LTC®5567 is optimized for RF downconverting mixer applications that require wide IF bandwidth. The part is also a pin-compatible upgrade to the LT5557 active mixer, offering higher linearity and 1dB compression, wider bandwidth, and lower output spurious levels. Integrated RF and LO transformers and LO buffer amplifiers allow a very compact solution.

The RF input is 50Ω matched from 1.4GHz to 3GHz, and easily matched for higher or lower RF frequencies with simple external matching. The LO input is 50Ω matched from 1GHz to 4GHz, even when the IC is disabled. The LO input is easily matched for higher or lower frequencies, as low as 300MHz, with simple external matching. The low capacitance differential IF output is usable up to 2.5GHz.

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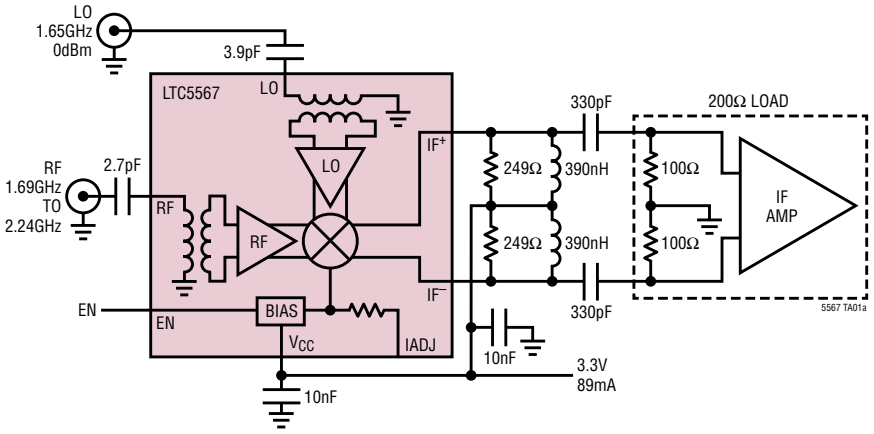
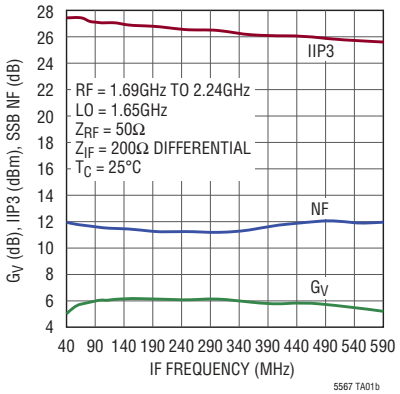
TYPICAL APPLICATION

DPD Observation Receiver Mixer with 500MHz IF Bandwidth and +13dBm Input P1dB into 200Ω Load



Voltage Conversion Gain, IIP3 and NF vs IF Frequency

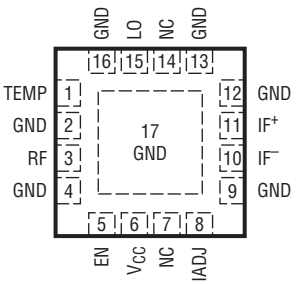


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}, IF^+, IF^-) 4.0V
Enable Input Voltage (EN) ..... –0.3V to V_{CC} + 0.3V
LO Input Power (300MHz to 4.5GHz) ..... +10dBm
LO Input DC Voltage ..... ±0.1V
RF Input Power (300MHz to 4GHz) ..... +15dBm
RF Input DC Voltage ..... ±0.1V
TEMP Monitor Input Current 10mA
Operating Temperature Range (T_C) ..... –40°C to 105°C
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5567IUF#PBF	LTC5567IUF#TRPBF	5567	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, EN = High. Test circuit shown in Figure 1.
(Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range			300 to 4000		MHz
LO Input Frequency Range			300 to 4500		MHz
IF Output Frequency Range	External Matching Required		5 to 2500		MHz
RF Input Return Loss	Z_0 = 50Ω, 1400MHz to 3000MHz, C3 = 2.7pF		>12		dB
LO Input Return Loss	Z_0 = 50Ω, 1000MHz to 4000MHz, C5 = 3.9pF		>10		dB
IF Output Impedance	Differential at 153MHz		532Ω||1.0pF		R||C
LO Input Power		–6	0	6	dBm
RF to LO Isolation	RF = 300MHz to 1000MHz RF = 1000MHz to 4000MHz		>59 >50		dB dB
RF to IF Isolation	RF = 300MHz to 700MHz RF = 700MHz to 1000MHz RF = 1000MHz to 4000MHz		>47 >40 >28		dB dB dB

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, EN = High. T_C = 25°C, P_{LO} = 0dBm, IF = 153MHz, P_{RF} = –6dBm (–6dBm/tone for 2-tone tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Conversion Gain	RF = 450MHz, High Side LO		1.5		dB
	RF = 850MHz, High Side LO		2.0		dB
	RF = 1950MHz, Low Side LO	0.8	1.9		dB
	RF = 2550MHz, Low Side LO		1.7		dB
	RF = 3500MHz, Low Side LO		1.2		dB
Conversion Gain Flatness	RF = 1950 ±30MHz, LO = 1797MHz, IF = 153 ±30MHz		±0.09		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 1950MHz, Low Side LO		–0.013		dB/°C
2-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	RF = 450MHz, High Side LO		26.0		dBm
	RF = 850MHz, High Side LO		26.7		dBm
	RF = 1950MHz, Low Side LO	24.2	26.9		dBm
	RF = 2550MHz, Low Side LO		26.0		dBm
	RF = 3500MHz, Low Side LO		26.5		dBm
2-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	RF = 450MHz (527MHz/373MHz), LO = 603MHz		67		dBm
	RF = 850MHz (927MHz/773MHz), LO = 1003MHz		64		dBm
	RF = 1950MHz (2027MHz/1873MHz), LO = 1797MHz		72		dBm
	RF = 2550MHz (2627MHz/2473MHz), LO = 2397MHz		71		dBm
	RF = 3500MHz (3577MHz/3423MHz), LO = 3347MHz		63		dBm
SSB Noise Figure	RF = 450MHz, High Side LO		12.5		dB
	RF = 850MHz, High Side LO		11.4		dB
	RF = 1950MHz, Low Side LO		11.8	13.5	dB
	RF = 2550MHz, Low Side LO		12.6		dB
	RF = 3500MHz, Low Side LO		14.6		dB
SSB Noise Figure Under Blocking	RF = 850MHz, High Side LO, 750MHz Blocker at 5dBm		16.5		dB
	RF = 1950MHz, Low Side LO, 2050MHz Blocker at 5dBm		16.5		dB
LO to RF Leakage	LO = 300MHz to 700MHz		<–62		dBm
	LO = 700MHz to 2200MHz		<–56		dBm
	LO = 2200MHz to 4500MHz		<–47		dBm
LO to IF Leakage	LO = 300MHz to 500MHz		<–43		dBm
	LO = 500MHz to 700MHz		<–37		dBm
	LO = 700MHz to 4500MHz		<–41		dBm
1/2IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: f_{RF} = 926.5MHz at –6dBm, f_{LO} = 1003MHz		–78		dBc
	1950MHz: f_{RF} = 1873.5MHz at –6dBm, f_{LO} = 1797MHz		–73		dBc
1/3IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	850MHz: f_{RF} = 952MHz at –6dBm, f_{LO} = 1003MHz		–82		dBc
	1950MHz: f_{RF} = 1848MHz at –6dBm, f_{LO} = 1797MHz		–80		dBc
Input 1dB Compression	RF = 450MHz, High Side LO		11.0		dBm
	RF = 850MHz, High Side LO		10.9		dBm
	RF = 1950MHz, Low Side LO		10.1		dBm
	RF = 2550MHz, Low Side LO		10.2		dBm
	RF = 3500MHz, Low Side LO		10.4		dBm

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, T_C = 25°C. Test circuit shown in Figure 1. (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})			3.0	3.3	3.6	V
Supply Current	Enabled Disabled	EN = High EN = Low		89	105 100	mA µA
Enable Logic Input (EN)						
Input High Voltage (On)			2.5			V
Input Low Voltage (Off)					0.3	V
Input Current		–0.3V to V_{CC} + 0.3V	–30		100	µA
Turn-On Time				0.6		µs
Turn-Off Time				0.5		µs
Mixer DC Current Adjust (IADJ)						
Open-Circuit DC Voltage				2.2		V
Short-Circuit DC Current		Pin Shorted to Ground		1.8		mA
Temperature Sensing Diode (TEMP)						
DC Voltage at T_J = 25°C		I_{IN} = 10µA I_{IN} = 80µA		716 773		mV mV
Voltage Temperature Coefficient		I_{IN} = 10µA I_{IN} = 80µA		–1.75 –1.56		mV/°C mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5567 is guaranteed functional over the –40°C to 105°C case temperature range (θ_{JC} = 8°C/W).

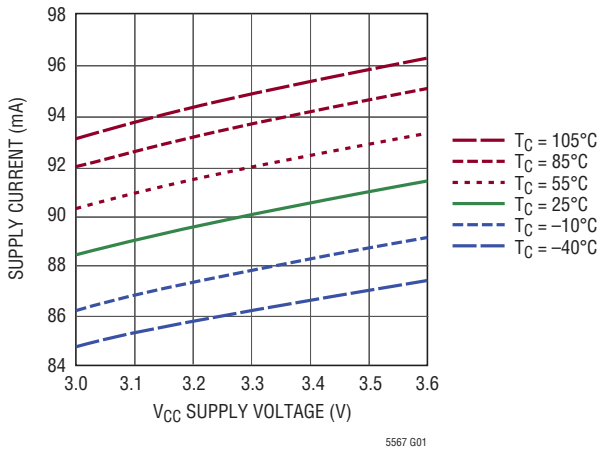
Note 3: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

Note 4: Specified performance includes 4:1 IF transformer and evaluation PCB losses.

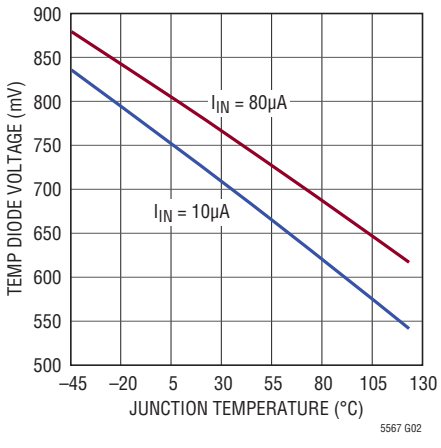
TYPICAL DC PERFORMANCE CHARACTERISTICS

EN = High, Test circuit shown in Figure 1.

Supply Current vs Supply Voltage



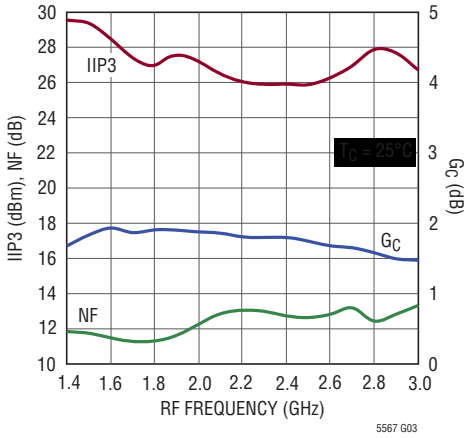
TEMP Diode Voltage vs Junction Temperature



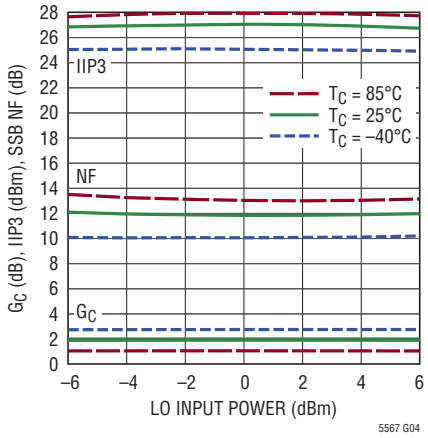
TYPICAL PERFORMANCE CHARACTERISTICS

1400MHz to 3000MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz unless otherwise noted.

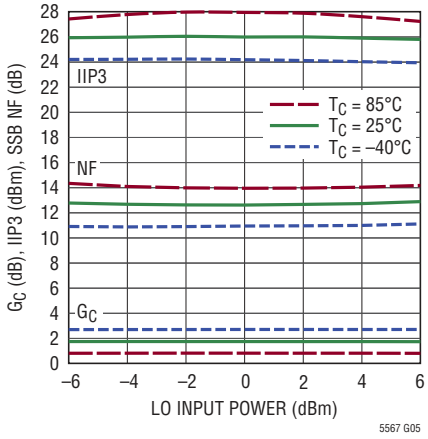
Conversion Gain, IIP3 and NF vs RF Frequency (Low Side LO)



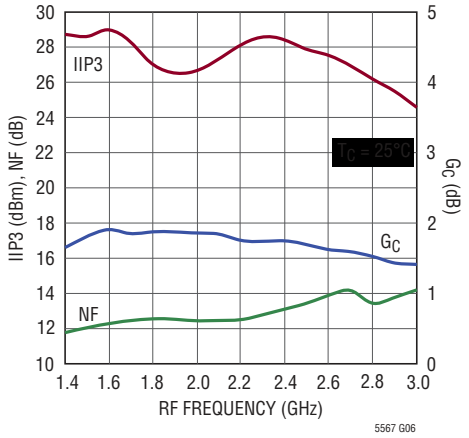
1950MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



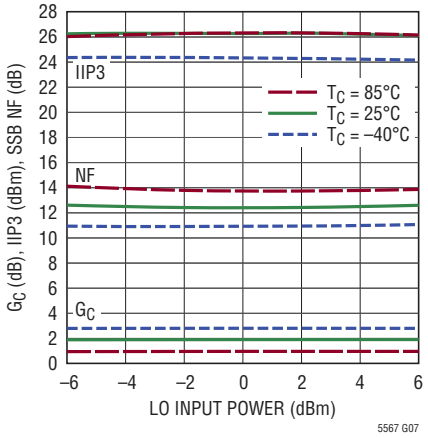
2550MHz Conversion Gain, IIP3 and NF vs LO Power (Low Side LO)



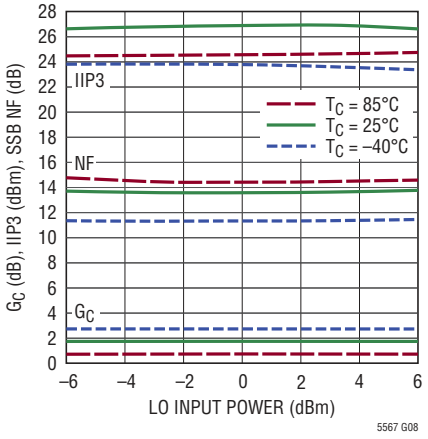
Conversion Gain, IIP3 and NF vs RF Frequency (High Side LO)



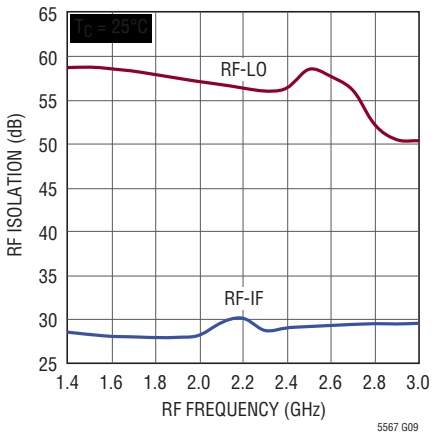
1950MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



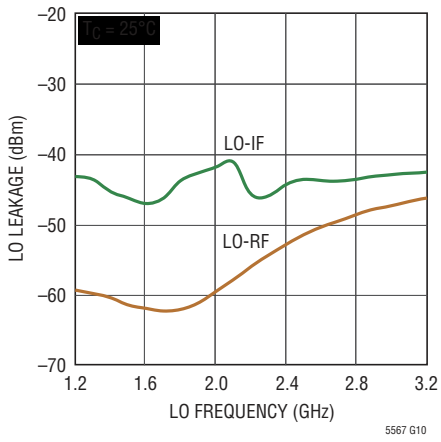
2550MHz Conversion Gain, IIP3 and NF vs LO Power (High Side LO)



RF Isolation vs RF Frequency



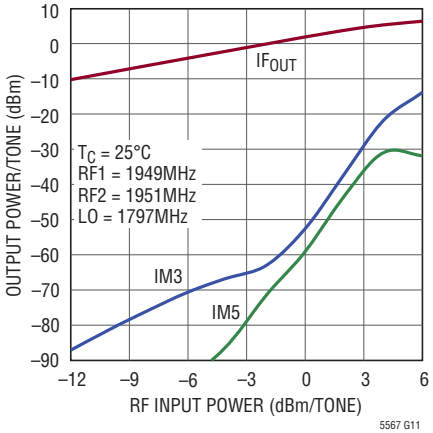
LO Leakage vs LO Frequency



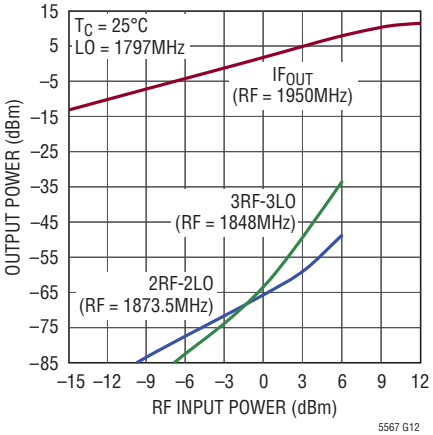
TYPICAL PERFORMANCE CHARACTERISTICS

1400MHz to 3000MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz unless otherwise noted.

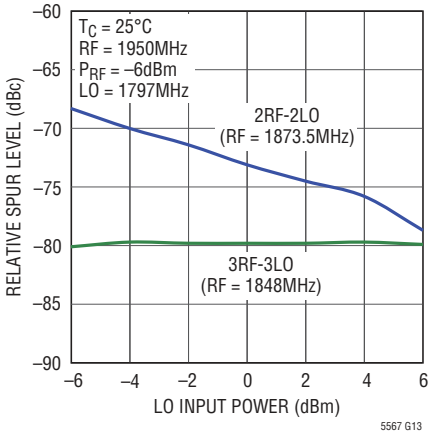
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



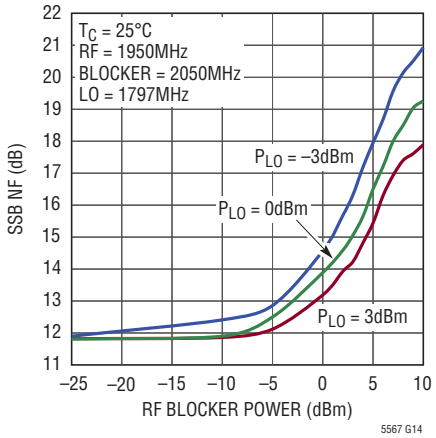
Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



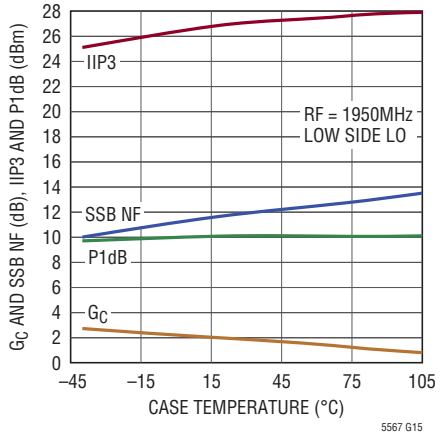
2 × 2 and 3 × 3 Spur Suppression vs LO Power



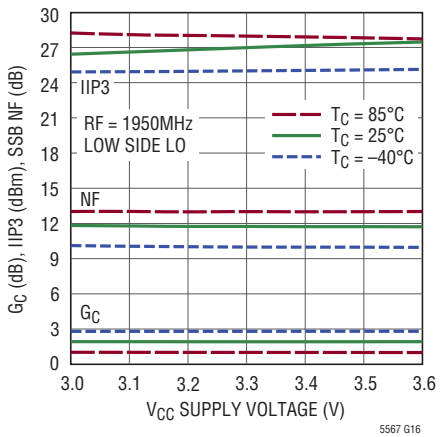
SSB Noise Figure vs RF Blocker Level



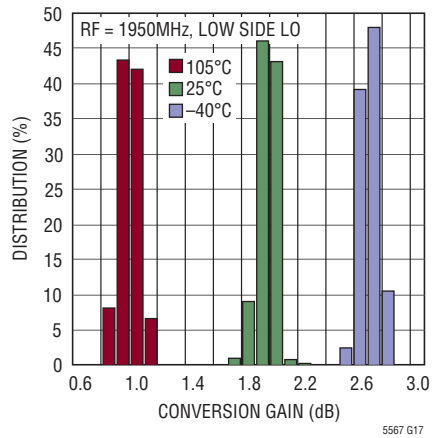
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



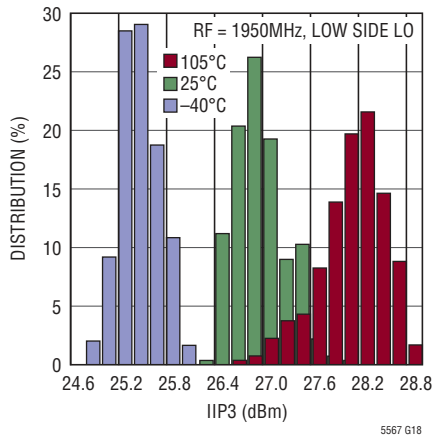
Conversion Gain, IIP3 and NF vs Supply Voltage



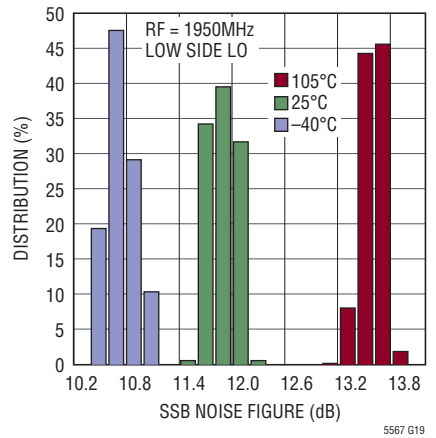
1950MHz Conversion Gain Distribution



1950MHz IIP3 Distribution



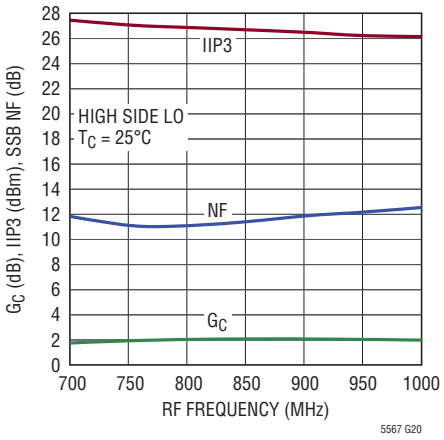
1950MHz SSB NF Distribution



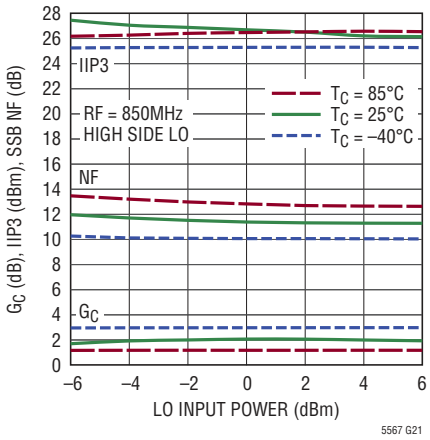
TYPICAL PERFORMANCE CHARACTERISTICS

700MHz to 1000MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz unless otherwise noted.

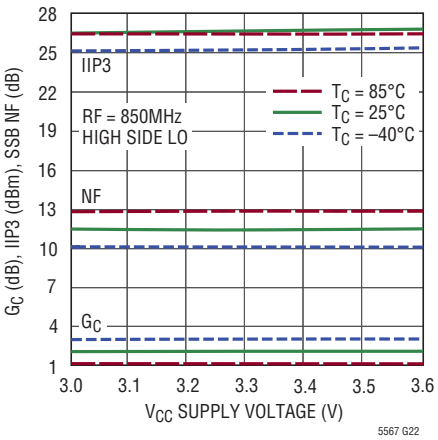
Conversion Gain, IIP3 and NF vs RF Frequency



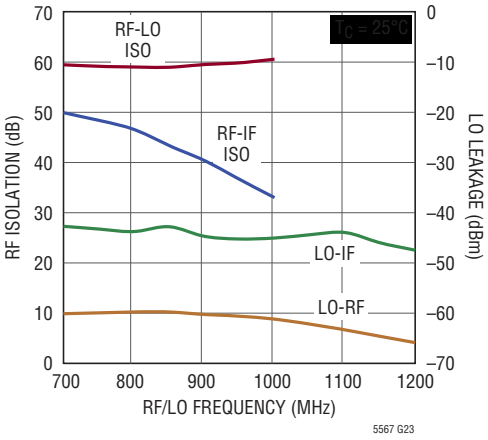
850MHz Conversion Gain, IIP3 and NF vs LO Power



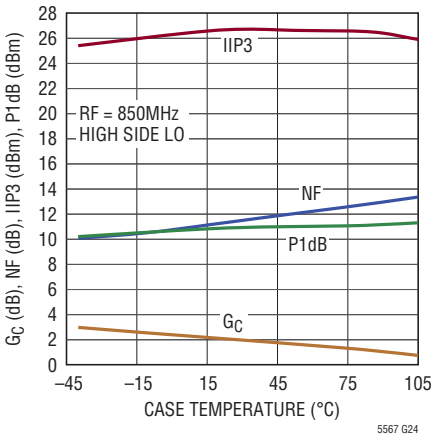
850MHz Conversion Gain, IIP3 and NF vs Supply Voltage



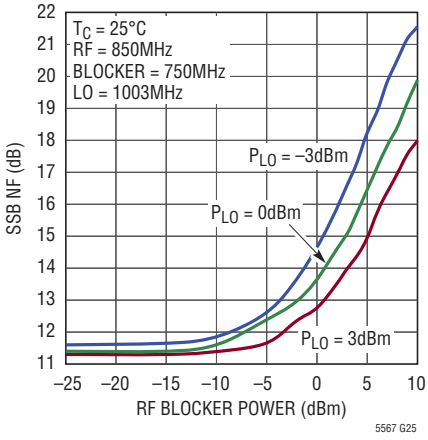
RF Isolation and LO Leakage vs Frequency



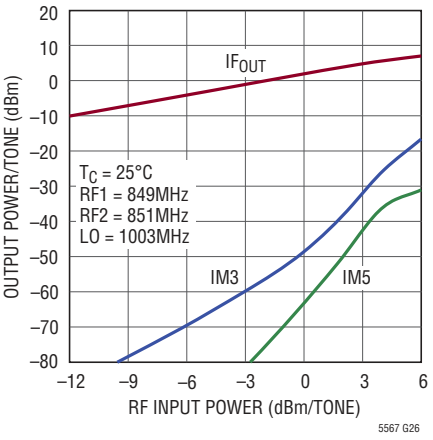
Conversion Gain, IIP3, NF and RF Input P1dB vs Temperature



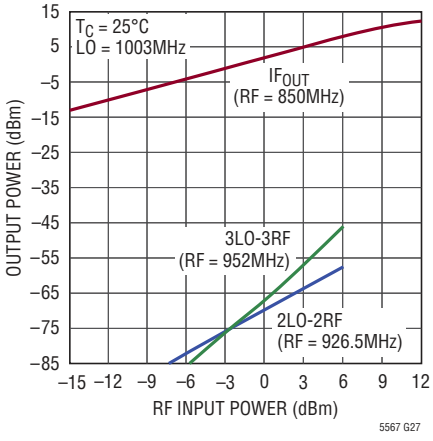
SSB Noise Figure vs RF Blocker Level



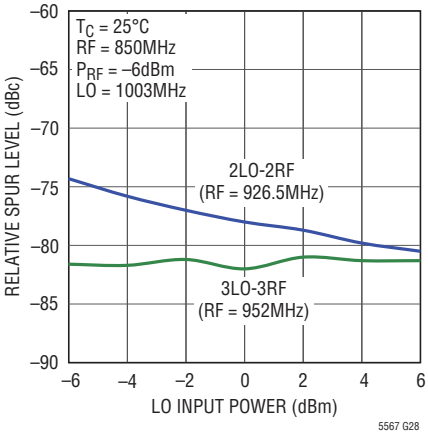
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



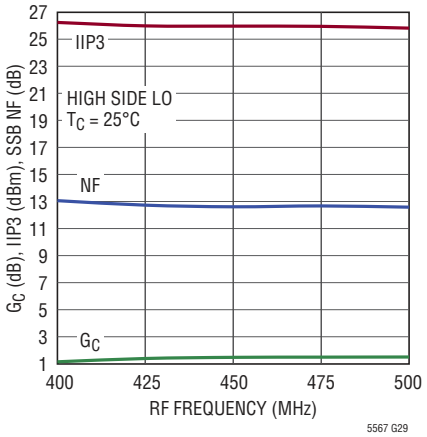
2 × 2 and 3 × 3 Spur Suppression vs LO Power



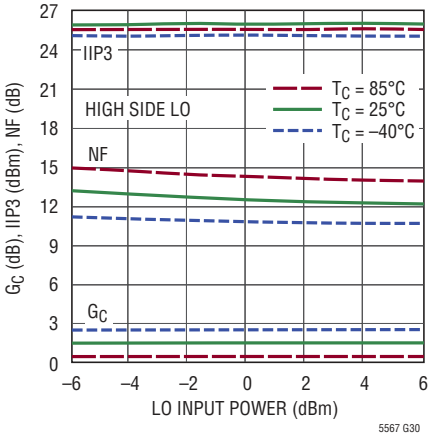
TYPICAL PERFORMANCE CHARACTERISTICS

400MHz to 500MHz application. Test circuit shown in Figure 1. V_{CC} = 3.3V, P_{LO} = 0dBm, P_{RF} = –6dBm (–6dBm/tone for 2-tone IIP3 tests, Δf = 2MHz), IF = 153MHz unless otherwise noted.

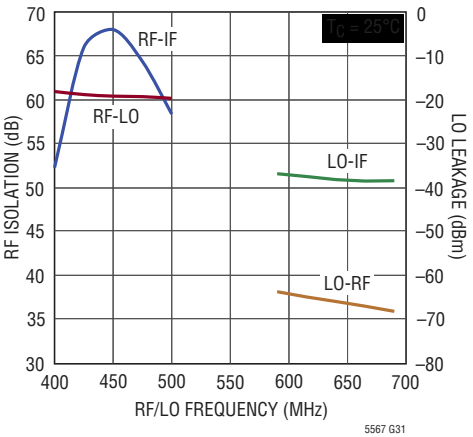
Conversion Gain, IIP3 and NF vs RF Frequency



450MHz Conversion Gain, IIP3 and NF vs LO Power

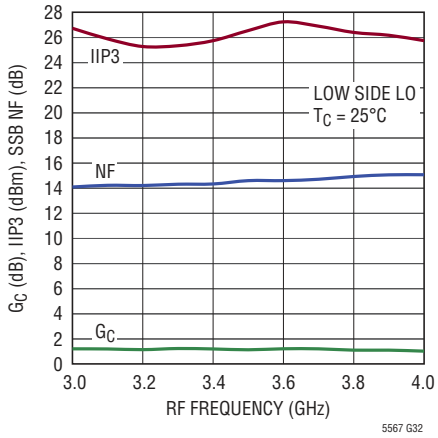


RF Isolation and LO Leakage vs RF and LO Frequency

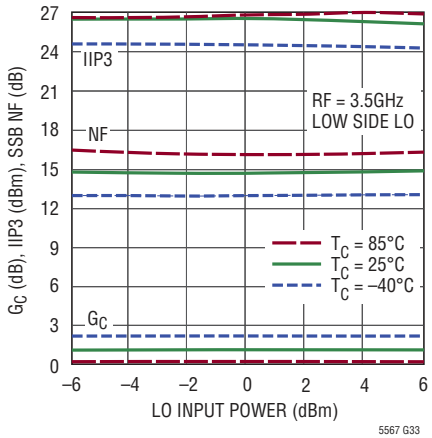


3GHz to 4GHz application. Test circuit shown in Figure 1.

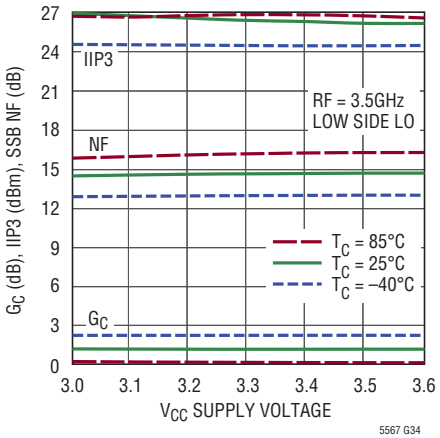
Conversion Gain, IIP3 and NF vs RF Frequency



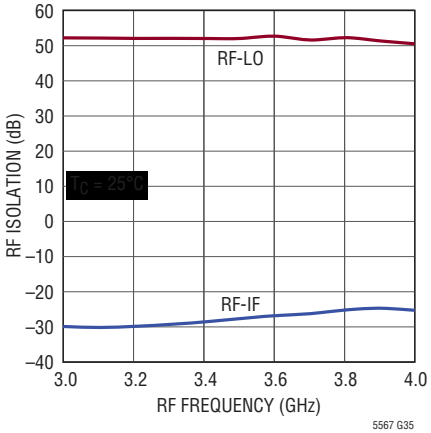
3500MHz Conversion Gain, IIP3 and NF vs LO Power



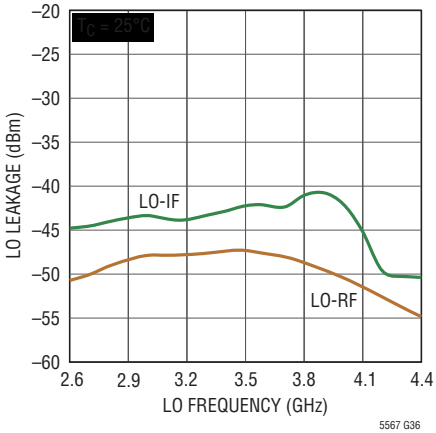
3500MHz Conversion Gain, IIP3 and NF vs Supply Voltage



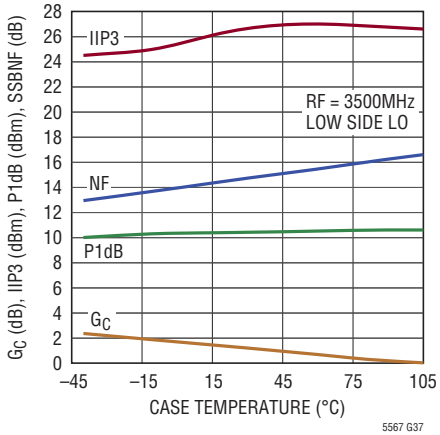
RF Isolation vs RF Frequency



LO leakage vs LO Frequency



Conversion Gain, IIP3 and RF Input P1dB vs Temperature



PIN FUNCTIONS

TEMP (Pin 1): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage.

GND (Pins 2, 4, 9, 12, 13, 16, Exposed Pad Pin 17): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

RF (Pin 3): Single-Ended RF Input. This pin is internally connected to the primary winding of the integrated RF transformer, which has low DC resistance to ground. **A series DC-blocking capacitor must be used if the RF source has DC voltage present.** The RF input is 50Ω impedance matched from 1.4GHz to 3GHz, as long as the mixer is enabled. Operation down to 300MHz or up to 4GHz is possible with external matching.

EN (Pin 5): Enable Pin. When the input voltage is greater than 2.5V, the mixer is enabled. When the input voltage is less than 0.3V, the mixer is disabled. Typical input current is less than 30µA. This pin has an internal pull-down resistor.

V_{CC} (Pin 6): Power Supply Pin. This pin must be connected to a regulated 3.3V supply, with a bypass capacitor located close to the pin. Typical DC current consumption is 34mA.

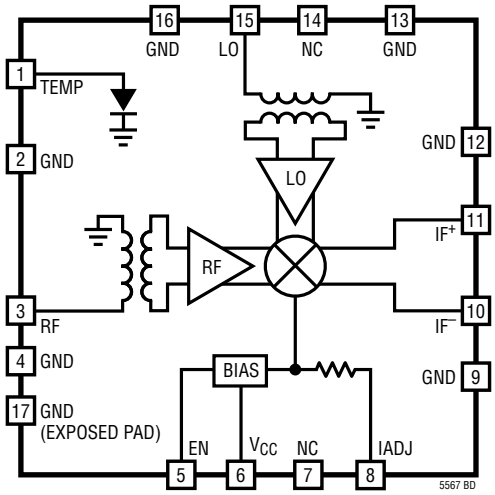
NC (Pins 7, 14): These pins are not connected internally. They can be left floating, connected to ground, or to V_{CC}.

IADJ (Pin 8): This pin allows adjustment of the mixer DC supply current. Typical open-circuit DC voltage is 2.2V. This pin should be left floating for optimum performance.

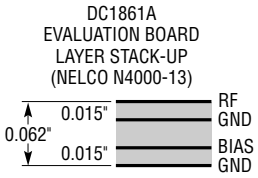
IF^+/IF^- (Pin 11/Pin 10): Open-Collector Differential IF Output. These pins must be connected to the V_{CC} supply through impedance-matching inductors or a transformer center tap. Typical DC current consumption is 27.5mA into each pin.

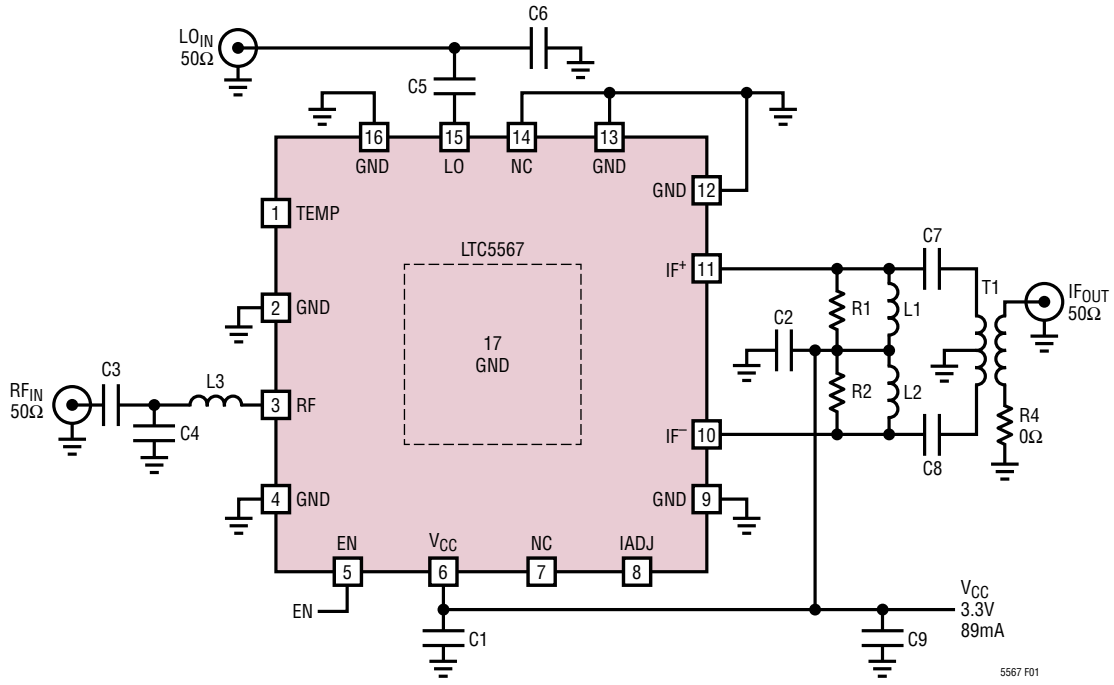
LO (Pin 15): Single-Ended Local Oscillator Input. This pin is internally connected to the primary winding of an integrated transformer, which has low DC resistance to ground. **A series DC-blocking capacitor must be used to avoid damage to the internal transformer.** This input is 50Ω impedance matched from 1GHz to 4GHz, even when the IC is disabled. Operation down to 300MHz or up to 4.5GHz is possible with external matching.

BLOCK DIAGRAM



TEST CIRCUIT





APPLICATION		RF MATCH			LO MATCH	
RF (MHz)	LO	C3	C4	L3	C5	C6
300 to 400	HS	120pF	18pF	2.2nH	47pF	15pF
400 to 500	HS	120pF	12pF	2nH	27pF	10pF
700 to 1000	HS	120pF	4.7pF	—	6.8pF	2.7pF
1400 to 3000	LS, HS	2.7pF	—	—	3.9pF	—
3000 to 4000	LS	3.9pF	0.7pF	—	3.9pF	—

LS = Low side, HS = High side

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C1, C2	10nF	0402	AVX	C9	1µF	0603	AVX
C3 - C6	See Table	0402	AVX	T1	4:1	—	Mini-Circuits TC8-1-10LN+
C7, C8	330pF	0402	AVX	L1, L2	300nH	0603	Coilcraft 0603HP
R1, R2	3.01k, 1%	0402		L3	See Table	0402	Coilcraft 0402HP

Figure 1. Standard Downmixer Test Circuit Schematic (153MHz Bandpass IF Matching)

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Introduction

The LTC5567 incorporates a high linearity double-balanced active mixer, a high-speed limiting LO buffer and bias/enable circuits. See the Pin Functions and Block Diagram sections for a description of each pin. A test circuit schematic showing all external components required for the data sheet specified performance is shown in Figure 1. A few additional components may be used to modify the DC supply current or frequency response, which will be discussed in the following sections.

The LO and RF inputs are single ended. The IF output is differential. Low side or high side LO injection may be used. The test circuit, shown in Figure 1, utilizes bandpass IF output matching and an 8:1 IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

RF Input

A simplified schematic of the mixer's RF input is shown in Figure 3. As shown, one terminal of the integrated RF transformer's primary winding is connected to Pin 3, while the other terminal is DC-grounded internally. For this reason, a series DC-blocking capacitor (C3) is needed if the RF source has DC voltage present. The DC resistance of the primary winding is approximately 4Ω. The secondary winding of the RF transformer is internally connected to the RF buffer amplifier.

The RF input is 50Ω matched from 1400MHz to 3000MHz with a single 2.7pF series capacitor on the input. Matching to RF frequencies above or below this frequency range is easily accomplished by adding shunt capacitor C4, shown in Figure 3. For RF frequencies below 500MHz, series

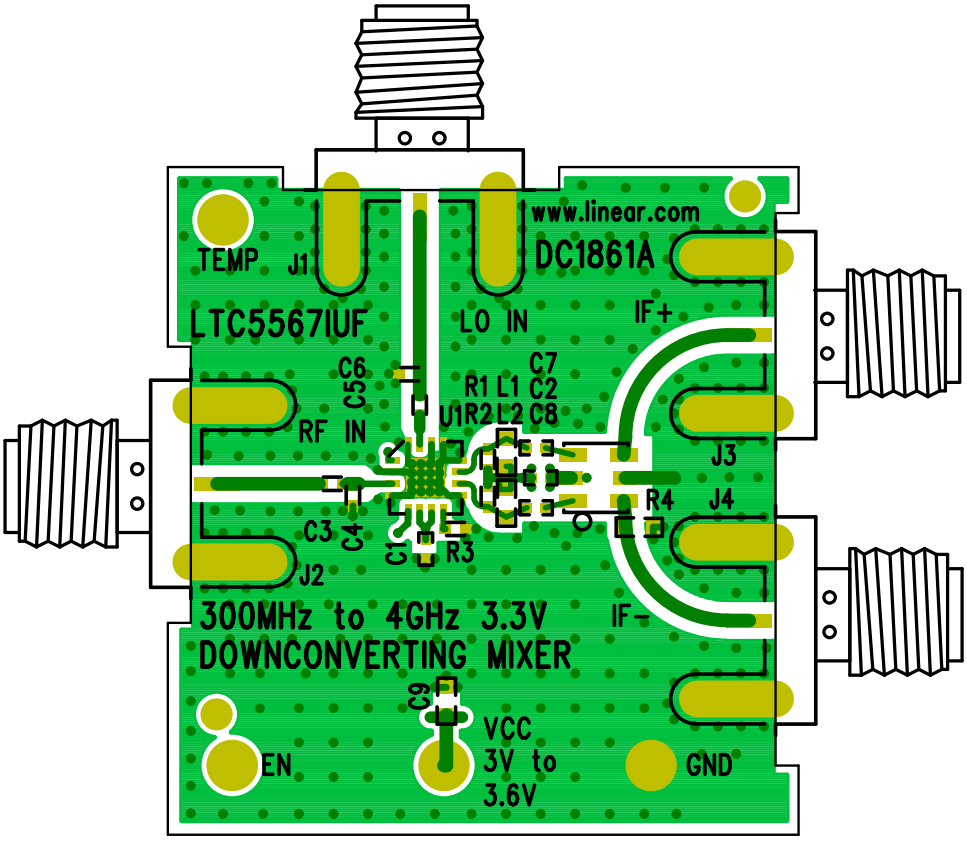

Figure 2. Evaluation Board Layout

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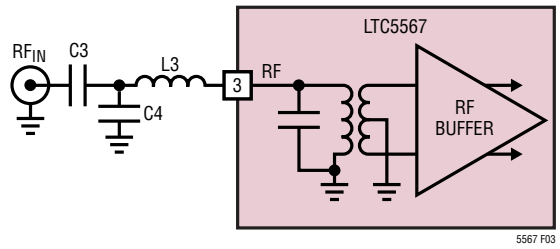

Figure 3. RF Input Schematic

inductor L3 is also needed. The evaluation board does not have provisions for L3, so the RF input trace needs to be cut to install it in series. The RF input matching element values for each application are tabulated in Figure 1. Measured RF input return losses are shown in Figure 4. The RF input impedance and input reflection coefficient, versus frequency are listed in Table 1.

Table 1. RF Input Impedance and S11 (At Pin 3, No External Matching, Mixer Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
200	6.0 + j8.0	0.79	161.6
350	9.0 + j11.9	0.71	152.1
450	11.0 + j14.1	0.66	147.0
575	13.3 + j15.9	0.61	142.5
700	15.4 + j17.5	0.57	138.1
900	18.5 + j20.0	0.52	131.1
1100	21.7 + j22.0	0.48	125.1
1400	27.4 + j24.2	0.41	115.6
1700	33.7 + j24.2	0.33	107.9
1950	39.1 + j21.6	0.26	103.1
2200	42.6 + j16.1	0.19	104.9
2450	42.6 + j9.9	0.13	120.8
2700	38.8 + j4.3	0.14	155.9
3000	31.9 + j2.3	0.22	171.3
3300	24.8 + j4.0	0.34	167.9
3600	19.5 + j8.2	0.45	158.3
3900	15.4 + j13.4	0.56	147.3
4200	12.6 + j18.7	0.64	136.8
4500	10.9 + j24.2	0.70	126.6

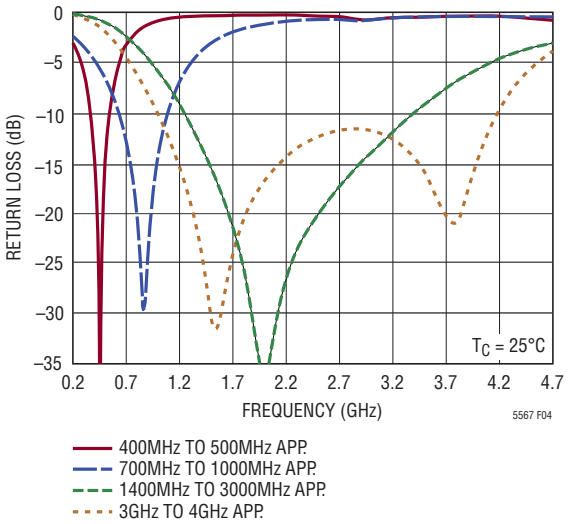

Figure 4. RF Input Return Loss

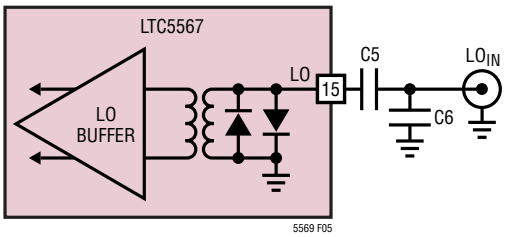

Figure 5. LO Input Schematic

LO Input

A simplified schematic of the LO input, with external components is shown in Figure 5. Similar to the RF input, the integrated LO transformer's primary winding is DC-grounded internally, and therefore requires an external DC-blocking capacitor. Capacitor C5 provides the necessary DC-blocking, and optimizes the LO input match over the 1GHz to 4GHz frequency range. The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±5dB input power range. LO input power greater than +6dBm may cause conduction of the internal ESD diodes.

To optimize the LO input match for frequencies below 1GHz, the value of C5 is increased and shunt capacitor C6 is added. A summary of values for C5 and C6, versus LO

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frequency range is listed in Table 2. Measured LO input return losses are shown in Figure 6. Finally, LO input impedance and input reflection coefficient, versus frequency is shown in Table 3.

Table 2. LO Input Matching Values vs LO Frequency Range

FREQUENCY (MHz)	C5 (pF)	C6 (pF)
285 to 392	330	33
338 to 415	330	22
415 to 505	56	18
525 to 635	27	10
645 to 803	15	7.5
800 to 1150	6.8	2.7
1000 to 4000	3.9	—
3000 to 4500	1.8	0.2

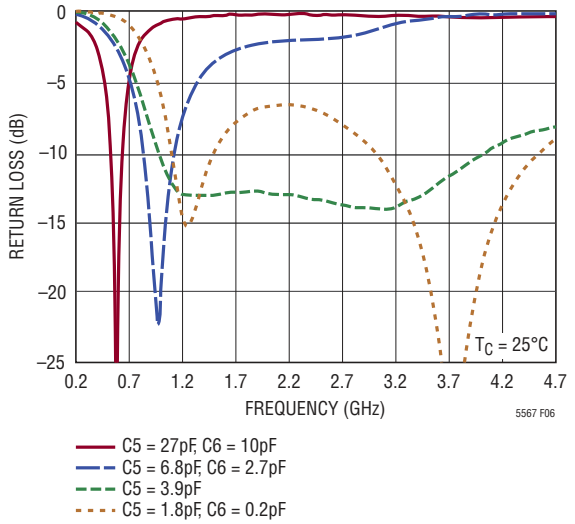

Figure 6. LO Input Return Loss

The LO buffers have been designed such that the LO input impedance does not change significantly when the IC is disabled. This feature only requires that supply voltage is applied. The actual performance of this feature is shown in Figure 7. As shown, the LO input return loss is better than 10dB over the 1GHz to 4GHz frequency range when the IC is enabled or disabled.

Table 3. LO Input Impedance and S11 (At Pin 15, No External Matching, Mixer Enabled)

FREQUENCY (MHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
350	5.2 + j14.9	0.83	146.5
400	6.0 + j17.3	0.81	141.7
450	6.6 + j19.5	0.80	137.0
500	7.2 + j21.5	0.78	132.7
600	9.1 + j26.5	0.75	123.6
800	15.1 + j35.7	0.67	106.0
1000	24.9 + j43.6	0.58	89.5
1500	67.5 + j36.4	0.33	47.1
2000	61.7 – j4.2	0.11	–18.3
2500	40.3 – j7.1	0.13	–139.4
3000	31.7 + j1.8	0.23	173.1
3500	29.8 + j12.3	0.29	140.0
4000	31.5 + j22.9	0.35	113.2
4500	36.0 + j32.4	0.38	92.8

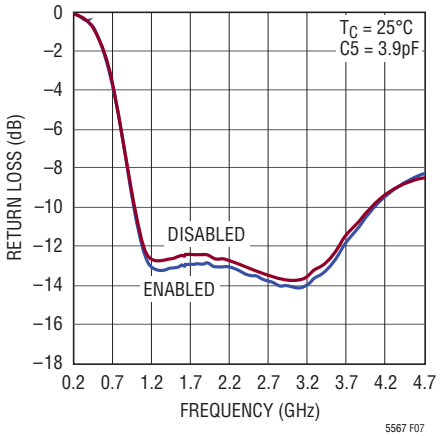

Figure 7. LO Input Return Loss—Mixer Enabled and Disabled

IF Output

The IF output schematic with external matching components is shown in Figure 8. As shown, the output is differential open collector. Each IF output pin must be biased at the supply voltage (V_{CC}), which is applied through the external matching inductors (L1 and L2) shown in Figure 8. Each pin draws approximately 27.5mA of DC supply current (55mA total).

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The differential IF output impedance can be modeled as a frequency-dependent parallel R-C circuit, using the values listed in Table 4. This data is referenced to the package pins (with no external components) and includes the effects of the IC and package parasitics. Resistors R1 and R2 are used to reduce the output resistance, which increases the IF bandwidth and input P1dB, but reduces the conversion gain. The standard downmixer test circuit shown in Figure 1 uses bandpass matching and 3.01k resistors to realize a 400Ω differential output, followed by an 8:1 transformer to get a 50Ω single-ended output. C7 and C8 are 330pF DC-blocking capacitors. The values of L1 and L2 are calculated to resonate with the internal IF capacitance (C_{IF}) at the desired IF center frequency, using the following equation:

$$L1, L2 = \frac{1}{(2 \bullet \pi \bullet f_{IF})^2 \bullet 2 \bullet C_{IF}}$$

For IF frequencies below 100MHz, the inductor values become unreasonably high and the highpass impedance matching network described in a later section is preferred, due to its lower inductor values.

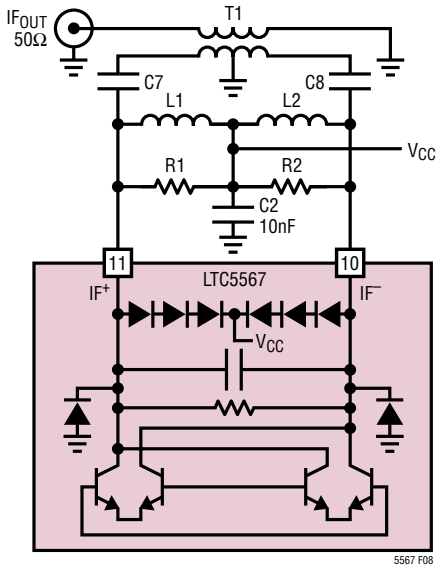

Figure 8. IF Output Schematic with External Matching

Table 4 summarizes the optimum IF matching inductor values, versus IF center frequency, to be used in the standard downmixer test circuit shown in Figure 1. The measured 1dB (conversion gain) IF frequency range for each inductor value is shown. The inductor values listed are less than the ideal calculated values due to the additional capacitance of the 8:1 transformer. For differential IF output applications where the 8:1 transformer is eliminated, the ideal calculated values should be used. Measured IF output return losses are shown in Figure 9.

Table 4. IF Output Impedance and Bandpass Matching Element Values vs IF Frequency.

IF FREQUENCY (MHz)	DIFFERENTIAL IF OUTPUT IMPEDANCE (R_{IF}||C_{IF})	IF MATCHING USING TC8-1	
		L1, L2	1dB IF FREQUENCY RANGE (MHz)
140	532Ω||1.0pF	390nH	65 to 327
153	532Ω||1.0pF	300nH	84 to 350
190	530Ω||1.0pF	210nH	107 to 375
250	525Ω||1.0pF	120nH	160 to 415
380	511Ω||1.0pF	51nH	288 to 520
500	500Ω||1.03pF		
1000	454Ω||1.07pF		
1500	364Ω||1.12pF		
2000	268Ω||1.24pF		
2500	209Ω||1.41pF		

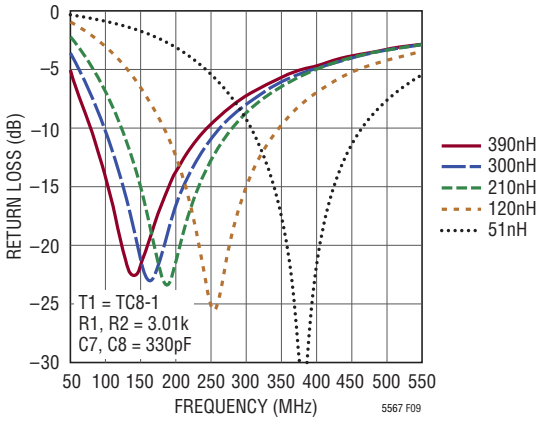

Figure 9. IF Output Return Loss—400Ω Bandpass Matching with 8:1 Transformer

Wideband Differential IF Output

Wide IF bandwidth and high input 1dB compression are obtained by reducing the IF output resistance with resistors R1 and R2. This will reduce the mixer's conversion gain, but will not degrade the IIP3 or noise figure.

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The IF matching shown in Figure 10 uses 249Ω resistors and 390nH supply chokes to produce a wideband 200Ω differential output. This differential output is suitable for driving a wideband differential amplifier, filter, or a wideband 4:1 transformer. The evaluation board layout allows the removal of the IF transformer to evaluate the mixer performance with a differential output.

The complete test circuit, shown in Figure 11, uses resistive impedance matching attenuators (L-pads) on the evaluation board to transform each 100Ω IF output to 50Ω. An external 0°/180° power combiner is then used to convert the 100Ω differential output to 50Ω single-ended, to facilitate measurement.

Table 5 compares the IF bandwidth and 1dB compression for the standard 400Ω and wideband 200Ω IF output resistances. As shown, the 200Ω matching doubles the IF bandwidth, and increases the RF input P1dB to +13dBm.

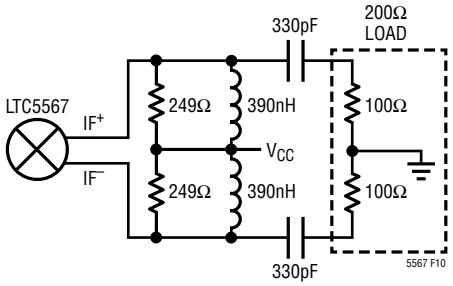

Figure 10. Wideband 200Ω Differential Output

Table 5. IF Bandwidth and 1dB Compression for 400Ω and 200Ω Differential IF Output Resistance (RF = 1.69 to 2.24GHz, LO = 1.65GHz, V_{CC} = 3.3V, T_C = 25°C, L1, L2 = 390nH)

R_{OUT} (Ω)	R1, R2 (Ω)	P1dB (dBm)	1dB (CONVERSION GAIN) IF FREQUENCY RANGE
400	3.01k	10.1	65MHz to 327MHz
200	249	13.0	45MHz to 580MHz

Measured voltage conversion gain, IIP3 and SSB noise figure, at the 200Ω differential output are plotted in Figure 12. Voltage gain, rather than power gain, is plotted to emphasize the voltage gain due to the 200Ω output. As shown, the conversion gain is flat within 1dB over the 45MHz to 590MHz IF output frequency range.

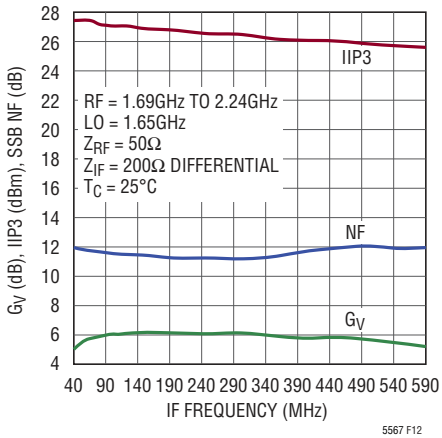

Figure 12. Voltage Conversion Gain, IIP3 and NF vs IF Output Frequency for Wideband 200Ω Differential IF

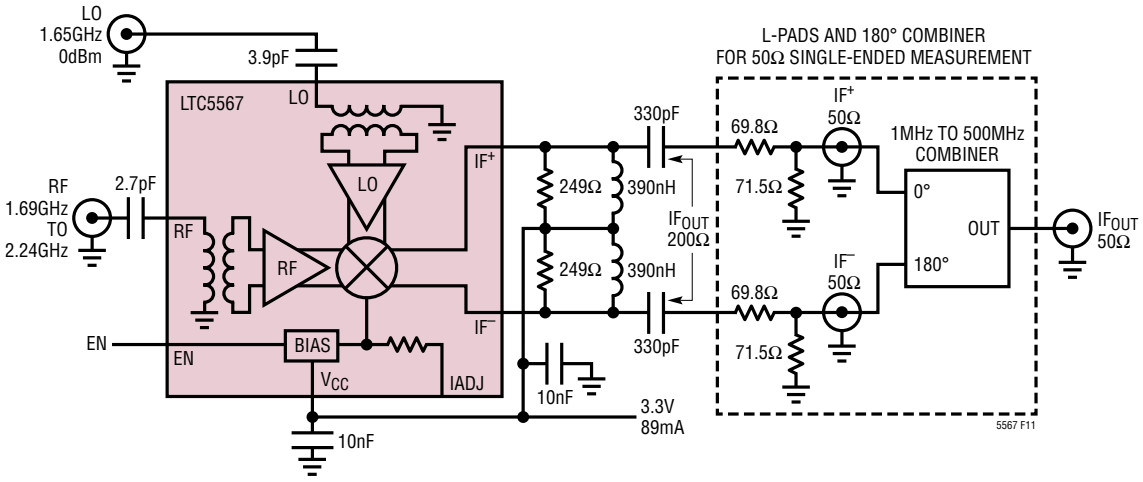

Figure 11. Test Circuit for Wideband 200Ω Differential Output

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Highpass IF Matching

By simply changing component values, the bandpass IF output matching network can be changed to a highpass impedance transforming network. This matching network will drive a lower impedance differential load (or transformer), like the 200Ω wideband bandpass matching previously described, while delivering higher conversion gain, similar to the 400Ω bandpass matching. The highpass matching network will have less IF bandwidth than the bandpass matching. It also uses smaller inductance values; an advantage when designing for IF center frequencies well below 100MHz.

Referring to the small-signal output network schematic in Figure 13, the reactive matching element values (L1, L2, C7 and C8) are calculated using the following equations. The source resistance (R_S) is the parallel combination of external resistors R1 + R2 and the internal IF resistance, R_{IF} taken from Table 4. The differential load resistance (R_L) is typically 200Ω, but can be less. C_{IF}, the IF output capacitance, is taken from Table 4. Choosing R_S in the 380Ω to 450Ω range will yield power conversion gains around 2dB.

$$R_S = R_{IF} \,||\, 2 \cdot R1 \qquad (R1 = R2)$$

$$Q = \sqrt{(R_S/R_L - 1)} \qquad (R_S > R_L)$$

$$Y_L = Q/R_S + (\omega_{IF} \bullet C_{IF})$$

$$L1, L2 = 1/(2 \bullet Y_L \bullet \omega_{IF})$$

$$C7, C8 = 2/(Q \bullet R_L \bullet \omega_{IF})$$

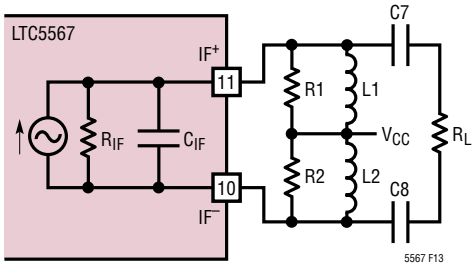

Figure 13. IF Output Circuit for Highpass Matching Element Value Calculations

To demonstrate the highpass impedance transformer output matching, these equations were used to calculate the element values for a 153MHz IF frequency and 200Ω differential load resistance. The output matching on the wideband test circuit, shown in Figure 11, was modified with the following new element values, and re-tested.

L1, L2 = 150nH

C7, C8 = 10pF

R1, R2 = 1.1k

Measured voltage conversion gain for the highpass and wideband bandpass methods are shown in Figure 14, for comparison. Both circuits are driving a 200Ω differential load, but the highpass version delivers 2.3dB of additional gain at 153MHz. Measured performance for both circuits is summarized in Table 6. As shown, the highpass method has less than half the IF bandwidth, and 3dB lower P1dB.

Table 6. Measured Performance Comparison for Highpass and Wideband IF Matching (RF = 1950MHz, IF = 153MHz, Low Side LO).

IF MATCHING	G_V (dB)	IIP3 (dBm)	P1dB (dBm)	1dB (CONVERSION GAIN) IF FREQUENCY RANGE
Highpass	8.5	26.9	10.0	110MHz to 320MHz
Wideband	6.2	26.9	13.0	45MHz to 590MHz

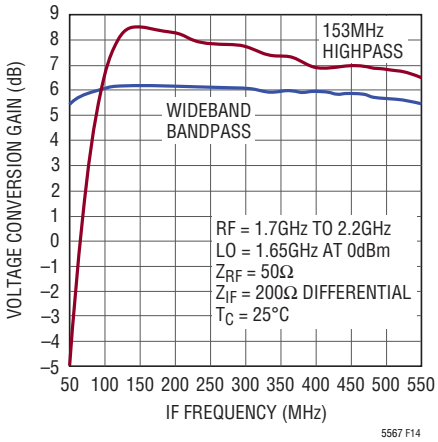

Figure 14. Voltage Conversion Gain versus IF Frequency for 153MHz Highpass and Wideband Bandpass IF Matching Networks

Mixer Bias Current Reduction

The IADJ pin (Pin 8) is available for reducing the mixer core DC current consumption at the expense of linearity and P1dB. For the highest performance, this pin should be left open circuit. As shown in Figure 15, an internal bias circuit produces a 3mA reference current for the mixer core. If a resistor is connected to Pin 8, as shown

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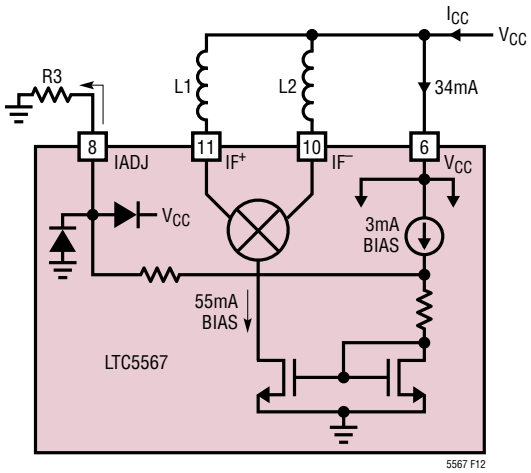


Figure 15. IADJ Interface

in Figure 15, a portion of the reference current can be shunted to ground, resulting in reduced mixer core current. For example, R3 = 1k will shunt away 1mA from Pin 8 and reduce the mixer core current by 33%. The nominal, open-circuit DC voltage at the IADJ pin is 2.2V. Table 7 lists DC supply current and RF performance at 1950MHz for various values of R3.

Table 7. Mixer Performance with Reduced Current (RF = 1950MHz, Low Side LO, IF = 153MHz)

R3 (Ω)	I_{CC} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
Open	89.0	1.9	26.9	10.2	11.8
10k	84.6	1.9	25.7	10.2	11.5
1k	70.4	1.6	21.4	10.1	10.5
330	62.9	1.3	19.3	9.5	10.3
100	58.3	1.0	17.9	8.5	10.1

Enable Interface

Figure 16 shows a simplified schematic of the enable interface. To enable the mixer, the EN voltage must be higher than 2.5V. If the enable function is not required, the pin should be connected directly to V_{CC}. The voltage at the EN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

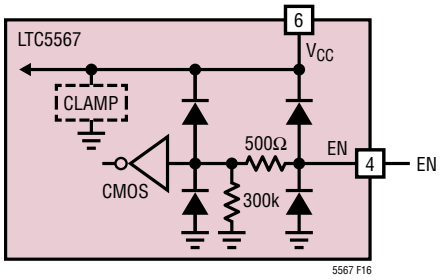


Figure 16. Enable Input Circuit

The EN pin has an internal 300k pull-down resistor. Therefore, the mixer will be disabled with the enable pin left floating.

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD clamp circuits connected to the V_{CC} pin. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the 4.0V maximum rating. A supply voltage ramp time greater than 1ms is recommended.

Spurious Output Levels

Mixer spurious output levels versus harmonics of the RF and LO are tabulated in Table 8. The spur levels were measured on a standard evaluation board using the test circuit shown in Figure 1. The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

Table 8. IF Output Spur Levels (dBm)

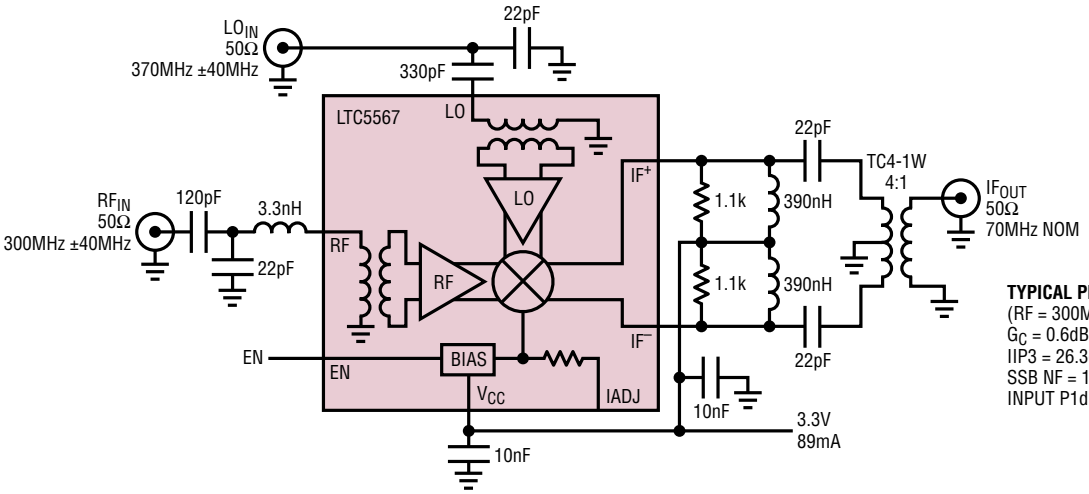
(RF = 1950MHz, P_{RF} = –2dBm, P_{IF} = 0dBm at 153MHz, Low Side LO, P_{LO} = 0dBm, V_{CC} = 3.3V, T_C = 25°C)

		N									
		0	1	2	3	4	5	6	7	8	9
M	0		–43	–24	–47	–30	–57	–46	–64	–50	–81
	1	–30	0	–56	–57	–59	–37	–69	–47	–78	–58
	2	–60	–56	–67	–68	–72	–78	–78	–85	–87	*
	3	*	–81	–89	*	*	*	*	*	*	*
	4	*	*	–73	*	*	*	*	*	–90	*
	5	*	*	*	*	*	*	*	*	*	*
	6		*	*	*	*	*	*	*	*	*
	7				*	*				*	

*Less than –90dBc

TYPICAL APPLICATIONS

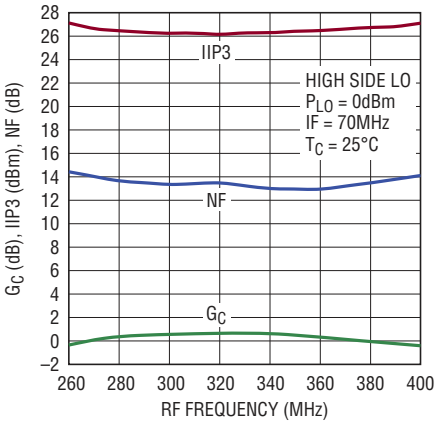
300MHz RF Application with 70MHz Highpass IF Matching



TYPICAL PERFORMANCE
(RF = 300MHz, IF = 70MHz, LO = 370MHz AT 0dBm)
G_C = 0.6dB
IIP3 = 26.3dBm
SSB NF = 13.3dB
INPUT P1dB = 10.9dBm

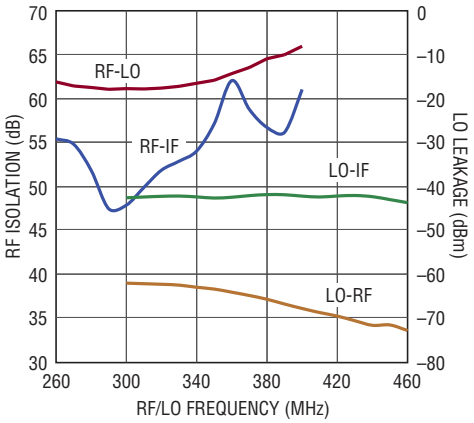
5567 TA03a

Conversion Gain, IIP3 and NF vs RF Frequency



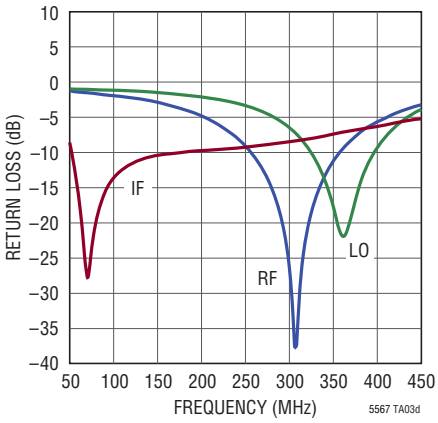
5567 TA03b

RF Isolation and LO leakage vs RF and LO Frequency



5567 TA03c

RF, LO and IF Port Return Losses

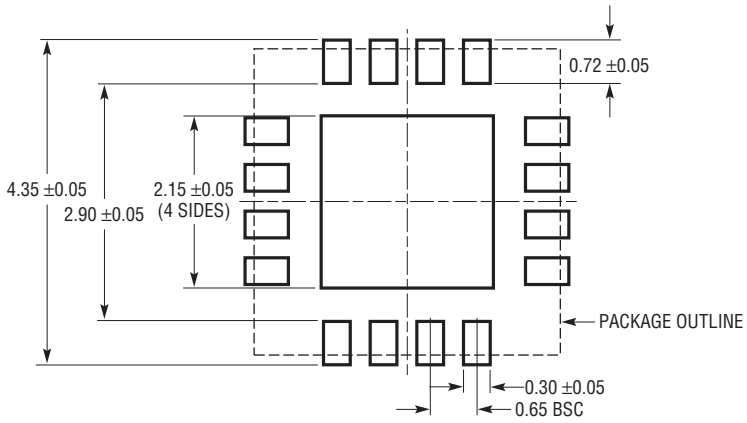


5567 TA03d

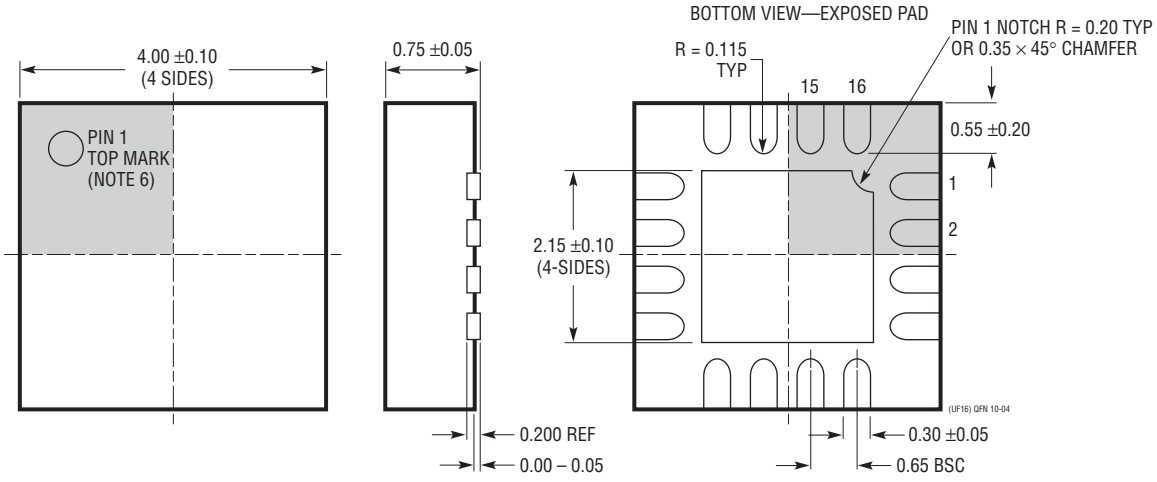
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

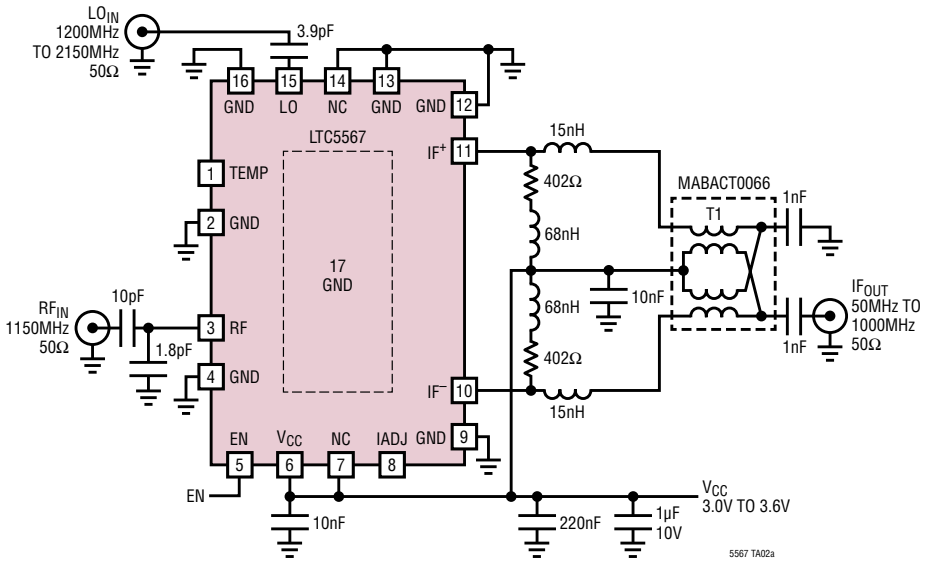


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

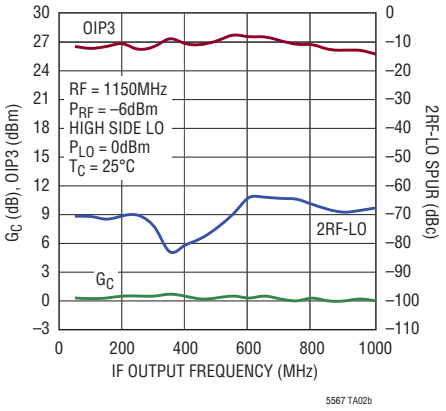
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

CATV Downconverting Mixer with 1GHz IF Bandwidth



Conversion Gain, OIP3 and 2RF-LO Spur vs IF Output Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT®5527	400MHz to 3.7GHz, 5V Downconverting Mixer	2.3dB Gain, 23.5dBm IIP3 and 12.5dB NF at 1900MHz, 5V/78mA Supply
LT5557	400MHz to 3.8GHz, 3.3V Downconverting Mixer	2.9dB Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply
LTC559x	600MHz to 4.5GHz Dual Downconverting Mixer Family	8.5dB Gain, 26.5dBm IIP3, 9.9dB NF, 3.3V/380mA Supply
LTC5569	300MHz to 4GHz, 3.3V Dual Active Downconverting Mixer	2dB Gain, 26.8dBm IIP3 and 11.7dB NF, 3.3V/180mA Supply
LTC554x	600MHz to 4GHz, 5V Downconverting Mixer Family	8dBm Gain, >25dBm IIP3 and 10dB NF, 3.3V/200mA Supply
LTC6400-X	300MHz Low Distortion IF Amp/ADC Driver	Fixed Gain of 8dB, 14dB, 20dB and 26dB; >36dBm OIP3 at 300MHz, Differential I/O
LTC6416	2GHz 16-Bit ADC Buffer	40dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LT5554	Ultralow Distort IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LT5578	400MHz to 2.7GHz Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer
LT5579	1.5GHz to 3.8GHz Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
LTC5588-1	200MHz to 6GHz I/Q Modulator	31dBm OIP3 at 2.14GHz, –160.6dBm/Hz Noise Floor
LTC5585	700MHz to 3GHz Wideband I/Q Demodulator	>530MHz Demodulation Bandwidth, IIP2 Tunable to >80dBm, DC Offset Nulling
RF Power Detectors		
LT5538	40MHz to 3.8GHz Log Detector	±0.8dB Accuracy Over Temperature, –72dBm Sensitivity, 75dB Dynamic Range
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5582	40MHz to 10GHz RMS Detector	±0.5dB Accuracy Over Temperature, ±0.2dB Linearity Error, 57dB Dynamic Range
LTC5583	Dual 6GHz RMS Power Detector	Up to 60dB Dynamic Range, ±0.5dB Accuracy Over Temperature, >50dB Isolation
ADCs		
LTC2208	16-Bit, 130Msps ADC	78dBFS Noise Floor, >83dB SFDR at 250MHz
LTC2153-14	14-Bit, 310Msps Low Power ADC	68.8dBFS SNR, 88dB SFDR, 401mW Power Consumption

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