WM8946

Stereo Low-Power CODEC with Video Buffer

DESCRIPTION

The WM8946 is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras.

Up to 6 analogue inputs may be connected; a 2-channel digital microphone interface is also provided. Flexible output mixing options support single-ended and differential configurations, with outputs derived from the digital audio paths or from analogue bypass paths. Twin stereo outputs or stereo line and mono BTL headphone/speaker drive may be supported.

Flexible digital mixing and powerful DSP functions are available. Programmable filters and other processes may be applied to the ADC or DAC signal paths. The DSP functions include 3D-stereo enhancement, 5 notch filters, 5-band EQ, dynamic range control and the ReTune™ feature.

The ReTune™ feature is a sophisticated digital filter that can compensate for imperfect characteristics of the housing, loudspeaker or microphone components in an application. The ReTune™ algorithm can provide acoustic equalisation and selective phase (delay) control of specific frequency bands.

The WM8946 is controlled via a I2C or SPI interface. Additional functions include Digital beep generator, Video buffer, programmable GPIO functions, Frequency Locked Loop (FLL) for flexible clocking support and integrated LDO for low noise supply regulation.

The WM8946 is supplied in 36-ball W-CSP package, ideal for portable systems.

FEATURES

- Hi-fi audio CODEC
  - 94dB SNR during ADC recording ('A' weighted)
  - 96dB SNR during DAC playback ('A' weighted)
- 6 analogue audio inputs
- Integrated bias reference for electret microphones
- 2-channel digital microphone interface
- Powerful digital mixing / DSP functions:
  - 3D-stereo enhancement
  - 5-notch filters
  - 5-band equalizer (EQ)
  - ReTune™ parametric filter
  - Dynamic range control and noise gate
  - Low-pass/High-pass filters
  - Direct Form 1 (DF1) programmable digital filter
- Digital beep generator
- 4 analogue audio outputs
- Stereo line output
- Mono BTL headphone/speaker output driver
- I2S digital audio interface - sample rates 8kHz to 48kHz
- Frequency Locked Loop (FLL) frequency conversion / filter
- Video buffer function
- Integrated LDO low-noise voltage regulator
- 36-ball W-CSP package (2.97 x 3.07 x 0.7mm, 0.5mm pitch)

APPLICATIONS

- Digital Still Cameras (DSC)
- Multimedia phones

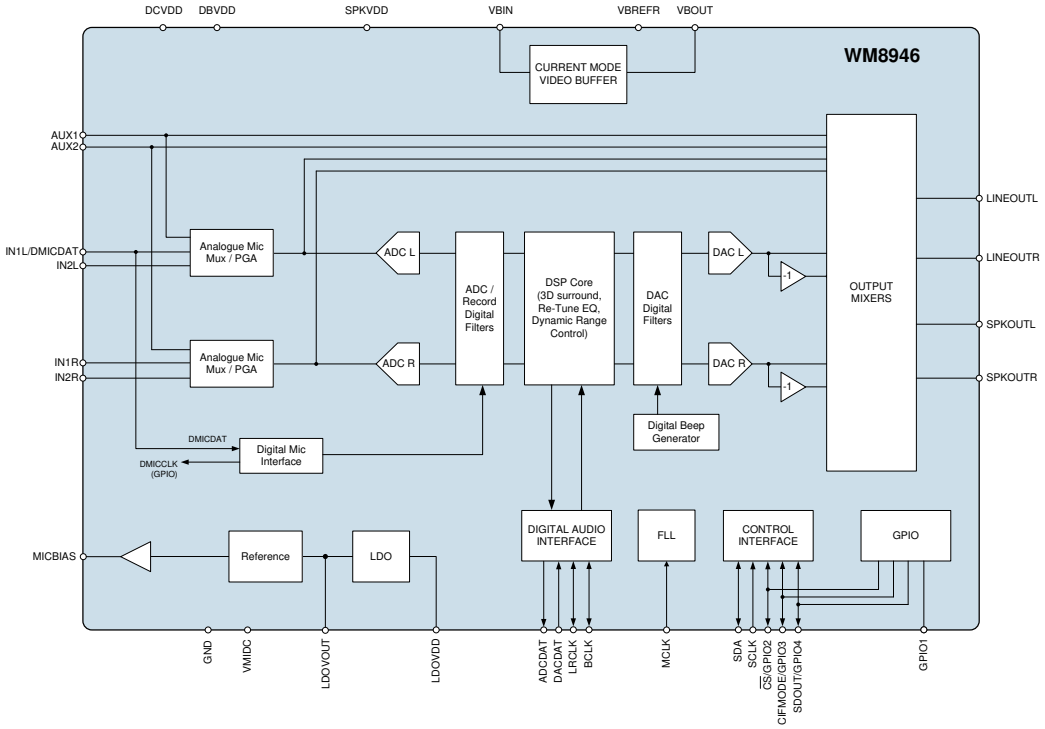
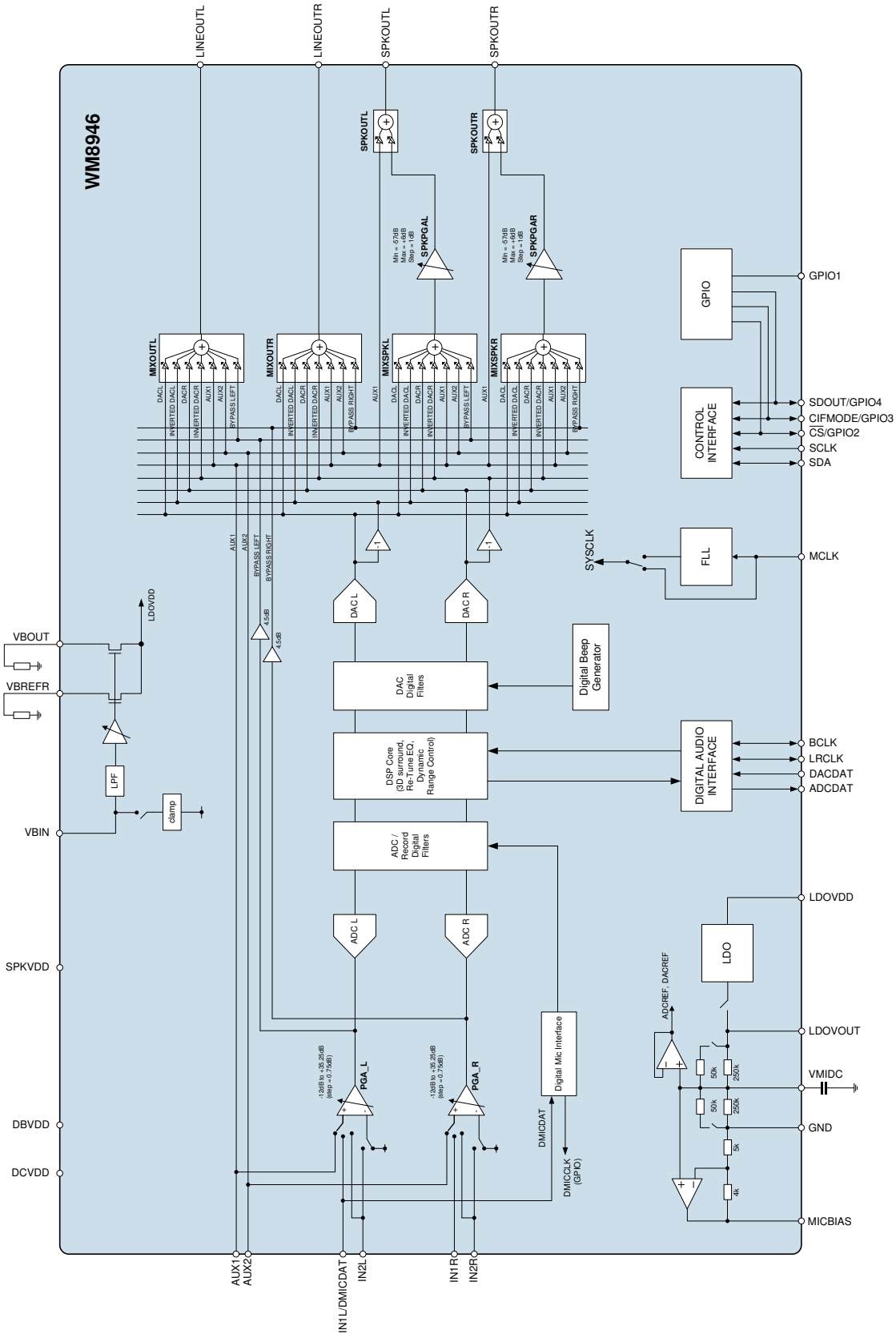


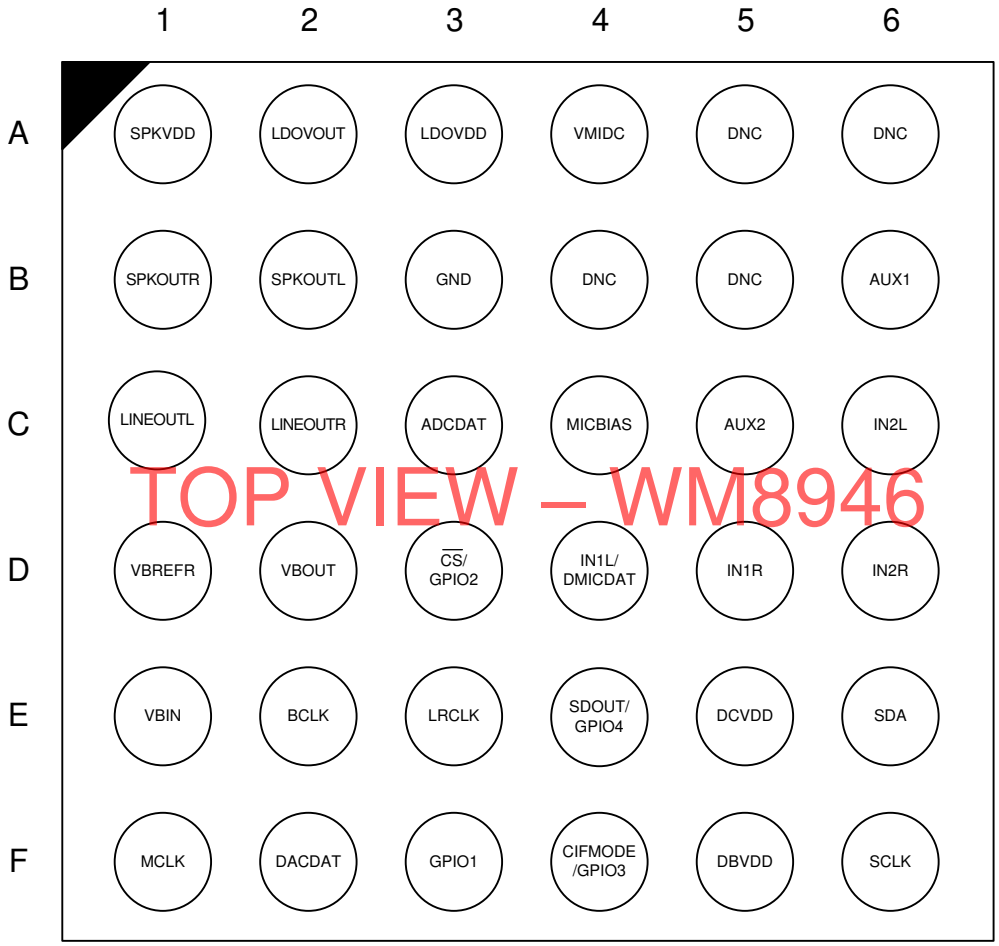
TABLE OF CONTENTS

BLOCK DIAGRAM



PIN CONFIGURATION

The WM8946 is supplied in a 36-pin CSP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8946ECS/R	-40°C to +85°C	36-ball W-CSP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 5000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKVDD	Supply	Supply for speaker driver
A2	LDOVOUT	Supply	LDO output
A3	LDOVDD	Supply	LDO supply input
A4	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
A5	DNC	N/A	Do Not Connect
A6	DNC	N/A	Do Not Connect
B1	SPKOUTR	Analogue Output	Right speaker mixer output
B2	SPKOUTL	Analogue Output	Left speaker mixer output
B3	GND	Supply	Ground
B4	DNC	N/A	Do Not Connect
B5	DNC	N/A	Do Not Connect
B6	AUX1	Analogue Input	Aux audio input
C1	LINEOUTL	Analogue Output	Left line mixer output
C2	LINEOUTR	Analogue Output	Right line mixer output
C3	ADCDAT	Digital Output	ADC / Digital Microphone digital audio data
C4	MICBIAS	Analogue Output	Microphone bias
C5	AUX2	Analogue Input	Aux audio input
C6	IN2L	Analogue Input	Left input 2
D1	VBREFR	Analogue Output	Video buffer current reference resistor connection
D2	VBOUT	Analogue Output	Video buffer output
D3	$\overline{CS}$/GPIO2	Digital Input / Output	Chip Select / GPIO2
D4	IN1L/DMICDAT	Analogue Input / Digital Input	Left input 1 / Digital Microphone data input
D5	IN1R	Analogue Input	Right input 1
D6	IN2R	Analogue Input	Right input 2
E1	VBIN	Analogue Input	Video buffer input
E2	BCLK	Digital Input / Output	Audio interface bit clock
E3	LRCLK	Digital Input / Output	Audio interface left / right clock
E4	SDOUT/GPIO4	Digital Input / Output	Control interface data output / GPIO4
E5	DCVDD	Supply	Digital core supply
E6	SDA	Digital Input / Output	Control interface data input / output
F1	MCLK	Digital Input	Master clock
F2	DACDAT	Digital Input	DAC digital audio data
F3	GPIO1	Digital Input / Output	GPIO1
F4	CIFMODE/GPIO3	Digital Input / Output	Control interface mode select / GPIO3
F5	DBVDD	Supply	Digital buffer (I/O) supply
F6	SCLK	Digital Input	Control interface clock input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	2.5V
Supply voltages (LDOVDD, DBVDD, SPKVDD)	-0.3V	4.5V
Voltage range digital inputs	-0.7V	DBVDD +0.7V
Voltage range analogue inputs	-0.7V	LDOVDD +0.7V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.62	1.8	1.98	V
Digital supply range (I/O)	DBVDD	1.71	3.3	3.6	V
Analogue supply	LDOVDD	2.4	3.3	3.6	V
Speaker supply range	SPKVDD	1.71	3.3	3.6	V
Ground	GND		0		V

Note:

To ensure pop-free device start-up, LDOVDD must be enabled before SPKVDD

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8946 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

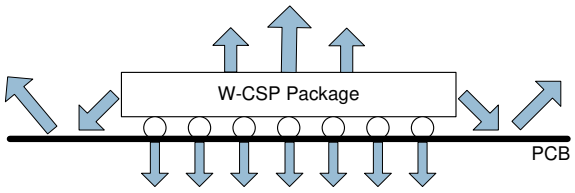


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance (Junction to Case)	Θ_{JC}		30		°C/W
Thermal Resistance (Junction to Ambient)	Θ_{JA}		60		°C/W

Notes:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN2L, IN1R, IN2R)						
Maximum input signal level (changes in proportion to LDOVOUT)		Single-ended input		1.0 0		Vrms dBV
		Pseudo-differential input		0.7 -3.1		Vrms dBV
Input resistance (IN1L, IN1R)		+35.25dB gain		3.5		kΩ
		0dB gain		104		kΩ
		-12dB gain		166		kΩ
Input resistance (IN2L, IN2R)		All gain settings		96		kΩ
Input capacitance				10		pF
Analogue Inputs (AUX1, AUX2)						
Maximum input signal level (changes in proportion to LDOVOUT)		AUX1 or AUX2 enabled as audio input		1.0 0		Vrms dBV
Input resistance		Input mixer path (0dB)		100		kΩ
		Output mixer / direct speaker path (0dB)		15		kΩ
		Output mixer / direct speaker path (-6dB)		30		kΩ
Input capacitance				10		pF
Analogue Inputs Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				-12		dB
Maximum programmable gain				35.25		dB
Gain step size		Guaranteed monotonic		0.75		dB
Mute attenuation				92		dB
Common Mode Rejection Ratio		1kHz input		110		dB
Speaker Output Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				-57		dB
Maximum programmable gain				6		dB
Gain step size		Guaranteed monotonic		1		dB
Mute attenuation				71		dB
ADC Input Path Performance (Input PGAs to ADC)						
SNR (A-weighted)			84	94		dB
THD		-1dBFS input		-83	-75	dB
THD+N		-1dBFS input		-77	-70	dB
Channel separation (Left/Right)				95		dB
PSRR (with respect to LDOVDD)		217Hz 1kHz		77 90		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bypass to Line Output (Single-ended IN2L, IN2R to Input PGA to Line Output, 10kΩ / 50pF)						
SNR (A-weighted)		PGA Gain = 0dB INPPGAVOL = 0dB	90	98		dB
THD+N		PGA Gain = 0dB INPPGAVOL = 0dB		-89.5	-82	dB
Bypass to Speaker Output (Single-ended AUX1, AUX2 to Input PGA to SPKMIX to Speaker Output, 10kΩ / 50pF)						
SNR (A-weighted)		PGA Gain = 0dB INPPGAVOL = 0dB	90	96		dB
THD+N		PGA Gain = 0dB INPPGAVOL = 0dB		-86.5	-77	dB
DAC Output Path Performance (DAC to Line Output, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)			85	96		dB
THD				-78	-72	dB
THD+N				-76	-70	dB
Channel separation (Left/Right)				90		dB
Mute attenuation				125		dB
PSRR (with respect to LDOVDD)				48 60		dB
Line Output Resistance				10		kΩ
Line Output Capacitance				50		pF
DAC Output Path Performance (DAC to Speaker Output, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)				96		dB
THD				-78		dB
THD+N				-76		dB
Speaker Output Performance (Speaker Output, 8Ω BTL)						
SNR (A-weighted)			90	96		dB
THD		P_O=150mW		0.03 -68		% dB
		P_O=350mW		2.944 -30.6		% dB
THD+N		P_O=150mW		0.05 -66		% dB
		P_O=350mW		3.72 -28.6		% dB
Channel separation (Left/Right)				90		dB
Mute attenuation				92		dB
PSRR (with respect to LDOVDD)		217Hz 1kHz		48 60		dB
PSRR (with respect to SPKVDD)		217Hz 1kHz		89 79		dB
Speaker Resistance				8		Ω
Speaker Capacitance				50		pF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs/Outputs						
Input high level			0.7×DBVDD			V
Input low level					0.3×DBVDD	V
Output high level		I_{OL} = 1mA	0.8×DBVDD			V
Output low level		I_{OH} = -1mA			0.2×DBVDD	V
Input capacitance				10		pF
Input leakage		All digital pins except CIFMODE	-900		900	nA
		CIFMODE pin	-90		90	nA
LDO Regulator						
Input voltage	LDOVDD		2.4	3.3	3.6	V
Output voltage	LDOVOUT	LDO_REF_SEL = 0		3.0		V
Maximum output current (see note)				50		mA
Output voltage accuracy		I_{LOAD} = 50mA		2		%
Quiescent current		No Load		55		µA
Leakage current				1		µA
PSRR (with respect to LDOVDD)		217Hz 1kHz		40 49		dB
Video Buffer						
Maximum output voltage swing	Vom	f=100kHz, THD=1%	1.10	1.25	1.50	V pk-pk
Voltage gain	Av	VB_GAIN = 1, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	5.08	6	7.94	dB
		VB_GAIN = 0, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	-0.92	0	1.94	dB
Gain step size				6		dB
Differential gain	DG	Vin = 1V pk-pk	-2.0	0.3	+2.0	%
Differential phase	DP	Vin = 1V pk-pk	-2.0%	0.7	+2.0	Deg
SNR	VSNR		40	60	100	dB
SYNC tip offset above GND		VB_PD = 0 VB_GAIN = 1	0	40	75	mV
Third order Low Pass Filter response (referenced to 100kHz) R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω, 0dB gain		2.4MHz	-0.5	0	0.5	dB
		5.13MHz	-0.5	-0.2	0.5	dB
		9.04MHz	-3.0	-1.6	0	dB
		13.32MHz	-11.0	-7.0	-3.0	dB
PSRR (with respect to LDOVOUT)		100kHz		60		dB
Clocking						
MCLK frequency			30Hz		27MHz	Hz
FLL output frequency			2.045		50	MHz
FLL lock time				2		ms
MICBIAS						
Bias voltage (changes in proportion to LDOVOUT)	MICBIAS	MICB_LVL = 0		2.7		V
		MICB_LVL = 1		1.95		V
Bias Current source					3	mA
Output noise spectral density		1kHz to 20kHz		15		nV/√Hz
PSRR (with respect to LDOVDD)		217Hz 1kHz		70 85		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
Midrail Reference Voltage (changes in proportion to LDOVOUT)	VMID	VMID_REF_SEL = 1 VMID_CTRL=1		1.5		V
Bandgap Reference		BG_VSEL=01010	-10%	1.5	+10%	V

Note:

The maximum LDO output current is the total internal and external load capability; internal circuits of the WM8946 will typically account for 25mA of this capacity.

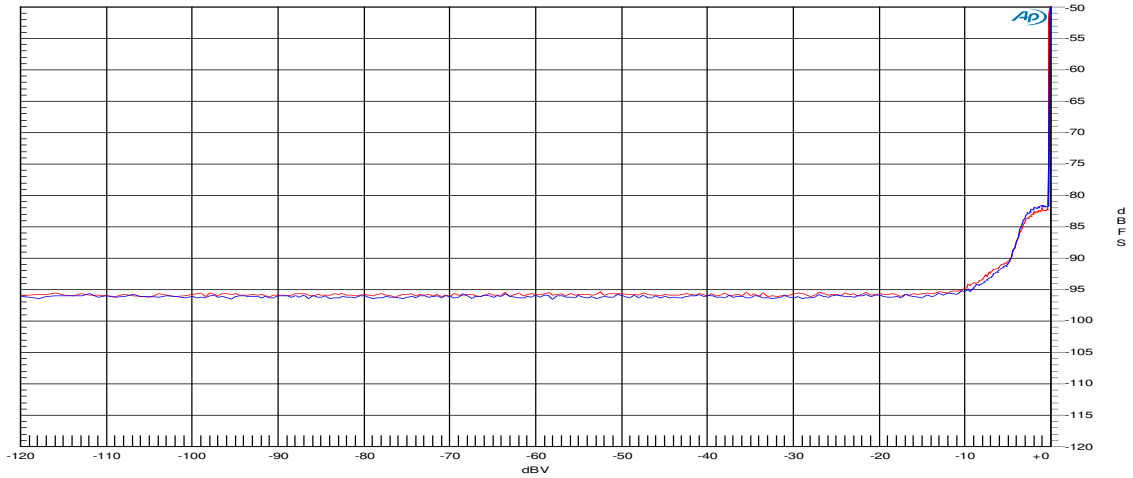
TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (L/R) (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, and the right channel amplitude is measured. Next, a full scale signal is applied to the right channel only, and the left channel amplitude is measured. The worst case channel separation is quoted; this is the difference in level between the full-scale output and the cross-channel output signal level, expressed as a ratio.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
7. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

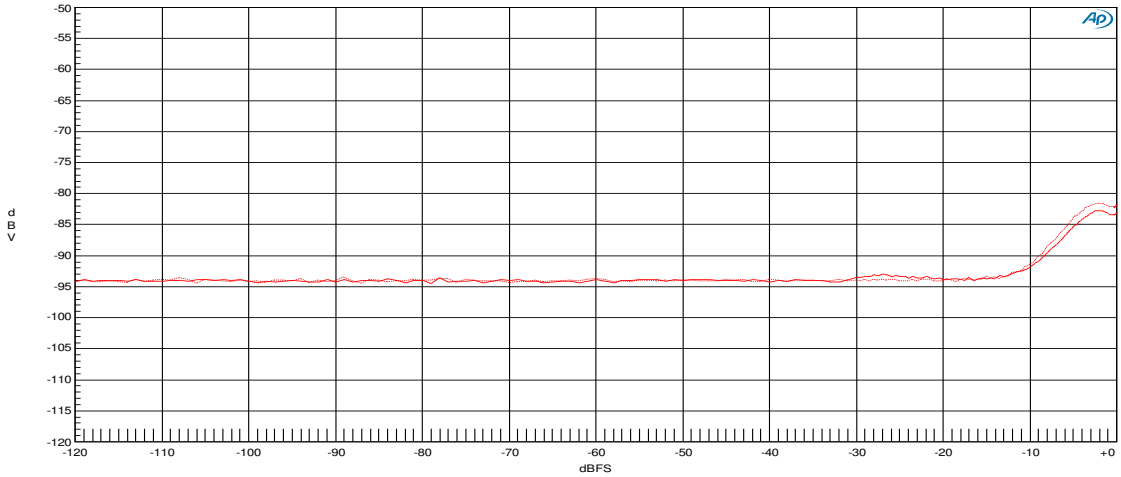
TYPICAL PERFORMANCE

INPUT PATH / OUTPUT PATH PERFORMANCE

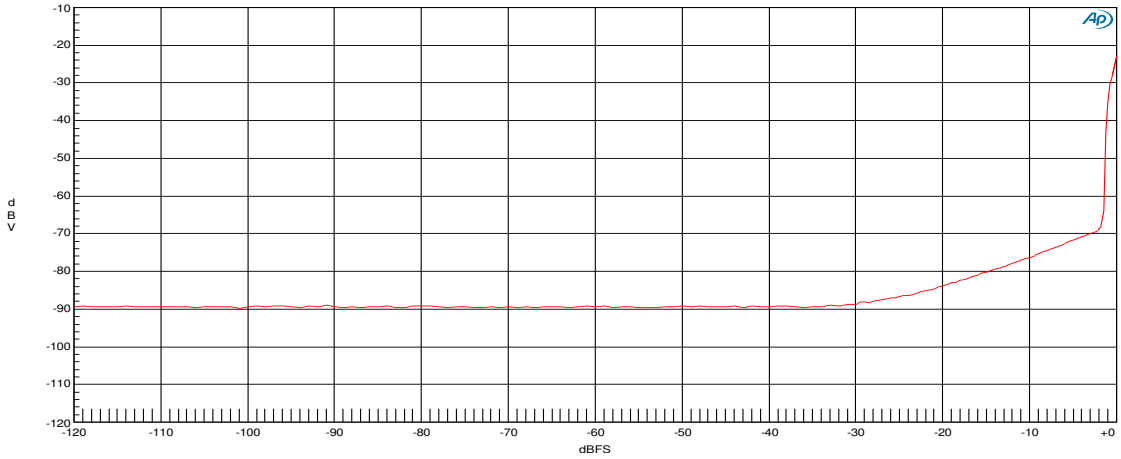
WM8946 ADC - THD+N v Ampltiude - ADC - Slave Mode



WM8946 - DAC to LINEOUT THD+N v Amplitude - Slave



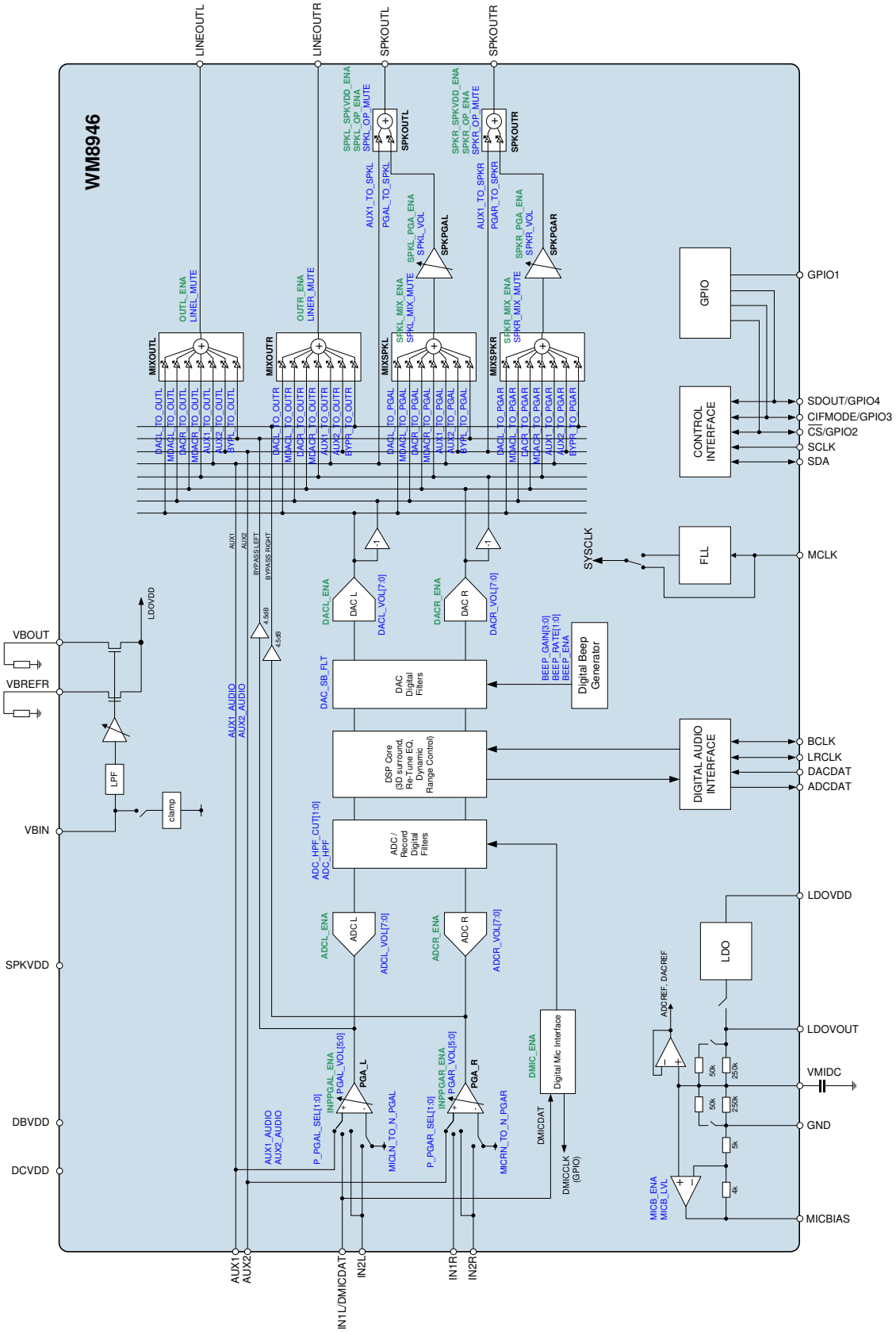
WM8946 - DAC to SPKOUT 8ohm BTL
THD+N v Amplitude - 48kHz



TYPICAL POWER CONSUMPTION

Condition	DCVDD Current @ 1.8V	DBVDD Current @ 3.3V	LDOVDD Current @ 3.3V	SPKVDD Current @ 3.3V	Total Current (mA)	Total Power (mW)
Powerdown (no data)	0.178	0.062	0.007	0.002	0.249	0.555
Powerdown (+Master BIAS)	0.178	0.062	0.021	0.002	0.263	0.601
Powerdown (+Master BIAS+VMID buffer)	0.178	0.062	0.142	0.002	0.384	1.000
Powerdown (+Master BIAS+VMID buffer+VMID)	0.178	0.063	1.092	0.002	1.335	4.139
Playback to Lineout (no data)	4.272	0.057	2.336	0.007	6.672	15.610
Playback to Lineout (with data)	4.293	0.062	2.356	0.007	6.718	15.730
Video Buffer Only	0.178	0.062	5.088	0.020	5.348	17.381
Playback to Speaker (no data)	4.272	0.057	2.877	4.707	11.913	32.905
Playback to Speaker (with data)	4.294	0.062	2.895	4.730	11.981	33.096
Playback to Speaker (with data) 32ohm	4.295	0.062	2.895	5.790	13.042	36.596
Playback to Speaker (with data) 16ohm	4.295	0.062	2.896	6.275	13.528	38.200
Mono Record (nodata)	2.992	0.088	3.728	0.007	6.815	18.002
Mono Record (with data)	2.999	0.100	3.727	0.007	6.833	18.050
Stereo Record (no data)	4.652	0.128	6.692	0.007	11.479	30.903
Stereo Record (with data)	4.654	0.128	6.692	0.007	11.481	30.906
Playback and Record (no data)	5.673	0.120	10.054	4.408	20.255	58.332
All On	5.408	0.099	62.323	4.211	24.253	71.923

AUDIO SIGNAL PATHS DIAGRAM



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

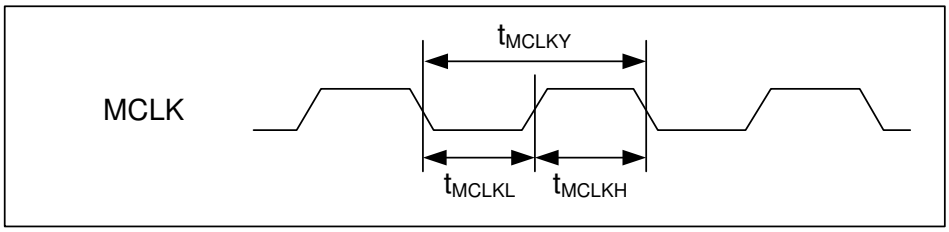


Figure 2 Master Clock Timing

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V, T_A = +25ºC.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK cycle time	T_{MCLKY}		0.037µs			s
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

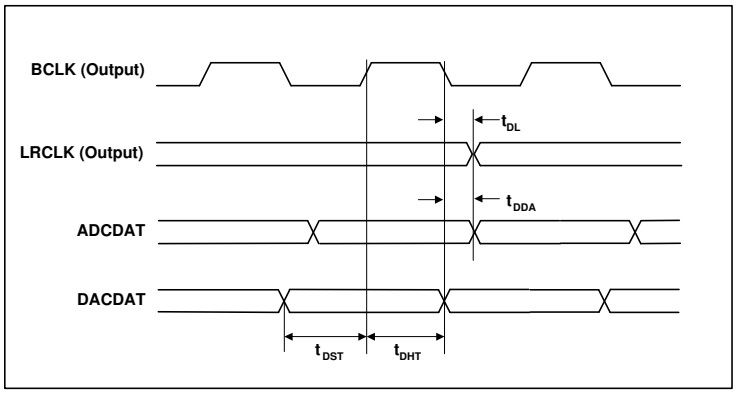


Figure 3 Audio Interface Timing - Master Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

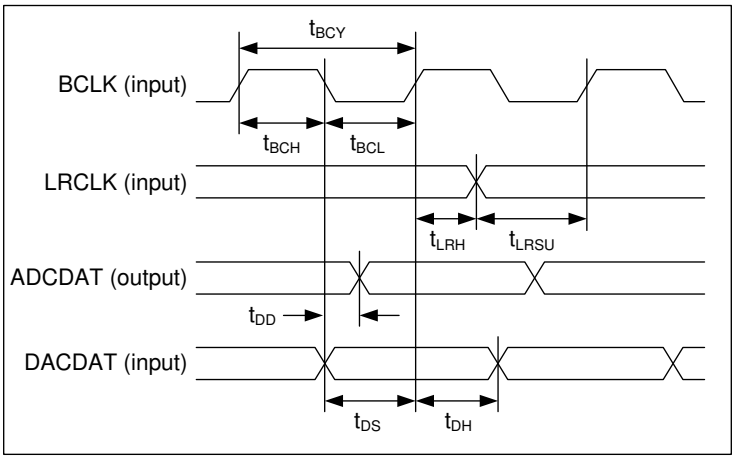


Figure 4 Audio Interface Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

Note: BCLK period must always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

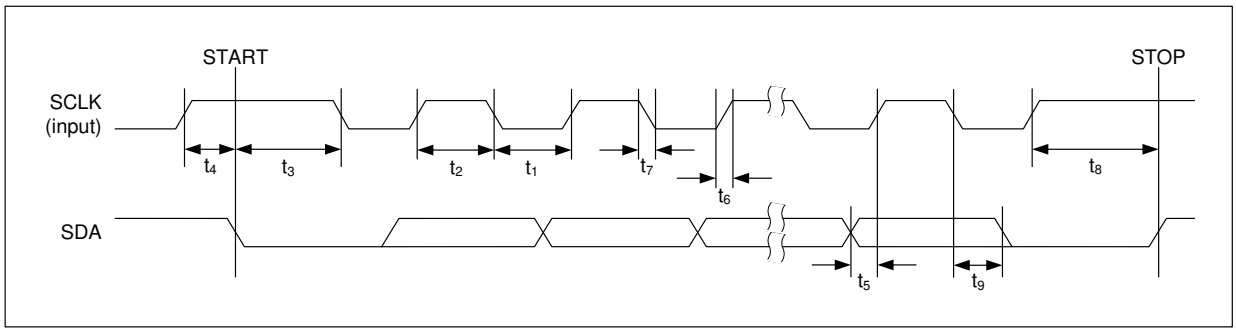


Figure 5 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

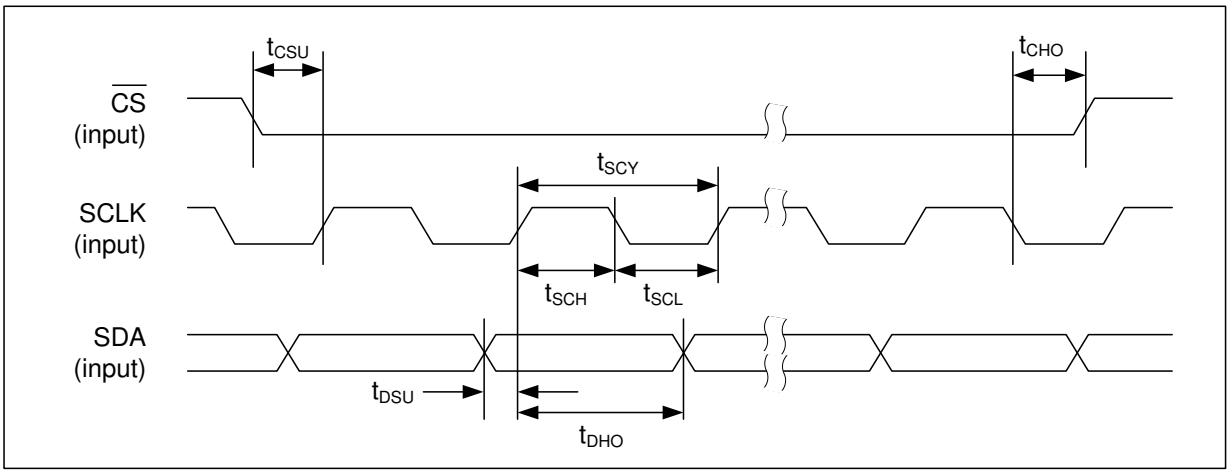


Figure 6 Control Interface Timing - 3-wire (SPI) Control Mode (Write Cycle)

Note: The data is latched on the 32nd falling edge of SCLK after 32 bits have been clocked into the device.

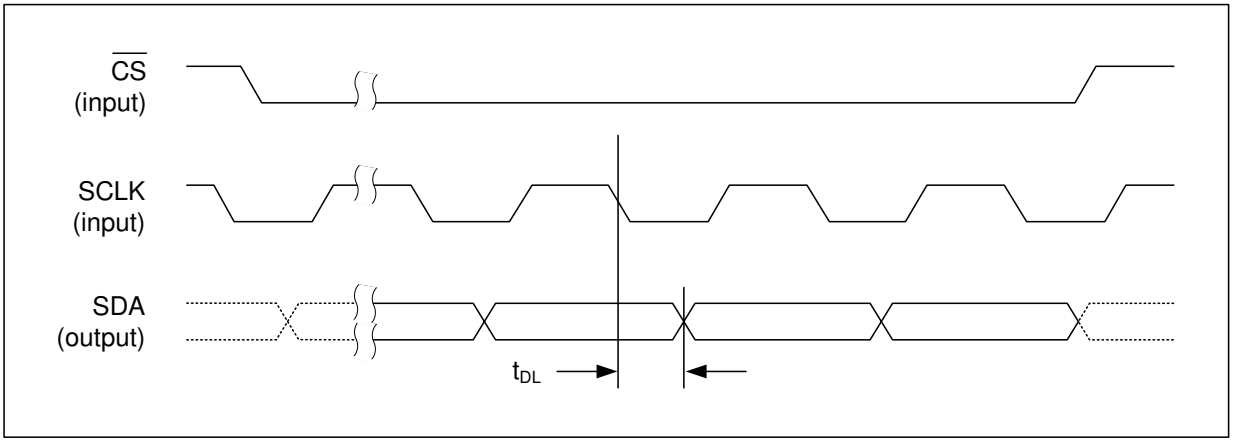


Figure 7 Control Interface Timing - 3-wire (SPI) Control Mode (Read Cycle)

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDA output transition	t_{DL}			40	ns

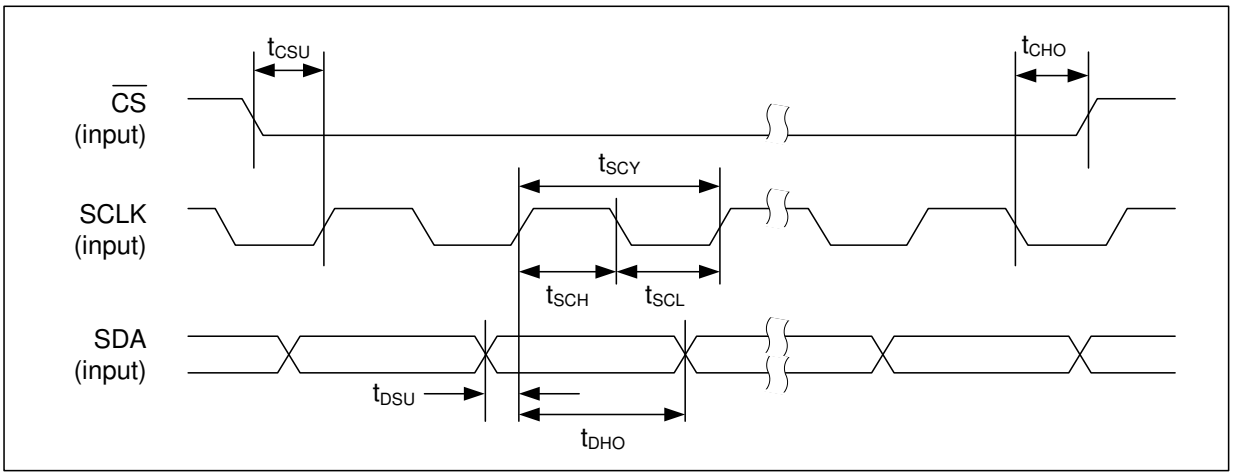


Figure 8 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

Note: The data is latched on the 32nd falling edge of SCLK after 32 bits have been clocked into the device.

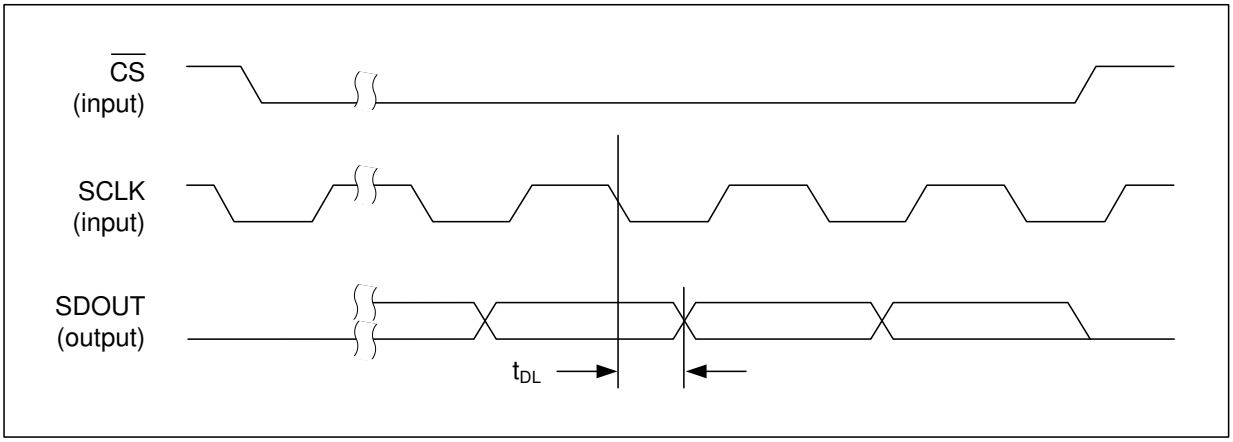


Figure 9 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8946 is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras and multimedia phones. Flexible analogue interfaces and powerful digital signal processing (DSP) in a 2.96 x 3.06mm footprint make it ideal for small portable devices.

The WM8946 supports up to 6 analogue audio inputs. One pair of single-ended or pseudo differential microphone / line inputs is selected as the ADC input source. The two auxiliary inputs can be selected as line inputs to the ADC, or as direct signal paths to the output mixers. An integrated bias reference is provided to power standard electret microphones. A two-channel digital microphone interface is also supported, with direct input to the DSP core via the ADCs.

The stereo hi-fi ADCs and DACs operate at sample rates from 8kHz up to 48kHz. A high pass filter is available in the ADC path for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital tone ('beep') generator allows audio tones to be injected into the DAC output path.

The WM8946 provides a powerful DSP capability for configurable filtering and processing of the digital audio paths. The DSP provides low-pass / high-pass filtering, 3D stereo enhancement, notch filters, 5-band EQ, dynamic range control and a programmable DF1 digital filter. The tuned notch filters allow narrow frequency bands to be attenuated, to provide filtering of motor noise or other unwanted sounds; the 5-band EQ allows the signal to be adjusted for user-preferences. The dynamic range control provides a range of compression, limiting and noise gate functions to support optimum configuration for recording or playback modes. The DF1 filter allows user-specified algorithms to be implemented in the digital signal chain.

The ReTune™ feature is a highly-configurable DSP algorithm which can be tailored to cancel or compensate for imperfect characteristics of the housing, loudspeaker or microphone components in the target application. The ReTune™ algorithm coefficients and register contents are calculated using Cirrus Logic's WISCE™ software; lab bench tests and audio reference measurements must be performed in order to determine the optimum settings.

The digital signal routing between the ADCs, DACs and I2S digital audio interface can be configured in different ways according to the application requirements. The DSP functions may be applied to the ADC record path, or the DAC record path, or may be distributed between these two paths.

Four analogue output mixers are provided, connected to 4 analogue output pins. Twin stereo outputs or stereo headphone/line and mono BTL speaker may be connected to these outputs.

The WM8946 incorporates an LDO regulator for compatibility with a wide range of supply rails; the internal LDO can also reduce any interference resulting from a noisy supply rail. The LDO regulator can also be used to provide a regulated supply voltage to other circuits.

I2C or SPI control interface modes for read/write access to the register map. A single external clock provides timing reference for all the digital functions; an integrated Frequency Locked Loop (FLL) also provides flexibility to perform frequency conversions and to remove noise/jitter from the external clock. The FLL can be configured for reduced power consumption, or for different filtering requirements of the reference source.

Additional functions include a current-mode video buffer providing excellent video signal reproduction at low operating voltages. Up to 4 GPIO pins may be configured for miscellaneous input/output, or for status indications from the temperature monitoring functions.

ANALOGUE INPUT SIGNAL PATH

The WM8946 has six analogue input pins, which may be selected in many different configurations. The analogue input paths can support line and microphone inputs, in single-ended or pseudo-differential modes. The auxiliary input pins (AUX1 and AUX2) may be configured as inputs to the input PGAs or to the output mixers.

The Left and Right input PGA audio channels are routed to the Analogue to Digital converters (ADCs). There is also a bypass path for each channel, enabling the signal to be routed directly to the output mixers.

The WM8946 input signal paths and control registers are illustrated in Figure 10.

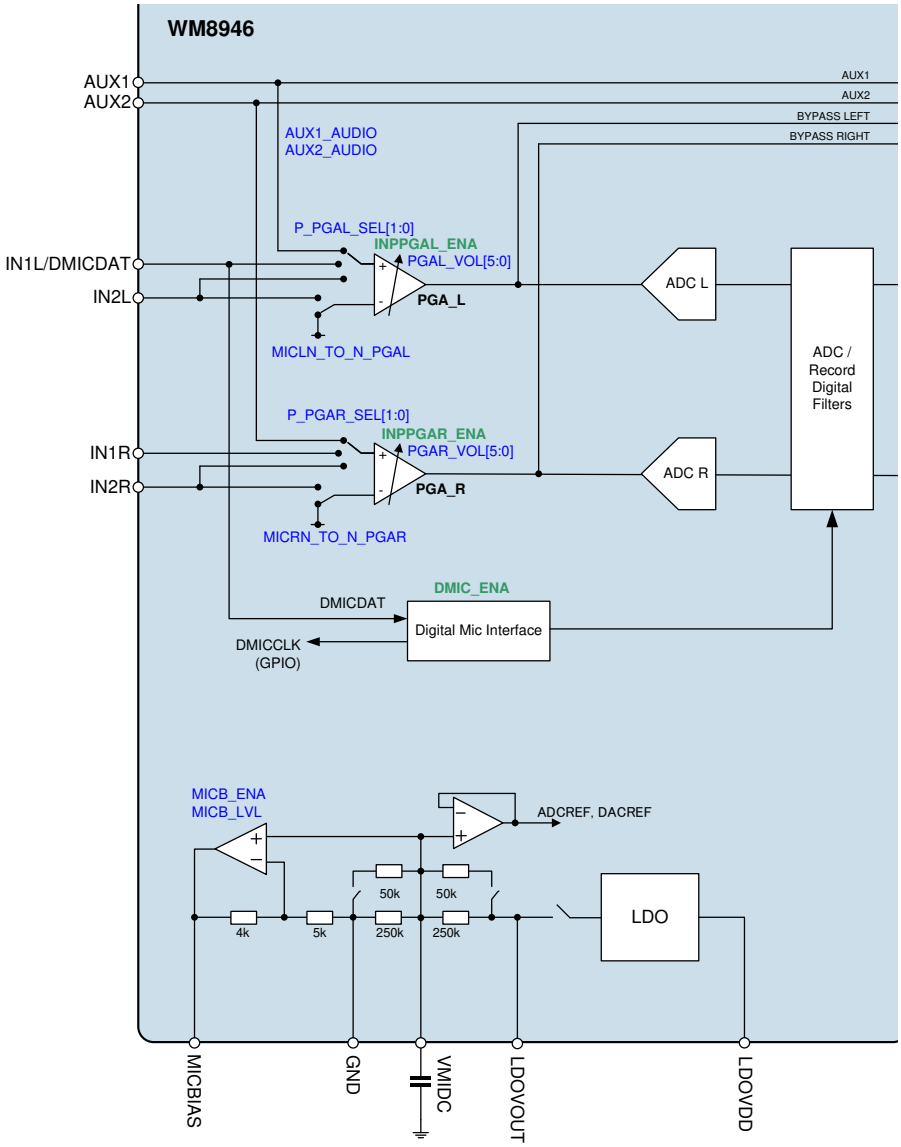


Figure 10 Input Signal Paths

INPUT PGA ENABLE

The input PGAs (Programmable Gain Amplifiers) are enabled using register bits INPPGAR_ENA and INPPGAL_ENA, as described in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	13	INPPGAR_ENA	0	Right Input PGA Enable 0 = Disabled 1 = Enabled
	12	INPPGAL_ENA	0	Left Input PGA Enable 0 = Disabled 1 = Enabled

Table 1 Input PGA Enable

To enable the input PGAs, the reference voltage VMID and the bias current must also be enabled. See "Reference Voltages and Master Bias" for details of the associated controls VMID_SEL and BIAS_ENA.

INPUT PGA CONFIGURATION

Microphone and Line level audio inputs can be connected to the WM8946 in single-ended or differential configurations. (These two configurations are illustrated in Figure 57 and Figure 58 in the section describing the external components requirements - see "Applications Information".)

For single-ended microphone inputs, the microphone signal is connected to the non-inverting input of the PGAs, whilst the inverting inputs of the PGAs are connected to VMID. For differential microphone inputs, the non-inverted microphone signal is connected to the non-inverting input of the PGAs, whilst the inverted (or 'noisy ground') signal is connected to the inverting input pins.

Line level inputs are connected in the same way as a single-ended microphone signal.

The non-inverting input of the PGAs is configured using the P_PGAR_SEL and P_PGAL_SEL registers. These registers allow the selection of three possible input pins to the associated PGA. When the AUX1 or AUX2 pin is used as an audio input, that pin must be configured for audio using the AUX1_AUDIO or AUX2_AUDIO register bits.

The inverting input of the PGAs is configured using MICRN_TO_N_PGAR and MICLN_TO_N_PGAL. These registers allow the PGA to operate in either single-ended or pseudo-differential configuration.

The registers for configuring the Input PGAs are described in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 (27h) Input Ctrl	8	AUX2_AUDIO	0	AUX2 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal
	7	AUX1_AUDIO	0	AUX1 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal
	5	MICRN_TO_N_PGAR	1	Right Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2R
	4	MICLN_TO_N_PGAL	1	Left Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:2	P_PGAR_SEL [1:0]	01	Right Input PGA Non-Inverting Input Select 00 = Connected to IN2R 01 = Connected to IN1R 10 = Connected to AUX2 11 = Reserved
	1:0	P_PGAL_SEL [1:0]	01	Left Input PGA Non-Inverting Input Select 00 = Connected to IN2L 01 = Connected to IN1L 10 = Connected to AUX1 11 = Reserved

Table 2 Input PGA Configuration

MICROPHONE BIAS CONTROL

The WM8946 provides a low noise reference voltage suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the "Applications Information" section for recommended components. The MICBIAS voltage is enabled using the MICB_ENA register bit; the voltage can be selected using the MICB_LVL bit, as described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	4	MICB_ENA	0	Microphone Bias Enable 0 = Disabled 1 = Enabled
R39 (27h) Input Ctrl	6	MICB_LVL	0	Microphone Bias Voltage control 0 = 0.9 x LDOVOUT 1 = 0.65 x LDOVOUT

Table 3 Microphone Bias Control

INPUT PGA GAIN CONTROL

The volume control gain for the Left and Right channels can be independently adjusted using the PGAL_VOL and PGAR_VOL register fields as described in Table 4. The gain range is -12dB to +35.25dB in 0.75dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each input PGA can be independently muted using the PGA mute bits.

To prevent "zipper noise", a zero-cross function is provided on the input PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA. See "Clocking and Sample Rates" for the definition of this bit. Note that the zero-cross function can be supported without TOCLK enabled, but the timeout function will not be provided in this case.

The PGA_VU bits control the loading of the input PGA volume data. When PGA_VU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The left and right input PGA volume settings are both updated when a 1 is written to PGA_VU; this makes it possible to update the gain of the left and right signal paths simultaneously.

Note that SYSCLK must be enabled when writing to the PGA_VU bits. (See "Clocking and Sample Rates" for details of SYSCLK.)

The Input PGA volume control register fields are described in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Left INP PGA gain ctrl	8	PGA_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause the Left and Right Input PGA volumes to be updated simultaneously.
	7	PGAL_ZC	0	Left Input PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	6	PGAL_MUTE	1	Left Input PGA Mute 0 = Disable Mute 1 = Enable Mute
	5:0	PGAL_VOL [5:0]	01_0000 (0dB)	Left Input PGA Volume 00_0000 = -12dB 00_0001 = -11.25dB … 01_0000 = 0dB ... 11_1111 = +35.25 (See Table 5 for volume range)
R41 (29h) Right INP PGA gain ctrl	8	PGA_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause the Left and Right Input PGA volumes to be updated simultaneously.
	7	PGAR_ZC	0	Right Input PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	6	PGAR_MUTE	1	Right Input PGA Mute 0 = Disable Mute 1 = Enable Mute
	5:0	PGAR_VOL [5:0]	01_0000 (0dB)	Right Input PGA Volume 00_0000 = -12dB 00_0001 = -11.25dB … 01_0000 = 0dB ... 11_1111 = +35.25 (See Table 5 for volume range)

Table 4 Input PGA Volume Control

PGAL_VOL[5:0], PGAR_VOL[5:0]	VOLUME (dB)	PGAL_VOL[5:0], PGAR_VOL[5:0]	VOLUME (dB)
00_0000	-12	10_0000	12
00_0001	-11.25	10_0001	12.75
00_0010	-10.5	10_0010	13.5
00_0011	-9.75	10_0011	14.25
00_0100	-9	10_0100	15
00_0101	-8.25	10_0101	15.75
00_0110	-7.5	10_0110	16.5
00_0111	-6.75	10_0111	17.25
00_1000	-6	10_1000	18
00_1001	-5.25	10_1001	18.75
00_1010	-4.5	10_1010	19.5
00_1011	-3.75	10_1011	20.25
00_1100	-3	10_1100	21
00_1101	-2.25	10_1101	21.75
00_1110	-1.5	10_1110	22.5
00_1111	-0.75	10_1111	23.25
01_0000	0	11_0000	24
01_0001	0.75	11_0001	24.75
01_0010	1.5	11_0010	25.5
01_0011	2.25	11_0011	26.25
01_0100	3	11_0100	27
01_0101	3.75	11_0101	27.75
01_0110	4.5	11_0110	28.5
01_0111	5.25	11_0111	29.25
01_1000	6	11_1000	30
01_1001	6.75	11_1001	30.75
01_1010	7.5	11_1010	31.5
01_1011	8.25	11_1011	32.25
01_1100	9	11_1100	33
01_1101	9.75	11_1101	33.75
01_1110	10.5	11_1110	34.5
01_1111	11.25	11_1111	35.25

Table 5 Input PGA Volume Range

DIGITAL MICROPHONE INTERFACE

The WM8946 supports a two-channel digital microphone interface. The two-channel audio data is multiplexed on the IN1L input pin and clocked using a GPIO output. The analogue signal path from the IN1L pin must be disabled when using the digital microphone interface; this is achieved by disabling the associated input PGA, (i.e. INPPGAL_ENA= 0).

The Digital Microphone Input, DMICDAT, is provided on the IN1L/DMICDAT pin. The associated clock, DMICCLK, is provided on a GPIO pin.

The Digital Microphone Input is selected as input by setting the DMIC_ENA bit. When the Digital Microphone Input is selected, the ADC input is deselected.

The digital microphone interface configuration is illustrated in Figure 11.

Note that the digital microphone may be powered from MICBIAS or from LDOVOUT; care must be taken to ensure that the respective digital logic levels of the microphone are compatible with the digital input thresholds of the WM8946. The digital input thresholds are referenced to DBVDD, as defined in "Electrical Characteristics".

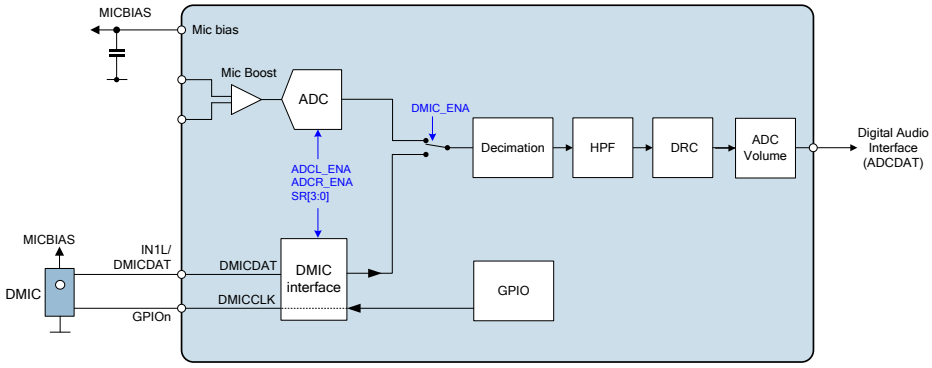


Figure 11 Digital Microphone Interface

When any GPIO pin is configured as DMICCLK output, the WM8946 outputs a clock which supports Digital Mic operation at the ADC sampling rate. The ADC and Record Path filters must be enabled and the ADC sampling rate must be set in order to ensure correct operation of all DSP functions associated with the digital microphone. Volume control for the Digital Microphone Interface signals is provided using the ADC Volume Control.

See "Analogue-to-Digital Converter (ADC)" for details of the ADC Enable and volume control functions. See "General Purpose Input / Output" for details of configuring the DMICCLK output. See "Clocking and Sample Rates" for the details of the sample rate control.

When the DMIC_ENA bit is set, then the IN1L pin is used as the digital microphone input DMICDAT. Up to two microphones can share this pin; the two microphones are interleaved as illustrated in Figure 12.

The digital microphone interface requires that MIC1 (Left Channel) transmits a data bit each time that DMICCLK is high, and MIC2 (Right Channel) transmits when DMICCLK is low. The WM8946 samples the digital microphone data in the middle of each DMICCLK clock phase. Each microphone must tri-state its data output when the other microphone is transmitting.

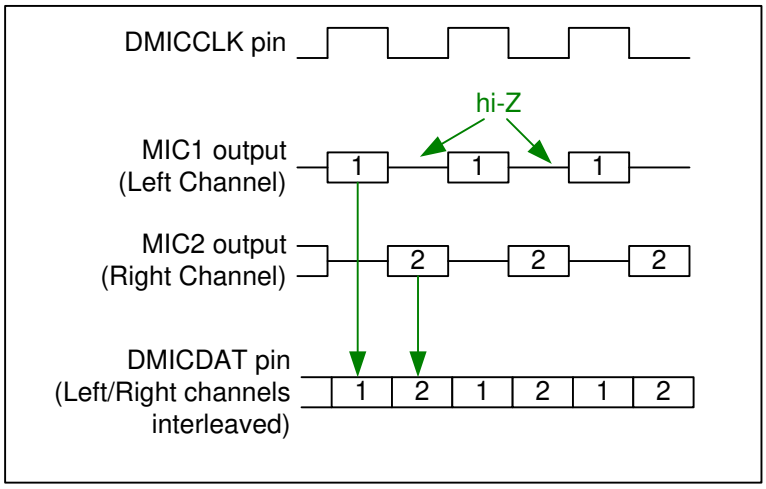


Figure 12 Digital Microphone Interface Timing

The digital microphone interface control fields are described in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	7	DMIC_ENA	0	Enables Digital Microphone mode 0 = Audio DSP input is from ADC 1 = Audio DSP input is from digital microphone interface When DMIC_ENA = 0, the Digital microphone clock (DMICCLK) is held low.

Table 6 Digital Microphone Interface Control

ANALOGUE-TO-DIGITAL CONVERTER (ADC)

The WM8946 uses two 24-bit sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC full-scale input level is proportional to LDOVOUT. See “Electrical Characteristics” section for further details. Any input signal greater than full scale may overload the ADC and cause distortion.

The ADCs and associated digital record filters are enabled by the ADCL_ENA and ADCR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	11	ADCR_ENA	0	Right ADC Enable 0 = Disabled 1 = Enabled ADCR_ENA must be set to 1 when processing right channel data from the ADC or Digital Microphone.
	10	ADCL_ENA	0	Left ADC Enable 0 = Disabled 1 = Enabled ADCL_ENA must be set to 1 when processing left channel data from the ADC or Digital Microphone.

Table 7 ADC Enable Control

ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from -71.625dB to +23.625dB in 0.375dB steps. The volume of each channel can be controlled separately using ADCL_VOL or ADCR_VOL. The ADC Volume is part of the ADC Digital Filters block. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The ADC_VU bit controls the loading of digital volume control data. When ADC_VU is set to 0, the ADCL_VOL or ADCR_VOL control data is loaded into the respective control register, but does not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to ADC_VU. This makes it possible to update the gain of both channels simultaneously.

The output of the ADCs can be digitally muted using the ADCL_MUTE or ADCR_MUTE bits. Both ADCs are muted simultaneously when the ADC_MUTEALL bit is set.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) ADC Control 1	8	ADC_MUTEALL	0	ADC Digital Mute for All Channels 0 = Disable Mute 1 = Enable Mute on all channels
R27 (1Bh) Left ADC Digital Vol	12	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause Left and Right ADC volume to be updated simultaneously
	8	ADCL_MUTE	0	Left ADC Digital Mute 0 = Disable Mute 1 = Enable Mute
	7:0	ADCL_VOL [7:0]	1100_0000 (0dB)	Left ADC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB (See Table 9 for volume range)
R28 (1Ch) Right ADC Digital Vol	12	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause Left and Right ADC volume to be updated simultaneously
	8	ADCR_MUTE	0	Right ADC Digital Mute 0 = Disable Mute 1 = Enable Mute
	7:0	ADCR_VOL [7:0]	1100_0000 (0dB)	Right ADC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB (See Table 9 for volume range)

Table 8 ADC Digital Volume Control

ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)	ADCL_VOL or ADCR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	18.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	18.375
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	18.750
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	19.125
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	19.500
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	19.875
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	20.250
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	20.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	21.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	21.375
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	21.750
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	22.125
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	22.500
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	22.875
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	23.250
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	23.625

Table 9 ADC Digital Volume Range

ADC HIGH PASS FILTER

A digital high-pass filter can be applied to the ADC path to remove DC offsets. This filter can also be programmed to remove low frequency noise in handheld applications (e.g. wind noise, handling noise or mechanical vibration). This filter is controlled using the ADC_HPF and ADC_HPF_CUT register bits (see Table 10).

Note that the ADC HPF is NOT enabled by default but must be used if DRC_ENA is enabled in register R29(1Dh) bit 7. The DRC will not function correctly unless this filter is enabled.

When ADC_HPF_CUT=00, the high pass filter is optimised for hi-fi audio modes; the filter is designed to remove DC offsets without degrading the bass response and has a cut-off frequency of 3.7Hz at fs=44.1kHz.

In the other ADC_HPF_CUT modes. The high pass filter is optimised for voice communication modes. It is recommended to select a cut-off frequency below 300Hz; the preferred setting may vary according to the voice communication sample rate. (e.g. ADC_HPF_CUT=11 at fs=8kHz or ADC_HPF_CUT=10 at fs=16kHz).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) ADC Control 2	2:1	ADC_HPF_CUT [1:0]	00	High pass filter configuration. 00 = 1st order HPF (fc=4Hz at fs=48kHz) 01 = 2nd order HPF (fc=122Hz at fs=48kHz) 10 = 2nd order HPF (fc=153Hz at fs=48kHz) 11 = 2nd order HPF (fc=196Hz at fs=48kHz) (See Table 11 for cut-off frequencies at all supported sample rates)
	0	ADC_HPF	0	ADC Digital High Pass Filter Enable 0 = Disabled 1 = Enabled

Table 10 ADC High-pass Filter Control Registers

Sample Rate (kHz)	Value of ADC_HPF_CUT bits			
	00	01	10	11
	Cut-off frequency (Hz)			
8.000	0.7	20	26	33
11.025	0.9	28	36	45
16.000	1.3	41	51	66
22.050	1.9	56	71	90
24.000	2.0	61	77	98
32.000	2.7	81	102	131
44.100	3.7	112	141	180
48.000	4.0	122	153	196

Table 11 ADC High-pass Filter Cut-off Frequencies

Filter response plots for the ADC high-pass filter are shown in “Digital Filter Characteristics”.

DSP CORE

DSP Core is at the centre of the ADC / DAC / Digital Audio Interface (I2S) blocks. It provides signal routing, and also implements a number of configurable signal processing functions.

The signal processing functions are arranged in three blocks, as follows:

- Signal Enhancement 1 (SE1) - Low-pass / High-pass filter, 3D-stereo enhancement, 5 notch filters, generic 'Direct-Form 1' filter.
- Signal Enhancement 2 (SE2) - ReTune™ processing, 5-band equalizer.
- Signal Enhancement 3 (SE3) - Dynamic range control

The DSP Configuration modes and each of the Signal Enhancement blocks is described in the following sections.

DSP CONFIGURATION MODES

The DSP Configuration Mode is determined using the SE_CONFIG register field; this configures the signal paths between the Signal Enhancement blocks and the ADC / DAC / I2S interfaces. The supported DSP modes are illustrated in Figure 13.

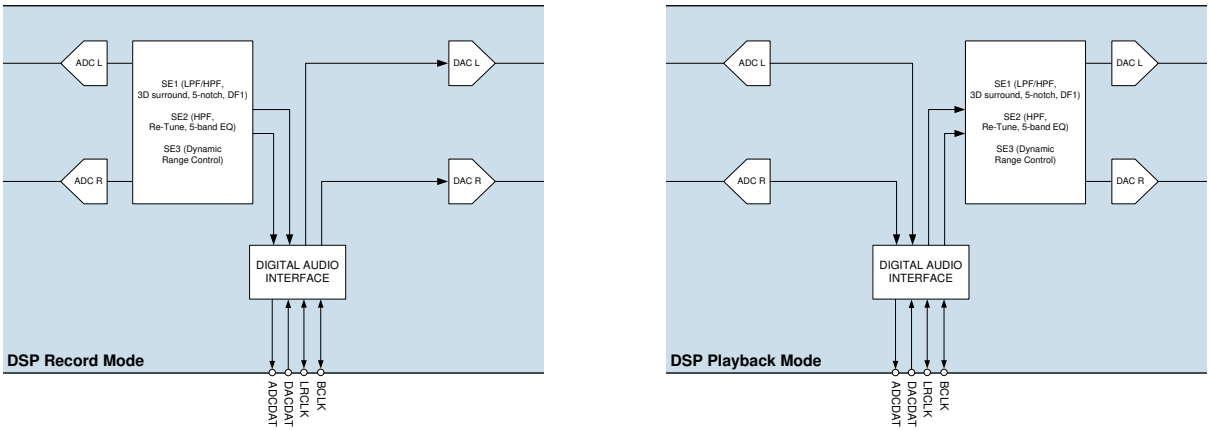


Figure 13 DSP Configuration Modes

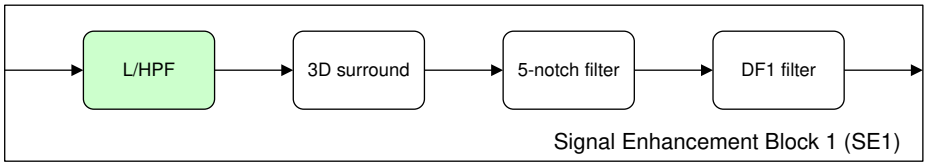
Record mode enables the entire set of Signal Enhancement functions in the ADC path. The direct DAC path is also active, without any Signal Enhancement functions; this allows basic audio playback and digital beep generation.

Playback mode enables the entire set of DSP functions in the DAC path. The direct ADC path is also active, without any DSP functions; this allows basic audio record functions to the host system.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R64 (40h) SE Config Selection	3:0	SE_CONFIG [3:0]	0000	DSP Configuration Mode select 0000 = Record mode 0001 = Playback mode 0010 = Reserved 0011 = Reserved

Table 12 DSP Configuration Mode Select

LOW-PASS / HIGH-PASS FILTER (LPF/HPF)



The Low-pass / High-pass filter is part of the SE1 block. This first-order filter can be configured to be high-pass, low-pass; it can also be bypassed. The cut-off frequency is programmable; the default setting is bypass (OFF). The left and right channel parameters may be programmed individually. The left and right filters are enabled using the SE1_LHPF_L_ENA and SE1_LHPF_R_ENA register bits defined in Table 13. For the derivation of the other associated registers, refer to the configuration tools supplied with the WM8946 Evaluation Kit.

Example plots of the Low-pass / High-pass filter response are shown in Figure 14.

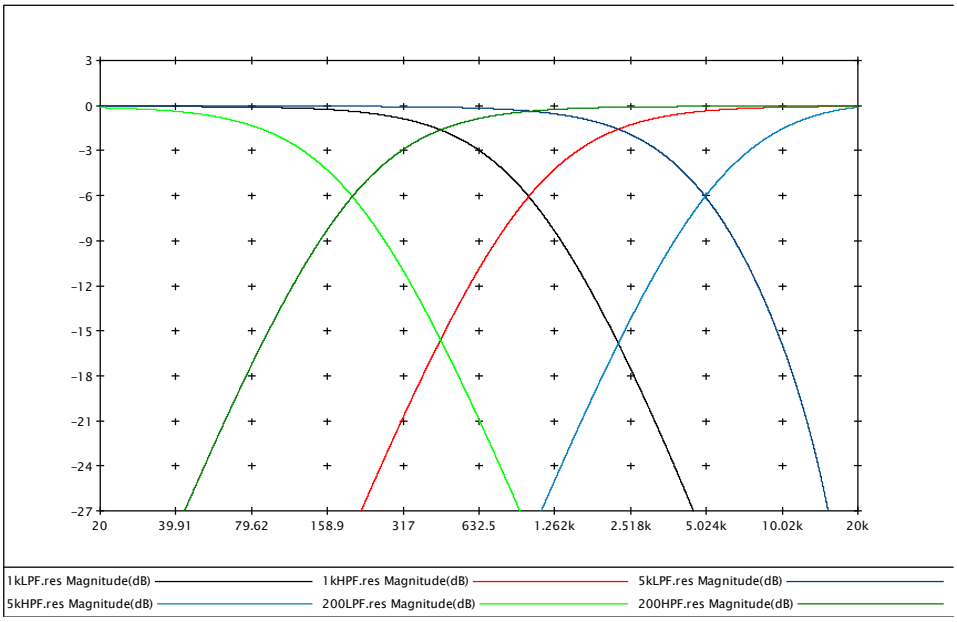
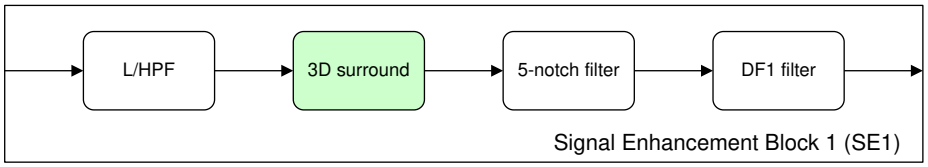


Figure 14 Low-pass / High-pass Filter Responses

3D SURROUND



The 3D-stereo surround effect is part of the SE1 block. This function uses time delays and controlled cross-talk mechanisms to adjust the depth or width of the stereo audio. The 3D-stereo surround effect includes programmable high-pass or low-pass filtering to limit the 3D effect to specific frequency bands if required. The structure of the 3D surround processing is illustrated in Figure 15.

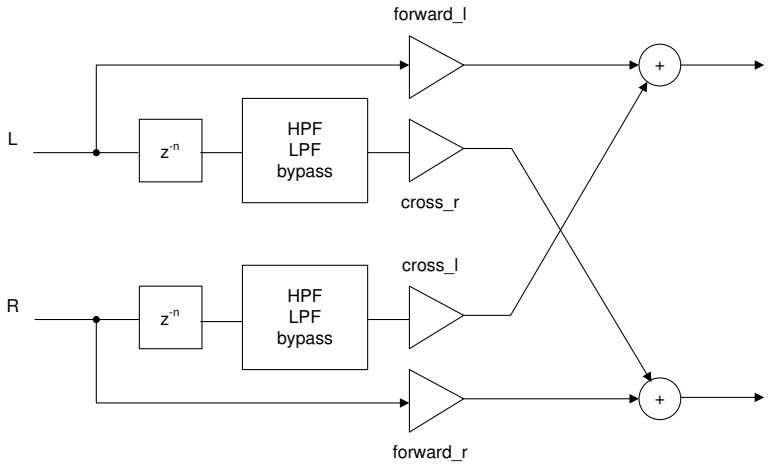
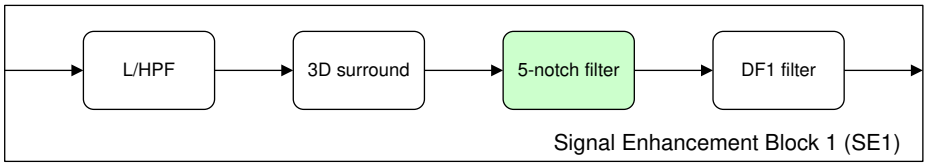


Figure 15 3D Surround Processing

The 3D surround depth is programmable; the default setting is OFF. The 3D surround processing can also be configured to create a mono mix of the Left and Right channels.

The 3D effect is enabled on the left and right channels using the SE1_3D_L_ENA and SE1_3D_R_ENA register bits defined in Table 13. These bits can be set independently of each other. For the derivation of the other associated registers, refer to the configuration tools supplied with the WM8946 Evaluation Kit.

5-NOTCH FILTER



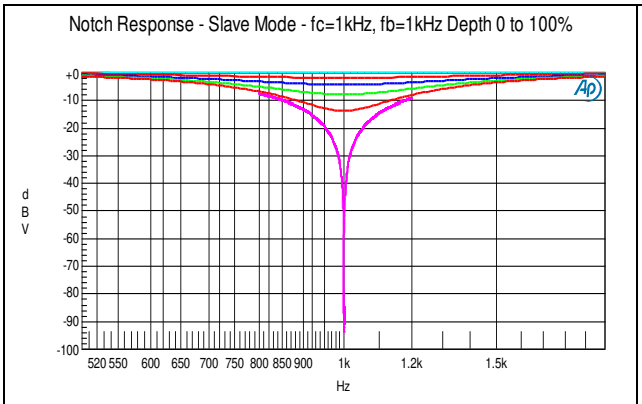
The 5-notch filter is part of the SE1 block. This function allows up to 5 programmable frequency bands to be attenuated. The frequency and width of each notch is configurable; the depth of the attenuation may also be adjusted. The default setting is bypass (OFF).

The notch filters may be enabled on the left and right channels using the SE1_NOTCH_L_ENA and SE1_NOTCH_R_ENA register bits defined in Table 13. Note that, although the 5-notch filter can be enabled on the left/right channels independently, the parameters that define the notch filters apply equally to the left and right channels, when enabled.

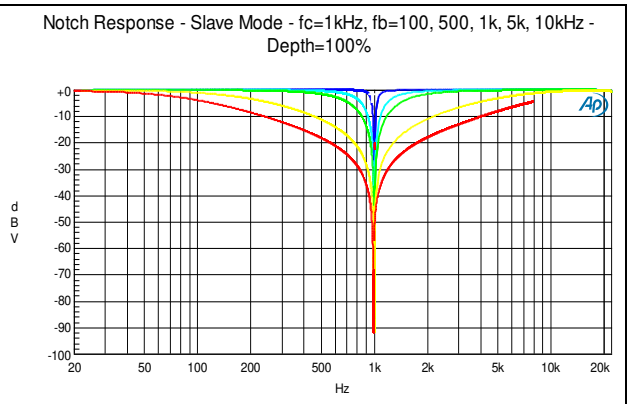
The notch filter coefficients are programmed in registers R72 to R91. For the derivation of these registers, refer to the configuration tools supplied with the WM8946 Evaluation Kit.

Note that the notch filters should not be configured for centre-frequencies below 120Hz. To apply filtering at low frequencies, the SE1 High Pass Filter should be used.

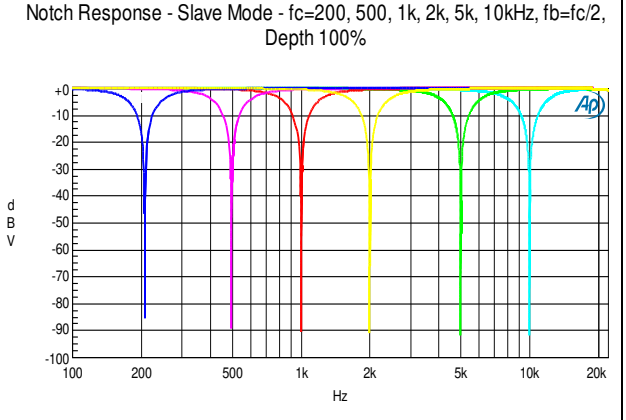
Typical applications for the notch filters are filtering of fixed-frequency noise or resonances; these might arise from a motor (e.g. DSC zoom lens motor) or from characteristics of the application housing. Example plots of the Notch filter response are shown in Figure 16.



1kHz notch, bandwidth 1kHz, depth 0% to 100% in 20% steps



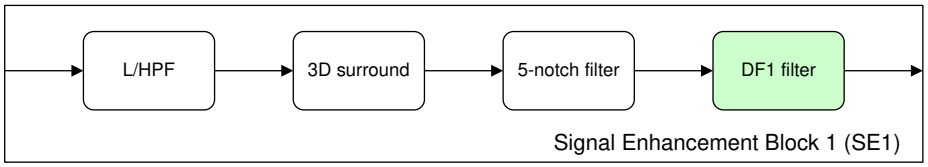
1kHz notch, 100% depth, bandwidth 100Hz, 500Hz, 1kHz, 5kHz, 10kHz



5 notches, bandwidth Fcentre/2, depth 100%

Figure 16 Notch Filter Responses

DF1 FILTER



The DF1 filter is part of the SE1 block. This provides a direct-form 1 standard filter, as illustrated in Figure 17. All of the filter coefficients are programmable for the left and right channels independently. The default coefficients give a transparent filter response.

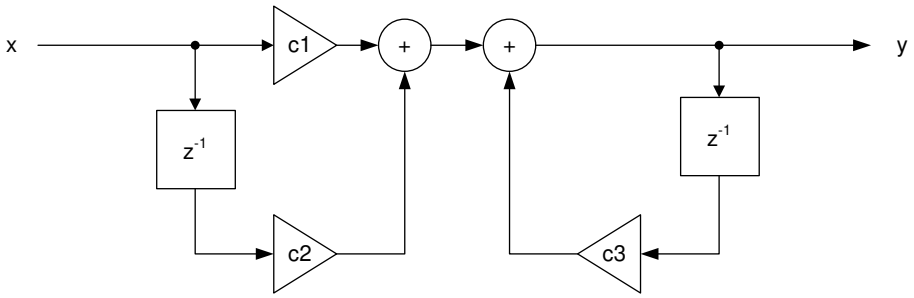


Figure 17 Direct-Form 1 Standard Filter Structure

The DF1 response is defined by the following equations:

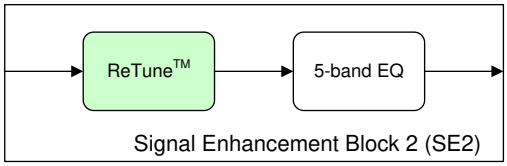
$$y[n] = c_1 x[n] + c_2 x[n-1] + c_3 y[n-1]$$

$$H = \frac{y}{x} = \frac{c_1 + c_2 z^{-1}}{1 - c_3 z^{-1}}$$

The DF1 filters may be enabled on the left and right channels using the SE1_DF1_L_ENA and SE1_DF1_R_ENA register bits defined in Table 13. For the derivation of the other associated registers, refer to the configuration tools supplied with the WM8946 Evaluation Kit.

The DF1 filter can be used to implement very complex response patterns, with specific phase and gain responses at different frequencies. Typical applications of this type of filter include the application of refinements or compensations to the 3D enhancement or other user-selected filters.

RETUNE™ FILTER



The ReTune™ filter is part of the SE2 block. This is a very advanced feature that is intended to perform frequency linearization according to the particular needs of the application microphone, loudspeaker or housing. The ReTune™ algorithms can provide acoustic equalisation and selective phase (delay) control of specific frequency bands.

The ReTune™ filters are enabled using the SE2_RETUNE_L_ENA and SE2_RETUNE_R_ENA register bits defined in Table 14.

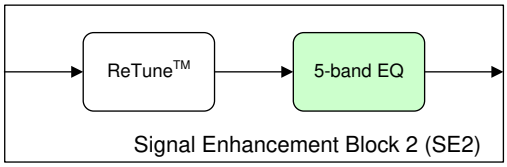
The ReTune™ filter coefficients are programmed in registers R101 to R132. For the derivation of the other ReTune configuration parameters, the WISCE™ software must be used to analyse the requirements of the application. (Refer to WISCE™ for further information.) If desired, one or more sets of register coefficients might be derived for different operating scenarios, and these may be

recalled and written to the CODEC registers as required in the target application. The ReTune configuration procedure involves the generation and analysis of test signals as outlined below.

To determine the characteristics of the microphone in an application, a test signal is applied to a loudspeaker that is in the acoustic path to the microphone. The received signal through the application microphone is analysed and compared with the received signal from a reference microphone in order to determine the characteristics of the application microphone.

To determine the characteristics of the loudspeaker in an application, a test signal is applied to the target application. A reference microphone is positioned in the normal acoustic path of the loudspeaker, and the received signal is analysed to determine how accurately the loudspeaker has reproduced the test signal.

5-BAND EQ

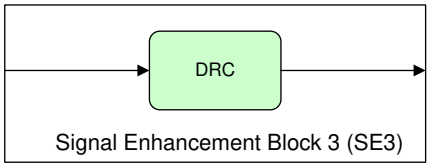


The 5-band EQ is part of the SE2 block. This function allows 5 frequency bands to be controlled. The upper and lower frequency bands are controlled by low-pass and high-pass filters respectively. The middle three frequency bands are notch filters. The cut-off / centre frequency of each filter is programmable, and up to 12dB gain or attenuation can be selected in each case. The left and right channel parameters may be programmed individually.

The 5-band EQ (Left channel) may be enabled using the SE2_5BEQ_L_ENA register bit defined in Table 14. Note that, to disable the 5-band EQ (Right channel), the gain of each Right channel frequency band must be set to 0dB. For the derivation of the other associated registers, refer to the WISCE software.

Typical applications of the 5-band EQ include the selection of user-preferences for different music types, such as ‘rock’, ‘dance’ or ‘classical’ EQ profiles.

DYNAMIC RANGE CONTROL (DRC)



The Dynamic Range Control (DRC) forms the SE3 block. The DRC provides a range of compression, limiting and noise gate functions to support optimum configuration for recording or playback modes. The DRC is configured using the control fields in registers R29 to R35 - see “Dynamic Range Control”.

SIGNAL ENHANCEMENT REGISTER CONTROLS

The SE1 'enable' bits are described in Table 13. Note that other control fields must also be determined and written to the WM8946 using WISCE™ or other tools. The registers described below only allow the sub-blocks of SE1 to be enabled or disabled.

Note that it is not recommended to access these control fields unless appropriate values have been written to the associated bits in registers R65 to R98.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R65 (41h) SE1_LHPF_CONFIG	1	SE1_LHPF_R_ENA	0	SE1 Right channel low-pass / high-pass filter enable 0 = Disabled 1 = Enabled
	0	SE1_LHPF_L_ENA	0	SE1 Left channel low-pass / high-pass filter enable 0 = Disabled 1 = Enabled
R68 (44h) SE1_3D_CONFIG	1	SE1_3D_R_ENA	0	SE1 Right channel 3D stereo enhancement filter enable 0 = Disabled 1 = Enabled
	0	SE1_3D_L_ENA	0	SE1 Left channel 3D stereo enhancement filter enable 0 = Disabled 1 = Enabled
R71 (47h) SE1_NOTCH_CONFIG	1	SE1_NOTCH_R_ENA	0	SE1 Right channel notch filters enable 0 = Disabled 1 = Enabled
	0	SE1_NOTCH_L_ENA	0	SE1 Left channel notch filters enable 0 = Disabled 1 = Enabled
R92 (5Ch) SE1_DF1_CONFIG	1	SE1_DF1_R_ENA	0	SE1 Right channel DF1 filter enable 0 = Disabled 1 = Enabled
	0	SE1_DF1_L_ENA	0	SE1 Left channel DF1 filter enable 0 = Disabled 1 = Enabled

Table 13 Signal Enhancement Block 1 (SE1)

The SE2 'enable' bits are described in Table 14. Note that (with the exception of the SE2 HPF) other control fields must also be determined and written to the WM8946 using WISCE™ or other tools. The registers described below only allow the sub-blocks of SE2 to be enabled or disabled.

Note that it is not recommended to access these control fields unless appropriate values have been written to the associated bits in registers R99 to R175.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R100 (64h) SE2_RETUNE_CONFIG	1	SE2_RETUNE_R_ENA	0	SE2 Right channel ReTune™ filter enable 0 = Disabled 1 = Enabled
	0	SE2_RETUNE_L_ENA	0	SE2 Left channel ReTune™ filter enable 0 = Disabled 1 = Enabled
R133 (85h) SE2_5BEQ_CONFIG	0	SE2_5BEQ_L_ENA	0	SE2 Left channel 5-band EQ enable 0 = Disabled 1 = Enabled

Table 14 Signal Enhancement Block 2 (SE2)

The register controls for Signal Enhancement Block SE3 are defined in the "Dynamic Range Control (DRC)" section.

DYNAMIC RANGE CONTROL (DRC)

The dynamic range controller (DRC) is a circuit which can be enabled in the digital playback or digital record path of the WM8946, depending upon the selected DSP mode. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system.

The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC also incorporates a Noise Gate function, which provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

The DRC is enabled as described in Table 15. The audio signal path controlled by the DRC depends upon the selected DSP Configuration mode - see "DSP Core" for details.

To remove any dc offsets from the input signal the ADC high pass filter must be enabled. The DRC will not function correctly unless this filter is enabled.

Note that the ADC HPF bit in register R26(1Ah) bit 0 is NOT enabled by default but MUST be used if DRC_ENA is enabled in register R29(1Dh) bit 7.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) DRC Control 1	7	DRC_ENA	0	DRC Enable 0 = Disabled 1 = Enabled

Table 15 DRC Enable

DRC COMPRESSION / EXPANSION / LIMITING

The DRC supports two different compression regions, separated by a “Knee” (shown as “Knee1” in Figure 18) at a specific input amplitude. In the region above the knee, the compression slope DRC_HI_COMP applies; in the region below the knee, the compression slope DRC_LO_COMP applies.

The DRC also supports a noise gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope DRC_NG_EXP.

For additional attenuation of signals in the noise gate region, an additional “knee” can be defined (shown as “Knee2” in Figure 18). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the DRC_LO_COMP and DRC_NG_EXP regions.

The overall DRC compression characteristic in “steady state” (i.e. where the input amplitude is near-constant) is illustrated in Figure 18.

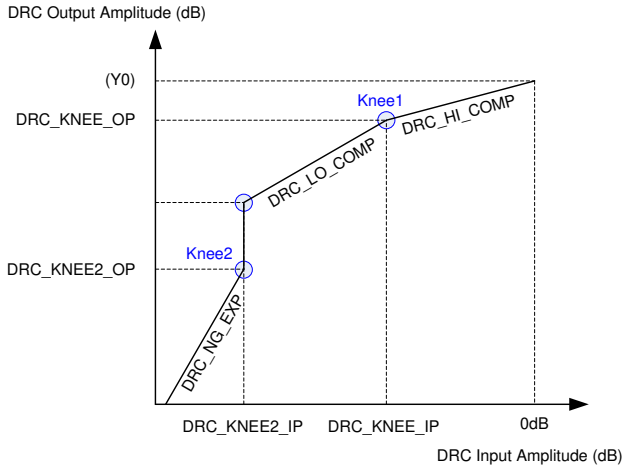


Figure 18 DRC Response Characteristic

The slope of the DRC response is determined by register fields DRC_HI_COMP and DRC_LO_COMP. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by the DRC_NG_EXP register. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (i.e. a change in input amplitude produces a larger change in output amplitude).

When the DRC_KNEE2_OP knee is enabled (“Knee2” in Figure 18), this introduces the vertical line in the response pattern illustrated, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in Table 16.

REF	PARAMETER	DESCRIPTION
1	DRC_KNEE_IP	Input level at Knee1 (dB)
2	DRC_KNEE_OP	Output level at Knee1 (dB)
3	DRC_HI_COMP	Compression ratio above Knee1
4	DRC_LO_COMP	Compression ratio below Knee1
5	DRC_KNEE2_IP	Input level at Knee2 (dB)
6	DRC_NG_EXP	Expansion ratio below Knee2
7	DRC_KNEE2_OP	Output level at Knee2 (dB)

Table 16 DRC Response Parameters

The noise gate is enabled when the DRC_NG_ENA register is set. When the noise gate is not enabled, parameters 5, 6, 7 above are ignored, and the DRC_LO_COMP slope applies to all input signal levels below Knee1.

The DRC_KNEE2_OP knee is enabled when the DRC_KNEE2_OP_ENA register is set. When this bit is not set, then parameter 7 above is ignored, and the Knee2 position always coincides with the low end of the DRC_LO_COMP region.

The "Knee1" point in Figure 18 is determined by register fields DRC_KNEE_IP and DRC_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation:

Y0 = DRC_KNEE_OP – (DRC_KNEE_IP * DRC_HI_COMP)

The DRC Compression / Expansion / Limiting parameters are defined in Table 17.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) DRC Control 1	8	DRC_NG_ENA	0	DRC Noise Gate Enable 0 = Disabled 1 = Enabled
R32 (20h) DRC Control 4	12:8	DRC_KNEE2_IP	000000	Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.
	7:2	DRC_KNEE_IP	000000	Input signal level at the Compressor 'Knee1'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved
R33 (21h) DRC Control 5	13	DRC_KNEE2_OP_ENA	0	DRC_KNEE2_OP Enable 0 = Disabled 1 = Enabled
	12:8	DRC_KNEE2_OP	00000	Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.
	7:3	DRC_KNEE_OP	00000	Output signal at the Compressor 'Knee1'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				11111 = Reserved
	2:0	DRC_HI_COMP	011	Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved
R35 (23h) DRC Control 7	9:8	DRC_NG_EXP	00	Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8
	7:5	DRC_LO_COMP	000	Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved

Table 17 DRC Control Registers

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields DRC_MINGAIN, DRC_MAXGAIN and DRC_NG_MINGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 18. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced.

The minimum gain in the Compression regions of the DRC response is set by DRC_MINGAIN. The minimum gain in the Noise Gate region is set by DRC_NG_MINGAIN. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by DRC_MAXGAIN prevents quiet signals (or silence) from being excessively amplified.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 (1Eh) DRC Control 2	12:9	DRC_NG_MINGAIN [3:0]	0110	Minimum gain the DRC can use to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved
	4:2	DRC_MINGAIN	001	Minimum gain the DRC can use to

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
		[2:0]		attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved
	1:0	DRC_MAXGAIN [1:0]	01	Maximum gain the DRC can use to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB

Table 18 DRC Gain Limits

GAIN READBACK

The gain applied by the DRC can be read from the DRC_GAIN register. This is a 16-bit, fixed-point value, which expresses the DRC gain as a voltage multiplier.

DRC_GAIN is coded as a fixed-point quantity, with an MSB weighting of 16. The first 7 bits represent the integer portion; the remaining bits represent the fractional portion. If desired, the value of this field may be interpreted by treating DRC_GAIN as an integer value, and dividing the result by 512, as illustrated in the following examples:

DRC_GAIN = 05D4 (hex) = 1380 (decimal)

Divide by 512 gives 2.914 voltage gain, or 4.645dB

DRC_GAIN = 0100 (hex) = 256 (decimal)

Divide by 512 gives 0.5 voltage gain, or -3.01dB

The DRC_GAIN register is defined in Table 19.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36 (24h) DRC Status	15:0	DRC_GAIN [15:0]		DRC Gain value. This is the DRC gain, expressed as a voltage multiplier. Fixed point coding, MSB = 64. The first 7 bits are the integer portion; the remaining bits are the fractional part.

Table 19 DRC Gain Readback

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the peak signal amplitude over a period of time.

The DRC_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. The DRC_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 20. Note that the register defaults are suitable for general purpose microphone use.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) DRC Control 3	7:4	DRC_ATK [3:0]	0100	Attack rate relative to input signal (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved
	3:0	DRC_DCY [3:0]	0010	Decay rate relative to input signal (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved

Table 20 DRC Time Constants

The Attack and Decay times noted in Table 20 describe the DRC response to a DC step signal. The Attack and Decay response to other signal conditions will be dependent on the characteristics of the audio signal (eg. frequency content). The applicable compression ratio, and the extent of the change in input signal amplitude, will also impact on the overall Attack and Decay times.

Typical response times, based upon sine wave test conditions, are described in Table 21. It is recommended that the DRC Decay rate should be at least 8 times longer than the DRC Attack rate.

DRC_ATK	ATTACK RATE (seconds/6dB)	DRC_DCY	DECAY RATE (seconds/6dB)
0000		0000	333ms
0001	400us	0001	550ms
0010	810us	0010	1.05s
0011	1.6ms	0011	2.1s
0100	3.2ms	0100	4.2s
0101	6.5ms	0101	8.4s
0110	13ms	0110	16.8s
0111	26ms	0111	33.6s
1000	52ms	1000	67.3s
1001	104ms		
1010	208ms		
1011	416ms		

Table 21 Typical Attack / Decay Time Constants (Sine Wave test signal)

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRC_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path. The DRC Anti-Clip control is described in Table 22.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) DRC Control 1	1	DRC_ANTICLIP	1	DRC Anti-clip Enable 0 = Disabled 1 = Enabled

Table 22 DRC Anti-Clip Control

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.

Note: The Anti-Clip and Quick Release features should not be used at the same time.

QUICK-RELEASE CONTROL

The DRC includes a Quick-Release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The Quick Release feature ensures that these transients do not cause the intended signal to be masked by the longer time constants of DRC_DCY.

The Quick-Release feature is enabled by setting the DRC_QR bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by DRC_QR_THR, then the normal decay rate (DRC_DCY) is ignored and a faster decay rate (DRC_QR_DCY) is used instead.

The DRC Quick-Release control bits are described in Table 23.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 (1Dh) DRC Control 1	2	DRC_QR	1	DRC Quick-release Enable 0 = Disabled 1 = Enabled
R34 (22h) DRC Control 6	3:2	DRC_QR_THR [1:0]	00	DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB
	1:0	DRC_QR_DCY [1:0]	00	DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved

Table 23 DRC Quick-Release Control

Note: The Anti-Clip and Quick Release features should not be used at the same time.

DRC INITIAL VALUE

The DRC can be set up to a defined initial condition based on the expected signal level when the DRC is enabled. This can be set using the DRC_INIT bits in register R35 (23h) bits 4 to 0.

Note: This does NOT set the initial gain of the DRC. It sets the expected signal level of the DRC input signal when the DRC is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h) DRC Control 7	4:0	DRC_INIT	00000	Initial value at DRC startup 00000 = 0dB 00001 = -3.75dB … (-3.75dB steps) 11111 = -116.25dB

Table 24 DRC Initial Value

DIGITAL-TO-ANALOGUE CONVERTER (DAC)

The WM8946 DACs receive digital input data from the digital audio interface. (Note that, depending on the DSP Configuration mode, the digital input may first be processed and filtered in the DSP Core.) The digital audio data is converted to oversampled bit-streams in the on-chip, true 24-bit digital interpolation filters. The bit-stream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals.

The analogue outputs from the DACs can then be mixed with other analogue inputs before being sent to the analogue output pins (see “Output Signal Path”).

The DACs are enabled by the DACL_ENA and DACR_ENA register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 2	1	DACR_ENA	0	Right DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing right channel data from the DAC or Digital Beep Generator.
	0	DACL_ENA	0	Left DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing left channel data from the DAC or Digital Beep Generator.

Table 25 DAC Enable Control

Note: If the WM8946 is to be used in mono mode for playback then the left and right DACs must both be enabled.

DAC DIGITAL VOLUME CONTROL

The output of the DACs can be digitally amplified or attenuated over a range from -71.625dB to +23.625dB in 0.375dB steps. The volume of each channel can be controlled separately using DACL_VOL or DACR_VOL. The DAC Volume is part of the DAC Digital Filters block. The gain for a given eight-bit code X is given by:

$0.375 \times (X-192)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The DAC_VU bit controls the loading of digital volume control data. When DAC_VU is set to 0, the DACL_VOL or DACR_VOL control data is loaded into the respective control register, but does not actually change the digital gain setting. Both left and right gain settings are updated when a 1 is written to DAC_VU. This makes it possible to update the gain of both channels simultaneously.

Note that SYSCLK must be enabled when writing to the DAC_VU bits. (See "Clocking and Sample Rates" for details of SYSCLK.)

The output of the DACs can be digitally muted using the DACL_MUTE or DACR_MUTE bits. Both DACs are muted simultaneously when the DAC_MUTEALL bit is set.

A digital soft-mute feature is provided in order to avoid sudden glitches in the analogue signal. When DAC_VOL_RAMP is enabled, then all mute, un-mute or volume change commands are implemented as a gradual volume change in the digital domain. The rate at which the volume ramps up is half of the sample freq (fs/2). The DAC_VOL_RAMP register field is described in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) DAC Control 1	8	DAC_MUTEALL	1	DAC Digital Mute for All Channels: 0 = Disable Mute 1 = Enable Mute on all channels
R22 (16h) DAC Control 2	4	DAC_VOL_RAMP	1	DAC Volume Ramp control 0 = Disabled 1 = Enabled
R23 (17h) Left DAC Digital Vol	12	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause Left and Right DAC volume to be updated simultaneously
	8	DACL_MUTE	0	Left DAC Digital Mute 0 = Disable Mute 1 = Enable Mute
	7:0	DACL_VOL [7:0]	1100_0000 (0dB)	Left DAC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB (See Table 27 for volume range)
R24 (18h) Right DAC Digital Vol	12	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause Left and Right DAC volume to be updated simultaneously
	8	DACR_MUTE	0	Right DAC Digital Mute 0 = Disable Mute 1 = Enable Mute
	7:0	DACR_VOL [7:0]	1100_0000 (0dB)	Right DAC volume control 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB (See Table 27 for volume range)

Table 26 DAC Digital Volume Control

DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)	DACL_VOL or DACR_VOL	Volume (dB)
0h	MUTE	40h	-48.000	80h	-24.000	C0h	0.000
1h	-71.625	41h	-47.625	81h	-23.625	C1h	0.375
2h	-71.250	42h	-47.250	82h	-23.250	C2h	0.750
3h	-70.875	43h	-46.875	83h	-22.875	C3h	1.125
4h	-70.500	44h	-46.500	84h	-22.500	C4h	1.500
5h	-70.125	45h	-46.125	85h	-22.125	C5h	1.875
6h	-69.750	46h	-45.750	86h	-21.750	C6h	2.250
7h	-69.375	47h	-45.375	87h	-21.375	C7h	2.625
8h	-69.000	48h	-45.000	88h	-21.000	C8h	3.000
9h	-68.625	49h	-44.625	89h	-20.625	C9h	3.375
Ah	-68.250	4Ah	-44.250	8Ah	-20.250	CAh	3.750
Bh	-67.875	4Bh	-43.875	8Bh	-19.875	CBh	4.125
Ch	-67.500	4Ch	-43.500	8Ch	-19.500	CCh	4.500
Dh	-67.125	4Dh	-43.125	8Dh	-19.125	CDh	4.875
Eh	-66.750	4Eh	-42.750	8Eh	-18.750	CEh	5.250
Fh	-66.375	4Fh	-42.375	8Fh	-18.375	CFh	5.625
10h	-66.000	50h	-42.000	90h	-18.000	D0h	6.000
11h	-65.625	51h	-41.625	91h	-17.625	D1h	6.375
12h	-65.250	52h	-41.250	92h	-17.250	D2h	6.750
13h	-64.875	53h	-40.875	93h	-16.875	D3h	7.125
14h	-64.500	54h	-40.500	94h	-16.500	D4h	7.500
15h	-64.125	55h	-40.125	95h	-16.125	D5h	7.875
16h	-63.750	56h	-39.750	96h	-15.750	D6h	8.250
17h	-63.375	57h	-39.375	97h	-15.375	D7h	8.625
18h	-63.000	58h	-39.000	98h	-15.000	D8h	9.000
19h	-62.625	59h	-38.625	99h	-14.625	D9h	9.375
1Ah	-62.250	5Ah	-38.250	9Ah	-14.250	DAh	9.750
1Bh	-61.875	5Bh	-37.875	9Bh	-13.875	DBh	10.125
1Ch	-61.500	5Ch	-37.500	9Ch	-13.500	DCh	10.500
1Dh	-61.125	5Dh	-37.125	9Dh	-13.125	DDh	10.875
1Eh	-60.750	5Eh	-36.750	9Eh	-12.750	DEh	11.250
1Fh	-60.375	5Fh	-36.375	9Fh	-12.375	DFh	11.625
20h	-60.000	60h	-36.000	A0h	-12.000	E0h	12.000
21h	-59.625	61h	-35.625	A1h	-11.625	E1h	12.375
22h	-59.250	62h	-35.250	A2h	-11.250	E2h	12.750
23h	-58.875	63h	-34.875	A3h	-10.875	E3h	13.125
24h	-58.500	64h	-34.500	A4h	-10.500	E4h	13.500
25h	-58.125	65h	-34.125	A5h	-10.125	E5h	13.875
26h	-57.750	66h	-33.750	A6h	-9.750	E6h	14.250
27h	-57.375	67h	-33.375	A7h	-9.375	E7h	14.625
28h	-57.000	68h	-33.000	A8h	-9.000	E8h	15.000
29h	-56.625	69h	-32.625	A9h	-8.625	E9h	15.375
2Ah	-56.250	6Ah	-32.250	AAh	-8.250	EAh	15.750
2Bh	-55.875	6Bh	-31.875	ABh	-7.875	EBh	16.125
2Ch	-55.500	6Ch	-31.500	ACh	-7.500	ECh	16.500
2Dh	-55.125	6Dh	-31.125	ADh	-7.125	EDh	16.875
2Eh	-54.750	6Eh	-30.750	AEh	-6.750	EEh	17.250
2Fh	-54.375	6Fh	-30.375	AFh	-6.375	EFh	17.625
30h	-54.000	70h	-30.000	B0h	-6.000	F0h	18.000
31h	-53.625	71h	-29.625	B1h	-5.625	F1h	18.375
32h	-53.250	72h	-29.250	B2h	-5.250	F2h	18.750
33h	-52.875	73h	-28.875	B3h	-4.875	F3h	19.125
34h	-52.500	74h	-28.500	B4h	-4.500	F4h	19.500
35h	-52.125	75h	-28.125	B5h	-4.125	F5h	19.875
36h	-51.750	76h	-27.750	B6h	-3.750	F6h	20.250
37h	-51.375	77h	-27.375	B7h	-3.375	F7h	20.625
38h	-51.000	78h	-27.000	B8h	-3.000	F8h	21.000
39h	-50.625	79h	-26.625	B9h	-2.625	F9h	21.375
3Ah	-50.250	7Ah	-26.250	BAh	-2.250	FAh	21.750
3Bh	-49.875	7Bh	-25.875	BBh	-1.875	FBh	22.125
3Ch	-49.500	7Ch	-25.500	BCh	-1.500	FCh	22.500
3Dh	-49.125	7Dh	-25.125	BDh	-1.125	FDh	22.875
3Eh	-48.750	7Eh	-24.750	BEh	-0.750	FEh	23.250
3Fh	-48.375	7Fh	-24.375	BFh	-0.375	FFh	23.625

Table 27 DAC Digital Volume Range

DAC AUTO-MUTE

The DAC digital mute and volume controls are described earlier in Table 26.

The DAC also incorporates an analogue auto-mute, which is enabled by setting DAC_AUTOMUTE. When the auto-mute is enabled, and a series of 1024 consecutive zero-samples is detected, the DAC output is muted in order to attenuate noise that might be present in output signal path. The DAC resumes normal operation as soon as digital audio data is detected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) DAC Control 1	4	DAC_AUTOMUTE	1	DAC Auto-Mute Control 0 = Disabled 1 = Enabled

Table 28 DAC Auto Mute

Note: The DAC_AUTOMUTE bit should not be set when the BEEP generator is used.

DAC SLOPING STOPBAND FILTER

Two DAC filter types are available, selected by the register bit DAC_SB_FLT. When operating at lower sample rates (e.g. during voice communication) it is recommended that the sloping stopband filter type is selected (DAC_SB_FLT=1) to reduce out-of-band noise which can be audible at low DAC sample rates. See “Digital Filter Characteristics” for details of DAC filter characteristics.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 (16h) DAC Control 2	0	DAC_SB_FLT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 29 DAC Sloping Stopband Filter

DIGITAL BEEP GENERATOR

The WM8946 provides a digital signal generator which can be used to inject an audio tone (beep) into the DAC signal path. The output of the beep generator is digitally mixed with the DAC outputs, after the DAC digital volume.

The beep is enabled using BEEP_ENA. The beep function creates an approximation of a Sine wave. The audio frequency is set using BEEP_RATE. The beep volume is set using BEEP_GAIN. Note that the volume of the digital beep generator is not affected by the DAC volume or DAC mute controls.

The DAC_AUTOMUTE bit should not be set when the BEEP generator is used.

The digital beep generator control fields are described in Table 30.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 (25h) Beep Control 1	6:3	BEEP_GAIN [3:0]	0000	Digital Beep Volume Control 0000 = mute 0001 = -83dB 0010 = -77dB … (6dB steps) 1111 = +1dB
	2:1	BEEP_RATE [1:0]	01	Beep Waveform Control 00 = Reserved 01 = 1kHz 10 = 2kHz 11 = 4kHz
	0	BEEP_ENA	0	Digital Beep Enable 0 = Disabled 1 = Enabled Note that the DAC and associated signal path needs to be enabled when using the digital beep.

Table 30 Digital Beep Generator

Note: The beep generator is clocked by the left channel DAC clock. If the beep signal is used on the right channel only, the left channel DAC must be enabled.

OUTPUT SIGNAL PATH

The WM8946 provides two Line Output mixers and two Speaker Output mixers. Multiple inputs to each mixer provide a high degree of flexibility to route different signal paths to each of the four analogue outputs.

The DAC outputs can be routed to the mixers either directly or in inverted phase. This makes it easy to generate differential (BTL) or mono output signals.

The Auxiliary input AUX1 may be routed directly to the Speaker outputs, bypassing the Speaker PGAs and mixers. This can be used to provide a fixed-gain signal path for a “PC Beep” or similar application.

The output signal paths and associated control registers are illustrated in Figure 19.

Note that the speaker outputs are intended to drive a mono headset or speaker (in BTL configuration). They are not designed to drive stereo speakers directly.

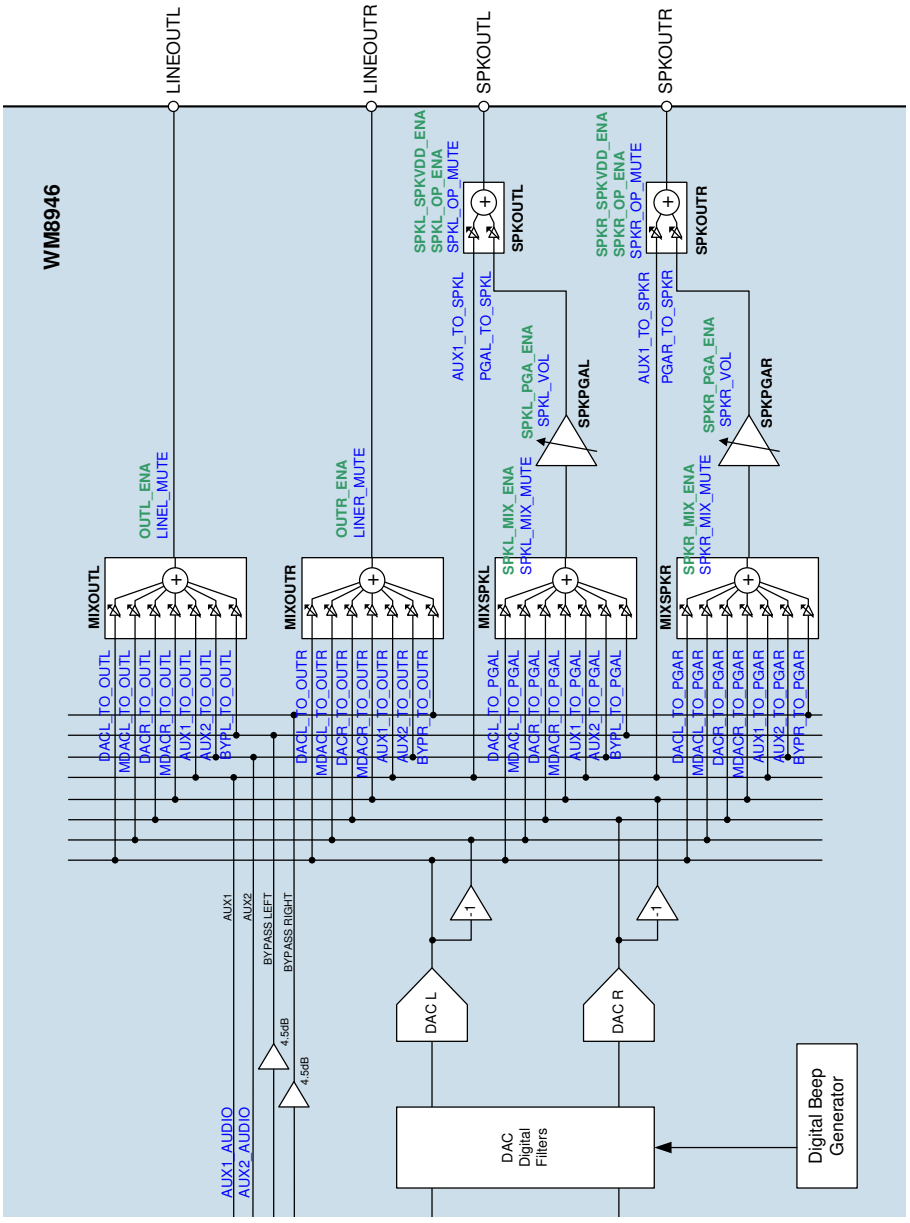


Figure 19 Output Signal Paths

OUTPUT SIGNAL PATHS ENABLE

Each analogue output pin can be independently enabled or disabled using the register bits described in Table 31. The speaker output PGAs and mixers can also be controlled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power management 2	15	OUTR_ENA	0	LINEOUTR enable 0 = Disabled 1 = Enabled
	14	OUTL_ENA	0	LINEOUTL enable 0 = Disabled 1 = Enabled
	13	SPKR_PGA_ENA	0	Speaker Right PGA enable 0 = Disabled 1 = Enabled
	12	SPKL_PGA_ENA	0	Speaker Left PGA enable 0 = Disabled 1 = Enabled
	11	SPKR_SPKVDD_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_OP_ENA. When powering down SPKOUTR, the SPKR_SPKVDD_ENA bit should be reset first.
	10	SPKL_SPKVDD_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_OP_ENA. When powering down SPKOUTL, the SPKL_SPKVDD_ENA bit should be reset first
	7	SPKR_OP_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_SPKVDD_ENA. When powering up SPKOUTR, the SPKR_OP_ENA bit should be enabled first.
	6	SPKL_OP_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_SPKVDD_ENA. When powering up SPKOUTL, the SPKL_OP_ENA bit should be enabled first
	3	SPKR_MIX_ENA	0	Right speaker output mixer enable 0 = Disabled 1 = Enabled
	2	SPKL_MIX_ENA	0	Left speaker output mixer enable 0 = Disabled 1 = Enabled

Table 31 Output Signal Paths Enable

To enable the output PGAs and mixers, the reference voltage VMID and the bias current must also be enabled. See “Reference Voltages and Master Bias” for details of the associated controls VMID_SEL and BIAS_ENA.

Note that the Line outputs, Speaker outputs and Speaker PGA mixers are all muted by default. The required signal paths must be un-muted using the control bits described in the respective tables below.

LINE OUTPUT MIXER CONTROL

The Line Output mixer controls are described in Table 32 for the Left Channel (MIXOUTL) and Table 33 for the Right Channel (MIXOUTR). These allow any of the DACL/R, Inverted DACL/R, AUX1/2 and one of the ADC Bypass signals to be mixed. The output of each mixer can be muted also, using the LINEL_MUTE and LINER_MUTE bits.

Note that a signal gain of 4.5dB is applied to the ADC Bypass signals, as shown in Figure 19. Care should be taken when mixing more than one path to the Line Output mixers in order to avoid clipping. The gain of each input path is adjustable using a selectable -6dB control in each path to facilitate this.

Note that the attenuation control fields DACL_TO_OUTL_ATTEN and DACR_TO_OUTL_ATTEN control both the DAC and the Inverted DAC mixer paths to the Left Channel output mixer. The equivalent applies to DACL_TO_OUTR_ATTEN and DACR_TO_OUTR_ATTEN also. Note that the DAC input levels may also be controlled by the DAC digital volume control - see “Digital to Analogue Converter (DAC)” for further details.

When the AUX1 or AUX2 pin is used as an audio input, that pin must be configured for audio using the AUX1_AUDIO or AUX2_AUDIO register bits. These bits are defined in Table 2 (see “Analogue Input Signal Path”).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) Output ctrl	8	LINEL_MUTE	1	LINEOUTL Output Mute 0 = Disable Mute 1 = Enable Mute
R49 (31h) Line L mixer control 1	6	BYPL_TO_OUTL	0	Left Input PGA (ADC bypass) to Left Output Mixer select 0 = Disabled 1 = Enabled
	5	MDACL_TO_OUTL	0	Inverted Left DAC to Left Output Mixer select 0 = Disabled 1 = Enabled
	4	MDACR_TO_OUTL	0	Inverted Right DAC to Left Output Mixer select 0 = Disabled 1 = Enabled
	3	DACL_TO_OUTL	0	Left DAC to Left Output Mixer select 0 = Disabled 1 = Enabled
	2	DACR_TO_OUTL	0	Right DAC to Left Output Mixer select 0 = Disabled 1 = Enabled
	1	AUX2_TO_OUTL	0	AUX2 Audio Input to Left Output Mixer select 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	AUX1_TO_OUTL	0	AUX1 Audio Input to Left Output Mixer select 0 = Disabled 1 = Enabled
R51 (33h) Line L mixer control 2	6	BYPL_TO_OUTL_ATTEN	0	Left Input PGA (ADC bypass) to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	3	DACL_TO_OUTL_ATTEN	0	Left DAC to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	2	DACR_TO_OUTL_ATTEN	0	Right DAC to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	1	AUX2_TO_OUTL_ATTEN	0	AUX2 Audio Input to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	0	AUX1_TO_OUTL_ATTEN	0	AUX1 Audio Input to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation

Table 32 Left Output Mixer (MIXOUTL) Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) Output ctrl	9	LINER_MUTE	1	LINEOUTR Output Mute 0 = Disable Mute 1 = Enable Mute
R50 (32h) Line R mixer control 1	6	BYPR_TO_OUTR	0	Right Input PGA (ADC bypass) to Right Output Mixer select 0 = Disabled 1 = Enabled
	5	MDACL_TO_OUTR	0	Inverted Left DAC to Right Output Mixer select 0 = Disabled 1 = Enabled
	4	MDACR_TO_OUTR	0	Inverted Right DAC to Right Output Mixer select 0 = Disabled 1 = Enabled
	3	DACL_TO_OUTR	0	Left DAC to Right Output Mixer select 0 = Disabled 1 = Enabled
	2	DACR_TO_OUTR	0	Right DAC to Right Output Mixer select 0 = Disabled 1 = Enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	AUX2_TO_OUTR	0	AUX2 Audio Input to Right Output Mixer select 0 = Disabled 1 = Enabled
	0	AUX1_TO_OUTR	0	AUX1 Audio Input to Right Output Mixer select 0 = Disabled 1 = Enabled
R52 (34h) Line R mixer control 2	6	BYPR_TO_OUTR_ATTEN	0	Right Input PGA (ADC bypass) to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	3	DACL_TO_OUTR_ATTEN	0	Left DAC to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	2	DACR_TO_OUTR_ATTEN	0	Right DAC to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	1	AUX2_TO_OUTR_ATTEN	0	AUX2 Audio Input to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	0	AUX1_TO_OUTR_ATTEN	0	AUX1 Audio Input to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation

Table 33 Right Output Mixer (MIXOUTR) Control

SPEAKER PGA MIXER CONTROL

The Speaker PGA mixer controls are described in Table 34 for the left channel (MIXSPKL) and Table 35 for the right channel (MIXSPKR). These allow any of the DACL/R, Inverted DACL/R, AUX1/2 and one of the ADC Bypass signals to be mixed. The output of each PGA mixer can be muted also, using the SPKL_MIX_MUTE and SPKR_MIX_MUTE bits.

Note that the output from the Speaker PGA mixer is also controlled by the Speaker PGA Volume control and the Speaker Output control described in the following sections.

Note that a signal gain of 4.5dB is applied to the ADC Bypass signals, as shown in Figure 19. Care should be taken when enabling more than one path to the Speaker PGA mixers in order to avoid clipping. The gain of each input path is adjustable using a selectable -6dB control in each path to facilitate this.

Note that the attenuation control fields DACL_TO_PGAL_ATTEN and DACR_TO_PGAL_ATTEN control both the DAC and the Inverted DAC mixer paths to the Left Speaker PGA mixer. The equivalent applies to DACL_TO_PGAR_ATTEN and DACR_TO_PGAR_ATTEN also. Note that the DAC input levels may also be controlled by the DAC digital volume control - see “Digital to Analogue Converter (DAC)” for further details.

When the AUX1 or AUX2 pin is used as an audio input, that pin must be configured for audio using the AUX1_AUDIO or AUX2_AUDIO register bits. These bits are defined in Table 2 (see “Analogue Input Signal Path”).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION

R3 (03h) Power Management 1	4	SPKL_MIX_MUTE	1	Left Speaker PGA Mixer Mute 0 = Disable Mute 1 = Enable Mute
R43 (2Bh) SPK mixer control 1	6	BYPL_TO_PGAL	0	Left Input PGA (ADC bypass) to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	5	MDACL_TO_PGAL	0	Inverted Left DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	4	MDACR_TO_PGAL	0	Inverted Right DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	3	DACL_TO_PGAL	0	Left DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	2	DACR_TO_PGAL	0	Right DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	1	AUX2_TO_PGAL	0	AUX2 Audio Input to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	0	AUX1_TO_PGAL	0	AUX1 Audio Input to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled
R45 (2Dh) SPK mixer control 3	6	BYPL_TO_PGAL_ATTEN	0	Left Input PGA (ADC bypass) to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	3	DACL_TO_PGAL_ATTEN	0	Left DAC to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	2	DACR_TO_PGAL_ATTEN	0	Right DAC to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	1	AUX2_TO_PGAL_ATTEN	0	AUX2 Audio Input to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	0	AUX1_TO_PGAL_ATTEN	0	AUX1 Audio Input to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation

Table 34 Left Speaker PGA Mixer (MIXSPKL) Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION

R3 (03h) Power Management 1	5	SPKR_MIX_MUTE	1	Right Speaker PGA Mixer Mute 0 = Disable Mute 1 = Enable Mute
R44 (2Ch) SPK mixer control 2	6	BYPR_TO_PGAR	0	Right Input PGA (ADC bypass) to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	5	MDACL_TO_PGAR	0	Inverted Left DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	4	MDACR_TO_PGAR	0	Inverted Right DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	3	DACL_TO_PGAR	0	Left DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	2	DACR_TO_PGAR	0	Right DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	1	AUX2_TO_PGAR	0	AUX2 Audio Input to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
	0	AUX1_TO_PGAR	0	AUX1 Audio Input to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled
R46 (2Eh) SPK mixer control 4	6	BYPR_TO_PGAR_ATTEN	0	Right Input PGA (ADC bypass) to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	3	DACL_TO_PGAR_ATTEN	0	Left DAC to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	2	DACR_TO_PGAR_ATTEN	0	Right DAC to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	1	AUX2_TO_PGAR_ATTEN	0	AUX2 Audio Input to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation
	0	AUX1_TO_PGAR_ATTEN	0	AUX1 Audio Input to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation

Table 35 Right Speaker PGA Mixer (MIXSPKR) Control

SPEAKER PGA VOLUME CONTROL

The volume control of the left and right Speaker PGAs can be independently adjusted using the SPKL_VOL and SPKR_VOL register fields as described in Table 36. The gain range is -57dB to +6dB in 1dB steps.

Note that the output from the Speaker PGA Volume control is an input to the Speaker Output control described in the following section.

To prevent "zipper noise", a zero-cross function is provided on the Speaker PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA. See “Clocking and Sample Rates” for the definition of this bit.

The SPK_VU bits control the loading of the Speaker PGA volume data. When SPK_VU is set to 0, the volume control data will be loaded into the respective control register, but will not actually change the gain setting. The left and right Speaker PGA volume settings are both updated when a 1 is written to either SPK_VU bit. This makes it possible to update the gain of the left and right output paths simultaneously.

Note that SYSCLK must be enabled when writing to the SPK_VU bits. (See “Clocking and Sample Rates” for details of SYSCLK.)

The Speaker PGA volume control register fields are described in Table 36.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Left SPK volume ctrl	8	SPK_VU	0	Speaker PGA Volume Update Writing a 1 to this bit will cause the Left and Right Speaker PGA volumes to be updated simultaneously.
	7	SPKL_ZC	0	Left Speaker PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	6	SPKL_PGA_MUTE	1	Left Speaker PGA Mute 0 = Disable Mute 1 = Enable Mute
	5:0	SPKL_VOL	11_1001 (0dB)	Left Speaker PGA Volume 00_0000 = -57dB gain 00_0001 = -56dB … 11_1001 = 0dB ... 11_1111 = +6dB (See Table 37 for volume range)
R48 (30h) Right SPK volume ctrl	8	SPK_VU	0	Speaker PGA Volume Update Writing a 1 to this bit will cause the Left and Right Speaker PGA volumes to be updated simultaneously.
	7	SPKR_ZC	0	Right Speaker PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	6	SPKR_PGA_MUTE	1	Right Speaker PGA Mute 0 = Disable Mute 1 = Enable Mute

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5:0	SPKR_VOL	11_1001 (0dB)	Right Speaker PGA Volume 00_0000 = -57dB gain 00_0001 = -56dB … 11_1001 = 0dB ... 11_1111 = +6dB (See Table 37 for volume range)

Table 36 Speaker PGA Volume Control

PGA GAIN SETTING	VOLUME (dB)	PGA GAIN SETTING	VOLUME (dB)
00h	-57	20h	-25
01h	-56	21h	-24
02h	-55	22h	-23
03h	-54	23h	-22
04h	-53	24h	-21
05h	-52	25h	-20
06h	-51	26h	-19
07h	-50	27h	-18
08h	-49	28h	-17
09h	-48	29h	-16
0Ah	-47	2Ah	-15
0Bh	-46	2Bh	-14
0Ch	-45	2Ch	-13
0Dh	-44	2Dh	-12
0Eh	-43	2Eh	-11
0Fh	-42	2Fh	-10
10h	-41	30h	-9
11h	-40	31h	-8
12h	-39	32h	-7
13h	-38	33h	-6
14h	-37	34h	-5
15h	-36	35h	-4
16h	-35	36h	-3
17h	-34	37h	-2
18h	-33	38h	-1
19h	-32	39h	0
1Ah	-31	3Ah	+1
1Bh	-30	3Bh	+2
1Ch	-29	3Ch	+3
1Dh	-28	3Dh	+4
1Eh	-27	3Eh	+5
1Fh	-26	3Fh	+6

Table 37 Speaker PGA Volume Range

SPEAKER OUTPUT CONTROL

Each Speaker output has its own output mixer. This allows the output of the respective Speaker PGA to be enabled or disabled, and also allows the Auxiliary input AUX1 to be routed directly to either Speaker output. The two Speaker outputs can be muted also, using the SPKR_OP_MUTE and SPKL_OP_MUTE.

The AUX1 path can be used to provide a fixed-gain signal path that is unaffected by the Speaker PGA setting. This feature is intended for a “PC Beep” or similar applications.

Care should be taken when enabling more than one path to the Speaker Output mixers in order to avoid clipping. The gain of each input path is adjustable using a selectable -6dB control in each path to facilitate this.

When the AUX1 pin is used as an audio input, that pin must be configured for audio using the AUX1_AUDIO register bit. This bit is defined in Table 2 (see “Analogue Input Signal Path”).

The Speaker Output control registers are described in Table 38.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 (03h) Power Management 1	9	SPKR_OP_MUTE	1	SPKOUTR Output Mute 0 = Disable Mute 1 = Enable Mute
	8	SPKL_OP_MUTE	1	SPKOUTL Output Mute 0 = Disable Mute 1 = Enable Mute
R43 (2Bh) SPK mixer control 1	8	AUX1_TO_SPKL	0	AUX1 Audio Input to Left Speaker Output select 0 = Disabled 1 = Enabled
	7	PGAL_TO_SPKL	0	Left Speaker PGA Mixer to Left Speaker Output select 0 = Disabled 1 = Enabled
R44 (2Ch) SPK mixer control 2	8	AUX1_TO_SPKR	0	AUX1 Audio Input to Right Speaker Output select 0 = Disabled 1 = Enabled
	7	PGAR_TO_SPKR	0	Right Speaker PGA Mixer to Right Speaker Output select 0 = Disabled 1 = Enabled
R45 (2Dh) SPK mixer control 3	8	AUX1_TO_SPKL_ATTEN	0	AUX1 Audio Input to Left Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation
	7	PGAL_TO_SPKL_ATTEN	0	Left Speaker PGA Mixer to Left Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation
R46 (2Eh) SPK mixer control 4	8	AUX1_TO_SPKR_ATTEN	0	AUX1 Audio Input to Right Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation
	7	PGAR_TO_SPKR_ATTEN	0	Right Speaker PGA Mixer to Right Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation

Table 38 Speaker Output Control

ANALOGUE OUTPUTS

The Line outputs and Speaker outputs are highly configurable and may be used in many different ways. The output mixers can be configured to generate mono or stereo, single-ended or differential outputs. The Class AB Speaker output driver can deliver up to 400mW into an 8Ω speaker in BTL mode. Alternatively, the Speaker outputs can deliver 40mW to a stereo 16Ω headphone load.

LINE OUTPUTS

The line outputs LINEOUTL and LINEOUTR are the external connections to the Line output mixers. In a typical application, these will deliver a stereo pair of outputs in single-ended configuration.

For stereo line output, the Left and Right output mixers are used to generate the Left and Right output signals respectively.

A differential mono (left+right) DAC output may be generated at the line outputs by routing an inverted DAC signal to one output and the non-inverted signal from the other DAC to the other line output.

A differential output from a single DAC may be generated at the line outputs by routing the inverted DAC signal to one output and the non-inverted DAC signal to the other. When the speaker outputs are similarly configured for the other DAC channel, then stereo differential output is possible.

SPEAKER OUTPUTS

The speaker outputs SPKOUTL and SPKOUTR are the external connections to the Speaker Output mixers. These outputs are intended for a mono speaker or headphone in BTL configuration or for a stereo line load.

For stereo line configuration, the Left and Right Speaker Output mixers are used to generate the Left and Right output signals respectively.

For mono speaker or headphone configuration, a BTL output from the DACs may be generated by routing an inverted DAC signal to one speaker output and the non-inverted signal from the other DAC to the other speaker output. The auxiliary inputs AUX1 or AUX2 may be routed to the mono speaker by enabling the respective signal path in either the Left or Right speaker output mixer. (Note that these signals should not be enabled in both mixers at once; this will lead to cancellation at the BTL output.)

Note that a differential output from a single DAC may be generated at the speaker outputs by routing the inverted DAC signal to one output and the non-inverted DAC signal to the other. When the line outputs are similarly configured for the other DAC channel, then stereo differential output is possible.

EXTERNAL COMPONENTS FOR LINE OUTPUT

In single-ended output configurations, DC blocking capacitors are required at the output pins (LINEOUTL, LINEOUTR, SPKOUTL and SPKOUTR). See “Applications Information” for details of these components.

LDO REGULATOR

The WM8946 provides an internal LDO which provides a regulated voltage for use as in internal supply and reference, which can also be used to power external circuits.

The LDO is enabled by setting the LDO_ENA register bit. The LDO supply is drawn from the LDOVDD pin; the LDO output is provided on the LDOVOUT pin. The LDO requires a reference voltage and a bias source; these are configured as described below.

The LDO bias source is selected using LDO_BIAS_SRC. Care is required during start-up to ensure that the selected bias is enabled; the master bias will not normally be available at initial start-up, and the fast bias should be selected in the first instance.

The LDO reference voltage can be selected using LDO_REF_SEL; this allows selection of either the internal bandgap reference or one of the VMID resistor strings. When VMID is selected as the reference, then LDO_REF_SEL_FAST selects either the Normal VMID reference or the Fast-Start VMID reference. Care is required during start-up to ensure that the selected reference is enabled; the VMID references are enabled using VMID_ENA and VMID_FAST_START as described in Table 44 and Table 45 respectively.

The internal bandgap reference is nominally 1.5V. Note that this value is not trimmed and may vary significantly (+/-10%) between different devices. When using this reference, the internal bandgap reference must be enabled by setting the BG_ENA register, as described in Table 41. The bandgap voltage can be adjusted using the BG_VSEL register as described in Table 43.

The LDO output voltage is set using the LDO_VSEL register, which sets the ratio of the output voltage to the LDO reference voltage. See Table 42 for LDO output voltages.

Two example LDO configurations are described below.

Table 39 describes how to generate LDOVOUT voltage of 3.0V, from a LDOVDD supply voltage of 3.3V, using VMID as the LDO reference.

Note that using VMID as the LDO reference offers the lowest power consumption, but any variation in the LDOVDD supply may cause a variation in VMID and, consequently, a variation in LDOVOUT.

DESCRIPTION	REGISTER
Select LDOVDD as the VMID source	VMID_REF_SEL = 0
Select 5/11 as the VMID ratio	VMID_CTRL = 0
Select 2 x 50kΩ VMID divider for normal operation	VMID_SEL = 01
Enable VMID	VMID_ENA = 1
VMID = LDOVDD x 5/11 = 1.5V	
Select VMID as the LDO Voltage reference	LDO_REF_SEL = 0 LDO_REF_SEL_FAST = 0
Select Vref x 1.97 as the LDO output voltage	LDO_VSEL = 07h
Enable LDO	LDO_ENA = 1
LDOVOUT = Vref x 1.97 = 1.5V x 1.97 = 2.97V	

Table 39 LDO Configuration using VMID as LDO reference

Table 40 describes how to generate LDOVOUT voltage of 2.4V, from a LDOVDD supply voltage of 3.0V, using the Bandgap as the LDO reference.

Note that using the Bandgap as the LDO reference offers the best voltage stability, as the Bandgap reference voltage does not change with LDOVDD. The Bandgap voltage is stable, but is not trimmed for accuracy; adjustment of the BG_VSEL register may be necessary when using the Bandgap as the LDO reference.

DESCRIPTION	REGISTER
Select 1.467V as Bandgap voltage	BG_VSEL = 0Ah
Enable the Bandgap	BG_ENA = 1
Select Bandgap as the LDO Voltage reference	LDO_REF_SEL = 1
Select Vref x 1.66 as the LDO output voltage	LDO_VSEL = 03h
Enable LDO	LDO_ENA = 1
LDOVOUT = Vref x 1.66 = 1.467V x 1.66 = 2.435V	
Select LDOVOUT as the VMID source	VMID_REF_SEL = 1
Select 1/2 as the VMID ratio	VMID_CTRL = 1
Select 2 x 50kΩ VMID divider for normal operation	VMID_SEL = 01
Enable VMID	VMID_ENA = 1
VMID = LDOVOUT x 1/2 = 1.2V	

Table 40 LDO Configuration using Bandgap as LDO reference

By default, the LDO output is actively discharged to GND through internal resistors when the LDO is disabled. This is desirable in shut-down to prevent any external connections being affected by the internal circuits. The LDO output can be set to float when the LDO is disabled; this is selected by setting the LDO_OP_FLT bit. This option should be selected if the LDO is bypassed and an external voltage is applied to LDOVOUT.

The LDO output is monitored for voltage accuracy. The LDO undervoltage status can be read at any time from the LDO_UV_STS bit, as described in Table 41. This bit can be polled at any time, or may output directly on a GPIO pin, or may be used to generate Interrupt events.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) Status Flags	0	LDO_UV_STS	0	LDO Undervoltage status 0 = Normal 1 = Undervoltage
R53 (35h) LDO	15	LDO_ENA	0	LDO Enable 0 = Disabled 1 = Enabled
	14	LDO_REF_SEL_FAST	0	LDO Voltage reference select 0 = VMID (normal) 1 = VMID (fast start) This field is only effective when LDO_REF_SEL = 0
	13	LDO_REF_SEL	0	LDO Voltage reference select 0 = VMID 1 = Bandgap
	12	LDO_OPFLT	0	LDO Output float 0 = Disabled (Output discharged when disabled) 1 = Enabled (Output floats when disabled)
	5	LDO_BIAS_SRC	0	LDO Bias Source select 0 = Master Bias 1 = Start-Up Bias
	4:0	LDO_VSEL	00111	LDO Voltage select (Sets the LDO output as a ratio of the selected voltage reference. The voltage reference is set by LDO_REF_SEL.) 00111 = Vref x 1.97 (default) (See Table 42 for range)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54 (36h) Bandgap	15	BG_ENA	0	Bandgap Reference Control 0 = Disabled 1 = Enabled
	4:0	BG_VSEL[4:0]	01010	Bandgap Voltage select (Sets the Bandgap voltage) 00000 = 1.200V … 26.7mV steps 01010 = 1.467V (default) … 01111 = 1.600V 10000 to 11111 = Reserved (See Table 43 for values)

Table 41 LDO Regulator Control

LDO_VSEL [4:0]	LDO OUTPUT	LDO_VSEL [4:0]	LDO OUTPUT
00h	Vref x 1.42	10h	Vref x 2.85
01h	Vref x 1.50	11h	Vref x 3.00
02h	Vref x 1.58	12h	Vref x 3.16
03h	Vref x 1.66	13h	Vref x 3.32
04h	Vref x 1.74	14h	Vref x 3.49
05h	Vref x 1.82	15h	Vref x 3.63
06h	Vref x 1.90	16h	Vref x 3.79
07h	Vref x 1.97	17h	Vref x 3.95
08h	Vref x 2.06	18h	Vref x 4.12
09h	Vref x 2.13	19h	Vref x 4.28
0Ah	Vref x 2.21	1Ah	Vref x 4.42
0Bh	Vref x 2.29	1Bh	Vref x 4.58
0Ch	Vref x 2.37	1Ch	Vref x 4.75
0Dh	Vref x 2.45	1Dh	Vref x 4.90
0Eh	Vref x 2.53	1Eh	Vref x 5.06
0Fh	Vref x 2.69	1Fh	Vref x 5.23
Note: Vref is the applicable voltage reference, selected by LDO_REF_SEL.			

Table 42 LDO Output Voltage Control

BG_VSEL [4:0]	BG Voltage (V)	BG_VSEL [4:0]	BG Voltage (V)
00h	1.200	08h	1.414
01h	1.227	09h	1.440
02h	1.253	0Ah	1.467
03h	1.280	0Bh	1.494
04h	1.307	0Ch	1.520
05h	1.334	0Dh	1.547
06h	1.360	0Eh	1.574
07h	1.387	0Fh	1.600

Table 43 Bandgap Voltage Control

REFERENCE VOLTAGES AND MASTER BIAS

This section describes the analogue reference voltage and bias current controls. It also describes the VMID soft-start circuit for pop suppressed start-up and shut-down.

The analogue circuits in the WM8946 require a mid-rail analogue reference voltage, VMID. This reference is generated via a programmable resistor chain. Together with the external decoupling capacitor (connected to the VMIDC pin), the programmable resistor chain results in a slow, normal or fast charging characteristic on the VMID reference. This is enabled using VMID_ENA and VMID_SEL. The different resistor options controlled by VMID_SEL can be used to optimize the reference for normal operation, low power standby or for fast start-up as described in Table 44.

The VMID resistor chain can be powered from the LDO output (LDOVOUT) or from the LDO supply (LDOVDD). This is selected using VMID_REF_SEL. .

Note that when VMID is selected as the LDO reference voltage, VMID cannot be generated from the LDOVOUT supply voltage (VMID_REF_SEL = 1) and must be generated from the LDOVDD supply voltage (VMID_REF_SEL = 0).

The VMID ratio can be selected using VMID_CTRL. This selects the ratio of VMID to the supply voltage that has been selected by VMID_REF_SEL. VMID should be half of the LDOVOUT supply voltage for maximum voltage swing. In the case where VMID_REF_SEL has selected the LDOVOUT supply voltage output, then VMID_CTRL should select the ratio “1/2”. In the case where VMID_REF_SEL has selected the LDOVDD supply voltage, then the alternate ratio “5/11” may be preferred provided LDOVDDD = 3.3V and LDOVOUT = 3.0V.

Note that the “5/11” ratio is designed for the case where LDOVDD = 3.3V and LDOVOUT = 3.0V. This results in a VMID = 3.3V x (5/11) = 1.5V which is half of the LDOVOUT voltage.

If these conditions are not being used or the LDO has been bypassed then VMID_REF should be set to select LDOVOUT as the VMID source and VMID_CTRL should be set to select the ratio “1/2”.

The analogue circuits in the WM8946 require a bias current. The normal bias current is enabled by setting BIAS_ENA. Note that the normal bias current source requires VMID to be enabled also.

The Master Reference and Bias Control bits are defined in Table 44.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Additional control	10	VMID_REF_SEL	0	VMID Source Select 0 = LDO supply (LDOVDD) 1 = LDO output (LDOVOUT)
	9	VMID_CTRL	0	VMID Ratio control Sets the ratio of VMID to the source selected by VMID_REF_SEL 0 = 5/11 1 = 1/2
	4	VMID_ENA	0	VMID Enable 0 = Disabled 1 = Enabled
R2 (02h) Power Management 1	3	BIAS_ENA	0	Master Bias Enable 0 = Disabled 1 = Enabled
	1:0	VMID_SEL [1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50kΩ divider (for normal operation) 10 = 2 x 250kΩ divider (for low power standby) 11 = 2 x 5kΩ divider (for fast start-up)

Table 44 Reference Voltages and Master Bias Enable

A pop-suppressed start-up requires VMID to be enabled smoothly, without the step change normally associated with the initial stage of the VMID capacitor charging. A pop-suppressed start-up also requires the analogue bias current to be enabled throughout the signal path prior to the VMID reference voltage being applied. The WM8946 incorporates pop-suppression circuits which address these requirements.

An alternate bias current source (Start-Up Bias) is provided for pop-free start-up; this is enabled by the STARTUP_BIAS_ENA register bit. The start-up bias is selected (in place of the normal bias) using the BIAS_SRC bit. It is recommended that the start-up bias is used during start-up, before switching back to the higher quality, normal bias.

A soft-start circuit is provided in order to control the switch-on of the VMID reference. The soft-start control circuit offers two slew rates for enabling the VMID reference; these are selected and enabled by VMID_RAMP. When the soft-start circuit is enabled prior to enabling VMID_SEL, the reference voltage rises smoothly, without the step change that would otherwise occur. It is recommended that the soft-start circuit and the output signal path be enabled before VMID is enabled by VMID_SEL.

A soft shut-down is provided, using the soft-start control circuit and the start-up bias current generator. The soft shut-down of VMID is achieved by setting VMID_RAMP, STARTUP_BIAS_ENA and BIAS_SRC to select the start-up bias current and soft-start circuit prior to setting VMID_SEL=00.

The internal LDO (described in the previous section) requires a voltage reference. Under normal operating conditions, this is provided from VMID, via the register controls described in Table 44. Note, however, that VMID is normally generated from the LDO output. Therefore, an alternative voltage reference is required for start-up, which is not dependent on the LDO output. The VMID_FAST_START bit enables a 'Fast-Start' reference powered from LDOVDD. This alternate VMID can be selected as the LDO reference using the LDO_REF_SEL_FAST bit as described in Table 41.

The VMID soft-start and fast start register controls are defined in Table 45.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Additional control	11	VMID_FAST_START	0	VMID (fast-start) Enable 0 = Disabled 1 = Enabled
	8	STARTUP_BIAS_ENA	0	Start-Up Bias Enable 0 = Disabled 1 = Enabled
	7	BIAS_SRC	0	Bias Source select 0 = Normal bias 1 = Start-Up bias
	6:5	VMID_RAMP [1:0]	00	VMID soft start enable / slew rate control 00 = Disabled 01 = Fast soft start 10 = Normal soft start 11 = Slow soft start

Table 45 Soft Start Control

POP SUPPRESSION CONTROL

The WM8946 incorporates a number of features which are designed to suppress pops normally associated with Start-Up, Shut-Down or signal path control. These include the option to maintain an analogue output to VMID even when the output driver is disabled. In addition, there is the ability to actively discharge an output to GND.

Note that, to achieve maximum benefit from these features, careful attention may be required to the sequence and timing of these controls.

DISABLED OUTPUT CONTROL

The line outputs and speaker outputs are biased to VMID in normal operation. In order to avoid audible pops caused by a disabled signal path dropping to GND, the WM8946 can maintain these connections at VMID when the relevant output stage is disabled. This is achieved by connecting a buffered VMID reference to the output.

The buffered VMID reference is enabled by setting VMID_BUF_ENA. This is applied to any disabled outputs, provided that the respective _VMID_OP_ENA bit is also set. The output resistance can be either 1kΩ or 20kΩ, depending on the respective _VROI register bit.

The disabled output control bits are described in Table 46. See “Output Signal Path” for details of how to disable any of the audio outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power management 1	2	VMID_BUF_ENA	0	VMID Buffer Enable. (The buffered VMID may be applied to disabled input and output pins.) 0 = Disabled 1 = Enabled
R42 (2Ah) Output ctrl	13	SPKR_VMID_OP_ENA	0	Buffered VMID to SPKOUTR Enable 0 = Disabled 1 = Enabled
	12	SPKL_VMID_OP_ENA	0	Buffered VMID to SPKOUTL Enable 0 = Disabled 1 = Enabled
	11	LINER_VMID_OP_ENA	0	Buffered VMID to LINEOUTR Enable 0 = Disabled 1 = Enabled
	10	LINEL_VMID_OP_ENA	0	Buffered VMID to LINEOUTL Enable 0 = Disabled 1 = Enabled
	1	SPK_VROI	0	Buffered VREF to SPKOUTL / SPKOUTR resistance (Disabled outputs) 0 = approx 20k 1 = approx 1k
	0	LINE_VROI	0	Buffered VREF to LINEOUTL / LINEOUTR resistance (Disabled outputs) 0 = approx 20k 1 = approx 1k

Table 46 Disabled Output Control

OUTPUT DISCHARGE CONTROL

The line outputs and speaker outputs can be actively discharged to GND through internal resistors if desired. This is desirable at start-up in order to achieve a known output stage condition prior to enabling the soft-start VMID reference voltage. This is also desirable in shut-down to prevent the external connections from being affected by the internal circuits.

The individual control bits for discharging each audio output are described in Table 47.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 (2Ah) Output ctrl	7	SPKR_DISCH	0	Discharges SPKOUTR output via approx 4k resistor 0 = Not active 1 = Actively discharging SPKOUTR
	6	SPKL_DISCH	0	Discharges SPKOUTL output via approx 4k resistor 0 = Not active 1 = Actively discharging SPKOUTL
	5	LINER_DISCH	0	Discharges LINEOUTR output via approx 4k resistor 0 = Not active 1 = Actively discharging LINEOUTR
	4	LINEL_DISCH	0	Discharges LINEOUTL output via approx 4k resistor 0 = Not active 1 = Actively discharging LINEOUTL

Table 47 Output Discharge Control

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8946 and outputting ADC data from it. It uses four pins:

- ADCDAT: ADC data output
- DACDAT: DAC data input
- LRCLK: DAC and ADC data alignment clock
- BCLK: Bit clock, for synchronisation

MASTER AND SLAVE MODE OPERATION

The digital audio interface can be configured as a Master or a Slave interface, using the MSTR register bit. The two modes are illustrated in Figure 20 and Figure 21.

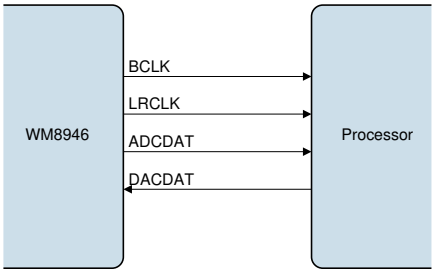


Figure 20 Master Mode

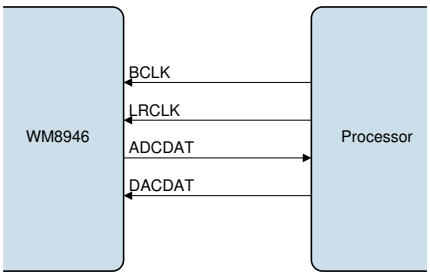


Figure 21 Slave Mode

In Master mode, LRCLK and BCLK are configured as outputs, and the WM8946 controls the timing of the data transfer on the ADCDAT and DACDAT pins.

In Master mode, the LRCLK frequency is determined automatically according to the sample rate (see "Clocking and Sample Rates"). The BCLK frequency is set by the BCLK_DIV register. BCLK_DIV must be set to an appropriate value to ensure that there are sufficient BCLK cycles to transfer the complete data words from the ADCs and to the DACs.

In Slave mode, LRCLK and BCLK are configured as inputs, and the data timing is controlled by an external master.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clock Gen control	3:1	BCLK_DIV [2:0]	011	BCLK Frequency (Master mode) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 4 011 = SYSCLK / 8 100 = SYSCLK / 16 101 = SYSCLK / 32 110 = reserved 111 = reserved
	0	MSTR	0	Digital Audio Interface Mode select 0 = Slave mode 1 = Master mode

Table 48 Digital Audio Interface Control

AUDIO DATA FORMATS

Three basic audio data formats are supported:

- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

PCM operation is supported using the DSP mode.

The WM8946 can control the channel selection between the ADCs and the ADCDAT pin. Similarly, the channel selection between the DACDAT pin and the DACs is selectable. Digital inversion of the ADC or DAC data is also possible.

The register bits controlling audio data format and channel configuration are described in Table 49.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Audio Interface	9	ADCR_SRC	1	Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel
	8	ADCL_SRC	0	Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	7	DACR_SRC	1	Right DAC Data Source Select 0 = Right DAC outputs left interface data 1 = Right DAC outputs right interface data
	6	DACL_SRC	0	Left DAC Data Source Select 0 = Left DAC outputs left interface data 1 = Left DAC outputs right interface data
	5	BCLK_INV	0	BCLK Invert 0 = BCLK not inverted 1 = BCLK inverted
	4	LRCLK_INV	0	LRCLK Polarity / DSP Mode A-B select. Right, left and I^2S modes – LRCLK polarity 0 = Not Inverted 1 = Inverted DSP Mode – Mode A-B select 0 = MSB is available on 2nd BCLK rising edge after LRCLK rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRCLK rising edge (mode B)
	3:2	WL [1:0]	10	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note – see "Companding" for the selection of 8-bit mode.
	1:0	FMT [1:0]	10	Digital Audio Interface Format 00 = Reserved 01 = Left Justified 10 = I2S format 11 = DSP/PCM mode
R21 (15h) DAC Control 1	1	DACR_DATINV	0	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted
	0	DACL_DATINV	0	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted
R25 (19h) ADC Control 1	1	ADCR_DATINV	0	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted
	0	ADCL_DATINV	0	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted

Table 49 Audio Data Format Control

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

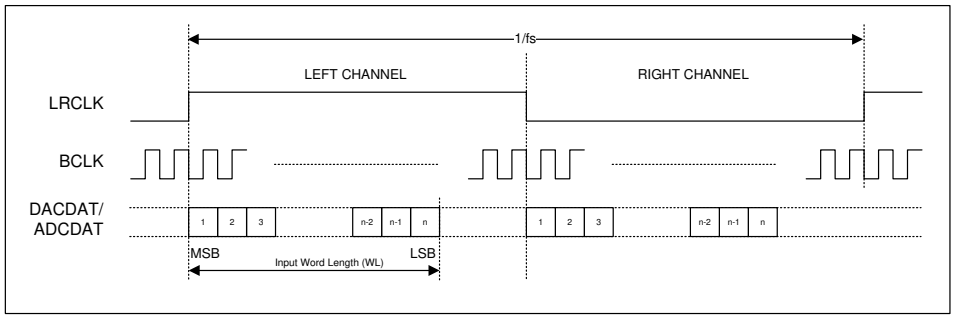


Figure 22 Left Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

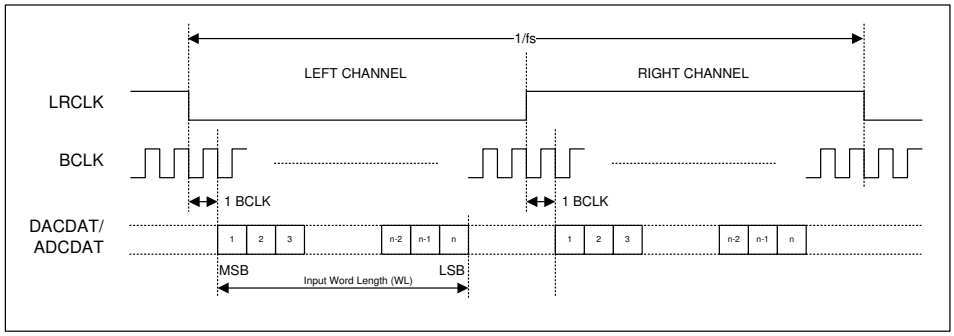


Figure 23 I²S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selected by LRCLK_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRCLK output resembles the frame pulse shown in Figure 24 and Figure 25. In device slave mode, Figure 26 and Figure 27, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

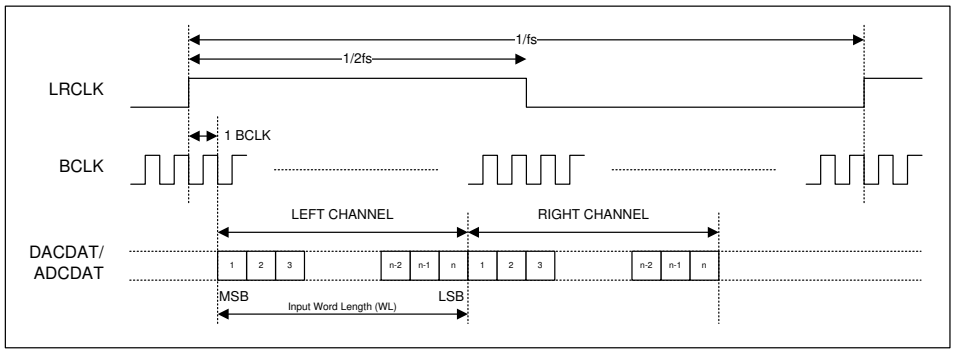


Figure 24 DSP/PCM Mode Audio Interface (mode A, LRCLK_INV=0, Master)

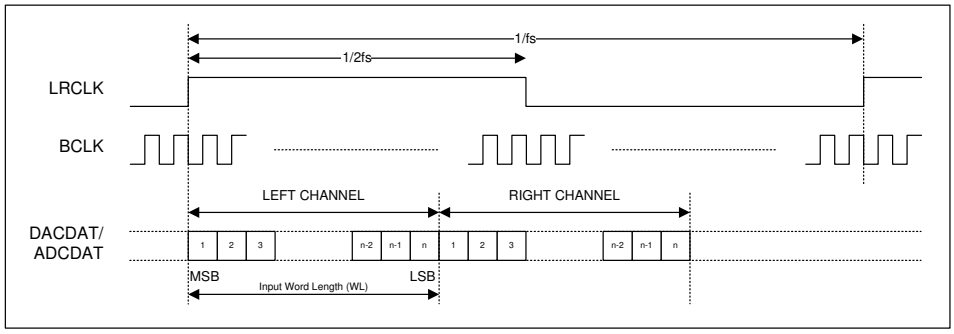


Figure 25 DSP/PCM Mode Audio Interface (mode B, LRCLK_INV=1, Master)

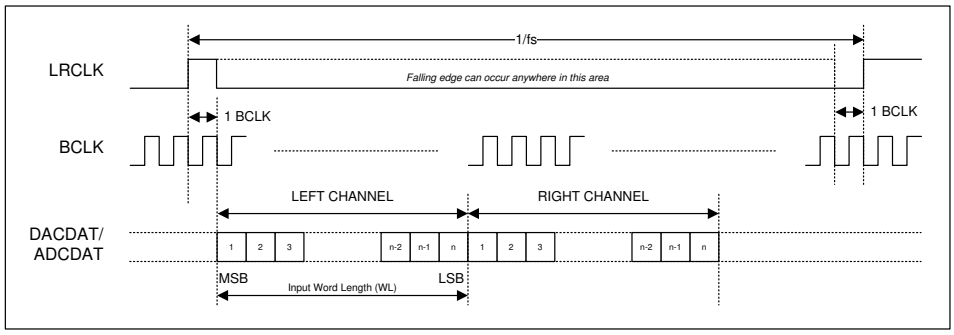


Figure 26 DSP/PCM Mode Audio Interface (mode A, LRCLK_INV=0, Slave)

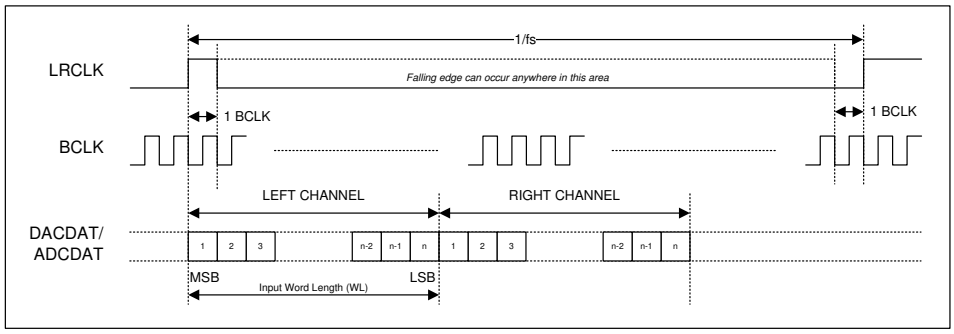


Figure 27 DSP/PCM Mode Audio Interface (mode B, LRCLK_INV=0, Slave)

COMPANDING

The WM8946 supports A-law and μ-law companding on both transmit (ADC) and receive (DAC) sides as shown in Table 50. Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. This provides greater precision for low-amplitude signals than for high-amplitude signals, resulting in a greater usable dynamic range than 8 bit linear quantization.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Companding control	3	DAC_COMP	0	DAC Companding Enable 0 = Disabled 1 = Enabled
	2	DAC_COMPMODE	0	DAC Companding Mode 0 = µ-law 1 = A-law
	1	ADC_COMP	0	ADC Companding Enable 0 = Disabled 1 = Enabled
	0	ADC_COMPMODE	0	ADC Companding Mode 0 = µ-law 1 = A-law

Table 50 Companding Control

Companding uses a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

µ-law (where µ=255 for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \quad \} \text{ for } -1 \le x \le 1$$

Table 1 law (where A=87.6 for Europe):

$$F(x) = A|x| / (1 + \ln A) \quad \} \text{ for } x \le 1/A$$

$$F(x) = (1 + \ln A|x|) / (1 + \ln A) \quad \} \text{ for } 1/A \le x \le 1$$

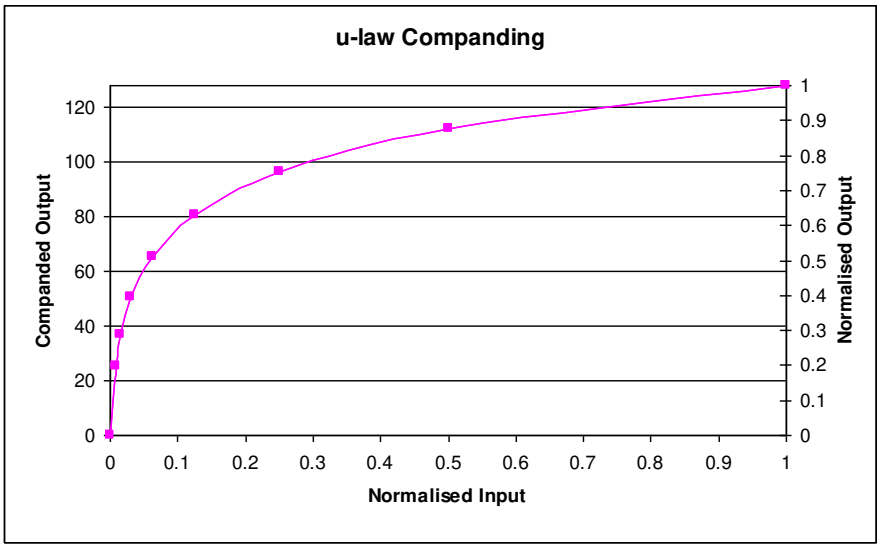


Figure 28 µ-Law Companding

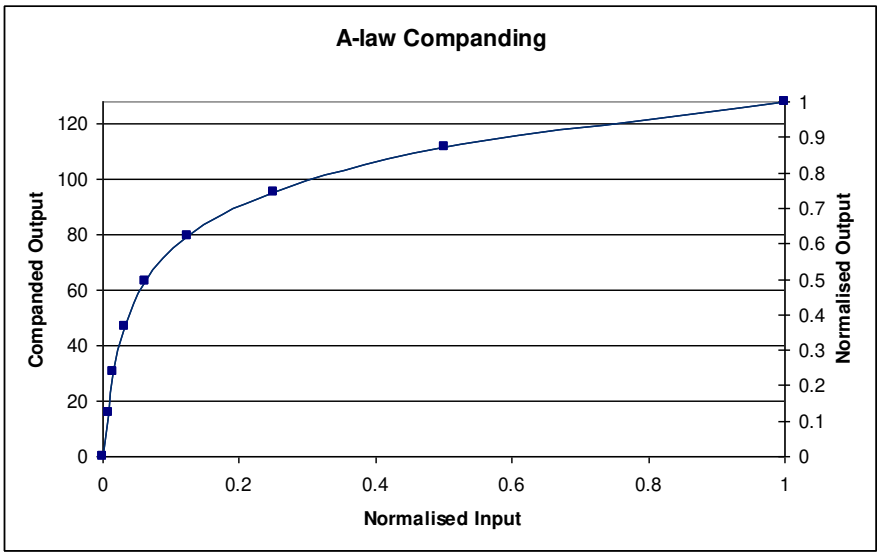


Figure 29 A-Law Companding

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). Companded data is transmitted in the first 8 MSBs of its respective data word, and consists of sign (1 bit), exponent (3 bits) and mantissa (4 bits), as shown in Table 51.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 51 8-bit Companded Word Composition

8-bit mode is selected whenever DAC_COMP=1 or ADC_COMP=1. The use of 8-bit data allows samples to be passed using as few as 8 BCLK cycles per Left/Right Clock frame. When using DSP mode B, 8-bit data words may be transferred consecutively every 8 BCLK cycles.

8-bit mode (without Companding) may be enabled by setting DAC_COMPMODE=1 or ADC_COMPMODE=1, when DAC_COMP=0 and ADC_COMP=0.

LOOPBACK

A loopback function is provided for test and evaluation purposes. When the LOOPBACK register bit is set, the DAC input data is fed through the DSP Core to the ADC output, as illustrated in Figure 30.

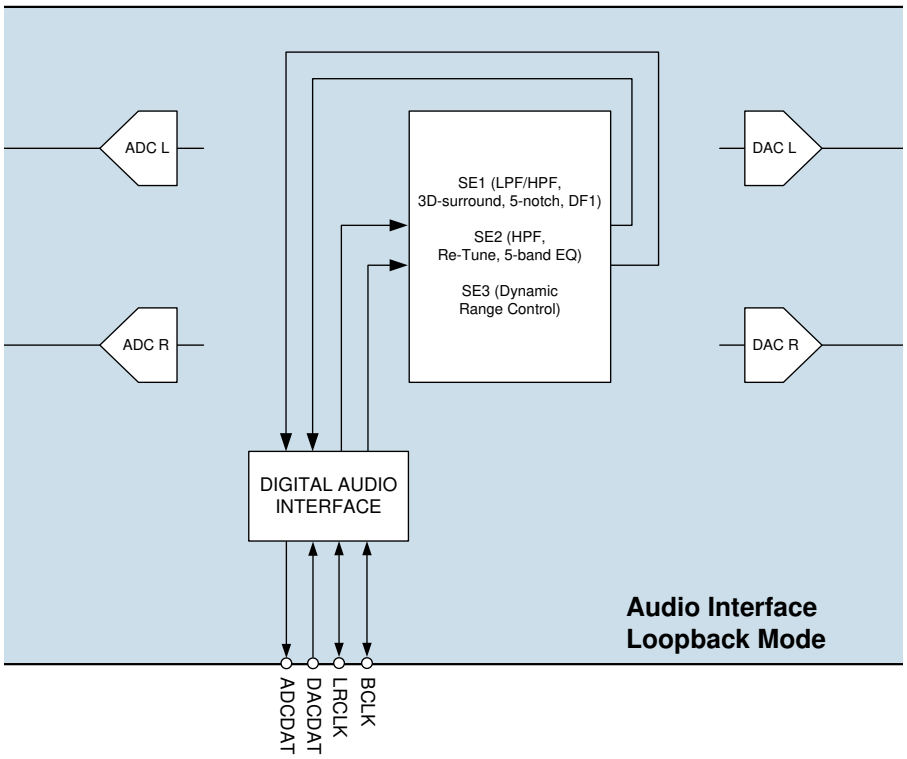


Figure 30 Audio Interface Loopback

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) Companding control	5	LOOPBACK	0	Digital Loopback Function 0 = No loopback 1 = Loopback enabled (DACDAT input is fed through the DSP Core to the ADCDAT output).

Table 52 Loopback Control

DIGITAL PULL-UP AND PULL-DOWN

The WM8946 provides integrated pull-up and pull-down resistors on each of the DACDAT, LRCLK and BCLK pins. This provides a flexible capability for interfacing with other devices. Each of the pull-up and pull-down resistors can be configured independently using the register bits described in Table 53.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Audio interface	15:14	DACDATA_PULL [1:0]	00	DACDAT pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	13:12	FRAME_PULL [1:0]	00	LRCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	11:10	BCLK_PULL [1:0]	00	BCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved

Table 53 Pull-Up and Pull-Down Control

CLOCKING AND SAMPLE RATES

The internal clocks for the CODEC and Digital Audio Interface are derived from a common internal clock source, SYSCLK. This clock can either be derived directly from MCLK, or may be generated using the Frequency Locked Loop (FLL) using MCLK as a reference. All commonly-used audio sample rates can be derived directly from typical MCLK frequencies; the FLL provides additional flexibility for a wider range of MCLK frequencies.

The WM8946 supports a wide range of standard audio sample rates from 8kHz to 48kHz. When the ADC and DAC are both enabled, they operate at the same sample rate, fs.

Other functions such as the Interrupts, GPIO input de-bounce and PGA zero-cross timeouts are clocked using a free-running oscillator.

The control registers associated with Clocking and Sample Rates are described in Table 54.

The overall clocking scheme for the WM8946 is illustrated in Figure 31.

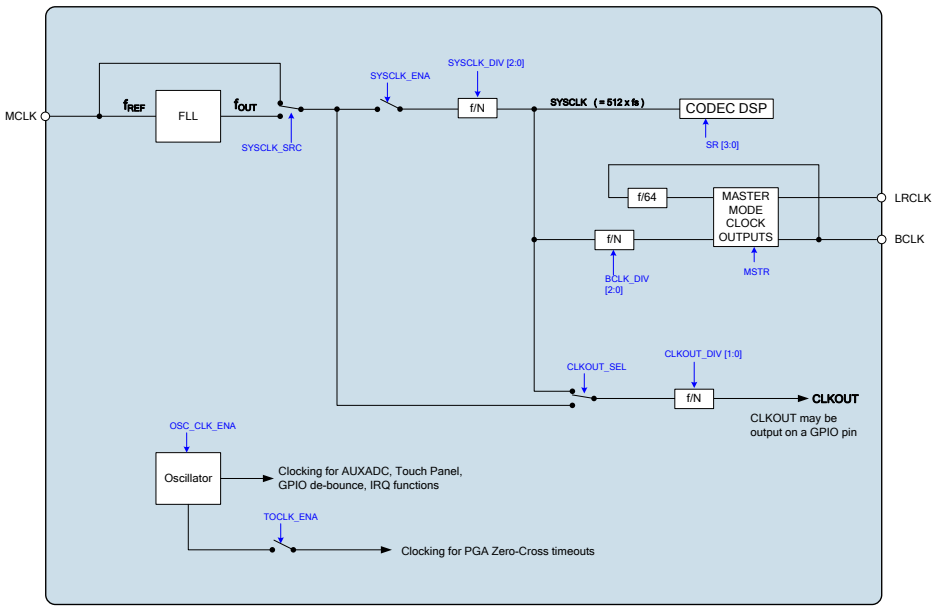


Figure 31 WM8946 Clocking Overview

SYSCLK may be derived either from MCLK or from the FLL; this is selected using the SYSCLK_SRC register bit. SYSCLK is enabled using the SYSCLK_ENA and may be modified using a programmable divider configured by SYSCLK_DIV. It is important that SYSCLK_DIV is correctly set in order to produce 512 x fs at its output, where fs is the audio sampling rate.

The sampling rate for the CODEC and Digital Audio Interface is configured using the SR register field. In Master mode, the frequency of the Left/Right Clock output on the LRCLK pin is the BCLK frequency divided by 64 producing 32 BCLK cycles per channel. In Master mode, the BCLK_DIV register configures the bit clock frequency output on BCLK.

The WM8946 can output a configurable clock on the GPIO pins; this is enabled automatically whenever a GPIO pin is configured for CLKOUT output. The source can either be before or after the SYSCLK divider, as shown in Figure 31. The source is selected using CLKOUT_SEL, and may be modified using a programmable divider configured by CLKOUT_DIV.

The WM8946 free-running oscillator required for GPIO input de-bounce and Interrupt functions must be enabled using OSC_CLK_ENA whenever any of these functions is required.

The zero-cross facility on input and output PGAs requires a timeout clock. This is enabled using the TOCLK_ENA bit. The oscillator must also be enabled using OSC_CLK_ENA.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) Clock Gen control	15	OSC_CLK_ENA	0	Oscillator Enable 0 = Disabled 1 = Enabled This needs to be set when a timeout clock is required for PGA zero cross or GPIO input detection
	14:13	MCLK_PULL [1:0]	00	MCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	12	CLKOUT_SEL	0	CLKOUT Source Select 0 = SYSCLK 1 = FLL or MCLK (set by SYSCLK_SRC register)
	11:10	CLKOUT_DIV [1:0]	00	CLKOUT Clock divider 00 = divide by 1 01 = divide by 2 10 = divide by 4 11 = divide by 8
	9	SYSCLK_ENA	0	SYSCLK Enable 0 = Disabled 1 = Enabled
	8	SYSCLK_SRC	0	SYSCLK Source Select 0 = MCLK 1 = FLL output
	7:5	SYSCLK_DIV [2:0]	000	SYSCLK Clock divider (Sets the scaling for either the MCLK or FLL clock output, depending on SYSCLK_SRC) 000 = divide by 1 001 = divide by 1.5 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12
	4	TOCLK_ENA	0	TOCLK Enabled (Enables timeout clock for GPIO level detection, AMU, and PGA zero cross timeout) 0 = Disabled 1 = Enabled
R7 (07h) Additional control	3:0	SR [3:0]	1101	Audio Sample Rate select 0011 = 8kHz 0100 = 11.025kHz 0101 = 12kHz 0111 = 16kHz 1000 = 22.05kHz 1001 = 24kHz 1011 = 32kHz 1100 = 44.1kHz 1101 = 48kHz

Table 54 Clocking and Sample Rate Control

DIGITAL MIC CLOCKING

When any GPIO is configured as DMICCLK output, the WM8946 outputs a clock which supports Digital Mic operation at the ADC sampling rate. Although the ADC is not used, the SYSCLK and Sample Rate control fields must still be set as they would for ADC operation.

The clock frequencies for each of the sample rates is shown in Table 55.

PCM SAMPLE RATE	DMICCLK	FS RATE
8kHz	1.024MHz	128fs
11.025kHz	1.411MHz	128fs
12kHz	1.536MHz	128fs
16kHz	2.048MHz	128fs
22.05kHz	2.8224MHz	128fs
24kHz	3.072MHz	128fs
32kHz	2.048MHz	64fs
44.1kHz	2.8224MHz	64fs
48kHz	3.072MHz	64fs

Table 55 Digital Microphone Clock Frequencies

FREQUENCY LOCKED LOOP (FLL)

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL uses MCLK as its reference, which may be a high frequency (e.g. 12.288MHz) or low frequency (e.g. 32,768kHz) reference. The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal. The FLL characteristics are summarised in “Electrical Characteristics”.

The FLL is enabled using the FLL_ENA register bit. At initial power on the VMID voltage must be allowed to settle at its final vale before enabling the FLL. Note that, when changing FLL settings, it is recommended that the digital circuit be disabled via FLL_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL_ENA to 0.

The field FLL_CLK_REF_DIV provides the option to divide the input reference (MCLK) by 1, 2, 4 or 8. This field should be set to bring the reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency – within the 13.5MHz limit – should be selected.

The field FLL_CTRL_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL_GAIN controls the internal loop gain and should be set to the recommended value.

The FLL output frequency is directly determined from FLL_FRATIO, FLL_OUTDIV and the real number represented by FLL_N and FLL_K. The field FLL_N is an integer (LSB = 1); FLL_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL_FRAC.

Power consumption in the FLL is reduced in integer mode; however, the performance may also be reduced, with increased noise or jitter on the output.

If low power consumption is required, then FLL settings must be chosen where N.K is an integer (i.e. FLL_K = 0). In this case, the fractional mode can be disabled by setting FLL_FRAC = 0.

For best FLL performance, a non-integer value of N.K is required. In this case, the fractional mode must be enabled by setting FLL_FRAC = 1. The FLL settings must be adjusted, if necessary, to produce a non-integer value of N.K.

The FLL output frequency is generated according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_FRATIO)$$

F_{REF} is the input frequency, as determined by FLL_CLK_REF_DIV.

F_{VCO} must be in the range 90-100 MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

In order to follow the above requirements for F_{VCO}, the value of FLL_OUTDIV should be selected according to the desired output F_{OUT}, as described in Table 56.

OUTPUT FREQUENCY F_{OUT}	FLL_OUTDIV
2.8125 MHz – 3.125 MHz	4h (divide by 32)
5.625 MHz – 6.25 MHz	3h (divide by 16)
11.25 MHz – 12.5 MHz	2h (divide by 8)
22.5 MHz – 25 MHz	1h (divide by 4)
45 MHz – 50 MHz	0h (divide by 2)

Table 56 Selection of FLL_OUTDIV

The value of FLL_FRATIO should be selected as described in Table 57.

REFERENCE FREQUENCY F_{REF}	FLL_FRATIO
1MHz – 13.5MHz	0h (divide by 1)
256kHz – 1MHz	1h (divide by 2)
128kHz – 256kHz	2h (divide by 4)
16kHz – 128kHz	3h (divide by 8)
Less than 16kHz	4h (divide by 16)

Table 57 Selection of FLL_FRATIO

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$$F_{VCO} = (F_{OUT} \times FLL\_OUTDIV)$$

The value of FLL_N and FLL_K can then be determined as follows:

$$N.K = F_{VCO} / (FLL\_FRATIO \times F_{REF})$$

Note that F_{REF} is the input frequency, after division by FLL_CLK_REF_DIV, where applicable.

In FLL Fractional Mode, the fractional portion of the N.K multiplier is held in the FLL_K register field. This field is coded as a fixed point quantity, where the MSB has a weighting of 0.5. Note that, if desired, the value of this field may be calculated by multiplying K by 2^16 and treating FLL_K as an integer value, as illustrated in the following example:

If N.K = 8.192, then K = 0.192.

Multiplying K by 2^16 gives 0.192 x 65536 = 12582.912 (decimal) = 3126 (hex).

For best FLL performance, the FLL fractional mode is recommended. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL_FRATIO in order to obtain a non-integer value of N.K. Care must always be taken to ensure that the FLL operating frequency, F_{VCO}, is within its recommended limits of 90-100 MHz.

The register fields that control the FLL are described in Table 58. Example settings for a variety of reference frequencies and output frequencies are shown in Table 59.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) FLL Control 1	12:11	FLL_CLK_REF_DIV [1:0]	00	FLL Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	10:8	FLL_OUTDIV [2:0]	001	F_{OUT} clock divider 000 = 2 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 111 = 256 (F_{OUT} = F_{VCO} / FLL_OUTDIV)
	7:5	FLL_CTRL_RATE [2:0]	000	Frequency of the FLL control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 3 011 = F_{VCO} / 4 100 = F_{VCO} / 5 101 = F_{VCO} / 6 110 = F_{VCO} / 7 111 = F_{VCO} / 8 Recommended that this register is not changed from default.
	4:2	FLL_FRATIO [2:0]	000	F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for F_{REF} > 1MHz 100 recommended for F_{REF} < 16kHz 011 recommended for all other cases

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	FLL_FRAC	1	Fractional enable 0 = Integer Mode 1 = Fractional Mode Integer mode offers reduced power consumption. Fractional mode offers best FLL performance, provided also that N.K is a non-integer value.
	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled
R9 (09h) FLL Control 2	15:0	FLL_K[15:0]	3137h	Fractional multiply for F_{REF} (MSB = 0.5)
R10 (0Ah) FLL Control 3	14:5	FLL_N[9:0]	008h	Integer multiply for F_{REF} (LSB = 1)
	3:0	FLL_GAIN [3:0]	0100	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that this register is set to 0000.

Table 58 Frequency Locked Loop Control

EXAMPLE FLL CALCULATION

To generate 24.576MHz output (F_{OUT}) from a 12.000MHz reference clock (F_{REF}):

- Set FLL_CLK_REF_DIV in order to generate F_{REF} <=13.5MHz:
  FLL_CLK_REF_DIV = 00 (divide by 1)
- Set FLL_CTRL_RATE to the recommended setting:
  FLL_CTRL_RATE = 000 (divide by 1)
- Sett FLL_GAIN to the recommended setting:
  FLL_GAIN = 0000 (multiply by 1)
- Set FLL_OUTDIV for the required output frequency as shown in Table 56:-
  F_{OUT} = 24.576MHz, therefore FLL_OUTDIV = 1h (divide by 4)
- Set FLL_FRATIO for the given reference frequency as shown in Table 57:
  F_{REF} = 12MHz, therefore FLL_FRATIO = 0h (divide by 1)
- Calculate F_{VCO} as given by $F_{VCO} = F_{OUT}$ x FLL_OUTDIV:-
  F_{VCO} = 24.576 x 4 = 98.304MHz
- Calculate N.K as given by N.K = F_{VCO} / (FLL_FRATIO x F_{REF}):
  N.K = 98.304 / (1 x 12) = 8.192
- Determine FLL_N and FLL_K from the integer and fractional portions of N.K:-
  FLL_N is 8(dec) = 008(hex). FLL_K is 0.192 (dec) = 3127(hex).
- Confirm that N.K is a fractional quantity and set FLL_FRAC:
  N.K is fractional. Set FLL_FRAC = 1.
  Note that, if N.K is an integer, then an alternative value of FLL_FRATIO may be selected in order to produce a fractional value of N.K.

EXAMPLE FLL SETTINGS

Table 59 provides example FLL settings for generating common SYSCLK frequencies from a variety of low and high frequency reference inputs.

F_{REF}	F_{OUT}	FLL_CLK_REF_DIV	F_{VCO}	FLL_N	FLL_K	FLL_FRATIO	FLL_OUTDIV	FLL_FRAC
8.000 kHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	705 (2C1h)	0.6 (9999h)	16 (4h)	4 (1h)	1
8.000 kHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	768 (300h)	0.0 (0000h)	16 (4h)	4 (1h)	0
32.768 kHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	344 (158h)	0.53125 (8800h)	8 (3h)	4 (1h)	1
32.768 kHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	375 (177h)	0.0 (0000h)	8 (3h)	4 (1h)	0
768.000 kHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	14 (00Eh)	0.7 (B333h)	8 (3h)	4 (1h)	1
768.000 kHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	16 (010h)	0.0 (0000h)	8 (3h)	4 (1h)	0
1.024 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	88 (058h)	0.2 (3333h)	1 (0h)	4 (1h)	1
1.024 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	96 (060h)	0.0 (0000h)	1 (0h)	4 (1h)	0
6.144 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	14 (00Eh)	0.7 (B333h)	1 (0h)	4 (1h)	1
6.144 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	16 (010h)	0.0 (0000h)	1 (0h)	4 (1h)	0
11.2896 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	8 (008h)	0.0 (0000h)	1 (0h)	4 (1h)	0
11.2896 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	8 (008h)	0.70749 (B51Eh)	1 (0h)	4 (1h)	1
12.000 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	7 (007h)	0.5264 (86C2h)	1 (0h)	4 (1h)	1
12.000 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	8 (008h)	0.192 (3127h)	1 (0h)	4 (1h)	1
12.288 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	7 (007h)	0.35 (599Ah)	1 (0h)	4 (1h)	1
12.288 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	8 (008h)	0.0 (0000h)	1 (0h)	4 (1h)	0
13.000 MHz	22.5792 MHz	divide by 1 (0h)	90.3168 MHz	6 (006h)	0.94745 (F28Ch)	1 (0h)	4 (1h)	1
13.000 MHz	24.576 MHz	divide by 1 (0h)	98.304 MHz	7 (007h)	0.56185 (8FD5h)	1 (0h)	4 (1h)	1
19.200 MHz	22.5792 MHz	divide by 2 (1h)	90.3168 MHz	9 (009h)	0.408 (6873h)	1 (0h)	4 (1h)	1
19.200 MHz	24.576 MHz	divide by 2 (1h)	98.304 MHz	10 (00Ah)	0.24 (3D71h)	1 (0h)	4 (1h)	1
27.000 MHz	22.5792 MHz	divide by 2 (1h)	90.3168 MHz	6 (006h)	0.69013 (B0Adh)	1 (0h)	4 (1h)	1
27.000 MHz	24.576 MHz	divide by 2 (1h)	98.304 MHz	7 (007h)	0.28178 (4823h)	1 (0h)	4 (1h)	1

Table 59 Example FLL Settings

VIDEO BUFFER

The WM8946 provides a current mode output video buffer with an input 3rd order Butterworth low pass filter (LPF) and clamp. The video buffer is powered from LDOVDD – typically 3.3V. The video buffer is compatible with PAL and NTSC video formats.

The low pass filter (LPF) is intended to remove images in the video DAC output waveform at multiples of the DAC clock frequency. The input clamp supports AC coupling at the input to the video buffer.

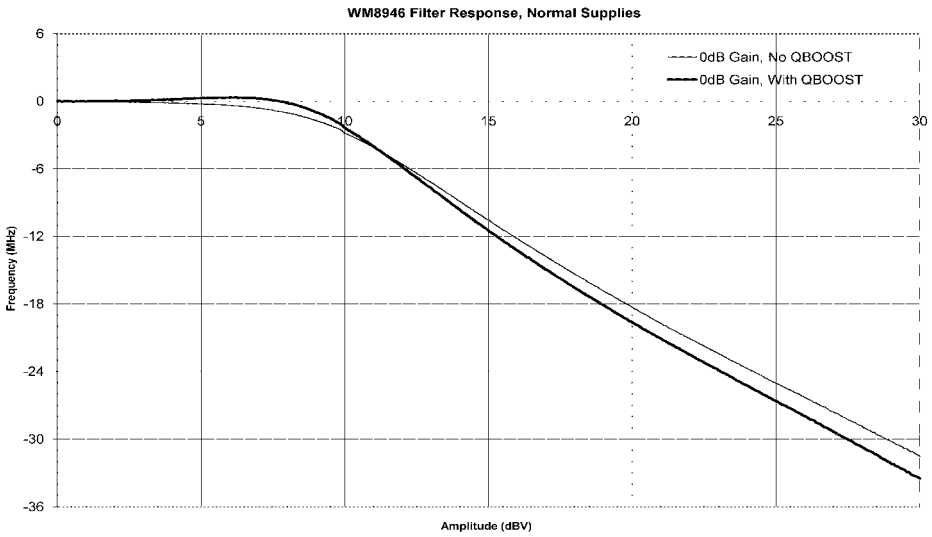


Figure 32 Video Buffer Lowpass Filter Frequency Response Gain=0dB

The current mode output employed by the WM8946 video buffer allows operation at lower supply voltages than voltage mode video buffers. The current mode output also provides inherent protection against short circuits during jack insertion and removal. A current reference resistor (positioned close to the WM8946) ensures that the signal swing at the output of the buffer is the same as that at the receiving equipment (e.g. a television set), thus providing excellent signal reproduction.

For best performance, the input to the video buffer should be AC coupled and terminated to 75Ω. Note that the input clamp and pull-down features described below are only applicable to the AC-coupled input configuration.

Care should be taken with PCB layout, designing for at least 1GHz frequencies to avoid degrading performance. PCB vias and sharp corners should be avoided and parasitic capacitance minimised on signal paths; these should be kept as short and straight as possible. The LDOVDD supply should be decoupled as close to the WM8946 as possible. See the “External Components” section for more information.

The video buffer is enabled using the VB_ENA register bit. The gain of the video buffer is selected using VB_GAIN; this can be set to 0dB or 6dB (corresponding to 6dB or 12dB unloaded). The LPF response can be adjusted by setting the VB_QBOOST register; this provides a small amount of additional gain in the region of the cut-off frequency.

The input signal clamp is enabled using VB_CLAMP; this controls the DC component of the video signal for compatibility with the WM8941. The video buffer pull-down can be enabled using VB_PD; this may be used during power-up of the video buffer in order to align the signal levels between the source and the WM8946. Note that the pull-down should not be enabled during normal operation of the video buffer; it should be enabled when the video buffer is first powered up, and subsequently disabled (e.g. After 20ms) once the circuit has settled.

A programmable DC offset can be applied to the output signal using the VB_DISOFF register field; this can be set to 0mV, 20mV or 40mV offset.

Note that the VMID reference (see “Voltage References and Master Bias”) must be enabled when using the WM8946 video buffer. VMID is enabled by setting VMID_ENA, as defined in Table 44.

The video buffer control registers are described in Table 60.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Video Buffer	7	VB_ENA	0	Video buffer enable 0 = Disabled 1 = Enabled
	6	VB_QBOOST	0	Video buffer filter Q-Boost control 0 = Disabled 1 = Enabled
	5	VB_GAIN	0	Video buffer gain 0 = 0dB (=6dB unloaded) 1 = 6dB (=12dB unloaded)
	4:3	VB_DISOFF	111	Video buffer DC offset control 000 = Reserved 001 = 40mV offset 010 = Reserved 011 = 20mV offset 100 = Reserved 101 = Reserved 110 = Reserved 111 = 0mV offset Note – the specified offset applies to the 0dB gain setting (VB_GAIN=0). When 6dB gain is selected, the DC offset is doubled.
	1	VB_PD	0	Video buffer pull-down 0 = pull-down disabled 1 = pull-down enabled
	0	VB_CLAMP	0	Enable the clamp between the video input and ground 0 = no clamp 1 = Video buffer input is clamped to ground

Table 60 Video Buffer Control

The video buffer circuit is illustrated in Figure 33.

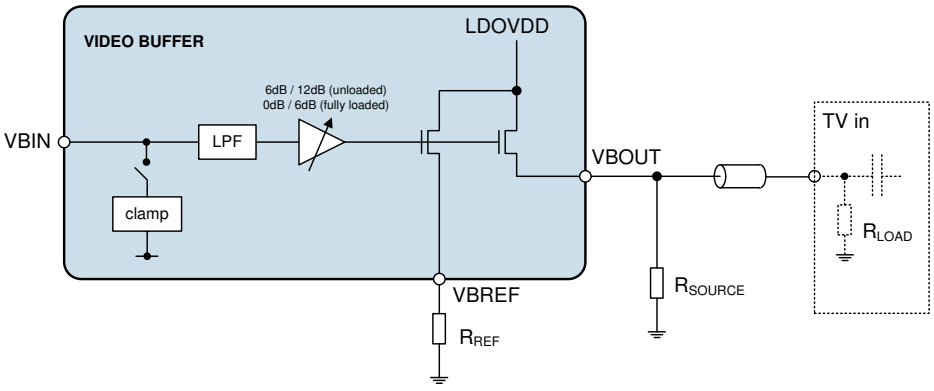


Figure 33 Video Buffer Block Diagram

The video buffer requires two external resistor components, as illustrated in Figure 33. For best performance, the resistor R_{SOURCE} should be matched (equal) to the load impedance R_{LOAD}.

The resistance R_{REF} is a function of the circuit gain and a function of the parallel combination of R_{SOURCE} and RL_{OAD}. When VB_GAIN = 0 (0dB gain), the current gain of the video buffer is 5, as described by the equation $I_{VBOUT} = 5 \times I_{VBREF}$.

The resistor R_{REF} should be set equal to 5 x (R_{SOURCE} // R_{LOAD}), where (R_{SOURCE} // R_{LOAD}) is the effective resistance of the parallel combination of R_{SOURCE} and R_{LOAD}. (Note that the required resistance R_{REF} is the same for both settings of VB_GAIN.)

In a typical application, R_{LOAD} = 75Ω, R_{SOURCE} = 75Ω, R_{REF} = 187Ω.

RECOMMENDED VIDEO BUFFER INITIALISATION SEQUENCES

Recommended power-up sequences for Video Buffer applications are described in Table 61 and Table 62.

DESCRIPTION	LABEL	REGISTER [BITS]
Turn on external supplies and wait for the supply voltages to settle.		
Reset registers to default state (software reset).	SW_RESET	R0 (00h) [15:0]
Enable VMID Fast Start and Start up Bias. Select Start-Up Bias and set VMID soft start for start-up ramp.	VMID_FAST_START = 1 STARTUP_BIAS_ENA = 1 BIAS_SRC = 1 VMID_RAMP[1:0] = 01	R7 (07h) [11] R7 (07h) [8] R7 (07h) [7] R7 (07h) [6:5]
If using VMID as the reference voltage for the LDO then select VMID fast start or set to 0 if using the Bandgap as the reference voltage for LDO. Select LDO Start-Up Bias and enable LDO. Delay 300ms for LDO to settle.	LDO_ENA = 1 LDO_REF_SEL_FAST = 1 LDO_BIAS_SRC = 1	R53 (35h) [15] R53 (35h) [14] R53 (35h) [5]
Enable VMID Buffer and Master Bias. Set VMID_SEL[1:0] for fast start-up.	BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_SEL[1:0] = 11	R2 (02h) [3] R2 (02h) [2] R2 (02h) [1:0]
Enable VMID. Delay 150ms to allow VMID to settle.	VMID_ENA = 1	R7 (07h) [4]
Set LDO and VMID for normal operation.	LDO_REF_SEL_FAST = 0 LDO_BIAS_SRC = 0 VMID_FAST_START = 0 STARTUP_BIAS_ENA = 0 VMID_SEL = 01	R53 (35h) [14] R53 (35h) [5] R7 (07h) [11] R7 (07h) [8] R2 (02h) [1:0]
Set Video Buffer Gain as required.	VB_GAIN	R38 (26h) [5]
Set Video Buffer Filter Q Boost as required.	VB_QBOOST	R38 (26h) [6]
Enable Video Buffer Clamp.	VB_CLAMP = 1	R38 (26h) [0]
Enable Video Buffer Pulldown.	VB_PD = 1	R38 (26h) [1]
Enable video buffer. Delay 20ms for buffer to capture input level.	VB_ENA = 1	R38 (26h) [7]
Disable Video Buffer Pulldown.	VB_PD = 0	R38 (26h) [1]

Table 61 Power-Up Sequence (Video Signal AC-coupled to Video Buffer input)

DESCRIPTION	LABEL	REGISTER [BITS]
Turn on external supplies and wait for the supply voltages to settle.		
Reset registers to default state (software reset).	SW_RESET	R0 (00h) [15:0]
Enable VMID Fast Start and Start up Bias. Select Start-Up Bias and set VMID soft start for start-up ramp.	VMID_FAST_START = 1 STARTUP_BIAS_ENA = 1 BIAS_SRC = 1 VMID_RAMP[1:0] = 01	R7 (07h) [11] R7 (07h) [8] R7 (07h) [7] R7 (07h) [6:5]
If using VMID as the reference voltage for the LDO then select VMID fast start or set to 0 if using the Bandgap as the reference voltage for LDO. Select LDO Start-Up Bias and enable LDO. Delay 300ms for LDO to settle.	LDO_ENA = 1 LDO_REF_SEL_FAST = 1 LDO_BIAS_SRC = 1	R53 (35h) [15] R53 (35h) [14] R53 (35h) [5]
Enable VMID Buffer and Master Bias. Set VMID_SEL[1:0] for fast start-up.	BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_SEL[1:0] = 11	R2 (02h) [3] R2 (02h) [2] R2 (02h) [1:0]
Enable VMID. Delay 150ms to allow VMID to settle.	VMID_ENA = 1	R7 (07h) [4]
Set LDO and VMID for normal operation.	LDO_REF_SEL_FAST = 0 LDO_BIAS_SRC = 0 VMID_FAST_START = 0 STARTUP_BIAS_ENA = 0 VMID_SEL = 01	R53 (35h) [14] R53 (35h) [5] R7 (07h) [11] R7 (07h) [8] R2 (02h) [1:0]
Set Video Buffer Gain as required.	VB_GAIN	R38 (26h) [5]
Set Video Buffer Filter Q Boost as required.	VB_QBOOST	R38 (26h) [6]
Enable video buffer.	VB_ENA = 1	R38 (26h) [7]

Table 62 Power-Up Sequence (Video Signal DC-coupled to Video Buffer input)

GENERAL PURPOSE INPUT/OUTPUT

The WM8946 provides four multi-function pins which can be configured to provide a number of different functions. These are digital input/output pins on the DBVDD power domain. The GPIO pins are:

- GPIO1
- CS/GPIO2
- CIFMODE/GPIO3
- SDOUT/GPIO4

Note that only GPIO1 is a dedicated GPIO pin; the other pins are shared with Control Interface functions. The pins available for GPIO function depend on the selected Control Interface mode, as described in Table 63.

CONTROL INTERFACE MODE	GPIO PIN AVAILABILITY			
2-wire (I2C)	GPIO1	GPIO2	GPIO3	GPIO4
3-wire (SPI)	GPIO1		GPIO3	GPIO4
4-wire (SPI)	GPIO1		GPIO3	

Table 63 GPIO Pin Availability

Note that CIFMODE/GPIO3 pin selects between I2C and SPI Control Interface modes (see “Control Interface”). To enable GPIO functions on GPIO3, the MODE_GPIO register bit must be set in order to disconnect this pin from the Control Interface circuit. Setting the MODE_GPIO register bit causes the Control Interface mode selection to be latched; it will remain latched until a Software Reset or Power On Reset occurs.

The register fields that control the GPIO pins are described in Table 64.

For each GPIO, the selected function is determined by the GPn_FN field, where n identifies the GPIO pin (1 to 4). The pin direction, set by GPn_DIR, must be set according to function selected by GPn_SEL.

When a pin is configured as a GPIO output, its level can be set to logic 0 or logic 1 using the GPn_LVL field. When a pin is configured as a GPIO input, the logic level can be read from the respective GPn_LVL bit. The GPIO output is inverted with respect to the GPn_LVL register when the polarity bit GPn_POL is set; the equivalent is true of GPIO inputs also.

Internal pull-up and pull-down resistors may be enabled using the GPn_PULL fields; this allows greater flexibility to interface with different signals from other devices.

Each of the GPIO pins is an input to the Interrupt control circuit and can be used to trigger an Interrupt event. This may be configured as level-triggered or edge-triggered using the GPn_FN registers. Edge detect raises an interrupt when the GPIO status changes; level detect asserts the interrupt for as long as the GPIO status is asserted. See “Interrupts”.

An edge-triggered GPIO can be configured to trigger on a single edge or on both edges of the input signal; this is selected using the GPn_INT_MODE registers. A level-triggered or single-edge-triggered input may be configured using the GPn_POL registers to respond to a high level/edge (when GPn_POL = 0) or a low level/edge (when GPn_POL = 1).

The GPIO control fields are defined in Table 64.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11 (0Bh) GPIO Config	0	GPIO_MODE	0	CIFMODE/GPIO3 pin configuration 0 = Pin configured as CIFMODE 1 = Pin configured as GPIO3 Note – when this bit is set to 1, it is latched and cannot be reset until Power-Off or Software Reset.
R12 (0Ch) GPIO1 Control	15	GP1_DIR	1	GPIO1 Pin Direction 0 = Output 1 = Input
	14:13	GP1_PULL [1:0]	00	GPIO1 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	12	GP1_INT_MODE	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=0) or falling edge triggered (if GP1_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges
	10	GP1_POL	0	GPIO1 Polarity Select 0 = Non-inverted 1 = Inverted
	5	GP1_LVL	0	GPIO1 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is set, the register contains the opposite logic level to the external pin.
	3:0	GP1_FN [3:0]	0000	GPIO1 Pin Function (see Table 65 for details)
R13 (0Dh) GPIO2 Control	15	GP2_DIR	1	GPIO2 Pin Direction 0 = Output 1 = Input
	14:13	GP2_PULL [1:0]	00	GPIO2 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	12	GP2_INT_MODE	0	GPIO2 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP2_POL=0) or falling edge triggered (if GP2_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges
	10	GP2_POL	0	GPIO2 Polarity Select 0 = Non-inverted 1 = Inverted
	5	GP2_LVL	0	GPIO2 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP2_POL is set, the register contains the opposite logic level to the external pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	GP2_FN [3:0]	0000	GPIO2 Pin Function (see Table 65 for details)
R14 (0Eh) GPIO3 Control	15	GP3_DIR	1	GPIO3 Pin Direction 0 = Output 1 = Input
	14:13	GP3_PULL [1:0]	10	GPIO3 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	12	GP3_INT_MODE	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=0) or falling edge triggered (if GP3_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges
	10	GP3_POL	0	GPIO3 Polarity Select 0 = Non-inverted 1 = Inverted
	5	GP3_LVL	0	GPIO3 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP3_POL is set, the register contains the opposite logic level to the external pin.
	3:0	GP3_FN [3:0]	0000	GPIO3 Pin Function (see Table 65 for details)
R15 (0Fh) GPIO4 Control	15	GP4_DIR	1	GPIO4 Pin Direction 0 = Output 1 = Input
	14:13	GP4_PULL [1:0]	00	GPIO4 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=0) or falling edge triggered (if GP4_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges
	10	GP4_POL	0	GPIO4 Polarity Select 0 = Non-inverted 1 = Inverted
	5	GP4_LVL	0	GPIO4 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP4_POL is set, the register contains the opposite logic level to the external pin.
	3:0	GP4_FN [3:0]	0000	GPIO4 Pin Function (see Table 65 for details)

Table 64 GPIO Control

GPIO FUNCTION SELECT

The available GPIO functions are described in Table 65. The function of each GPIO is set using the GPn_FN register, where n identifies the GPIO pin (1 to 4).

Note that the polarity of the GPIO inputs and outputs may be selected using the GPn_POL register bits. When GPn_POL = 1, then the polarity is inverted with respect to the descriptions below.

The GPIO input functions may be used to detect headphone jack insertion or a button press. These signals may be used as inputs to the Interrupt Controller, via the integrated de-bounce circuit.

GPn_FN	DESCRIPTION	COMMENTS
0000	Logic level input	External logic level is read from GPn_LVL. Associated interrupt (when enabled) is level-triggered.
0001	Edge detection input	External logic level is read from GPn_LVL. Associated interrupt (when enabled) is edge triggered. Note that TOCLK_ENA must be set.
0010	CLKOUT output	Output clock frequency is set by CLKOUT_DIV.
0011	Interrupt (IRQ) output	Hardware output of all unmasked Interrupts.
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Temperature flag output	Indicates the temperature sensor output. This is a hardware output of the TEMP_STS bit (assuming GPn_POL = 0). 0 = Normal 1 = Overtemperature
1000	Reserved	
1001	DMICCLK output	Output clock for digital microphone interface
1010	Logic level output	Pin logic level is set by GPn_LVL.
1011	LDO_UV output	Indicates the LDO undervoltage status. This is a hardware output of the LDO_UV_STS bit (assuming GPn_POL = 0). 0 = Normal 1 = LDO undervoltage
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	

Table 65 GPIO Function Select

INTERRUPTS

The Interrupt Controller has multiple inputs. These include the GPIO input pins, Temperature sensor and the LDO Regulator. Any combination of these inputs can be used to trigger an Interrupt (IRQ) event.

There is an Interrupt Status field associated with each of the IRQ inputs. These are listed within the System Interrupts Register (R16), as described in Table 66. The status of the IRQ inputs can be read at any time from this register or else in response to the Interrupt (IRQ) output being signalled via a GPIO pin.

Individual mask bits can select or deselect different functions from the Interrupt controller. These are listed within the System Interrupts Mask Register (R19), as described in Table 66. Note that the status fields remain valid, even when masked, but the masked bits will not cause the Interrupt (IRQ) output to be asserted.

The Interrupt (IRQ) output represents the logical 'OR' of all the unmasked IRQ inputs. The bits within the System Interrupts Register (R16) are latching fields and, once they are set, they are not reset until the System Interrupts Register is read. Accordingly, the Interrupt (IRQ) output is not reset until the System Interrupts Register has been read. Note that, if the condition that caused the IRQ input to be asserted is still valid, then the Interrupt (IRQ) output will remain set even after the System Interrupts Register has been read.

When GPIO input is used to trigger an Interrupt event, polarity can be set using the GPn_POL bits as described in Table 64. This allows the IRQ event to be used to indicate a rising or a falling edge of the external logic signal. If desired, the GPn_INT_MODE bits can be used to select an Interrupt event on both the rising and falling edges.

The GPIO inputs to the Interrupt Controller are de-bounced to avoid false detections. The timeout clock (TOCLK) is required for this function. When using GPIO inputs to the Interrupt Controller, the TOCLK must be enabled by setting the TOCLK_ENA and OSC_CLK_ENA bits as described in "Clocking and Sample Rates".

The Interrupt (IRQ) output can be globally masked by setting the IM_IRQ register. The Interrupt is masked by default.

The Interrupt (IRQ) output may be configured on any of the GPIO pins. See "General Purpose Input / Output" for details of how to configure GPIO pins for Interrupt (IRQ) output.

The Interrupt control fields are defined in Table 66.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) System Interrupts	15	TEMP_INT	0	Thermal Interrupt status 0 = Thermal interrupt not set 1 = Thermal interrupt set This bit is latched when set; it is cleared when the register is Read.
	14	GP4_INT	0	GPIO4 Interrupt status 0 = GPIO4 interrupt not set 1 = GPIO4 interrupt set This bit is latched when set; it is cleared when the register is Read.
	13	GP3_INT	0	GPIO3 Interrupt status 0 = GPIO3 interrupt not set 1 = GPIO3 interrupt set This bit is latched when set; it is cleared when the register is Read.
	12	GP2_INT	0	GPIO2 Interrupt status 0 = GPIO2 interrupt not set 1 = GPIO2 interrupt set This bit is latched when set; it is cleared when the register is Read.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11	GP1_INT	0	GPIO1 Interrupt status 0 = GPIO1 interrupt not set 1 = GPIO1 interrupt set This bit is latched when set; it is cleared when the register is Read.
	0	LDO_UV_INT	0	LDO Undervoltage Interrupt 0 = LDO Undervoltage interrupt not set 1 = LDO Undervoltage interrupt set This bit is latched when set; it is cleared when the register is Read.
R18 (12h) IRQ Config	0	IM_IRQ	1	IRQ (GPIO output) Mask 0 = Normal 1 = IRQ output is masked
R19 (13h) System Interrupts Mask	15	IM_TEMP_INT	0	Interrupt mask for thermal status 0 = Not masked 1 = Masked
	14	IM_GP4_INT	0	Interrupt mask for GPIO4 0 = Not masked 1 = Masked
	13	IM_GP3_INT	0	Interrupt mask for GPIO3 0 = Not masked 1 = Masked
	12	IM_GP2_INT	0	Interrupt mask for GPIO2 0 = Not masked 1 = Masked
	11	IM_GP1_INT	0	Interrupt mask for GPIO1 0 = Not masked 1 = Masked
	0	IM_LDO_UV_INT	0	Interrupt mask for LDO Undervoltage status 0 = Not masked 1 = Masked

Table 66 Interrupt Control

CONTROL INTERFACE

The WM8946 is controlled by writing to its control registers. Readback is available for all registers. The Control Interface can operate as either a 2-, 3- or 4-wire interface:

- 2-wire (I2C) mode uses pins SCLK and SDA
- 3-wire (SPI) mode uses pins CS, SCLK and SDA
- 4-wire (SPI) mode uses pins CS, SCLK, SDA and SDOUT

Readback is provided on the bi-directional pin SDA in 2-/3-wire modes.

The device address in 2-wire (I2C) mode is 34h.

The WM8946 uses 15-bit register addresses and 16-bit data in all Control Interface modes.

SELECTION OF CONTROL INTERFACE MODE

The WM8946 Control Interface can be configured for I2C mode or SPI modes using the CIFMODE/GPIO3 pin at power-up. The mode selection is as described in Table 68.

CIFMODE/GPIO3	INTERFACE FORMAT
Low	2 wire
High	3- or 4- wire

Table 67 Control Interface Mode Selection

After the Control Interface Mode has been configured, the MODE_GPIO register bit should be set in order to latch the selection and to allow GPIO functions to be supported on the CIFMODE/GPIO3 pin. After the MODE_GPIO register bit has been set, the Control Interface mode selection will remain latched until a Software Reset or Power On Reset occurs. See “General Purpose Input / Output” for details.

In 2-wire (I2C) Control Interface mode, Auto-Increment mode may be selected. This enables multiple write and multiple read operations to be scheduled faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 68. Auto-increment is disabled by default.

In SPI modes, 3-wire or 4-wire operation may be selected using the SPI_4WIRE register bit. In 3-wire mode, register readback is provided using the bi-directional pin SDA. In 4-wire mode, register readback is provided using SDOUT. The SDOUT pin may be configured as CMOS or as Open Drain using the SPI_OD bit. In 3-wire mode the SDA pin may be configured as CMOS or as Open Drain using the SPI_OD bit. If the open drain option is selected (SPI_OD = 1) then an external pull-up resistor is required on the SDOUT or SDA output pin.

The Control Interface configuration bits are described in Table 68.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
t(14h) Control Interface	2	SPI_OD	0	SDOUT pin configuration (applies to 3-wire and 4-wire mode only) 0 = SDOUT output is CMOS 1 = SDOUT output is open drain
	1	SPI_4WIRE	1	SPI control mode select 0 = 3-wire using bidirectional SDA 1 = 4-wire using SDOUT
	0	AUTO_INC	0	Enables address auto-increment (applies to 2-wire / I2C mode only) 0 = Disabled 1 = Enabled

Table 68 Control Interface Configuration

2-WIRE (I2C) CONTROL MODE

In 2-wire mode, the WM8946 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8946 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 7-bit device ID (this is not the same as the 15-bit address of each register in the WM8946). The WM8946 device ID is 34h. The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

The WM8946 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device ID, register address and data will follow. The WM8946 responds to the start condition and shifts in the next eight bits on SDA (7-bit device ID + Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8946, then the WM8946 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is ‘1’ when operating in write only mode, the WM8946 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8946, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM8946 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM8946 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

The sequence of signals associated with a single register write operation is illustrated in Figure 34.

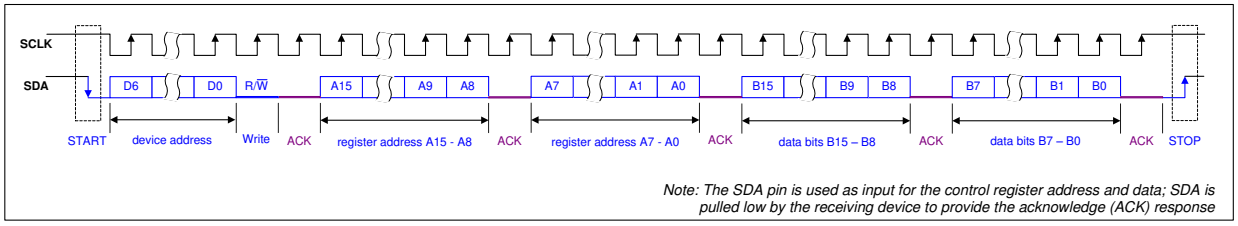


Figure 34 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 35.

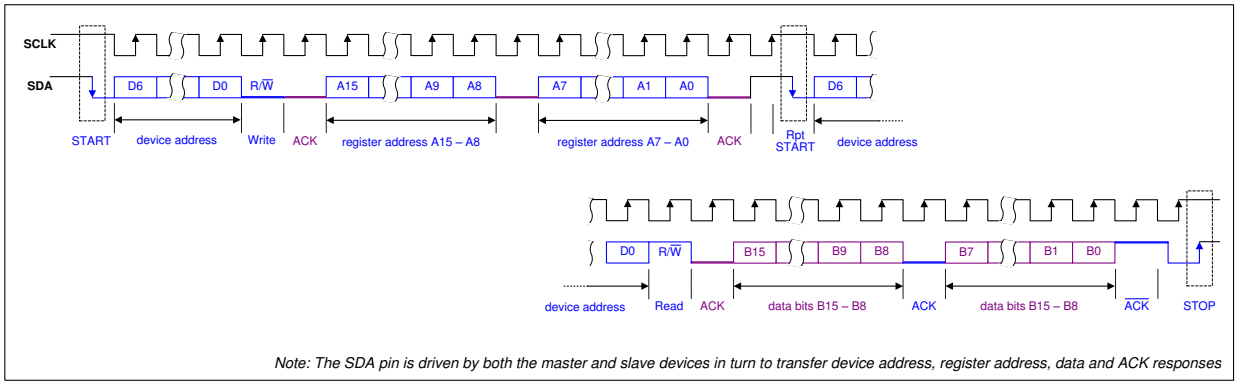


Figure 35 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 69.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default, as noted in Table 68.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge	
P	Stop Condition	
R/$\overline{W}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8946	
[Grey field]	Data flow from WM8946 to bus master	

Table 69 Control Interface Terminology

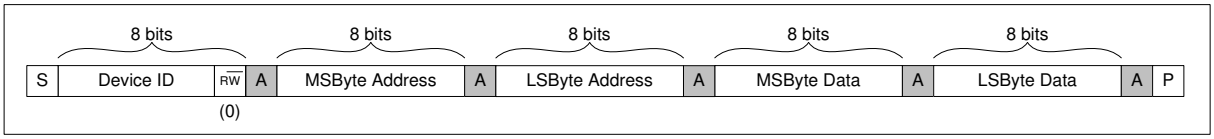


Figure 36 Single Register Write to Specified Address

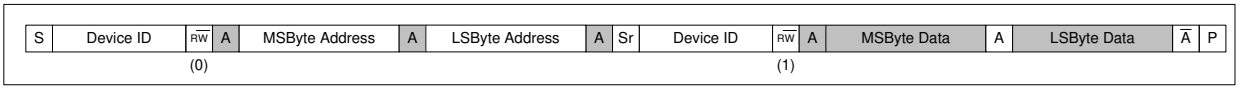


Figure 37 Single Register Read from Specified Address

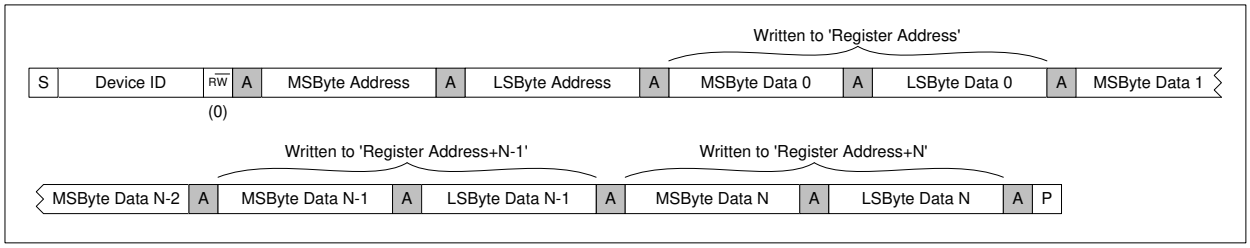


Figure 38 Multiple Register Write to Specified Address using Auto-increment

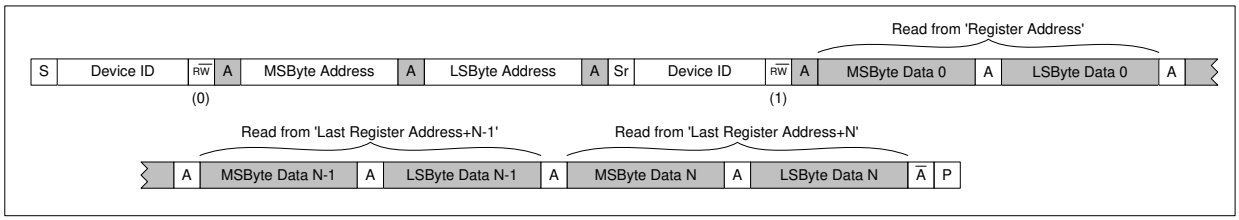


Figure 39 Multiple Register Read from Specified Address using Auto-increment

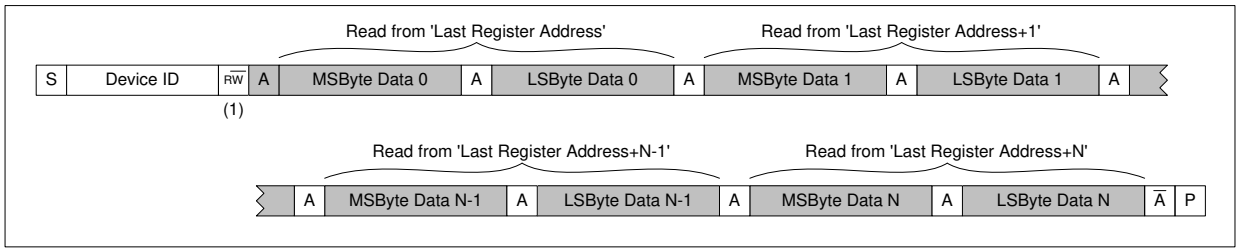


Figure 40 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8946 register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTO_INC register bit is set. This bit is defined in Table 68. Auto-increment is disabled by default.

3-WIRE (SPI) CONTROL MODE

The 3-wire control interface uses the CS, SCLK and SDA pins.

In 3-wire control mode, a control word consists of 32 bits. The first bit is the read/write bit (R/W), which is followed by 15 address bits (A14 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDA pin. The data is latched on the 32nd falling edge of SCLK after 32 bits of data have been clocked into the device.

In Write operations (R/W=0), all SDA bits are driven by the controlling device.

In Read operations (R/W=1), the SDA pin is driven by the controlling device to clock in the register address, after which the WM8946 drives the SDA pin to output the applicable data bits.

Similarly to 2-wire control mode, the WM8946 can be set to transmit logic 1 by tri-stating the SDA pin, rather than pulling it high (SPI_OD = 1). An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

The 3-wire control mode timing is illustrated in Figure 41.

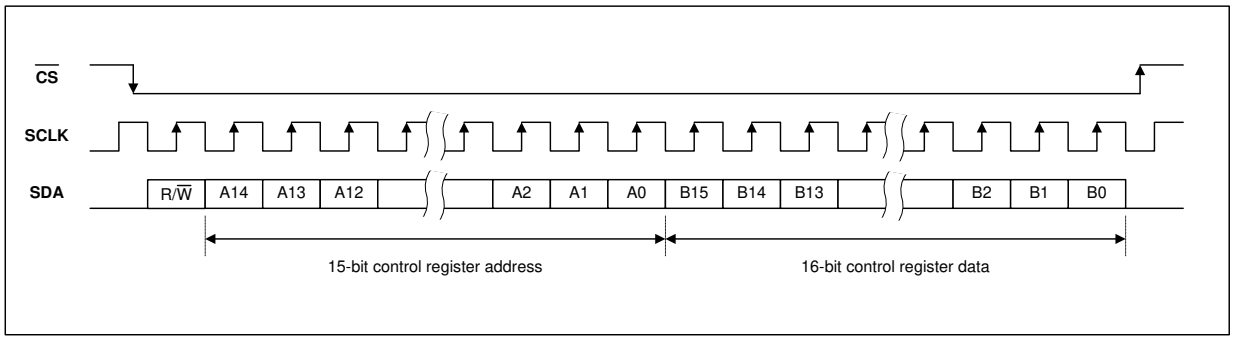


Figure 41 3-Wire Serial Control Interface

4-WIRE (SPI) CONTROL MODE

The 4-wire control interface uses the CS, SCLK, SDA and SDOUT pins.

The Data Output pin, SDOUT, can be configured as CMOS or Open Drain, as described in Table 68. In CMOS mode, SDOUT is driven low when not outputting register data bits. In Open Drain mode, SDOUT is undriven (high impedance) when not outputting register data bits.

In Write operations (R/W=0), this mode is the same as 3-wire mode described above.

In Read operations (R/W=1), the SDATA pin is ignored following receipt of the valid register address. SDOUT is driven by the WM8946.

The 4-wire control mode timing is illustrated in Figure 42 and Figure 43.

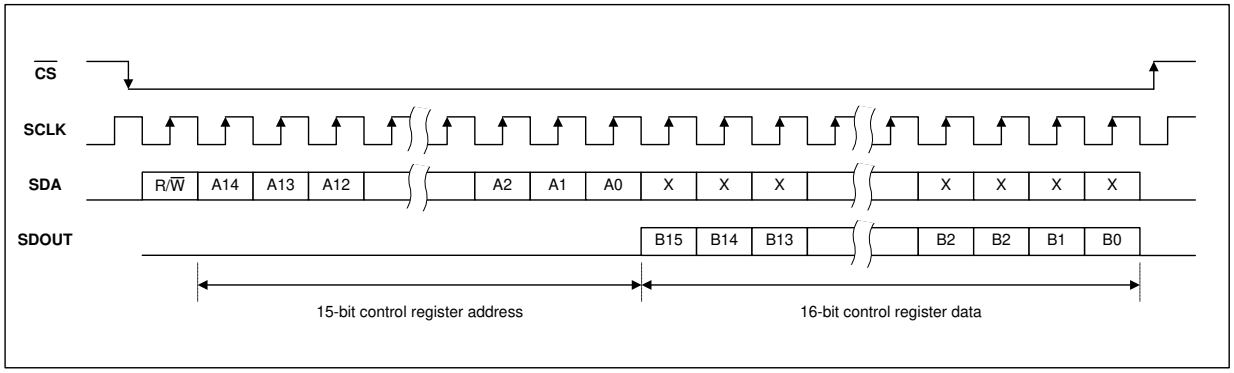


Figure 42 4-Wire Readback (CMOS)

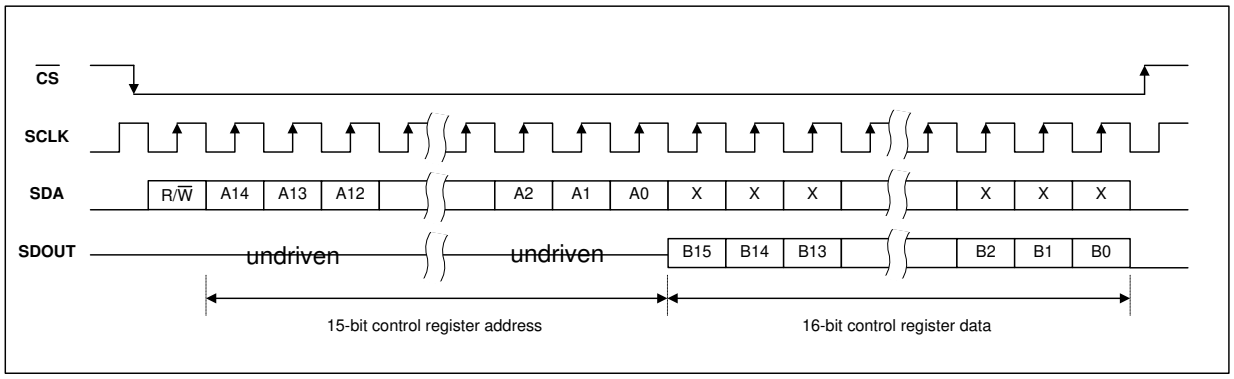


Figure 43 4-Wire Readback (Open Drain)

POWER MANAGEMENT

The WM8946 has two control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To minimise pop or click noise, it is important to enable or disable these functions in the correct order, and to use the signal mute registers as part of a carefully structured control sequence. Refer to the "Recommended Power Up/Down Sequence" section for more details.

The power management control registers are described in Table 70.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power management 1	13	INPPGAR_ENA	0	Right Input PGA Enable 0 = Disabled 1 = Enabled
	12	INPPGAL_ENA	0	Left Input PGA Enable 0 = Disabled 1 = Enabled
	11	ADCR_ENA	0	Right ADC and Record filter Enable 0 = Disabled 1 = Enabled ADCR_ENA must be set to 1 when processing right channel data from the ADC or Digital Microphone.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	ADCL_ENA	0	Left ADC and Record filter Enable 0 = Disabled 1 = Enabled ADCL_ENA must be set to 1 when processing left channel data from the ADC or Digital Microphone.
	4	MICB_ENA	0	Microphone Bias Enable 0 = Disabled 1 = Enabled
	3	BIAS_ENA	0	Master Bias Enable 0 = Disabled 1 = Enabled
R3 (03h) Power management 2	15	OUTR_ENA	0	LINEOUTR enable 0 = Disabled 1 = Enabled
	14	OUTL_ENA	0	LINEOUTL enable 0 = Disabled 1 = Enabled
	13	SPKR_PGA_ENA	0	Speaker Right PGA enable 0 = Disabled 1 = Enabled
	12	SPKL_PGA_ENA	0	Speaker Left PGA enable 0 = Disabled 1 = Enabled
	11	SPKR_SPKVDD_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_OP_ENA. When powering down SPKOUTR, the SPKR_SPKVDD_ENA bit should be reset first.
	10	SPKL_SPKVDD_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_OP_ENA. When powering down SPKOUTL, the SPKL_SPKVDD_ENA bit should be reset first
	7	SPKR_OP_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_SPKVDD_ENA. When powering up SPKOUTR, the SPKR_OP_ENA bit should be enabled first.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	SPKL_OP_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_SPKVDD_ENA. When powering up SPKOUTL, the SPKL_OP_ENA bit should be enabled first
	3	SPKR_MIX_ENA	0	Right speaker output mixer enable 0 = Disabled 1 = Enabled
	2	SPKL_MIX_ENA	0	Left speaker output mixer enable 0 = Disabled 1 = Enabled
	1	DACR_ENA	0	Right DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing right channel data from the DAC or Digital Beep Generator.
	0	DACL_ENA	0	Left DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing left channel data from the DAC or Digital Beep Generator.

Table 70 Power Management Control

THERMAL SHUTDOWN

The WM8946 incorporates a temperature sensor which detects when the device temperature is within normal limits. The temperature status can be read at any time from the TEMP_STS bit, as described in Table 71. This bit can be polled at any time, or may output directly on a GPIO pin, or may be used to generate Interrupt events.

The temperature sensor can be configured to shut down the speaker outputs in the event of an overtemperature condition. This is configured using the THERR_ACT register field.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) Status Flags	15	TEMP_STS	0	Thermal Sensor status 0 = Normal 1 = Overtemperature
R42 (2Ah) Output ctrl	15	THERR_ACT	1	Thermal Shutdown enable 0 = Disabled 1 = Enabled When THERR_ACT = 1, then an overtemperature condition will cause the speaker outputs to be disabled.

Table 71 Thermal Shutdown Control

POWER ON RESET

The WM8946 includes a Power-On Reset (POR) circuit, which is used to reset the digital logic into a default state after power up. The POR circuit derives its output from LDOVDD and DCVDD. The internal $\overline{POR}$ signal is asserted low when either LDOVDD or DCVDD are below minimum thresholds.

The specific behaviour of the circuit will vary, depending on relative timing of the supply voltages. Typical scenarios are illustrated in Figure 44 and Figure 45.

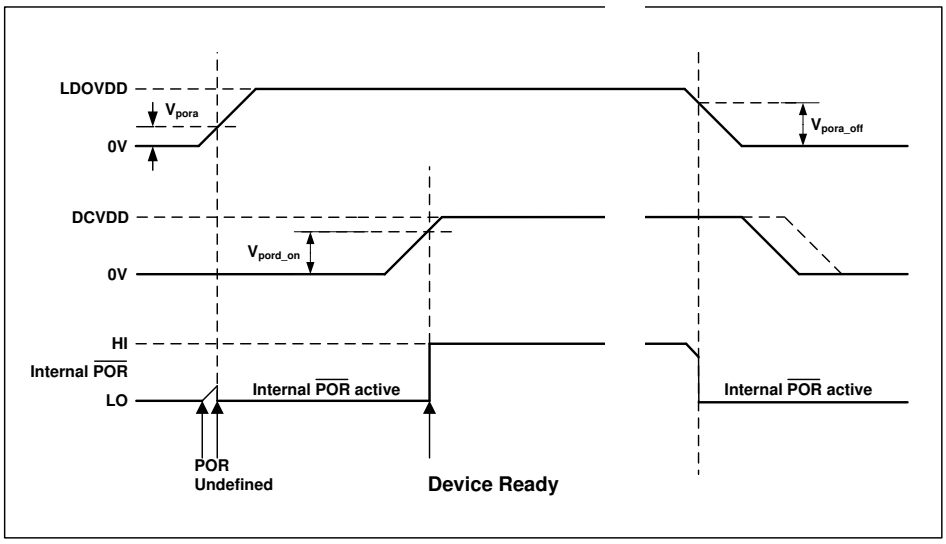


Figure 44 Power On Reset Timing – LDOVDD Enabled First

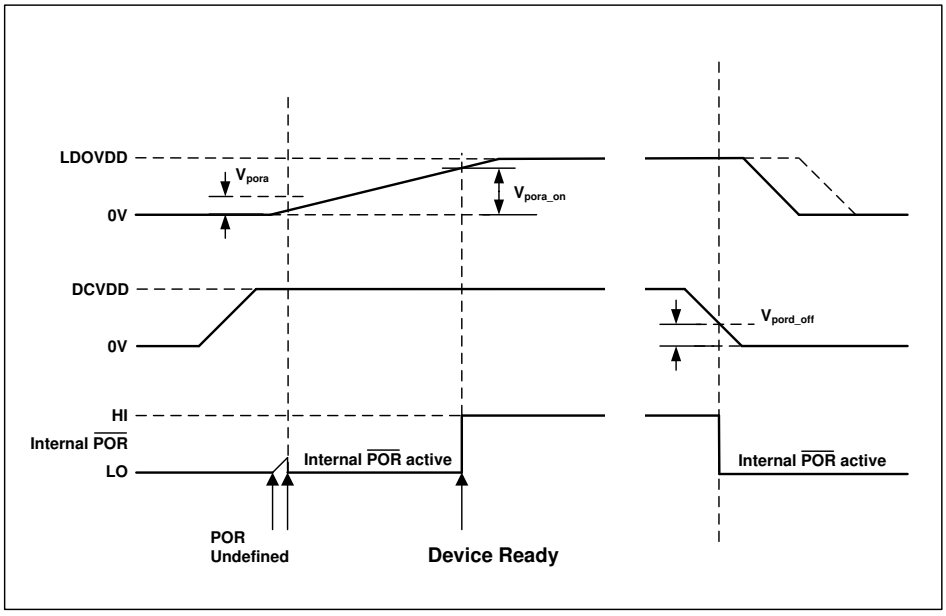


Figure 45 Power On Reset Timing – DCVDD Enabled First

The $\overline{POR}$ signal is undefined until LDOVDD has exceeded the minimum threshold, V_{pora} Once this threshold has been exceeded, $\overline{POR}$ is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Once LDOVDD and DCVDD have both reached their respective power on thresholds, $\overline{POR}$ is released high, all registers are in their default state, and writes to the control interface may take place.

Note that a minimum power-on reset period, T_{POR}, applies even if LDOVDD and DCVDD have zero rise time. (This specification is guaranteed by design rather than test.)

On power down, PŌR is asserted low when LDOVDD or DCVDD falls below their respective power-down thresholds.

Typical Power-On Reset parameters for the WM8946 are defined in Table 72.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{pora}	Power-On undefined threshold (LDOVDD)		0.5		V
V_{pora_on}	Power-On threshold (LDOVDD)		1.15		V
V_{pora_off}	Power-Off threshold (LDOVDD)		1.12		V
V_{pord_on}	Power-On threshold (DCVDD)		0.57		V
V_{pord_off}	Power-Off threshold (DCVDD)		0.56		V
T_{POR}	Minimum Power-On Reset period		10.6		µs

Table 72 Typical Power-On Reset Parameters

Separate Power-On Reset circuits are also implemented on the DBVDD and SPKVDD domains. These circuits ensure correct device behaviour whenever these supplies are enabled or disabled.

SOFTWARE RESET AND DEVICE ID

The WM8946 can be reset by writing to Register R0. This is a read-only register, and the contents of R0 will not be affected by writing to this Register.

The Device ID can be read back from Register R0. The Chip Revision ID can be read back from Register 1, as described in Table 73.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Software Reset/Chip ID 1	15:0	SW_RESET [15:0]	6229h	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 6229h.
R1 (01h) Revision Number	3:0	CHIP_REV [3:0]		Reading from this register will indicate the Revision ID.

Table 73 Chip Reset and ID

RECOMMENDED POWER UP / POWER-DOWN SEQUENCES

In order to minimise output pop and click noise, it is recommended that the WM8946 device is powered-up and powered-down using the control sequences described in Table 74 and Table 75 respectively.

The power-up sequence described here includes enabling the DACs and output drivers; note that additional configuration will be required to enable the required internal signal paths.

The sequences noted here are provided as guidance only; each sequence will require to be adjusted to the particular application requirements.

DESCRIPTION	LABEL	REGISTER [BITS]
Turn on external supplies and wait for the supply voltages to settle.		
Reset registers to default state (software reset).	SW_RESET	R0 (00h) [15:0]
Enable speaker and line discharge bits.	SPKR_DISCH = 1 SPKL_DISCH = 1 LINER_DISCH = 1 LINEL_DISCH = 1	R42 (2Ah) [7] R42 (2Ah) [6] R42 (2Ah) [5] R42 (2Ah) [4]
Enable VMID to speaker and line outputs.	SPKR_VMID_OP_ENA = 1 SPKL_VMID_OP_ENA = 1 LINER_VMID_OP_ENA = 1 LINEL_VMID_OP_ENA = 1	R42 (2Ah) [13] R42 (2Ah) [12] R42 (2Ah) [11] R42 (2Ah) [10]
Enable VMID Fast Start and Start up Bias. Select Start-Up Bias and set VMID soft start for start-up ramp.	VMID_FAST_START = 1 STARTUP_BIAS_ENA = 1 BIAS_SRC = 1 VMID_RAMP[1:0] = 01	R7 (07h) [11] R7 (07h) [8] R7 (07h) [7] R7 (07h) [6:5]
If using VMID as the reference voltage for the LDO then select VMID fast start or set to 0 if using the Bandgap as the reference voltage for LDO. Select LDO Start-Up Bias and enable LDO. Delay 300ms for LDO to settle.	LDO_ENA = 1 LDO_REF_SEL_FAST = 1 LDO_BIAS_SRC = 1	R53 (35h) [15] R53 (35h) [14] R53 (35h) [5]
Enable VMID Buffer and Master Bias. Set VMID_SEL[1:0] for fast start-up.	BIAS_ENA = 1 VMID_BUF_ENA = 1 VMID_SEL[1:0] = 11	R2 (02h) [3] R2 (02h) [2] R2 (02h) [1:0]
Disable speaker and line output discharge bits.	SPKP_DISCH = 0 SPKN_DISCH = 0 LINER_DISCH = 0 LINEL_DISCH = 0	R42 (2Ah) [6] R42 (2Ah) [7] R42 (2Ah) [5] R42 (2Ah) [4]
Enable speaker mixers and DACs.	SPKR_MIX_ENA = 1 SPKL_MIX_ENA = 1 DACR_ENA = 1 DACL_ENA = 1	R3 (03h) [3] R3 (03h) [2] R3 (03h) [1] R3 (03h) [0]
Enable speaker outputs, speaker PGAs, and lineout outputs.	OUTR_ENA = 1 OUTL_ENA = 1 SPKR_PGA_ENA = 1 SPKL_PGA_ENA = 1 SPKN_OP_ENA = 1 SPKP_OP_ENA = 1	R3 (03h) [15] R3 (03h) [14] R3 (03h) [13] R3 (03h) [12] R3 (03h) [7] R3 (03h) [6]
Enable power to speaker driver (must be done after enabling the speaker outputs).	SPKR_SPKVDD_ENA = 1 SPKL_SPKVDD_ENA = 1	R3 (03h) [11] R3 (03h) [10]
Enable VMID. Delay 150ms to allow VMID to settle.	VMID_ENA = 1	R7 (07h) [4]
Set LDO and VMID for normal operation.	LDO_REF_SEL_FAST = 0 LDO_BIAS_SRC = 0 VMID_FAST_START = 0 STARTUP_BIAS_ENA = 0 VMID_SEL = 01	R53 (35h) [14] R53 (35h) [5] R7 (07h) [11] R7 (07h) [8] R2 (02h) [1:0]
Un-mute outputs as required.		

Table 74 Recommended Power-Up Sequence

DESCRIPTION	LABEL	REGISTER [BITS]
Mute speaker PGAs and DACs.	SPKR_PGA_ENA = 1 SPKL_PGA_ENA = 1 SPKR_VOL = 00h SPKL_VOL = 00h DACR_MUTE = 1 DACL_MUTE = 1 DACR_VOL = 0 DACL_VOL = 0	R3 (03h) [13] R3 (03h) [12] R47 (2Fh) [5:0] R48 (30h) [5:0] R24 (18h) [8] R23 (17h) [8] R24 (18h) [7:0] R23 (17h) [7:0]
Select LDO for fast start-up.	LDO_REF_SEL_FAST = 1 LDO_BIAS_SRC = 1	R53 (35h) [14] R53 (35h) [5]
Select VMID for fast start-up.	VMID_SEL = 11 VMID_FAST_START =1 BIAS_SRC = 1 VMID_RAMP = 01	R2 (02h) [1:0] R7 (07h) [11] R7 (07h) [7] R7 (07h) [6:5]
Disable VMID. Delay 500ms for VMID to discharge.	VMID_ENA = 0	R7 (07h) [4]
Discharge the speaker and line outputs. Delay 50ms for outputs to discharge.	SPKR_DISCH = 1 SPKL_DISCH = 1 LINER_DISCH = 1 LINEL_DISCH = 1	R42 (2Ah) [7] R42 (2Ah) [6] R42 (2Ah) [5] R42 (2Ah) [4]
Mute the speaker and line outputs.	LINER_MUTE = 1 LINEL_MUTE = 1 SPKR_OP_MUTE = 1 SPKL_OP_MUTE = 1	R42 (2Ah) [9] R42 (2Ah) [8] R03 (03h) [9] R03 (03h) [8]
Disable power to speaker drivers (must be done before disabling the speaker outputs).	SPKR_SPKVDD_ENA = 0 SPKL_SPKVDD_ENA = 0	R3 (03h) [11] R3 (03h) [10]
Disable speaker outputs.	SPKN_OP_ENA = 0 SPKP_OP_ENA = 0	R3 (03h) [7] R3 (03h) [6]
Reset registers to default state (software reset).	SW_RESET	R0 (00h) [15:0]
Turn off external power supply voltages.		

Table 75 Recommended Power-Down Sequence

REGISTER MAP

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R0 (0h)	Software Reset/Chip ID 1	SW_RESET[15:0]																6229h
R1 (1h)	Chip ID 2	0	0	0	0	0	0	0	0	0	0	0	0	CHIP_REV[3:0]				0000h
R2 (2h)	Power management 1	0	0	INPPGAR_ENA	INPPGAL_ENA	ADCR_ENA	ADCL_ENA	0	0	DMIC_ENA	0	0	MICB_ENA	BIAS_ENA	VMID_BUF_ENA	VMID_SEL[1:0]		0000h
R3 (3h)	Power management 2	OUTR_ENA	OUTL_ENA	SPKR_PGA_ENA	SPKL_PGA_ENA	SPKR_SPKVDD_ENA	SPKL_SPKVDD_ENA	SPKR_OP_MUTE	SPKL_OP_MUTE	SPKR_OP_ENA	SPKL_OP_ENA	SPKR_MIX_MUTE	SPKL_MIX_MUTE	SPKR_MIX_ENA	SPKL_MIX_ENA	DACR_ENA	DACL_ENA	0330h
R4 (4h)	Audio Interface	DACDATA_PULL[1:0]		FRAME_PULL[1:0]		BCLK_PULL[1:0]		ADCR_SRC	ADCL_SRC	DACR_SRC	DACL_SRC	BCLK_INV	LRCLK_INV	WL[1:0]		FMT[1:0]		028Ah
R5 (5h)	Companding control	0	0	0	0	0	0	0	0	0	0	LOOPBACK	0	DAC_COMP	DAC_COMPMODE	ADC_COMP	ADC_COMPMODE	0000h
R6 (6h)	Clock Gen control	OSC_CLK_ENA	MCLK_PULL[1:0]		CLKOUT_SEL	CLKOUT_DIV[1:0]		SYSCLK_ENA	SYSCLK_SRC	SYSCLK_DIV[2:0]			TOCLK_ENA	BCLK_DIV[2:0]			MSTR	0106h
R7 (7h)	Additional control	0	0	0	0	VMID_FAST_START	VMID_REF_SEL	VMID_CTRL	STARTUP_BIAS_ENA	BIAS_SRC	VMID_RAMP[1:0]		VMID_ENA	SR[3:0]				000Dh
R8 (8h)	FLL Control 1	0	0	0	FLL_CLK_REF_DIV[1:0]		FLL_OUTDIV[2:0]			FLL_CTRL_RATE[2:0]			FLL_FRATIO[2:0]			FLL_FRAC	FLL_ENA	0102h
R9 (9h)	FLL Control 2	FLL_K[15:0]																3127h
R10 (Ah)	FLL Control 3	0	FLL_N[9:0]										0	FLL_GAIN[3:0]				0104h
R11 (Bh)	GPIO Config	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MODE_GPIO	0000h
R12 (Ch)	GPIO1 Control	GP1_DIR	GP1_PULL[1:0]		GP1_INT_MODE	0	GP1_POL	0	0	0	0	GP1_LVL	0	GP1_FN[3:0]				8000h
R13 (Dh)	GPIO2 Control	GP2_DIR	GP2_PULL[1:0]		GP2_INT_MODE	0	GP2_POL	0	0	0	0	GP2_LVL	0	GP2_FN[3:0]				8000h
R14 (Eh)	GPIO3 Control	GP3_DIR	GP3_PULL[1:0]		GP3_INT_MODE	0	GP3_POL	0	0	0	0	GP3_LVL	0	GP3_FN[3:0]				C000h
R15 (Fh)	GPIO4 Control	GP4_DIR	GP4_PULL[1:0]		GP4_INT_MODE	0	GP4_POL	0	0	0	0	GP4_LVL	0	GP4_FN[3:0]				8000h
R16 (10h)	System Interrupts	TEMP_INT	GP4_INT	GP3_INT	GP2_INT	GP1_INT	0	0	0	0	0	0	0	0	0	0	LDO_UV_INT	0000h
R17 (11h)	Status Flags	TEMP_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LDO_UV_STS	0000h
R18 (12h)	IRQ Config	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IM_IRQ	0001h
R19 (13h)	System Interrupts Mask	IM_TEMP_INT	IM_GP4_INT	IM_GP3_INT	IM_GP2_INT	IM_GP1_INT	0	0	0	0	0	0	0	0	0	0	IM_LDO_UV_INT	0000h
R20 (14h)	Control Interface	0	0	0	0	0	0	0	0	0	0	0	0	0	SPI_OD	SPI_4WIRE	AUTO_INC	0002h
R21 (15h)	DAC Control 1	0	0	0	0	0	0	0	DAC_MUTEALL	0	0	0	DAC_AUTOMUTE	0	0	DACR_DATINV	DACL_DATINV	0110h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R22 (16h)	DAC Control 2	0	0	0	0	0	0	0	0	0	0	0	DAC_VOL_RAMP	0	0	0	DAC_SB_FLT	0010h
R23 (17h)	Left DAC digital Vol	0	0	0	DAC_VU	0	0	0	DACL_MUTE	DACL_VOL[7:0]								00C0h
R24 (18h)	Right DAC digital Vol	0	0	0	DAC_VU	0	0	0	DACR_MUTE	DACR_VOL[7:0]								00C0h
R25 (19h)	ADC Control 1	0	0	0	0	0	0	0	ADC_MUTEALL	0	0	0	0	0	0	ADCR_DATINV	ADCL_DATINV	0100h
R26 (1Ah)	ADC Control 2	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC_HPF_CUT[1:0]		ADC_HPF	0000h
R27 (1Bh)	Left ADC Digital Vol	0	0	0	ADC_VU	0	0	0	ADCL_MUTE	ADCL_VOL[7:0]								00C0h
R28 (1Ch)	Right ADC Digital Vol	0	0	0	ADC_VU	0	0	0	ADCR_MUTE	ADCR_VOL[7:0]								00C0h
R29 (1Dh)	DRC Control 1	0	0	0	0	0	0	0	DRC_NG_ENA	DRC_ENA	0	0	0	1	DRC_QR	DRC_ANTICLIP	1	000Fh
R30 (1Eh)	DRC Control 2	0	0	0	DRC_NG_MINGAIN[3:0]				0	0	0	1	DRC_MINGAIN[2:0]			DRC_MAXGAIN[1:0]		0C25h
R31 (1Fh)	DRC Control 3	0	0	0	0	0	0	1	1	DRC_ATK[3:0]				DRC_DCY[3:0]				0342h
R32 (20h)	DRC Control 4	0	0	0	DRC_KNEE2_IP[4:0]					DRC_KNEE_IP[5:0]						0	0	0000h
R33 (21h)	DRC Control 5	0	0	DRC_KNEE2_OP_ENA	DRC_KNEE2_OP[4:0]					DRC_KNEE_OP[4:0]				DRC_HI_COMP[2:0]				0003h
R34 (22h)	DRC Control 6	0	0	0	0	0	0	0	0	0	0	0	0	DRC_QR_THR[1:0]		DRC_QR_DCY[1:0]		0000h
R35 (23h)	DRC Control 7	0	0	0	0	0	0	DRC_NG_EXP[1:0]		DRC_LO_COMP[2:0]			DRC_INIT[4:0]					0000h
R36 (24h)	DRC Status	DRC_GAIN[15:0]																0000h
R37 (25h)	Beep Control 1	0	0	0	0	0	0	0	0	0	BEEP_GAIN[3:0]				BEEP_RATE[1:0]		BEEP_ENA	0002h
R38 (26h)	Video Buffer	0	0	0	0	0	0	0	0	VB_ENA	VB_QBOOST	VB_GAIN	VB_DISOFF[2:0]			VB_PD	VB_CLAMP	001Ch
R39 (27h)	Input ctrl	0	0	0	0	0	0	0	AUX2_AUDIO	AUX1_AUDIO	MICB_LVL	MICRN_TO_N_PGAR	MICLN_TO_N_PGAL	P_PGAR_SEL[1:0]		P_PGAL_SEL[1:0]		0035h
R40 (28h)	Left INP PGA gain ctrl	0	0	0	0	0	0	0	PGA_VU	PGAL_ZC	PGAL_MUTE	PGAL_VOL[5:0]						0050h
R41 (29h)	Right INP PGA gain ctrl	0	0	0	0	0	0	0	PGA_VU	PGAR_ZC	PGAR_MUTE	PGAR_VOL[5:0]						0050h
R42 (2Ah)	Output ctrl	THERR_ACT	0	SPKR_VMID_OP_ENA	SPKL_VMID_OP_ENA	LINER_VMID_OP_ENA	LINEL_VMID_OP_ENA	LINER_MUTE	LINEL_MUTE	SPKR_DISCH	SPKL_DISCH	LINER_DISCH	LINEL_DISCH	0	0	SPK_VROI	LINE_VROI	8300h
R43 (2Bh)	SPK mixer control1	0	0	0	0	0	0	0	AUX1_TO_SPKL	PGAL_TO_SPKL	BYPL_TO_PGAL	MDACL_TO_PGAL	MDACR_TO_PGAL	DACL_TO_PGAL	DACR_TO_PGAL	AUX2_TO_PGAL	AUX1_TO_PGAL	0000h
R44 (2Ch)	SPK mixer control2	0	0	0	0	0	0	0	AUX1_TO_SPKR	PGAR_TO_SPKR	BYPR_TO_PGAR	MDACL_TO_PGAR	MDACR_TO_PGAR	DACL_TO_PGAR	DACR_TO_PGAR	AUX2_TO_PGAR	AUX1_TO_PGAR	0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R45 (2Dh)	SPK mixer control3	0	0	0	0	0	0	0	AUX1_TO_SPKL_ATTEN	PGAL_TO_SPKL_ATTEN	BYPL_TO_PGAL_ATTEN	0	0	DACL_TO_PGAL_ATTEN	DACR_TO_PGAL_ATTEN	AUX2_TO_PGAL_ATTEN	AUX1_TO_PGAL_ATTEN	0000h
R46 (2Eh)	SPK mixer control4	0	0	0	0	0	0	0	AUX1_TO_SPKR_ATTEN	PGAR_TO_SPKR_ATTEN	BYPR_TO_PGAR_ATTEN	0	0	DACL_TO_PGAR_ATTEN	DACR_TO_PGAR_ATTEN	AUX2_TO_PGAR_ATTEN	AUX1_TO_PGAR_ATTEN	0000h
R47 (2Fh)	Left SPK volume ctrl	0	0	0	0	0	0	0	SPK_VU	SPKL_ZC	SPKL_PGA_MUTE	SPKL_VOL[5:0]						0079h
R48 (30h)	Right SPK volume ctrl	0	0	0	0	0	0	0	SPK_VU	SPKR_ZC	SPKR_PGA_MUTE	SPKR_VOL[5:0]						0079h
R49 (31h)	Line L mixer control 1	0	0	0	0	0	0	0	0	0	BYPL_TO_OUTL	MDACL_TO_OUTL	MDACR_TO_OUTL	DACL_TO_OUTL	DACR_TO_OUTL	AUX2_TO_OUTL	AUX1_TO_OUTL	0000h
R50 (32h)	Line R mixer control 1	0	0	0	0	0	0	0	0	0	BYPR_TO_OUTR	MDACL_TO_OUTR	MDACR_TO_OUTR	DACL_TO_OUTR	DACR_TO_OUTR	AUX2_TO_OUTR	AUX1_TO_OUTR	0000h
R51 (33h)	Line L mixer control 2	0	0	0	0	0	0	0	0	0	BYPL_TO_OUTL_ATTEN	0	0	DACL_TO_OUTL_ATTEN	DACR_TO_OUTL_ATTEN	AUX2_TO_OUTL_ATTEN	AUX1_TO_OUTL_ATTEN	0000h
R52 (34h)	Line R mixer control 2	0	0	0	0	0	0	0	0	0	BYPR_TO_OUTR_ATTEN	0	0	DACL_TO_OUTR_ATTEN	DACR_TO_OUTR_ATTEN	AUX2_TO_OUTR_ATTEN	AUX1_TO_OUTR_ATTEN	0000h
R53 (35h)	LDO	LDO_ENA	LDO_REF_SEL_FAST	LDO_REF_SEL	LDO_OPFLT	0	0	0	0	0	0	LDO_BIAS_SRC	LDO_VSEL[4:0]					0007h
R54 (36h)	Bandgap	BG_ENA	0	0	0	0	0	0	0	0	0	0	BG_VSEL[4:0]					000Ah
R64 (40h)	SE Config Selection	0	0	0	0	0	0	0	0	0	0	0	0	SE_CONFIG[3:0]				0000h
R65 (41h)	SE1_LHPF_CONFIG	0	0	0	0	0	0	0	0	0	0	SE1_LHPF_R_SIGN	SE1_LHPF_L_SIGN	0	0	SE1_LHPF_R_ENA	SE1_LHPF_L_ENA	0000h
R66 (42h)	SE1_LHPF_L	SE1_LHPF_L[15:0]																0000h
R67 (43h)	SE1_LHPF_R	SE1_LHPF_R[15:0]																0000h
R68 (44h)	SE1_3D_CONFIG	0	0	0	SE1_3D_MONO	0	0	SE1_3D_R_SIGN	SE1_3D_L_SIGN	SE1_3D_LHPF_R_ENA	SE1_3D_LHPF_L_ENA	SE1_3D_R_LHPF_SIGN	SE1_3D_L_LHPF_SIGN	0	0	SE1_3D_R_ENA	SE1_3D_L_ENA	0000h
R69 (45h)	SE1_3D_L	0	0	SE1_3D_L_DELAY[2:0]			SE1_3D_L_CUTOFF[2:0]			SE1_3D_L_CGAIN[3:0]				SE1_3D_L_FGAIN[3:0]				0408h
R70 (46h)	SE1_3D_R	0	0	SE1_3D_R_DELAY[2:0]			SE1_3D_R_CUTOFF[2:0]			SE1_3D_R_CGAIN[3:0]				SE1_3D_R_FGAIN[3:0]				0408h
R71 (47h)	SE1_NOTCH_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE1_NOTCH_R_ENA	SE1_NOTCH_L_ENA	0000h
R72 (48h)	SE1_NOTCH_A10	SE1_NOTCH_A10[15:0]																0000h
R73 (49h)	SE1_NOTCH_A11	SE1_NOTCH_A11[15:0]																0000h
R74 (4Ah)	SE1_NOTCH_A20	SE1_NOTCH_A20[15:0]																0000h
R75 (4Bh)	SE1_NOTCH_A21	SE1_NOTCH_A21[15:0]																0000h
R76 (4Ch)	SE1_NOTCH_A30	SE1_NOTCH_A30[15:0]																0000h
R77 (4Dh)	SE1_NOTCH_A31	SE1_NOTCH_A31[15:0]																0000h
R78 (4Eh)	SE1_NOTCH_A40	SE1_NOTCH_A40[15:0]																0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R79 (4Fh)	SE1_NOTCH_A41	SE1_NOTCH_A41[15:0]																0000h
R80 (50h)	SE1_NOTCH_A50	SE1_NOTCH_A50[15:0]																0000h
R81 (51h)	SE1_NOTCH_A51	SE1_NOTCH_A51[15:0]																0000h
R82 (52h)	SE1_NOTCH_M10	SE1_NOTCH_M10[15:0]																0000h
R83 (53h)	SE1_NOTCH_M11	SE1_NOTCH_M11[15:0]																1000h
R84 (54h)	SE1_NOTCH_M20	SE1_NOTCH_M20[15:0]																0000h
R85 (55h)	SE1_NOTCH_M21	SE1_NOTCH_M21[15:0]																1000h
R86 (56h)	SE1_NOTCH_M30	SE1_NOTCH_M30[15:0]																0000h
R87 (57h)	SE1_NOTCH_M31	SE1_NOTCH_M31[15:0]																1000h
R88 (58h)	SE1_NOTCH_M40	SE1_NOTCH_M40[15:0]																0000h
R89 (59h)	SE1_NOTCH_M41	SE1_NOTCH_M41[15:0]																1000h
R90 (5Ah)	SE1_NOTCH_M50	SE1_NOTCH_M50[15:0]																0000h
R91 (5Bh)	SE1_NOTCH_M51	SE1_NOTCH_M51[15:0]																1000h
R92 (5Ch)	SE1_DF1_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE1_DF1_R_ENA	SE1_DF1_L_ENA	0000h
R93 (5Dh)	SE1_DF1_L0	SE1_DF1_L0[15:0]																1000h
R94 (5Eh)	SE1_DF1_L1	SE1_DF1_L1[15:0]																0000h
R95 (5Fh)	SE1_DF1_L2	SE1_DF1_L2[15:0]																0000h
R96 (60h)	SE1_DF1_R0	SE1_DF1_R0[15:0]																1000h
R97 (61h)	SE1_DF1_R1	SE1_DF1_R1[15:0]																0000h
R98 (62h)	SE1_DF1_R2	SE1_DF1_R2[15:0]																0000h
R100 (64h)	SE2_RETUNE_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE2_RETUNE_R_ENA	SE2_RETUNE_L_ENA	0000h
R101 (65h)	SE2_RETUNE_C0	SE2_RETUNE_C0[15:0]																1000h
R102 (66h)	SE2_RETUNE_C1	SE2_RETUNE_C1[15:0]																0000h
R103 (67h)	SE2_RETUNE_C2	SE2_RETUNE_C2[15:0]																0000h
R104 (68h)	SE2_RETUNE_C3	SE2_RETUNE_C3[15:0]																0000h
R105 (69h)	SE2_RETUNE_C4	SE2_RETUNE_C4[15:0]																0000h
R106 (6Ah)	SE2_RETUNE_C5	SE2_RETUNE_C5[15:0]																0000h
R107 (6Bh)	SE2_RETUNE_C6	SE2_RETUNE_C6[15:0]																0000h
R108 (6Ch)	SE2_RETUNE_C7	SE2_RETUNE_C7[15:0]																0000h
R109 (6Dh)	SE2_RETUNE_C8	SE2_RETUNE_C8[15:0]																0000h
R110 (6Eh)	SE2_RETUNE_C9	SE2_RETUNE_C9[15:0]																0000h
R111 (6Fh)	SE2_RETUNE_C10	SE2_RETUNE_C10[15:0]																0000h
R112 (70h)	SE2_RETUNE_C11	SE2_RETUNE_C11[15:0]																0000h
R113 (71h)	SE2_RETUNE_C12	SE2_RETUNE_C12[15:0]																0000h
R114 (72h)	SE2_RETUNE_C13	SE2_RETUNE_C13[15:0]																0000h
R115 (73h)	SE2_RETUNE_C14	SE2_RETUNE_C14[15:0]																0000h
R116 (74h)	SE2_RETUNE_C15	SE2_RETUNE_C15[15:0]																0000h
R117 (75h)	SE2_RETUNE_C16	SE2_RETUNE_C16[15:0]																0000h
R118 (76h)	SE2_RETUNE_C17	SE2_RETUNE_C17[15:0]																0000h
R119 (77h)	SE2_RETUNE_C18	SE2_RETUNE_C18[15:0]																0000h
R120 (78h)	SE2_RETUNE_C19	SE2_RETUNE_C19[15:0]																0000h
R121 (79h)	SE2_RETUNE_C20	SE2_RETUNE_C20[15:0]																0000h
R122 (7Ah)	SE2_RETUNE_C21	SE2_RETUNE_C21[15:0]																0000h
R123 (7Bh)	SE2_RETUNE_C22	SE2_RETUNE_C22[15:0]																0000h
R124 (7Ch)	SE2_RETUNE_C23	SE2_RETUNE_C23[15:0]																0000h
R125 (7Dh)	SE2_RETUNE_C24	SE2_RETUNE_C24[15:0]																0000h
R126 (7Eh)	SE2_RETUNE_C25	SE2_RETUNE_C25[15:0]																0000h
R127 (7Fh)	SE2_RETUNE_C26	SE2_RETUNE_C26[15:0]																0000h

REG	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DEFAULT
R128 (80h)	SE2_RETUNE_C27	SE2_RETUNE_C27[15:0]																0000h
R129 (81h)	SE2_RETUNE_C28	SE2_RETUNE_C28[15:0]																0000h
R130 (82h)	SE2_RETUNE_C29	SE2_RETUNE_C29[15:0]																0000h
R131 (83h)	SE2_RETUNE_C30	SE2_RETUNE_C30[15:0]																0000h
R132 (84h)	SE2_RETUNE_C31	SE2_RETUNE_C31[15:0]																0000h
R133 (85h)	SE2_5BEQ_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SE2_5BEQ_L_ENA	0000h
R134 (86h)	SE2_5BEQ_L10G	0	0	0	SE2_5BEQ_L1G[4:0]					0	0	0	SE2_5BEQ_L0G[4:0]					0C0Ch
R135 (87h)	SE2_5BEQ_L32G	0	0	0	SE2_5BEQ_L3G[4:0]					0	0	0	SE2_5BEQ_L2G[4:0]					0C0Ch
R136 (88h)	SE2_5BEQ_L4G	0	0	0	0	0	0	0	0	0	0	0	SE2_5BEQ_L4G[4:0]					000Ch
R137 (89h)	SE2_5BEQ_L0P	SE2_5BEQ_L0P[15:0]																00D8h
R138 (8Ah)	SE2_5BEQ_L0A	SE2_5BEQ_L0A[15:0]																0FCAh
R139 (8Bh)	SE2_5BEQ_L0B	SE2_5BEQ_L0B[15:0]																0400h
R140 (8Ch)	SE2_5BEQ_L1P	SE2_5BEQ_L1P[15:0]																01C5h
R141 (8Dh)	SE2_5BEQ_L1A	SE2_5BEQ_L1A[15:0]																1EB5h
R142 (8Eh)	SE2_5BEQ_L1B	SE2_5BEQ_L1B[15:0]																F145h
R143 (8Fh)	SE2_5BEQ_L1C	SE2_5BEQ_L1C[15:0]																0B75h
R144 (90h)	SE2_5BEQ_L2P	SE2_5BEQ_L2P[15:0]																0558h
R145 (91h)	SE2_5BEQ_L2A	SE2_5BEQ_L2A[15:0]																1C58h
R146 (92h)	SE2_5BEQ_L2B	SE2_5BEQ_L2B[15:0]																F373h
R147 (93h)	SE2_5BEQ_L2C	SE2_5BEQ_L2C[15:0]																0A54h
R148 (94h)	SE2_5BEQ_L3P	SE2_5BEQ_L3P[15:0]																1103h
R149 (95h)	SE2_5BEQ_L3A	SE2_5BEQ_L3A[15:0]																168Eh
R150 (96h)	SE2_5BEQ_L3B	SE2_5BEQ_L3B[15:0]																F829h
R151 (97h)	SE2_5BEQ_L3C	SE2_5BEQ_L3C[15:0]																07Adh
R152 (98h)	SE2_5BEQ_L4P	SE2_5BEQ_L4P[15:0]																4000h
R153 (99h)	SE2_5BEQ_L4A	SE2_5BEQ_L4A[15:0]																0564h
R154 (9Ah)	SE2_5BEQ_L4B	SE2_5BEQ_L4B[15:0]																0559h
R155 (9Bh)	SE2_5BEQ_R10G	0	0	0	SE2_5BEQ_R1G[4:0]					0	0	0	SE2_5BEQ_R0G[4:0]					0C0Ch
R156 (9Ch)	SE2_5BEQ_R32G	0	0	0	SE2_5BEQ_R3G[4:0]					0	0	0	SE2_5BEQ_R2G[4:0]					0C0Ch
R157 (9Dh)	SE2_5BEQ_R4G	0	0	0	0	0	0	0	0	0	0	0	SE2_5BEQ_R4G[4:0]					000Ch
R158 (9Eh)	SE2_5BEQ_R0P	SE2_5BEQ_R0P[15:0]																00D8h
R159 (9Fh)	SE2_5BEQ_R0A	SE2_5BEQ_R0A[15:0]																0FCAh
R160 (A0h)	SE2_5BEQ_R0B	SE2_5BEQ_R0B[15:0]																0400h
R161 (A1h)	SE2_5BEQ_R1P	SE2_5BEQ_R1P[15:0]																01C5h
R162 (A2h)	SE2_5BEQ_R1A	SE2_5BEQ_R1A[15:0]																1EB5h
R163 (A3h)	SE2_5BEQ_R1B	SE2_5BEQ_R1B[15:0]																F145h
R164 (A4h)	SE2_5BEQ_R1C	SE2_5BEQ_R1C[15:0]																0B75h
R165 (A5h)	SE2_5BEQ_R2P	SE2_5BEQ_R2P[15:0]																0558h
R166 (A6h)	SE2_5BEQ_R2A	SE2_5BEQ_R2A[15:0]																1C58h
R167 (A7h)	SE2_5BEQ_R2B	SE2_5BEQ_R2B[15:0]																F373h
R168 (A8h)	SE2_5BEQ_R2C	SE2_5BEQ_R2C[15:0]																0A54h
R169 (A9h)	SE2_5BEQ_R3P	SE2_5BEQ_R3P[15:0]																1103h
R170 (Aah)	SE2_5BEQ_R3A	SE2_5BEQ_R3A[15:0]																168Eh
R171 (Abh)	SE2_5BEQ_R3B	SE2_5BEQ_R3B[15:0]																F829h
R172 (Ach)	SE2_5BEQ_R3C	SE2_5BEQ_R3C[15:0]																07Adh
R173 (Adh)	SE2_5BEQ_R4P	SE2_5BEQ_R4P[15:0]																4000h
R174 (Aeh)	SE2_5BEQ_R4A	SE2_5BEQ_R4A[15:0]																0564h
R175 (Afh)	SE2_5BEQ_R4B	SE2_5BEQ_R4B[15:0]																0559h

REGISTER BITS BY ADDRESS

The complete register map is shown below. The detailed description can be found in the relevant text of the device description.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Software Reset/Chip ID 1	15:0	SW_RESET [15:0]	0110_0010_0010_1001	Writing to this register resets all registers to their default state. Reading from this register will indicate device family ID 6229h.	

Register 00h Software Reset/Chip ID 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Chip ID 2	3:0	CHIP_REV[3:0]	0000	Reading from this register will indicate the Revision ID.	

Register 01h Chip ID 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R2 (02h) Power management 1	13	INPPGAR_ENA	0	Right Input PGA Enable 0 = Disabled 1 = Enabled	
	12	INPPGAL_ENA	0	Left Input PGA Enable 0 = Disabled 1 = Enabled	
	11	ADCR_ENA	0	Right ADC Enable 0 = Disabled 1 = Enabled ADCR_ENA must be set to 1 when processing right channel data from the ADC or Digital Microphone.	
	10	ADCL_ENA	0	Left ADC Enable 0 = Disabled 1 = Enabled ADCL_ENA must be set to 1 when processing left channel data from the ADC or Digital Microphone.	
	7	DMIC_ENA	0	Enables Digital Microphone mode 0 = Audio DSP input is from ADC 1 = Audio DSP input is from digital microphone interface When DMIC_ENA = 0, the Digital microphone clock (DMICCLK) is held low.	
	4	MICB_ENA	0	Microphone Bias Enable 0 = Disabled 1 = Enabled	
	3	BIAS_ENA	0	Master Bias Enable 0 = Disabled 1 = Enabled	
	2	VMID_BUF_ENA	0	VMID Buffer Enable. (The buffered VMID may be applied to disabled input and output pins.) 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	VMID_SEL[1:0]	00	VMID Divider Enable and Select 00 = VMID disabled (for OFF mode) 01 = 2 x 50k divider (for normal operation) 10 = 2 x 250k divider (for low power standby) 11 = 2 x 5k divider (for fast start-up)	

Register 02h Power management 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R3 (03h) Power management 2	15	OUTR_ENA	0	LINEOUTR enable 0 = Disabled 1 = Enabled	
	14	OUTL_ENA	0	LINEOUTL enable 0 = Disabled 1 = Enabled	
	13	SPKR_PGA_ENA	0	Speaker Right PGA enable 0 = Disabled 1 = Enabled	
	12	SPKL_PGA_ENA	0	Speaker Left PGA enable 0 = Disabled 1 = Enabled	
	11	SPKR_SPKVDD_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_OP_ENA. When powering down SPKOUTR, the SPKR_SPKVDD_ENA bit should be reset first.	
	10	SPKL_SPKVDD_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_OP_ENA. When powering down SPKOUTL, the SPKL_SPKVDD_ENA bit should be reset first	
	9	SPKR_OP_MUTE	1	SPKOUTR Output Mute 0 = Disable Mute 1 = Enable Mute	
	8	SPKL_OP_MUTE	1	SPKOUTL Output Mute 0 = Disable Mute 1 = Enable Mute	
	7	SPKR_OP_ENA	0	SPKOUTR enable 0 = Disabled 1 = Enabled Note that SPKOUTR is also controlled by SPKR_SPKVDD_ENA. When powering up SPKOUTR, the SPKR_OP_ENA bit should be enabled first.	
	6	SPKL_OP_ENA	0	SPKOUTL enable 0 = Disabled 1 = Enabled Note that SPKOUTL is also controlled by SPKL_SPKVDD_ENA. When powering up SPKOUTL, the SPKL_OP_ENA bit should be enabled first	
	5	SPKR_MIX_MUTE	1	Right Speaker PGA Mixer Mute 0 = Disable Mute	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Enable Mute	
	4	SPKL_MIX_MUTE	1	Left Speaker PGA Mixer Mute 0 = Disable Mute 1 = Enable Mute	
	3	SPKR_MIX_ENA	0	Right speaker output mixer enable 0 = Disabled 1 = Enabled	
	2	SPKL_MIX_ENA	0	Left speaker output mixer enable 0 = Disabled 1 = Enabled	
	1	DACR_ENA	0	Right DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing right channel data from the DAC or Digital Beep Generator.	
	0	DACL_ENA	0	Left DAC Enable 0 = Disabled 1 = Enabled DACR_ENA must be set to 1 when processing left channel data from the DAC or Digital Beep Generator.	

Register 03h Power management 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R4 (04h) Audio Interface	15:14	DACDATA_PULL[1:0]	00	DACDAT pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	13:12	FRAME_PULL[1:0]	00	LRCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	11:10	BCLK_PULL[1:0]	00	BCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	9	ADCR_SRC	1	Right Digital Audio interface source 0 = Left ADC data is output on right channel 1 = Right ADC data is output on right channel	
	8	ADCL_SRC	0	Left Digital Audio interface source 0 = Left ADC data is output on left channel 1 = Right ADC data is output on left channel	
	7	DACR_SRC	1	Right DAC Data Source Select 0 = Right DAC outputs left interface data 1 = Right DAC outputs right interface data	
	6	DACL_SRC	0	Left DAC Data Source Select 0 = Left DAC outputs left interface data 1 = Left DAC outputs right interface data	
	5	BCLK_INV	0	BCLK Invert	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = BCLK not inverted 1 = BCLK inverted	
	4	LRCLK_INV	0	LRCLK Polarity / DSP Mode A-B select. Right, left and I2S modes – LRCLK polarity 0 = Not Inverted 1 = Inverted DSP Mode – Mode A-B select 0 = MSB is available on 2nd BCLK rising edge after LRCLK rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRCLK rising edge (mode B)	
	3:2	WL[1:0]	10	Digital Audio Interface Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits Note – see "Companding" for the selection of 8-bit mode.	
	1:0	FMT[1:0]	10	Digital Audio Interface Format 00 = Reserved 01 = Left Justified 10 = I2S format 11 = DSP/PCM mode	

Register 04h Audio Interface

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R5 (05h) Companding control	5	LOOPBACK	0	Digital Loopback Function 0 = No loopback 1 = Loopback enabled (ADC data output is directly input to DAC data input).	
	3	DAC_COMP	0	DAC Companding Enable 0 = Disabled 1 = Enabled	
	2	DAC_COMPMODE	0	DAC Companding Mode 0 = µ-law 1 = A-law	
	1	ADC_COMP	0	ADC Companding Enable 0 = Disabled 1 = Enabled	
	0	ADC_COMPMODE	0	ADC Companding Mode 0 = µ-law 1 = A-law	

Register 05h Companding control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R6 (06h) Clock Gen control	15	OSC_CLK_ENA	0	Oscillator Enable 0 = Disabled 1 = Enabled This needs to be set when a timeout clock is required for PGA zero cross or GPIO input detection	
	14:13	MCLK_PULL [1:0]	00	MCLK pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	12	CLKOUT_SEL	0	CLKOUT Source Select 0 = SYSCLK 1 = FLL or MCLK (set by SYSCLK_SRC register)	
	11:10	CLKOUT_DIV [1:0]	00	CLKOUT Clock divider 00 = divide by 1 01 = divide by 2 10 = divide by 4 11 = divide by 8	
	9	SYSCLK_ENA	0	SYSCLK Enable 0 = Disabled 1 = Enabled	
	8	SYSCLK_SRC	1	SYSCLK Source Select 0 = MCLK 1 = FLL output	
	7:5	SYSCLK_DIV [2:0]	000	SYSCLK Clock divider (Sets the scaling for either the MCLK or FLL clock output, depending on SYSCLK_SRC) 000 = divide by 1 001 = divide by 1.5 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12	
	4	TOCLK_ENA	0	TOCLK Enabled (Enables timeout clock for GPIO level detection, AMU, and PGA zero cross timeout) 0 = Disabled 1 = Enabled	
	3:1	BCLK_DIV[2:0]	011	BCLK Frequency (Master mode) 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 4 011 = SYSCLK / 8 100 = SYSCLK / 16 101 = SYSCLK / 32 110 = reserved 111 = reserved	
	0	MSTR	0	Digital Audio Interface Mode select 0 = Slave mode 1 = Master mode	

Register 06h Clock Gen control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R7 (07h) Additional control	11	VMID_FAST_START	0	VMID (fast-start) Enable 0 = Disabled 1 = Enabled	
	10	VMID_REF_SEL	0	VMID Source Select 0 = LDO supply (LDOVDD) 1 = LDO output (LDOVOUT)	
	9	VMID_CTRL	0	VMID Ratio control Sets the ratio of VMID to the source selected by VMID_REF_SEL 0 = 5/11 1 = 1/2	
	8	STARTUP_BIAS_ENA	0	Start-Up Bias Enable 0 = Disabled 1 = Enabled	
	7	BIAS_SRC	0	Bias Source select 0 = Normal bias 1 = Start-Up bias	
	6:5	VMID_RAMP [1:0]	00	VMID soft start enable / slew rate control 00 = Disabled 01 = Fast soft start 10 = Normal soft start 11 = Slow soft start	
	4	VMID_ENA	0	VMID Enable 0 = Disabled 1 = Enabled	
	3:0	SR[3:0]	1101	Audio Sample Rate select 0011 = 8kHz 0100 = 11.025kHz 0101 = 12kHz 0111 = 16kHz 1000 = 22.05kHz 1001 = 24kHz 1011 = 32kHz 1100 = 44.1kHz 1101 = 48kHz	

Register 07h Additional control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R8 (08h) FLL Control 1	12:11	FLL_CLK_REF_DIV[1:0]	00	FLL Clock Reference Divider 00 = MCLK / 1 01 = MCLK / 2 10 = MCLK / 4 11 = MCLK / 8 MCLK (or other input reference) must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10:8	FLL_OUTDIV [2:0]	001	FOUT clock divider 000 = 2 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 111 = 256 (FOUT = FVCO / FLL_OUTDIV)	
	7:5	FLL_CTRL_RATE[2:0]	000	Frequency of the FLL control block 000 = FVCO / 1 (Recommended value) 001 = FVCO / 2 010 = FVCO / 3 011 = FVCO / 4 100 = FVCO / 5 101 = FVCO / 6 110 = FVCO / 7 111 = FVCO / 8 Recommended that this register is not changed from default.	
	4:2	FLL_FRATIO [2:0]	000	FVCO clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for FREF > 1MHz 100 recommended for FREF < 16kHz 011 recommended for all other cases	
	1	FLL_FRAC	1	Fractional enable 0 = Integer Mode 1 = Fractional Mode Integer mode offers reduced power consumption. Fractional mode offers best FLL performance, provided also that N.K is a non-integer value.	
	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled	

Register 08h FLL Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R9 (09h) FLL Control 2	15:0	FLL_K[15:0]	0011_0001_0010_0111	Fractional multiply for FREF (MSB = 0.5)	

Register 09h FLL Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R10 (0Ah) FLL Control 3	14:5	FLL_N[9:0]	00_0000_1000	Integer multiply for FREF (LSB = 1)	
	3:0	FLL_GAIN[3:0]	0100	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1000 = x 256 Recommended that this register is not changed from default.	

Register 0Ah FLL Control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R11 (0Bh) GPIO Config	0	MODE_GPIO	0	CIFMODE/GPIO3 pin configuration 0 = Pin configured as CIFMODE 1 = Pin configured as GPIO3 Note – when this bit is set to 1, it is latched and cannot be reset until Power-Off or Software Reset.	

Register 0Bh GPIO Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R12 (0Ch) GPIO1 Control	15	GP1_DIR	1	GPIO1 Pin Direction 0 = Output 1 = Input	
	14:13	GP1_PULL[1:0]	00	GPIO1 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	12	GP1_INT_MODE	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=0) or falling edge triggered (if GP1_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP1_POL	0	GPIO1 Polarity Select 0 = Non-inverted 1 = Inverted	
	5	GP1_LVL	0	GPIO1 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is set, the register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP1_FN[3:0]	0000	GPIO1 Pin Function 0000 = Logic Level Input 0001 = Edge Detection Input 0010 = CLKOUT output 0011 = Interrupt (IRQ) output 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Temperature flag output 1000 = Reserved 1001 = DMICCLK output 1010 = Logic Level output 1011 = LDO_UV output 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved	

Register 0Ch GPIO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R13 (0Dh) GPIO2 Control	15	GP2_DIR	1	GPIO2 Pin Direction 0 = Output 1 = Input	
	14:13	GP2_PULL[1:0]	00	GPIO2 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	12	GP2_INT_MODE	0	GPIO2 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP2_POL=0) or falling edge triggered (if GP2_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP2_POL	0	GPIO2 Polarity Select 0 = Non-inverted 1 = Inverted	
	5	GP2_LVL	0	GPIO2 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP2_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP2_FN[3:0]	0000	GPIO2 Pin Function 0000 = Logic Level Input 0001 = Edge Detection Input 0010 = CLKOUT output 0011 = Interrupt (IRQ) output 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Temperature flag output 1000 = Reserved 1001 = DMICCLK output 1010 = Logic Level output 1011 = LDO_UV output 1100 = Reserved 1101 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1110 = Reserved 1111 = Reserved	

Register 0Dh GPIO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R14 (0Eh) GPIO3 Control	15	GP3_DIR	1	GPIO3 Pin Direction 0 = Output 1 = Input	
	14:13	GP3_PULL[1:0]	10	GPIO3 pull-up / pull-down Enable 00 = no pull-up or pull-down 01 = pull-down 10 = pull-up 11 = reserved	
	12	GP3_INT_MODE	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=0) or falling edge triggered (if GP3_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP3_POL	0	GPIO3 Polarity Select 0 = Non-inverted 1 = Inverted	
	5	GP3_LVL	0	GPIO3 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP3_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP3_FN[3:0]	0000	GPIO3 Pin Function 0000 = Logic Level Input 0001 = Edge Detection Input 0010 = CLKOUT output 0011 = Interrupt (IRQ) output 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Temperature flag output 1000 = Reserved 1001 = DMICCLK output 1010 = Logic Level output 1011 = LDO_UV output 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved	

Register 0Eh GPIO3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R15 (0Fh) GPIO4 Control	15	GP4_DIR	1	GPIO4 Pin Direction 0 = Output 1 = Input	
	14:13	GP4_PULL[1:0]	00	GPIO4 pull-up / pull-down Enable 00 = no pull-up or pull-down	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				01 = pull-down 10 = pull-up 11 = reserved	
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=0) or falling edge triggered (if GP4_POL =1) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP4_POL	0	GPIO4 Polarity Select 0 = Non-inverted 1 = Inverted	
	5	GP4_LVL	0	GPIO4 level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP4_POL is set, the register contains the opposite logic level to the external pin.	
	3:0	GP4_FN[3:0]	0000	GPIO4 Pin Function 0000 = Logic Level Input 0001 = Edge Detection Input 0010 = CLKOUT output 0011 = Interrupt (IRQ) output 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Temperature flag output 1000 = Reserved 1001 = DMICCLK output 1010 = Logic Level output 1011 = LDO_UV output 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved	

Register 0Fh GPIO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16 (10h) System Interrupts	15	TEMP_INT	0	Thermal Interrupt status 0 = Thermal interrupt not set 1 = Thermal interrupt set This bit is latched when set; it is cleared when the register is Read.	
	14	GP4_INT	0	GPIO4 Interrupt status 0 = GPIO4 interrupt not set 1 = GPIO4 interrupt set This bit is latched when set; it is cleared when the register is Read.	
	13	GP3_INT	0	GPIO3 Interrupt status 0 = GPIO3 interrupt not set 1 = GPIO3 interrupt set This bit is latched when set; it is cleared when the register is Read.	
	12	GP2_INT	0	GPIO2 Interrupt status 0 = GPIO2 interrupt not set	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = GPIO2 interrupt set This bit is latched when set; it is cleared when the register is Read.	
	11	GP1_INT	0	GPIO1 Interrupt status 0 = GPIO1 interrupt not set 1 = GPIO1 interrupt set This bit is latched when set; it is cleared when the register is Read.	
	0	LDO_UV_INT	0	LDO Undervoltage Interrupt 0 = LDO Undervoltage interrupt not set 1 = LDO Undervoltage interrupt set This bit is latched when set; it is cleared when the register is Read.	

Register 10h System Interrupts

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R17 (11h) Status Flags	15	TEMP_STS	0	Thermal Sensor status 0 = Normal 1 = Overtemperature	
	0	LDO_UV_STS	0	LDO Undervoltage status 0 = Normal 1 = Undervoltage	

Register 11h Status Flags

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R18 (12h) IRQ Config	0	IM_IRQ	1	IRQ (GPIO output) Mask 0 = Normal 1 = IRQ output is masked	

Register 12h IRQ Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R19 (13h) System Interrupts Mask	15	IM_TEMP_INT	0	Interrupt mask for thermal status 0 = Not masked 1 = Masked	
	14	IM_GP4_INT	0	Interrupt mask for GPIO4 0 = Not masked 1 = Masked	
	13	IM_GP3_INT	0	Interrupt mask for GPIO3 0 = Not masked 1 = Masked	
	12	IM_GP2_INT	0	Interrupt mask for GPIO2 0 = Not masked 1 = Masked	
	11	IM_GP1_INT	0	Interrupt mask for GPIO1 0 = Not masked 1 = Masked	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	IM_LDO_UV_INT	0	Interrupt mask for LDO Undervoltage status 0 = Not masked 1 = Masked	

Register 13h System Interrupts Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R20 (14h) Control Interface	2	SPI_OD	0	SDOUT pin configuration (applies to 3-wire and 4-wire mode only)0 = SDOUT output is CMOS 1 = SDOUT output is open drain	
	1	SPI_4WIRE	1	SPI control mode select 0 = 3-wire using bidirectional SDA 1 = 4-wire using SDOUT	
	0	AUTO_INC	0	Enables address auto-increment (applies to 2-wire / I2C mode only) 0 = Disabled 1 = Enabled	

Register 14h Control Interface

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R21 (15h) DAC Control 1	8	DAC_MUTEALL	1	DAC Digital Mute for All Channels: 0 = Disable Mute 1 = Enable Mute on all channels	
	4	DAC_AUTOMUTE	1	DAC Auto-Mute Control 0 = Disabled 1 = Enabled	
	1	DACR_DATINV	0	Right DAC Invert 0 = Right DAC output not inverted 1 = Right DAC output inverted	
	0	DACL_DATINV	0	Left DAC Invert 0 = Left DAC output not inverted 1 = Left DAC output inverted	

Register 15h DAC Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R22 (16h) DAC Control 2	4	DAC_VOL_RAMP	1	DAC Volume Ramp control 0 = Disabled 1 = Enabled	
	0	DAC_SB_FLT	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode	

Register 16h DAC Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R23 (17h) Left DAC digital Vol	12	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause Left and Right DAC volume to be updated simultaneously	
	8	DACL_MUTE	0	Left DAC Digital Mute 0 = Disable Mute 1 = Enable Mute	
	7:0	DACL_VOL [7:0]	1100_0000	Left DAC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB	

Register 17h Left DAC digital Vol

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R24 (18h) Right DAC digital Vol	12	DAC_VU	0	DAC Volume Update Writing a 1 to this bit will cause Left and Right DAC volume to be updated simultaneously	
	8	DACR_MUTE	0	Right DAC Digital Mute 0 = Disable Mute 1 = Enable Mute	
	7:0	DACR_VOL [7:0]	1100_0000	Right DAC volume control 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB	

Register 18h Right DAC digital Vol

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R25 (19h) ADC Control 1	8	ADC_MUTEALL	1	ADC Digital Mute for All Channels 0 = Disable Mute 1 = Enable Mute on all channels	
	1	ADCR_DATINV	0	Right ADC Invert 0 = Right ADC output not inverted 1 = Right ADC output inverted	
	0	ADCL_DATINV	0	Left ADC Invert 0 = Left ADC output not inverted 1 = Left ADC output inverted	

Register 19h ADC Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R26 (1Ah) ADC Control 2	2:1	ADC_HPF_CUT[1:0]	00	High pass filter configuration. 00 = 1st order HPF (fc=4Hz at fs=48kHz) 01 = 2nd order HPF (fc=122Hz at fs=48kHz) 10 = 2nd order HPF (fc=153Hz at fs=48kHz) 11 = 2nd order HPF (fc=196Hz at fs=48kHz)	Table 11
	0	ADC_HPF	0	ADC Digital High Pass Filter Enable 0 = Disabled 1 = Enabled	

Register 1Ah ADC Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R27 (1Bh) Left ADC Digital Vol	12	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause Left and Right ADC volume to be updated simultaneously	
	8	ADCL_MUTE	0	Left ADC Digital Mute 0 = Disable Mute 1 = Enable Mute	
	7:0	ADCL_VOL [7:0]	1100_0000	Left ADC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB	

Register 1Bh Left ADC Digital Vol

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R28 (1Ch) Right ADC Digital Vol	12	ADC_VU	0	ADC Volume Update Writing a 1 to this bit will cause Left and Right ADC volume to be updated simultaneously	
	8	ADCR_MUTE	0	Right ADC Digital Mute 0 = Disable Mute 1 = Enable Mute	
	7:0	ADCR_VOL [7:0]	1100_0000	Right ADC Digital Volume 0000_0000 = mute 0000_0001 = -71.625dB 0000_0010 = -71.250dB … 1100_0000 = 0dB ... 1111_1111 = +23.625dB	

Register 1Ch Right ADC Digital Vol

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R29 (1Dh) DRC Control 1	8	DRC_NG_ENA	0	DRC Noise Gate Enable 0 = Disabled 1 = Enabled	
	7	DRC_ENA	0	DRC Enable 0 = Disabled 1 = Enabled	
	2	DRC_QR	1	DRC Quick-release Enable 0 = Disabled 1 = Enabled	
	1	DRC_ANTICLIP	1	DRC Anti-clip Enable 0 = Disabled 1 = Enabled	

Register 1Dh DRC Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30 (1Eh) DRC Control 2	12:9	DRC_NG_MINGAIN[3:0]	0110	Minimum gain the DRC can use to attenuate audio signals when the noise gate is active. 0000 = -36dB 0001 = -30dB 0010 = -24dB 0011 = -18dB 0100 = -12dB 0101 = -6dB 0110 = 0dB 0111 = 6dB 1000 = 12dB 1001 = 18dB 1010 = 24dB 1011 = 30dB 1100 = 36dB 1101 to 1111 = Reserved	
	4:2	DRC_MINGAIN[2:0]	001	Minimum gain the DRC can use to attenuate audio signals 000 = 0dB 001 = -12dB (default) 010 = -18dB 011 = -24dB 100 = -36dB 101 = Reserved 11X = Reserved	
	1:0	DRC_MAXGAIN[1:0]	01	Maximum gain the DRC can use to boost audio signals (dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 36dB	

Register 1Eh DRC Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R31 (1Fh) DRC Control 3	7:4	DRC_ATK[3:0]	0100	Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 181us 0010 = 363us 0011 = 726us 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011 = 185.6ms 1100-1111 = Reserved	
	3:0	DRC_DCY[3:0]	0010	Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved	

Register 1Fh DRC Control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R32 (20h) DRC Control 4	12:8	DRC_KNEE2_IP [4:0]	0_0000	Input signal level at the Noise Gate threshold 'Knee2'. 00000 = -36dB 00001 = -37.5dB 00010 = -39dB … (-1.5dB steps) 11110 = -81dB 11111 = -82.5dB Only applicable when DRC_NG_ENA = 1.	
	7:2	DRC_KNEE_IP[5:0]	00_0000	Input signal level at the Compressor 'Knee1'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 = Reserved 11111X = Reserved	

Register 20h DRC Control 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R33 (21h) DRC Control 5	13	DRC_KNEE2_OP_ENA	0	DRC_KNEE2_OP Enable 0 = Disabled 1 = Enabled	
	12:8	DRC_KNEE2_OP[4:0]	0_0000	Output signal at the Noise Gate threshold 'Knee2'. 00000 = -30dB 00001 = -31.5dB 00010 = -33dB … (-1.5dB steps) 11110 = -75dB 11111 = -76.5dB Only applicable when DRC_KNEE2_OP_ENA = 1.	
	7:3	DRC_KNEE_OP[4:0]	0_0000	Output signal at the Compressor 'Knee1'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved	
	2:0	DRC_HI_COMP[2:0]	011	Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 = Reserved 111 = Reserved	

Register 21h DRC Control 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R34 (22h) DRC Control 6	3:2	DRC_QR_THR[1:0]	00	DRC Quick-release threshold (crest factor in dB) 00 = 12dB 01 = 18dB 10 = 24dB 11 = 30dB	
	1:0	DRC_QR_DCY[1:0]	00	DRC Quick-release decay rate (seconds/6dB) 00 = 0.725ms 01 = 1.45ms 10 = 5.8ms 11 = reserved	

Register 22h DRC Control 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R35 (23h) DRC Control 7	9:8	DRC_NG_EXP[1:0]	00	Noise Gate slope 00 = 1 (no expansion) 01 = 2 10 = 4 11 = 8	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:5	DRC_LO_COMP[2:0]	000	Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 = Reserved 11X = Reserved	
	4:0	DRC_INIT	00000	Initial value at DRC startup 00000 = 0dB 00001 = -3.75dB … (-3.75dB steps) 11111 = -116.25dB	

Register 23h DRC Control 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R36 (24h) DRC Status	15:0	DRC_GAIN [15:0]	0000_0000_0000_0000	DRC Gain value. This is the DRC gain, expressed as a voltage multiplier. Fixed point coding, MSB = 64. The first 7 bits are the integer portion; the remaining bits are the fractional part.	

Register 24h DRC Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R37 (25h) Beep Control 1	6:3	BEEP_GAIN [3:0]	0000	Digital Beep Volume Control 0000 = mute 0001 = -83dB 0010 = -77dB … (6dB steps) 1111 = +1dB	
	2:1	BEEP_RATE [1:0]	01	Beep Waveform Control 00 = Reserved 01 = 1kHz 10 = 2kHz 11 = 4kHz	
	0	BEEP_ENA	0	Digital Beep Enable 0 = Disabled 1 = Enabled Note that the DAC and associated signal path needs to be enabled when using the digital beep.	

Register 25h Beep Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R38 (26h) Video Buffer	7	VB_ENA	0	Video buffer enable 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6	VB_QBOOST	0	Video buffer filter Q-Boost control 0 = Disabled 1 = Enabled	
	5	VB_GAIN	0	Video buffer gain 0 = 0dB (=6dB unloaded) 1 = 6dB (=12dB unloaded)	
	4:2	VB_DISOFF [2:0]	111	Video buffer DC offset control 000 = Reserved 001 = 40mV offset 010 = Reserved 011 = 20mV offset 100 = Reserved 101 = Reserved 110 = Reserved 111 = 0mV offset Note – the specified offset applies to the 0dB gain setting (VB_GAIN=0). When 6dB gain is selected, the DC offset is doubled.	
	1	VB_PD	0	Video buffer pull-down 0 = pull-down disabled 1 = pull-down enabled	
	0	VB_CLAMP	0	Enable the clamp between the video input and ground 0 = no clamp 1 = Video buffer input is clamped to ground	

Register 26h Video Buffer

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R39 (27h) Input ctrl	8	AUX2_AUDIO	0	AUX2 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal	
	7	AUX1_AUDIO	0	AUX1 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal	
	6	MICB_LVL	0	Microphone Bias Voltage control 0 = 0.9 x LDOVOUT 1 = 0.65 x LDOVOUT	
	5	MICRN_TO_N_PGAR	1	Right Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2R	
	4	MICLN_TO_N_PGAL	1	Left Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2L	
	3:2	P_PGAR_SEL [1:0]	01	Right Input PGA Non-Inverting Input Select 00 = Connected to IN2R 01 = Connected to IN1R 10 = Connected to AUX2 11 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	P_PGAL_SEL [1:0]	01	Left Input PGA Non-Inverting Input Select 00 = Connected to IN2L 01 = Connected to IN1L 10 = Connected to AUX1 11 = Reserved	

Register 27h Input ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R40 (28h) Left INP PGA gain ctrl	8	PGA_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause the Left and Right Input PGA volumes to be updated simultaneously.	
	7	PGAL_ZC	0	Left Input PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	PGAL_MUTE	1	Left Input PGA Mute 0 = Disable Mute 1 = Enable Mute	
	5:0	PGAL_VOL[5:0]	01_0000	Left Input PGA Volume 00_0000 = -12dB 00_0001 = -11.25dB … 01_0000 = 0dB ... 11_1111 = +35.25	

Register 28h Left INP PGA gain ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R41 (29h) Right INP PGA gain ctrl	8	PGA_VU	0	Input PGA Volume Update Writing a 1 to this bit will cause the Left and Right Input PGA volumes to be updated simultaneously.	
	7	PGAR_ZC	0	Right Input PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	PGAR_MUTE	1	Right Input PGA Mute 0 = Disable Mute 1 = Enable Mute	
	5:0	PGAR_VOL[5:0]	01_0000	Right Input PGA Volume 00_0000 = -12dB 00_0001 = -11.25dB … 01_0000 = 0dB ... 11_1111 = +35.25	

Register 29h Right INP PGA gain ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R42 (2Ah) Output ctrl	15	THERR_ACT	1	Thermal Shutdown enable 0 = Disabled 1 = Enabled When THERR_ACT = 1, then an overtemperature condition will cause the speaker outputs to be disabled.	
	13	SPKR_VMID_OP_ENA	0	Buffered VMID to SPKOUTR Enable 0 = Disabled 1 = Enabled	
	12	SPKL_VMID_OP_ENA	0	Buffered VMID to SPKOUTL Enable 0 = Disabled 1 = Enabled	
	11	LINER_VMID_OP_ENA	0	Buffered VMID to LINEOUTR Enable 0 = Disabled 1 = Enabled	
	10	LINEL_VMID_OP_ENA	0	Buffered VMID to LINEOUTL Enable 0 = Disabled 1 = Enabled	
	9	LINER_MUTE	1	LINEOUTR Output Mute 0 = Disable Mute 1 = Enable Mute	
	8	LINEL_MUTE	1	LINEOUTL Output Mute 0 = Disable Mute 1 = Enable Mute	
	7	SPKR_DISCH	0	Discharges SPKOUTR output via approx 4k resistor 0 = Not active 1 = Actively discharging SPKOUTR	
	6	SPKL_DISCH	0	Discharges SPKOUTL output via approx 4k resistor 0 = Not active 1 = Actively discharging SPKOUTL	
	5	LINER_DISCH	0	Discharges LINEOUTR output via approx 4k resistor 0 = Not active 1 = Actively discharging LINEOUTR	
	4	LINEL_DISCH	0	Discharges LINEOUTL output via approx 4k resistor 0 = Not active 1 = Actively discharging LINEOUTL	
	1	SPK_VROI	0	Buffered VREF to SPKOUTL / SPKOUTR resistance (Disabled outputs) 0 = approx 20k 1 = approx 1k	
	0	LINE_VROI	0	Buffered VREF to LINEOUTL / LINEOUTR resistance (Disabled outputs) 0 = approx 20k 1 = approx 1k	

Register 2Ah Output ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R43 (2Bh) SPK mixer control1	8	AUX1_TO_SPKL	0	AUX1 Audio Input to Left Speaker Output select 0 = Disabled 1 = Enabled	
	7	PGAL_TO_SPKL	0	Left Speaker PGA Mixer to Left Speaker Output select 0 = Disabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Enabled	
	6	BYPL_TO_PGAL	0	Left Input PGA (ADC bypass) to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	5	MDACL_TO_PGAL	0	Inverted Left DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	4	MDACR_TO_PGAL	0	Inverted Right DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	3	DACL_TO_PGAL	0	Left DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	2	DACR_TO_PGAL	0	Right DAC to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	1	AUX2_TO_PGAL	0	AUX2 Audio Input to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	0	AUX1_TO_PGAL	0	AUX1 Audio Input to Left Speaker PGA Mixer select 0 = Disabled 1 = Enabled	

Register 2Bh SPK mixer control1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R44 (2Ch) SPK mixer control2	8	AUX1_TO_SPKR	0	AUX1 Audio Input to Right Speaker Output select 0 = Disabled 1 = Enabled	
	7	PGAR_TO_SPKR	0	Right Speaker PGA Mixer to Right Speaker Output select 0 = Disabled 1 = Enabled	
	6	BYPR_TO_PGAR	0	Right Input PGA (ADC bypass) to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	5	MDACL_TO_PGAR	0	Inverted Left DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	4	MDACR_TO_PGAR	0	Inverted Right DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	3	DACL_TO_PGAR	0	Left DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	2	DACR_TO_PGAR	0	Right DAC to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	
	1	AUX2_TO_PGAR	0	AUX2 Audio Input to Right Speaker PGA Mixer select 0 = Disabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = Enabled	
	0	AUX1_TO_PGA R	0	AUX1 Audio Input to Right Speaker PGA Mixer select 0 = Disabled 1 = Enabled	

Register 2Ch SPK mixer control2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R45 (2Dh) SPK mixer control3	8	AUX1_TO_SPK L_ATTEN	0	AUX1 Audio Input to Left Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation	
	7	PGAL_TO_SPK L_ATTEN	0	Left Speaker PGA Mixer to Left Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation	
	6	BYPL_TO_PGA L_ATTEN	0	Left Input PGA (ADC bypass) to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	3	DACL_TO_PGA L_ATTEN	0	Left DAC to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	2	DACR_TO_PGA L_ATTEN	0	Right DAC to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	1	AUX2_TO_PGA L_ATTEN	0	AUX2 Audio Input to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	0	AUX1_TO_PGA L_ATTEN	0	AUX1 Audio Input to Left Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	

Register 2Dh SPK mixer control3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R46 (2Eh) SPK mixer control4	8	AUX1_TO_SPK R_ATTEN	0	AUX1 Audio Input to Right Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation	
	7	PGAR_TO_SPK R_ATTEN	0	Right Speaker PGA Mixer to Right Speaker Output attenuation 0 = 0dB 1 = -6dB attenuation	
	6	BYPR_TO_PGA R_ATTEN	0	Right Input PGA (ADC bypass) to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	3	DACL_TO_PGA R_ATTEN	0	Left DAC to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	2	DACR_TO_PGA R_ATTEN	0	Right DAC to Right Speaker PGA Mixer attenuation 0 = 0dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1 = -6dB attenuation	
	1	AUX2_TO_PGA R_ATTEN	0	AUX2 Audio Input to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	0	AUX1_TO_PGA R_ATTEN	0	AUX1 Audio Input to Right Speaker PGA Mixer attenuation 0 = 0dB 1 = -6dB attenuation	

Register 2Eh SPK mixer control4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R47 (2Fh) Left SPK volume ctrl	8	SPK_VU	0	Speaker PGA Volume Update Writing a 1 to this bit will cause the Left and Right Speaker PGA volumes to be updated simultaneously.	
	7	SPKL_ZC	0	Left Speaker PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	SPKL_PGA_MU TE	1	Left Speaker PGA Mute 0 = Disable Mute 1 = Enable Mute	
	5:0	SPKL_VOL[5:0]	11_1001	Left Speaker PGA Volume 00_0000 = -57dB gain 00_0001 = -56dB … 11_1001 = 0dB ... 11_1111 = +6dB	

Register 2Fh Left SPK volume ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R48 (30h) Right SPK volume ctrl	8	SPK_VU	0	Speaker PGA Volume Update Writing a 1 to this bit will cause the Left and Right Speaker PGA volumes to be updated simultaneously.	
	7	SPKR_ZC	0	Right Speaker PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only	
	6	SPKR_PGA_MU TE	1	Right Speaker PGA Mute 0 = Disable Mute 1 = Enable Mute	
	5:0	SPKR_VOL[5:0]	11_1001	Right Speaker PGA Volume 00_0000 = -57dB gain 00_0001 = -56dB … 11_1001 = 0dB ... 11_1111 = +6dB	

Register 30h Right SPK volume ctrl

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R49 (31h) Line L mixer control 1	6	BYPL_TO_OUTL	0	Left Input PGA (ADC bypass) to Left Output Mixer select 0 = Disabled 1 = Enabled	
	5	MDACL_TO_OUTL	0	Inverted Left DAC to Left Output Mixer select 0 = Disabled 1 = Enabled	
	4	MDACR_TO_OUTL	0	Inverted Right DAC to Left Output Mixer select 0 = Disabled 1 = Enabled	
	3	DACL_TO_OUTL	0	Left DAC to Left Output Mixer select 0 = Disabled 1 = Enabled	
	2	DACR_TO_OUTL	0	Right DAC to Left Output Mixer select 0 = Disabled 1 = Enabled	
	1	AUX2_TO_OUTL	0	AUX2 Audio Input to Left Output Mixer select 0 = Disabled 1 = Enabled	
	0	AUX1_TO_OUTL	0	AUX1 Audio Input to Left Output Mixer select 0 = Disabled 1 = Enabled	

Register 31h Line L mixer control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R50 (32h) Line R mixer control 1	6	BYPR_TO_OUTR	0	Right Input PGA (ADC bypass) to Right Output Mixer select 0 = Disabled 1 = Enabled	
	5	MDACL_TO_OUTR	0	Inverted Left DAC to Right Output Mixer select 0 = Disabled 1 = Enabled	
	4	MDACR_TO_OUTR	0	Inverted Right DAC to Right Output Mixer select 0 = Disabled 1 = Enabled	
	3	DACL_TO_OUTR	0	Left DAC to Right Output Mixer select 0 = Disabled 1 = Enabled	
	2	DACR_TO_OUTR	0	Right DAC to Right Output Mixer select 0 = Disabled 1 = Enabled	
	1	AUX2_TO_OUTR	0	AUX2 Audio Input to Right Output Mixer select 0 = Disabled 1 = Enabled	
	0	AUX1_TO_OUTR	0	AUX1 Audio Input to Right Output Mixer select 0 = Disabled 1 = Enabled	

Register 32h Line R mixer control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R51 (33h) Line L mixer control 2	6	BYPL_TO_OUT L_ATTEN	0	Left Input PGA (ADC bypass) to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	3	DACL_TO_OUT L_ATTEN	0	Left DAC to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	2	DACR_TO_OUT L_ATTEN	0	Right DAC to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	1	AUX2_TO_OUT L_ATTEN	0	AUX2 Audio Input to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	0	AUX1_TO_OUT L_ATTEN	0	AUX1 Audio Input to Left Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	

Register 33h Line L mixer control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R52 (34h) Line R mixer control 2	6	BYPR_TO_OUT R_ATTEN	0	Right Input PGA (ADC bypass) to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	3	DACL_TO_OUT R_ATTEN	0	Left DAC to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	2	DACR_TO_OUT R_ATTEN	0	Right DAC to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	1	AUX2_TO_OUT R_ATTEN	0	AUX2 Audio Input to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	
	0	AUX1_TO_OUT R_ATTEN	0	AUX1 Audio Input to Right Output Mixer attenuation 0 = 0dB 1 = -6dB attenuation	

Register 34h Line R mixer control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R53 (35h) LDO	15	LDO_ENA	0	LDO Enable 0 = Disabled 1 = Enabled	
	14	LDO_REF_SEL _FAST	0	LDO Voltage reference select 0 = VMID (normal) 1 = VMID (fast start) This field is only effective when LDO_REF_SEL = 0	
	13	LDO_REF_SEL	0	LDO Voltage reference select 0 = VMID 1 = Bandgap	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12	LDO_OPFLT	0	LDO Output float 0 = Disabled (Output discharged when disabled) 1 = Enabled (Output floats when disabled)	
	5	LDO_BIAS_SRC	0	LDO Bias Source select 0 = Master Bias 1 = Start-Up Bias	
	4:0	LDO_VSEL [4:0]	0_0111	LDO Voltage select (Sets the LDO output as a ratio of the selected voltage reference. The voltage reference is set by LDO_REF_SEL.) 00111 = Vref x 1.97 (default)	

Register 35h LDO

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R54 (36h) Bandgap	15	BG_ENA	0	Bandgap Reference Control 0 = Disabled 1 = Enabled	
	4:0	BG_VSEL[4:0]	0_1010	Bandgap Voltage select (Sets the Bandgap voltage) 00000 = 1.200V … 26.7mV steps 01010 = 1.467V (default) … 01111 = 1.600V 10000 to 11111 = reserved (See Table 43 for values)	

Register 36h Bandgap

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R64 (40h) SE Config Selection	3:0	SE_CONFIG [3:0]	0000	DSP Configuration Mode select 0000 = Record mode 0001 = Playback mode 0010 = Reserved 0011 = Reserved	

Register 40h SE Config Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R65 (41h) SE1_LHPF_CONFIG	5	SE1_LHPF_R_SIGN	0	SE1_LHPF_R_SIGN 0 : sum internal result (LPF) 1 : sub internal result (HPF)	
	4	SE1_LHPF_L_SIGN	0	SE1_LHPF_L_SIGN 0 : sum internal result (LPF) 1 : sub internal result (HPF)	
	1	SE1_LHPF_R_ENA	0	SE1 Right channel low-pass / high-pass filter enable 0 = Disabled 1 = Enabled	
	0	SE1_LHPF_L_E	0	SE1 Left channel low-pass / high-pass filter enable	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
		NA		0 = Disabled 1 = Enabled	

Register 41h SE1_LHPF_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R66 (42h) SE1_LHPF_L	15:0	SE1_LHPF_L [15:0]	0000_0000_0000_0000	SE1_LHPF left channel coefficient	

Register 42h SE1_LHPF_L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R67 (43h) SE1_LHPF_R	15:0	SE1_LHPF_R [15:0]	0000_0000_0000_0000	SE1_LHPF right channel coefficient	

Register 43h SE1_LHPF_R

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R68 (44h) SE1_3D_CONFIG	12	SE1_3D_MONO	0	SE1_3D_MONO : 0 : L, R configs active 1 : L config applied to both L and R	
	9	SE1_3D_R_SIGN	0	SE1_3D_R_SIGN 0 : add cross path values 1 : sub cross path values	
	8	SE1_3D_L_SIGN	0	SE1_3D_L_SIGN 0 : add cross path values 1 : sub cross path values	
	7	SE1_3D_LHPF_R_ENA	0	SE1_3D_LHPF_R_ENA : 0 : R channel disabled (bypass coeffs applied) 1 : R channel enabled (bank coeffs applied)	
	6	SE1_3D_LHPF_L_ENA	0	SE1_3D_LHPF_L_ENA : 0 : L channel disabled (bypass coeffs applied) 1 : L channel enabled (bank coeffs applied)	
	5	SE1_3D_R_LHPF_SIGN	0	SE1_3D_R_LHPF_SIGN 0 : sum internal result (LPF) 1 : sub internal result (HPF)	
	4	SE1_3D_L_LHPF_SIGN	0	SE1_3D_L_LHPF_SIGN 0 : sum internal result (LPF) 1 : sub internal result (HPF)	
	1	SE1_3D_R_ENA	0	SE1 Right channel 3D stereo enhancement filter enable 0 = Disabled 1 = Enabled	
	0	SE1_3D_L_ENA	0	SE1 Left channel 3D stereo enhancement filter enable 0 = Disabled 1 = Enabled	

Register 44h SE1_3D_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R69 (45h) SE1_3D_L	13:11	SE1_3D_L_DELAY[2:0]	000	Sets the number of delay samples: 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4	
	10:8	SE1_3D_L_CUTOFF[2:0]	100	Cut Off Frequency 0000 = 50Hz 0001 = 100Hz 0010 = 200Hz 0011 = 400 Hz 0100 = 1KHz 0101 = 2KHz 0110 = 4KHz 0111 = 10KHz 1000 to 1111 = reserved	
	7:4	SE1_3D_L_CGAIN[3:0]	0000	SE1 3D Left Channel cross gain setting 0000 = -12dB 0001 = -10.5db ……. 1000= 0dB 1001 to 1111 = reserved	
	3:0	SE1_3D_L_FGAIN[3:0]	1000	SE1 3D Left Channel forward gain setting 0000 = -12dB 0001 = -10.5db ……. 1000= 0dB 1001 to 1111 = reserved	

Register 45h SE1_3D_L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R70 (46h) SE1_3D_R	13:11	SE1_3D_R_DELAY[2:0]	000	Sets the number of delay samples: 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4	
	10:8	SE1_3D_R_CUTOFF[2:0]	100	Cut Off Frequency 0000 = 50Hz 0001 = 100Hz 0010 = 200Hz 0011 = 400 Hz 0100 = 1KHz 0101 = 2KHz 0110 = 4KHz 0111 = 10KHz 1000 to 1111 = reserved	
	7:4	SE1_3D_R_CGAIN[3:0]	0000	SE1 3D Right Channel cross gain setting 0000 = -12dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0001 = -10.5db ……. 1000= 0dB 1001 to 1111 = reserved	
	3:0	SE1_3D_R_FGAIN[3:0]	1000	SE1 3D Right Channel forward gain setting 0000 = -12dB 0001 = -10.5db ……. 1000= 0dB 1001 to 1111 = reserved	

Register 46h SE1_3D_R

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R71 (47h) SE1_NOTCH_CONFIG	1	SE1_NOTCH_R_ENA	0	SE1 Right channel notch filters enable 0 = Disabled 1 = Enabled	
	0	SE1_NOTCH_L_ENA	0	SE1 Left channel notch filters enable 0 = Disabled 1 = Enabled	

Register 47h SE1_NOTCH_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R72 (48h) SE1_NOTCH_A10	15:0	SE1_NOTCH_A10[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 48h SE1_NOTCH_A10

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R73 (49h) SE1_NOTCH_A11	15:0	SE1_NOTCH_A11[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 49h SE1_NOTCH_A11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R74 (4Ah) SE1_NOTCH_A20	15:0	SE1_NOTCH_A20[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Ah SE1_NOTCH_A20

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R75 (4Bh) SE1_NOTCH_A21	15:0	SE1_NOTCH_A21[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Bh SE1_NOTCH_A21

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R76 (4Ch) SE1_NOTCH_A30	15:0	SE1_NOTCH_A30[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Ch SE1_NOTCH_A30

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R77 (4Dh) SE1_NOTCH_A31	15:0	SE1_NOTCH_A31[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Dh SE1_NOTCH_A31

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R78 (4Eh) SE1_NOTCH_A40	15:0	SE1_NOTCH_A40[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Eh SE1_NOTCH_A40

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R79 (4Fh) SE1_NOTCH_A41	15:0	SE1_NOTCH_A41[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 4Fh SE1_NOTCH_A41

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R80 (50h) SE1_NOTCH_A50	15:0	SE1_NOTCH_A50[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 50h SE1_NOTCH_A50

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R81 (51h) SE1_NOTCH_A51	15:0	SE1_NOTCH_A51[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 51h SE1_NOTCH_A51

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R82 (52h) SE1_NOTCH_M10	15:0	SE1_NOTCH_M10[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 52h SE1_NOTCH_M10

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R83 (53h) SE1_NOTCH_M11	15:0	SE1_NOTCH_M11[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 53h SE1_NOTCH_M11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R84 (54h) SE1_NOTCH_M20	15:0	SE1_NOTCH_M20[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 54h SE1_NOTCH_M20

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R85 (55h) SE1_NOTCH_M21	15:0	SE1_NOTCH_M21[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 55h SE1_NOTCH_M21

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R86 (56h) SE1_NOTCH_M30	15:0	SE1_NOTCH_M30[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 56h SE1_NOTCH_M30

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R87 (57h) SE1_NOTCH_M31	15:0	SE1_NOTCH_M31[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 57h SE1_NOTCH_M31

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R88 (58h) SE1_NOTCH_M40	15:0	SE1_NOTCH_M40[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 58h SE1_NOTCH_M40

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R89 (59h) SE1_NOTCH_M41	15:0	SE1_NOTCH_M41[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 59h SE1_NOTCH_M41

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R90 (5Ah) SE1_NOTCH_M50	15:0	SE1_NOTCH_M50[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 5Ah SE1_NOTCH_M50

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R91 (5Bh) SE1_NOTCH_M51	15:0	SE1_NOTCH_M51[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) notch filter	

Register 5Bh SE1_NOTCH_M51

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R92 (5Ch) SE1_DF1_CONFIG	1	SE1_DF1_R_ENA	0	SE1 Right channel DF1 filter enable 0 = Disabled 1 = Enabled	
	0	SE1_DF1_L_ENA	0	SE1 Left channel DF1 filter enable 0 = Disabled 1 = Enabled	

Register 5Ch SE1_DF1_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R93 (5Dh) SE1_DF1_L0	15:0	SE1_DF1_L0[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) left channel DF1 filter	

Register 5Dh SE1_DF1_L0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R94 (5Eh) SE1_DF1_L1	15:0	SE1_DF1_L1[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) left channel DF1 filter	

Register 5Eh SE1_DF1_L1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R95 (5Fh) SE1_DF1_L2	15:0	SE1_DF1_L2[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) left channel DF1 filter	

Register 5Fh SE1_DF1_L2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R96 (60h) SE1_DF1_R0	15:0	SE1_DF1_R0[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) right channel DF1 filter	

Register 60h SE1_DF1_R0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R97 (61h) SE1_DF1_R1	15:0	SE1_DF1_R1[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) right channel DF1 filter	

Register 61h SE1_DF1_R1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R98 (62h) SE1_DF1_R2	15:0	SE1_DF1_R2[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 1 (SE1) right channel DF1 filter	

Register 62h SE1_DF1_R2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R100 (64h) SE2_RETUNE_CONFIG	1	SE2_RETUNE_R_ENA	0	SE2 Right channel ReTune™ filter enable 0 = Disabled 1 = Enabled	
	0	SE2_RETUNE_L_ENA	0	SE2 Left channel ReTune™ filter enable 0 = Disabled 1 = Enabled	

Register 64h SE2_RETUNE_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R101 (65h) SE2_RETUNE_C0	15:0	SE2_RETUNE_C0[15:0]	0001_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 65h SE2_RETUNE_C0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R102 (66h) SE2_RETUNE_C1	15:0	SE2_RETUNE_C1[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 66h SE2_RETUNE_C1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R103 (67h) SE2_RETUNE_C2	15:0	SE2_RETUNE_C2[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 67h SE2_RETUNE_C2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R104 (68h) SE2_RETUNE_C3	15:0	SE2_RETUNE_C3[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 68h SE2_RETUNE_C3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R105 (69h) SE2_RETUNE_C4	15:0	SE2_RETUNE_C4[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 69h SE2_RETUNE_C4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R106 (6Ah) SE2_RETUNE_C5	15:0	SE2_RETUNE_C5[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Ah SE2_RETUNE_C5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R107 (6Bh) SE2_RETUNE_C6	15:0	SE2_RETUNE_C6[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Bh SE2_RETUNE_C6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R108 (6Ch) SE2_RETUNE_C7	15:0	SE2_RETUNE_C7[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Ch SE2_RETUNE_C7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R109 (6Dh) SE2_RETUNE_C8	15:0	SE2_RETUNE_C8[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Dh SE2_RETUNE_C8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R110 (6Eh) SE2_RETUNE_C9	15:0	SE2_RETUNE_C9[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Eh SE2_RETUNE_C9

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R111 (6Fh) SE2_RETUNE_C10	15:0	SE2_RETUNE_C10[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 6Fh SE2_RETUNE_C10

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R112 (70h) SE2_RETUNE_C11	15:0	SE2_RETUNE_C11[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 70h SE2_RETUNE_C11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R113 (71h) SE2_RETUNE_C12	15:0	SE2_RETUNE_C12[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 71h SE2_RETUNE_C12

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R114 (72h) SE2_RETUNE_C13	15:0	SE2_RETUNE_C13[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 72h SE2_RETUNE_C13

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R115 (73h) SE2_RETUNE_C14	15:0	SE2_RETUNE_C14[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 73h SE2_RETUNE_C14

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R116 (74h) SE2_RETUNE_C15	15:0	SE2_RETUNE_C15[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 74h SE2_RETUNE_C15

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R117 (75h) SE2_RETUNE_C16	15:0	SE2_RETUNE_C16[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 75h SE2_RETUNE_C16

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R118 (76h) SE2_RETUNE_C17	15:0	SE2_RETUNE_C17[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 76h SE2_RETUNE_C17

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R119 (77h) SE2_RETUNE_C18	15:0	SE2_RETUNE_C18[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 77h SE2_RETUNE_C18

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R120 (78h) SE2_RETUNE_C19	15:0	SE2_RETUNE_C19[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 78h SE2_RETUNE_C19

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R121 (79h) SE2_RETUNE_C20	15:0	SE2_RETUNE_C20[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 79h SE2_RETUNE_C20

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R122 (7Ah) SE2_RETUNE_C21	15:0	SE2_RETUNE_C21[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Ah SE2_RETUNE_C21

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R123 (7Bh) SE2_RETUNE_C22	15:0	SE2_RETUNE_C22[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Bh SE2_RETUNE_C22

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R124 (7Ch) SE2_RETUNE_C23	15:0	SE2_RETUNE_C23[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Ch SE2_RETUNE_C23

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R125 (7Dh) SE2_RETUNE_C24	15:0	SE2_RETUNE_C24[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Dh SE2_RETUNE_C24

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R126 (7Eh) SE2_RETUNE_C25	15:0	SE2_RETUNE_C25[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Eh SE2_RETUNE_C25

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R127 (7Fh) SE2_RETUNE_C26	15:0	SE2_RETUNE_C26[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 7Fh SE2_RETUNE_C26

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R128 (80h) SE2_RETUNE_C27	15:0	SE2_RETUNE_C27[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 80h SE2_RETUNE_C27

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R129 (81h) SE2_RETUNE_C28	15:0	SE2_RETUNE_C28[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 81h SE2_RETUNE_C28

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R130 (82h) SE2_RETUNE_C29	15:0	SE2_RETUNE_C29[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 82h SE2_RETUNE_C29

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R131 (83h) SE2_RETUNE_C30	15:0	SE2_RETUNE_C30[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 83h SE2_RETUNE_C30

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R132 (84h) SE2_RETUNE_C31	15:0	SE2_RETUNE_C31[15:0]	0000_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) ReTune™ filter	

Register 84h SE2_RETUNE_C31

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R133 (85h) SE2_5BEQ_CONFIG	0	SE2_5BEQ_L_ENA	0	SE2 Left channel 5-band EQ enable 0 = Disabled 1 = Enabled	

Register 85h SE2_5BEQ_CONFIG

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R134 (86h) SE2_5BEQ_L10G	12:8	SE2_5BEQ_L1G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB 00100 : -8dB 00101 : -7dB 00110 : -6dB 00111 : -5dB 01000 : -4dB 01001 : -3dB 01010 : -2dB 01011 : -1dB 01100 : 0dB 01101 : 1dB 01110 : 2dB 01111 : 3dB 10000 : 4dB 10001 : 5dB 10010 : 6dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				10011 : 7dB 10100 : 8dB 10101 : 9dB 10110 : 10dB 10111 : 11dB 11000 : 12dB 11001 to 11111 : Reserved	
	4:0	SE2_5BEQ_L0G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	

Register 86h SE2_5BEQ_L10G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R135 (87h) SE2_5BEQ_L32G	12:8	SE2_5BEQ_L3G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	
	4:0	SE2_5BEQ_L2G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	

Register 87h SE2_5BEQ_L32G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R136 (88h) SE2_5BEQ_L4G	4:0	SE2_5BEQ_L4G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	

Register 88h SE2_5BEQ_L4G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R137 (89h) SE2_5BEQ_L0P	15:0	SE2_5BEQ_L0P [15:0]	0000_0000_1101_1000	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 89h SE2_5BEQ_L0P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R138 (8Ah) SE2_5BEQ_L0A	15:0	SE2_5BEQ_L0A [15:0]	0000_1111_1100_1010	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Ah SE2_5BEQ_L0A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R139 (8Bh) SE2_5BEQ_L0B	15:0	SE2_5BEQ_L0B [15:0]	0000_0100_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Bh SE2_5BEQ_L0B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R140 (8Ch) SE2_5BEQ_L1P	15:0	SE2_5BEQ_L1P [15:0]	0000_0001_1100_0101	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Ch SE2_5BEQ_L1P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R141 (8Dh) SE2_5BEQ_L1A	15:0	SE2_5BEQ_L1A [15:0]	0001_1110_1011_0101	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Dh SE2_5BEQ_L1A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R142 (8Eh) SE2_5BEQ_L1B	15:0	SE2_5BEQ_L1B [15:0]	1111_0001_0100_0101	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Eh SE2_5BEQ_L1B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R143 (8Fh) SE2_5BEQ_L1C	15:0	SE2_5BEQ_L1C [15:0]	0000_1011_0111_0101	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 8Fh SE2_5BEQ_L1C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R144 (90h) SE2_5BEQ_L2P	15:0	SE2_5BEQ_L2P [15:0]	0000_0101_0101_1000	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 90h SE2_5BEQ_L2P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R145 (91h) SE2_5BEQ_L2A	15:0	SE2_5BEQ_L2A [15:0]	0001_1100_0101_1000	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 91h SE2_5BEQ_L2A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R146 (92h) SE2_5BEQ_L2B	15:0	SE2_5BEQ_L2B [15:0]	1111_0011_0111_0011	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 92h SE2_5BEQ_L2B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R147 (93h) SE2_5BEQ_L2C	15:0	SE2_5BEQ_L2C [15:0]	0000_1010_0101_0100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 93h SE2_5BEQ_L2C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R148 (94h) SE2_5BEQ_L3P	15:0	SE2_5BEQ_L3P [15:0]	0001_0001_0000_0011	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 94h SE2_5BEQ_L3P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R149 (95h) SE2_5BEQ_L3A	15:0	SE2_5BEQ_L3A [15:0]	0001_0110_1000_1110	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 95h SE2_5BEQ_L3A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R150 (96h) SE2_5BEQ_L3B	15:0	SE2_5BEQ_L3B [15:0]	1111_1000_0010_1001	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 96h SE2_5BEQ_L3B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R151 (97h) SE2_5BEQ_L3C	15:0	SE2_5BEQ_L3C [15:0]	0000_0111_1010_1101	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 97h SE2_5BEQ_L3C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R152 (98h) SE2_5BEQ_L4P	15:0	SE2_5BEQ_L4P [15:0]	0100_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 98h SE2_5BEQ_L4P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R153 (99h) SE2_5BEQ_L4A	15:0	SE2_5BEQ_L4A [15:0]	0000_0101_0110_0100	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 99h SE2_5BEQ_L4A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R154 (9Ah) SE2_5BEQ_L4B	15:0	SE2_5BEQ_L4B [15:0]	0000_0101_0101_1001	Filter coefficients for Signal Enhancement 2 (SE2) left channel 5-band EQ filter	

Register 9Ah SE2_5BEQ_L4B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R155 (9Bh) SE2_5BEQ_R10G	12:8	SE2_5BEQ_R1G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				00100 : -8dB 00101 : -7dB 00110 : -6dB 00111 : -5dB 01000 : -4dB 01001 : -3dB 01010 : -2dB 01011 : -1dB 01100 : 0dB 01101 : 1dB 01110 : 2dB 01111 : 3dB 10000 : 4dB 10001 : 5dB 10010 : 6dB 10011 : 7dB 10100 : 8dB 10101 : 9dB 10110 : 10dB 10111 : 11dB 11000 : 12dB 11001 to 11111 : Reserved	
	4:0	SE2_5BEQ_R0G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	

Register 9Bh SE2_5BEQ_R10G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R156 (9Ch) SE2_5BEQ_R32G	12:8	SE2_5BEQ_R3G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	
	4:0	SE2_5BEQ_R2G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				11001 to 11111 : Reserved	

Register 9Ch SE2_5BEQ_R32G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R157 (9Dh) SE2_5BEQ_R4G	4:0	SE2_5BEQ_R4G[4:0]	0_1100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter Gain 00000 : -12dB 00001 : -12dB 00010 : -10dB 00011 : -9dB …. (1dB steps) 11000 : 12dB 11001 to 11111 : Reserved	

Register 9Dh SE2_5BEQ_R4G

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R158 (9Eh) SE2_5BEQ_R0P	15:0	SE2_5BEQ_R0P[15:0]	0000_0000_1101_1000	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register 9Eh SE2_5BEQ_R0P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R159 (9Fh) SE2_5BEQ_R0A	15:0	SE2_5BEQ_R0A[15:0]	0000_1111_1100_1010	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register 9Fh SE2_5BEQ_R0A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R160 (A0h) SE2_5BEQ_R0B	15:0	SE2_5BEQ_R0B[15:0]	0000_0100_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A0h SE2_5BEQ_R0B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R161 (A1h) SE2_5BEQ_R1P	15:0	SE2_5BEQ_R1P[15:0]	0000_0001_1100_0101	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A1h SE2_5BEQ_R1P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R162 (A2h) SE2_5BEQ_R1A	15:0	SE2_5BEQ_R1A[15:0]	0001_1110_1011_0101	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A2h SE2_5BEQ_R1A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R163 (A3h) SE2_5BEQ_R1B	15:0	SE2_5BEQ_R1B[15:0]	1111_0001_0100_0101	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A3h SE2_5BEQ_R1B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R164 (A4h) SE2_5BEQ_R1C	15:0	SE2_5BEQ_R1C[15:0]	0000_1011_0111_0101	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A4h SE2_5BEQ_R1C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R165 (A5h) SE2_5BEQ_R2P	15:0	SE2_5BEQ_R2P[15:0]	0000_0101_0101_1000	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A5h SE2_5BEQ_R2P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R166 (A6h) SE2_5BEQ_R2A	15:0	SE2_5BEQ_R2A[15:0]	0001_1100_0101_1000	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A6h SE2_5BEQ_R2A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R167 (A7h) SE2_5BEQ_R2B	15:0	SE2_5BEQ_R2B[15:0]	1111_0011_0111_0011	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A7h SE2_5BEQ_R2B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R168 (A8h) SE2_5BEQ_R2C	15:0	SE2_5BEQ_R2C[15:0]	0000_1010_0101_0100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A8h SE2_5BEQ_R2C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R169 (A9h) SE2_5BEQ_R3P	15:0	SE2_5BEQ_R3P[15:0]	0001_0001_0000_0011	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register A9h SE2_5BEQ_R3P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R170 (Aah) SE2_5BEQ_R3A	15:0	SE2_5BEQ_R3A[15:0]	0001_0110_1000_1110	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Aah SE2_5BEQ_R3A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R171 (Abh) SE2_5BEQ_R3B	15:0	SE2_5BEQ_R3B[15:0]	1111_1000_0010_1001	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Abh SE2_5BEQ_R3B

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R172 (Ach) SE2_5BEQ_R3C	15:0	SE2_5BEQ_R3C[15:0]	0000_0111_1010_1101	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Ach SE2_5BEQ_R3C

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R173 (Adh) SE2_5BEQ_R4P	15:0	SE2_5BEQ_R4P[15:0]	0100_0000_0000_0000	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Adh SE2_5BEQ_R4P

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R174 (Aeh) SE2_5BEQ_R4A	15:0	SE2_5BEQ_R4A[15:0]	0000_0101_0110_0100	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Aeh SE2_5BEQ_R4A

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R175 (Afh) SE2_5BEQ_R4B	15:0	SE2_5BEQ_R4B[15:0]	0000_0101_0101_1001	Filter coefficients for Signal Enhancement 2 (SE2) right channel 5-band EQ filter	

Register Afh SE2_5BEQ_R4B

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.1dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.1	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
DAC Normal Filter					
Passband	+/- 0.03dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		ADC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
Normal	16.5 / fs	Normal	16.5 / fs
Sloping Stopband	18 / fs		

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

Notes:

1. The Group Delays are quoted with the DSP SE1, SE2, and SE3 filters disabled. Enabling the DSP SE1, SE2, and SE3 filters will increase the Group Delay

ADC FILTER RESPONSE

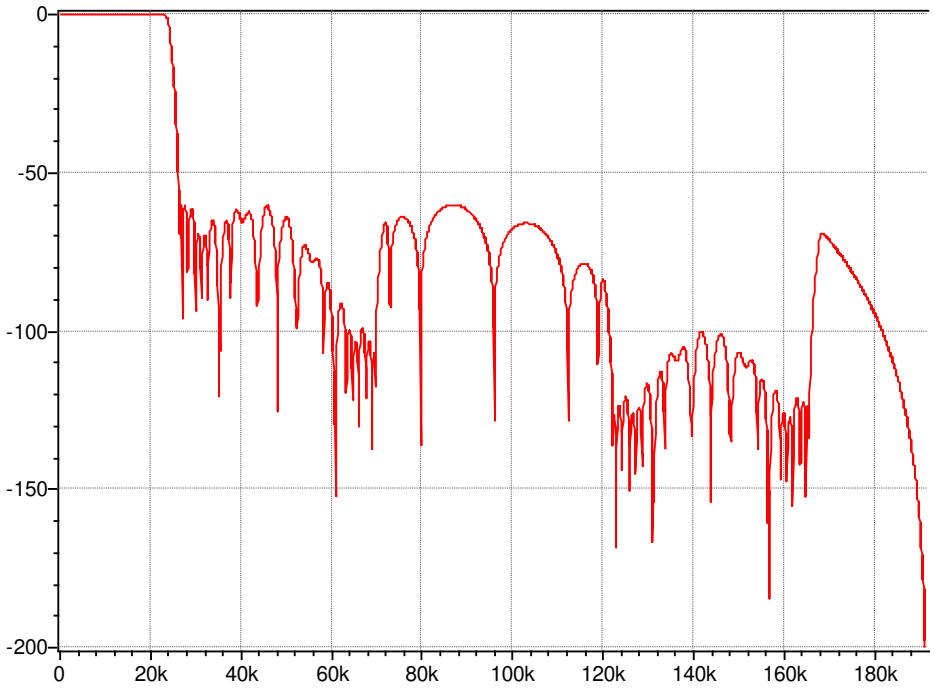


Figure 46 ADC Frequency Response up to 4 x fs (Sample rate, fs = 48kHz)

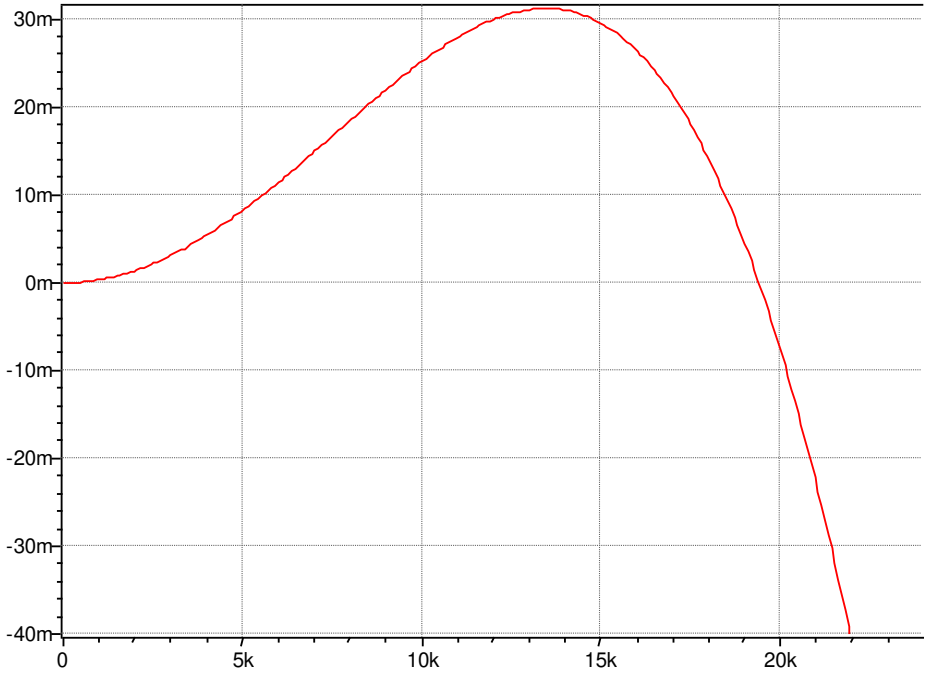


Figure 47 ADC Pass Band Frequency Response up to fs/2 (Sample rate, fs = 48kHz)

ADC HIGHPASS FILTER RESPONSE

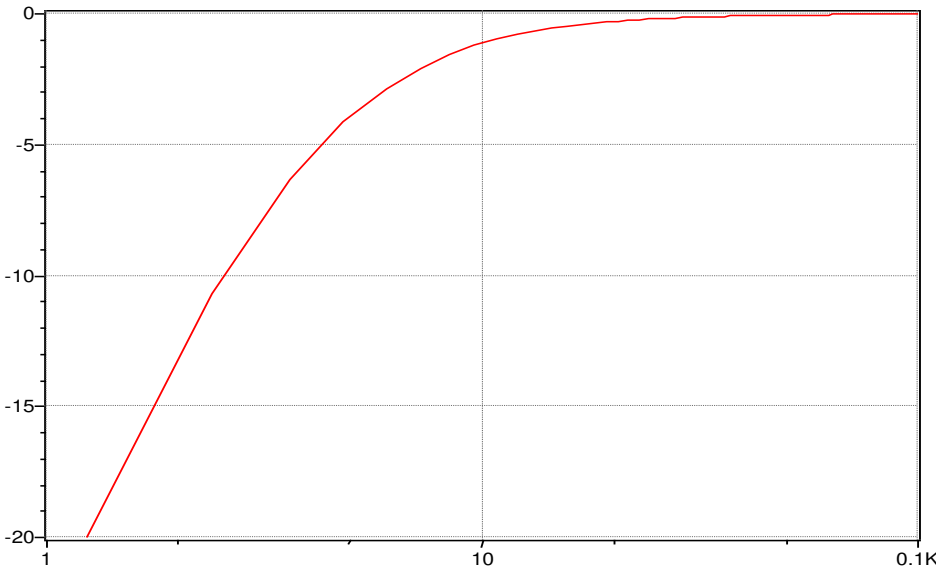


Figure 48 ADC High Pass Filter Frequency Response for the Hi-Fi Mode (Sample rate, fs = 48kHz)

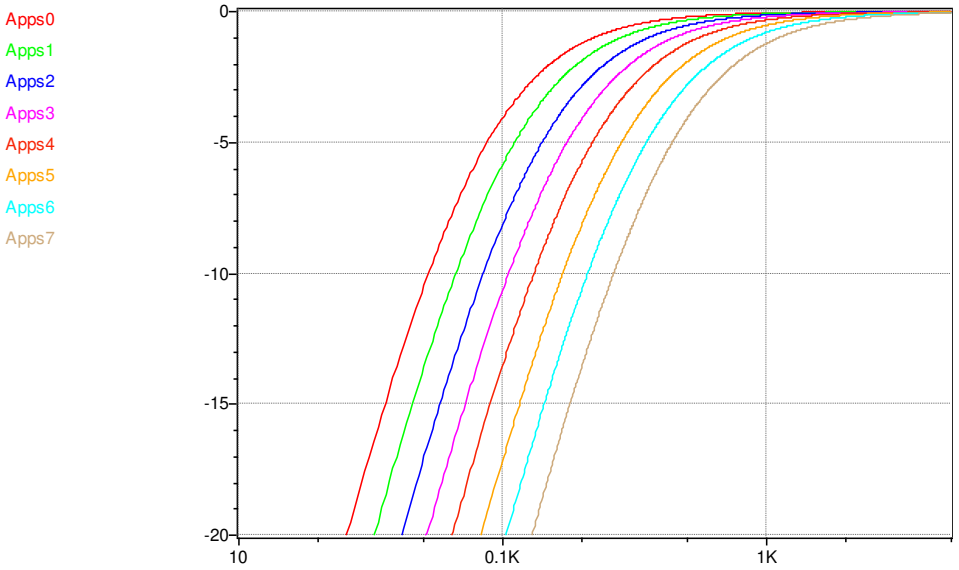


Figure 49 ADC High Pass Filter Frequency Response for the Application Mode (Sample rate, fs = 48kHz)

DAC FILTER RESPONSE

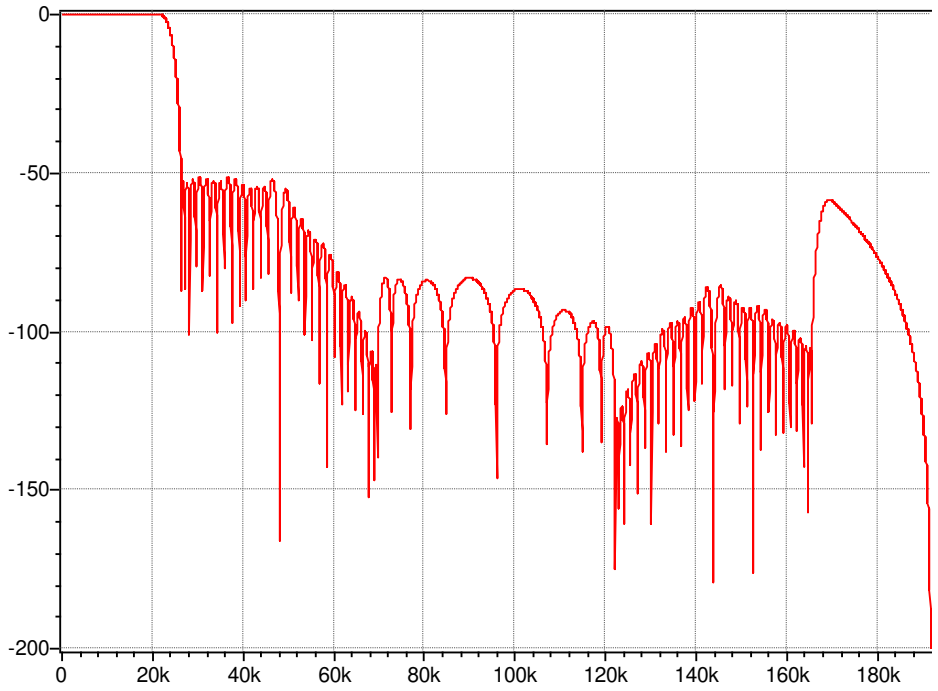


Figure 50 DAC Frequency Response up to 4 x fs (Sample rate, fs = 32k to 48kHz)

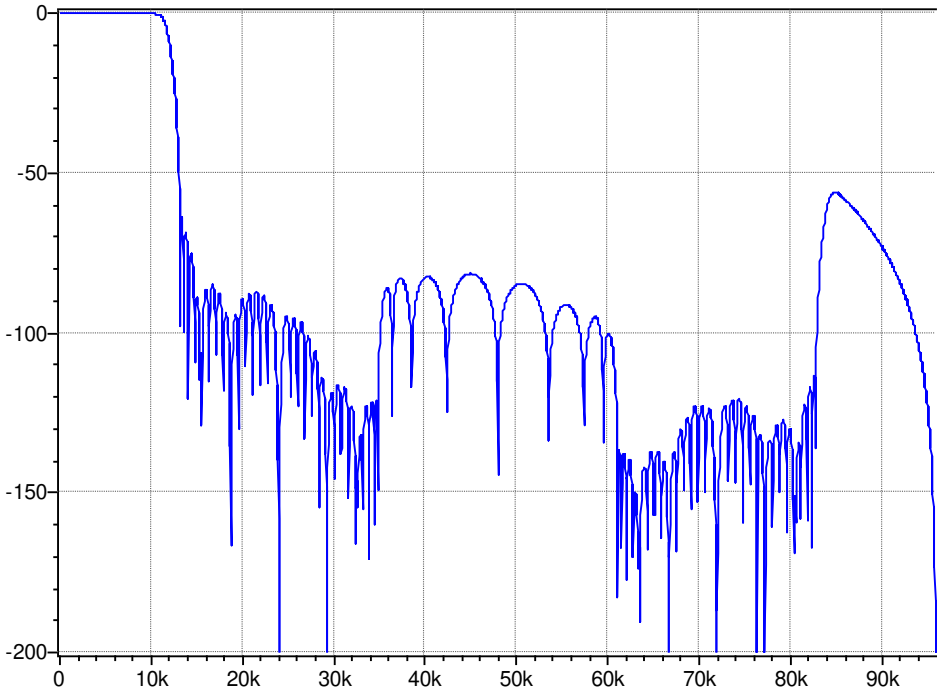


Figure 51 DAC Frequency Response up to 4 x fs (Sample rate, fs = 16k to 24kHz)

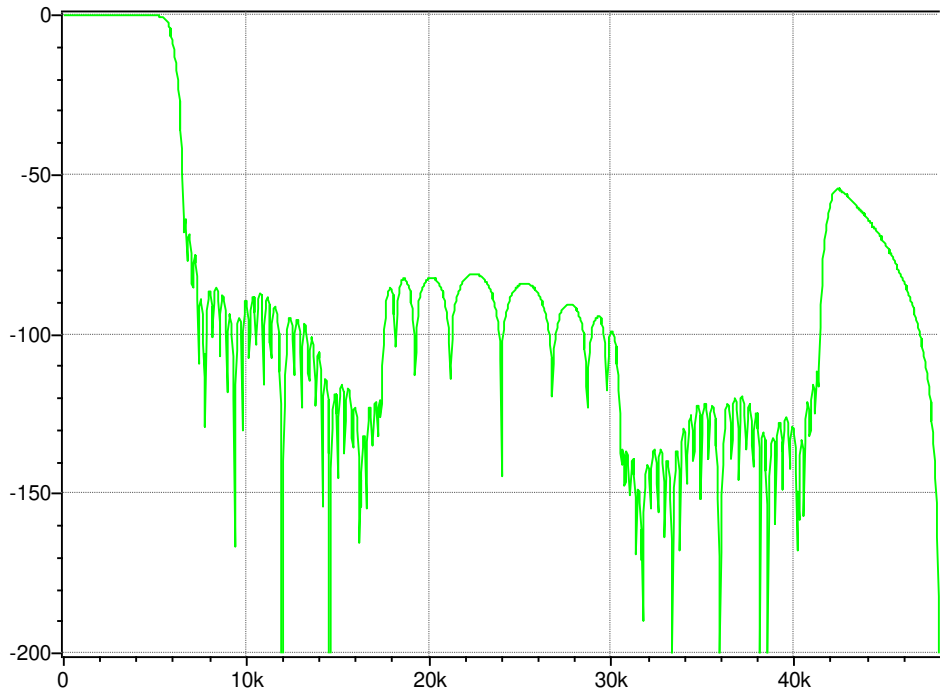


Figure 52 DAC Frequency Response up to 4 x fs (Sample rate, fs = 8k to 12kHz)

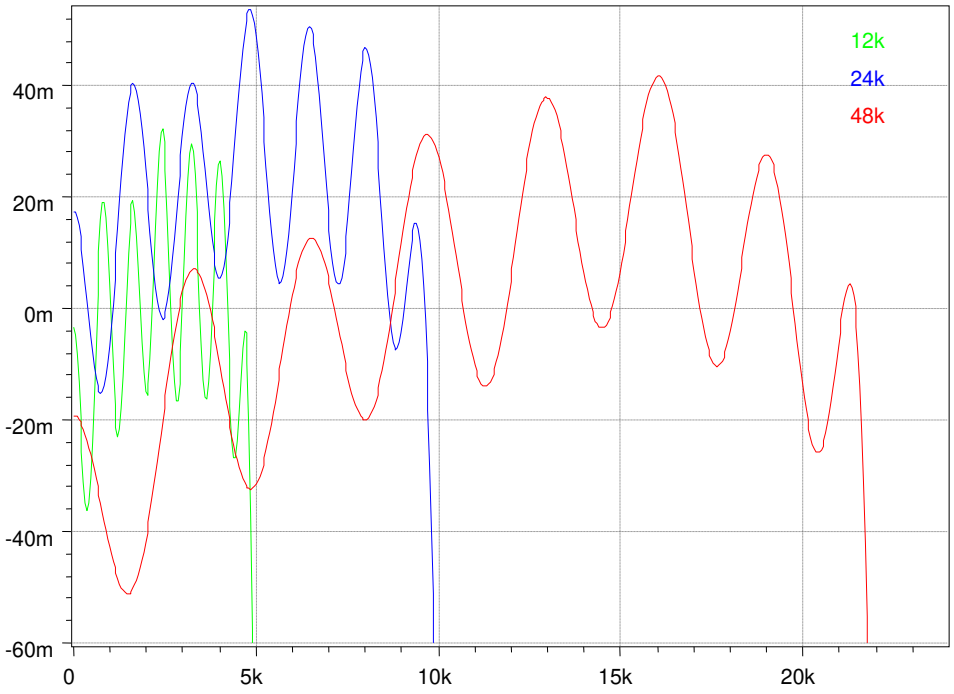


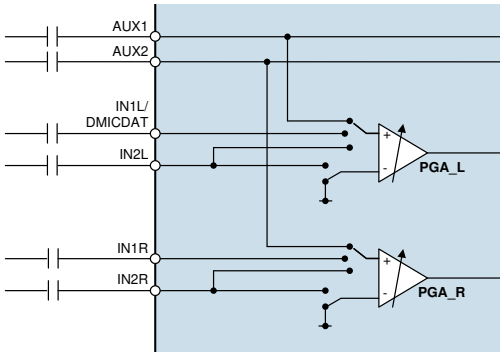
Figure 53 DAC Pass Band Frequency Response up to fs/2 (Sample rate, fs = 8k to 12kHz, 16k to 24kHz, 32k to 48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

AUDIO INPUT PATHS

The WM8946 provides up to 6 analogue audio inputs (including the auxiliary inputs AUX1 and AUX2). Each of these inputs is referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin. The circuit is illustrated in Figure 54. (Note that capacitors are not required on any unused audio input.)



$$Fc = \frac{1}{2\pi RC}$$

Fc = high pass 3dB cut-off frequency

Figure 54 Audio Input Path DC Blocking Capacitor

When the input impedance is known, and the cut-off frequency is known, then the minimum capacitor value may be derived easily. For practical use, a 1µF capacitance for all audio inputs can be recommended for most cases. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

Ceramic equivalents are a cost effective alternative to the superior tantalum packages, but care must be taken to ensure the desired capacitance is maintained at the LDOVOUT operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a line input or single-ended microphone connection. In the case of a differential microphone connection, a DC blocking capacitor is required on both input pins.

HEADPHONE / LINE OUTPUT PATHS

The WM8946 provides four outputs (LINEOUTL, LINEOUTR, SPKOUTL and SPKOUTR). Each of these outputs is referenced to the internal DC reference, VMID. In any case where a line output is used in a single-ended configuration (i.e. referenced to GND), a DC blocking capacitor is required in order to remove the DC bias. In the case where a pair of line outputs is configured as a BTL differential pair, then the DC blocking capacitor should be omitted.

The choice of capacitor is determined from the filter that is formed between the capacitor and the load impedance. A 1µF capacitance would be a suitable choice for a line load. For a headphone load a larger value (100uF for a 32 ohm load or 220uF for a 16 ohm load) would be required. Tantalum electrolytic capacitors are again particularly suitable but ceramic equivalents are a cost effective alternative. Care must be taken to ensure the desired capacitance is maintained at the appropriate operating voltage.

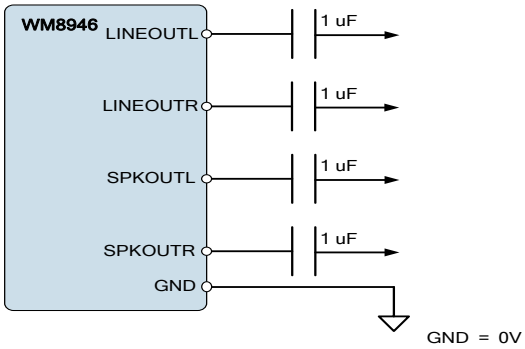


Figure 55 DC-blocking Components for Line Output

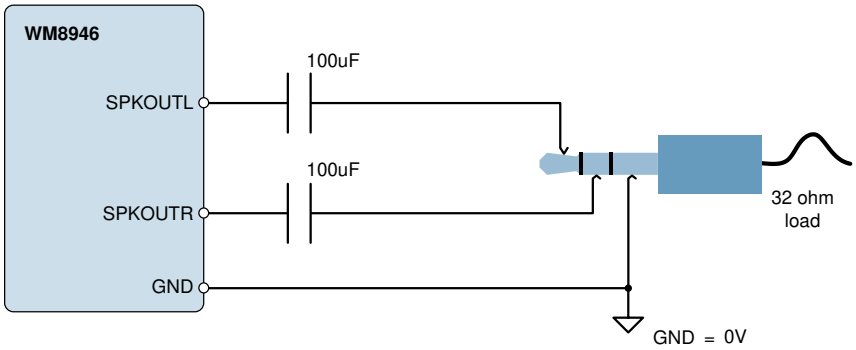


Figure 56 DC-blocking Components for Headphone Output

BTL SPEAKER OUTPUT CONNECTION

The BTL speaker output connection is a differential mode of operation. The loudspeaker may be connected directly across the SPKOUTL and SPKOUTR pins. No additional external components are required in this case.

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8946, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM8946 are listed below in Table 76.

POWER SUPPLY	DECOUPLING CAPACITOR
DCVDD, DBVDD, LDOVDD, SPKVDD	4.7μF ceramic
LDOVOUT	2.2μF ceramic
VMIDC	4.7μF ceramic

Table 76 Power Supply Decoupling Capacitors

All decoupling capacitors should be placed as close as possible to the WM8946 device. The connection between GND, the LDOVOUT decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND ball of the WM8946.

The VMIDC capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID reference. The connection between GND, the VMID decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND ball of the WM8946.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

MICROPHONE BIAS CIRCUIT

The WM8946 is designed to interface easily with electret microphones. These may be connected in single-ended or differential configurations. The single-ended method allows greater capability for the connection of multiple audio sources simultaneously, whilst the differential method provides better performance due to its rejection of common-mode noise.

In either configuration, the microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones), which can be provided by MICBIAS. This reference is generated by an output-compensated amplifier, which requires an external capacitor in order to guarantee accuracy and stability. The recommended capacitance is 4.7μF, although it may be possible to reduce this to 1μF if the analogue supply (LDOVOUT) is not too noisy. A ceramic type is a suitable choice here, providing that care is taken to choose a component that exhibits this capacitance at the intended MICBIAS voltage.

Note that the MICBIAS voltage may be adjusted using register control to suit the requirements of the microphone. Also note the WM8946 supports a maximum current of 3mA. If more than one microphone is connected to the MICBIAS, then combined current must not exceed 3mA.

A current-limiting resistor is also required when using an electret condenser microphone (ECM). The resistance should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the WM8946 is not exceeded. Cirrus Logic recommends a 2.2kΩ current limiting resistor as it provides compatibility with a wide range of microphone models.

The recommended connections for single-ended and differential microphone modes are illustrated in Figure 57 and Figure 58.

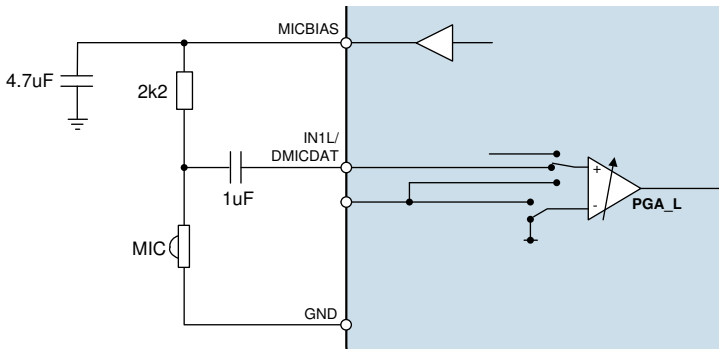


Figure 57 Single-Ended Microphone Connection

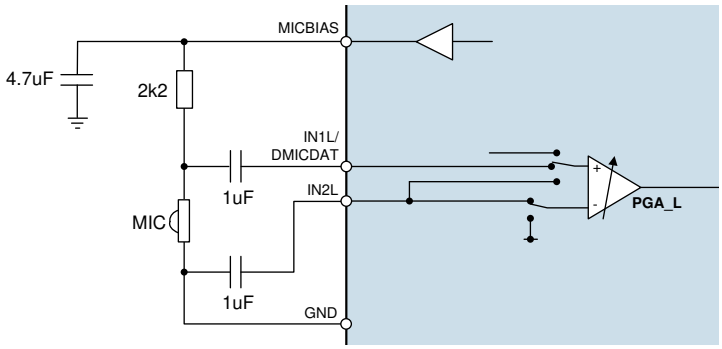


Figure 58 Pseudo-Differential Microphone Connection

VIDEO BUFFER COMPONENTS

External components are required for the Video Buffer.

In a typical application, R_{LOAD} = 75Ω, R_{SOURCE} = 75Ω, R_{REF} = 187Ω.

See "Video Buffer" for details of alternative components under different load impedance conditions.

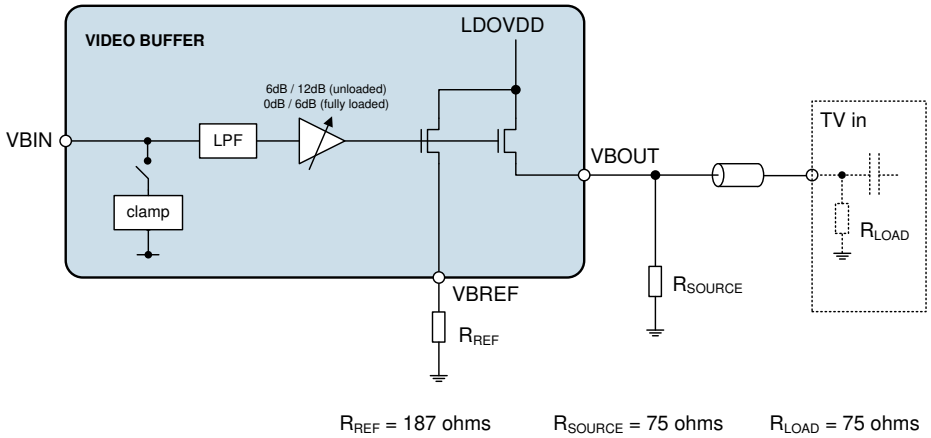


Figure 59 Typical Components for Video Buffer

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 60 provides a summary of recommended external components for WM8946. Note that the actual requirements may differ according to the specific target application.

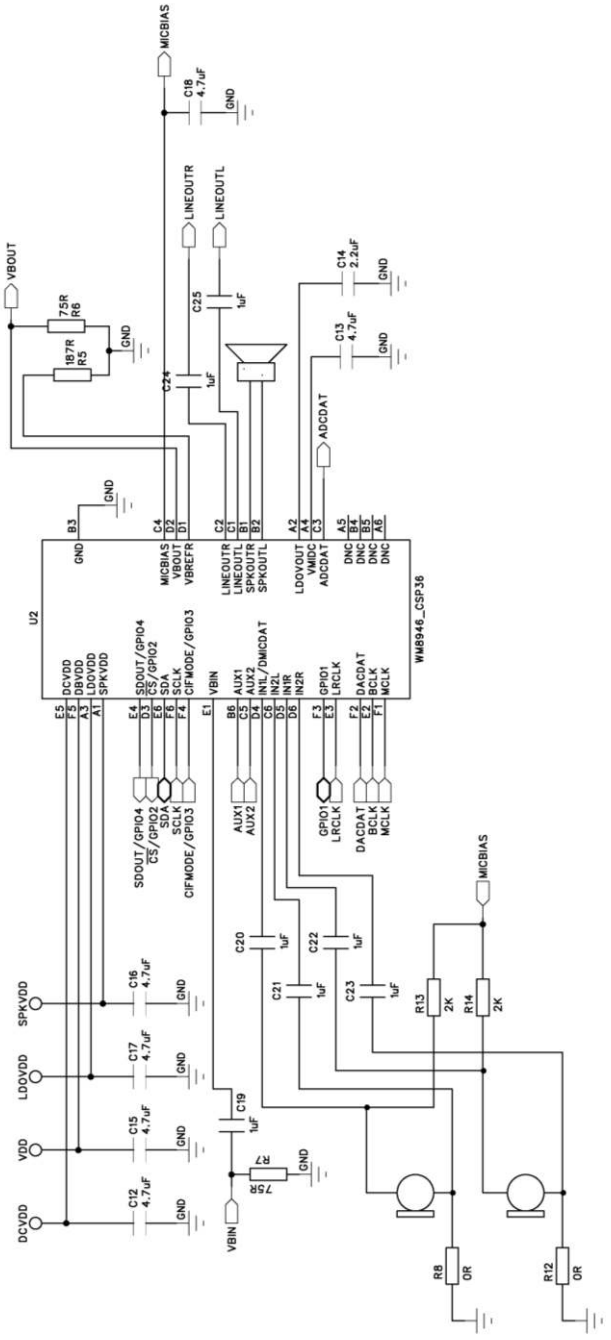


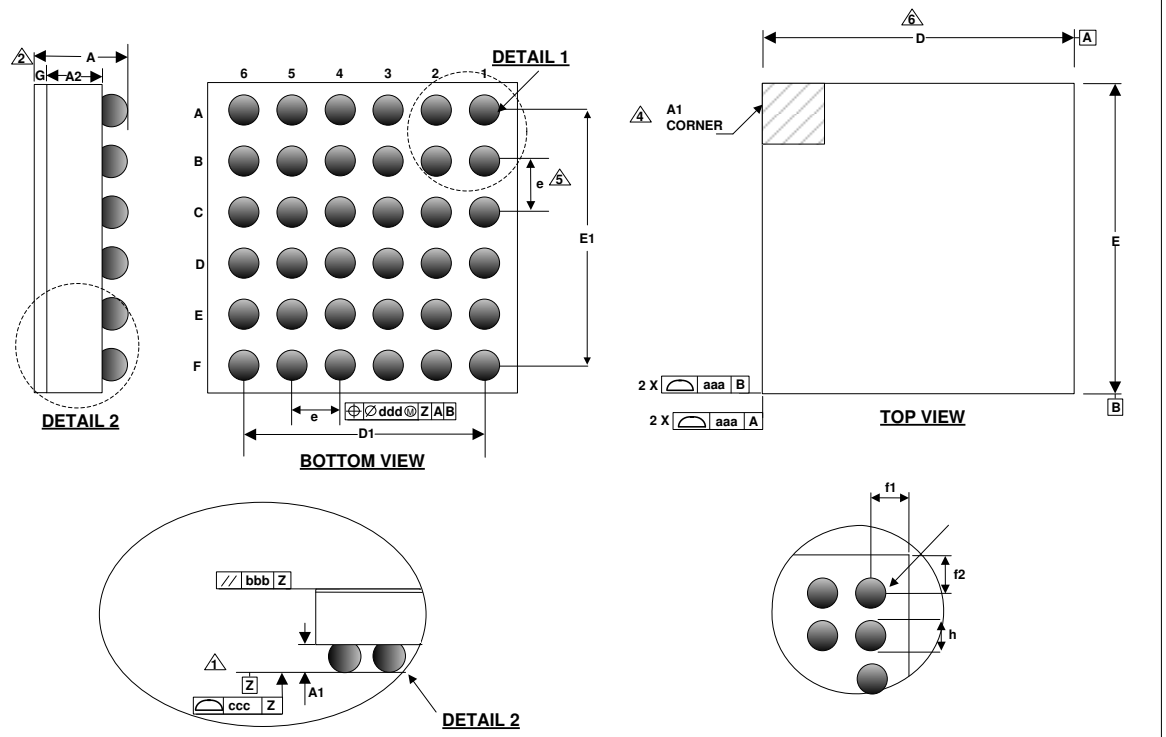
Figure 60 WM8946 Recommended External Components Diagram

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8946 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

B: 36 BALL W-CSP PACKAGE 2.970 x 3.070 x 0.7mm BODY, 0.50 mm BALL PITCH **DM063.B**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.660	0.700	0.740	
A1	0.207	0.244	0.281	
A2	0.418	0.434	0.450	
D	2.945	2.970	2.995	
D1		2.500 BSC		
E	3.045	3.070	3.095	
E1		2.500 BSC		
e		0.500 BSC		5
f1	0.223			
f2	0.273			
g		0.022		
h	0.264	0.314	0.364	
aaa		0.025		
bbb		0.060		
ccc		0.030		
ddd		0.015		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
11/10/10	4.0	Product Status updated to Production Data Added comment about ADC volume being in digital filter block Added comment about DAC volume being in digital filter block Notch filter plots updated Added note about DAC_VOL_RAMP rate	 30 47 36 48	
15/05/11	4.1	Added note about LDOVDD being enabled before SPKVDD to ensure pop-free start-up	8	JJ
25/06/12	4.2	Package Diagram updated to DM063B	172	JMacD
26/06/12	4.2	Added note that SYSCLK is required for Volume Update functions. Noted the notch filter is not usable below 120Hz	25, 47, 59 35	PH
04/07/12	4.2	Reel quantity changed to 5,000	6	JMacD/TS
27/07/12	4.3	Package Diagram dimensions updated in Features	1	JMacD
12/07/13	4.4	Typical Power Consumption data updated Clarification of DRC Attack/Decay times Clarification of LDO Regulator example configurations	15 45 63, 64	PH
13/10/14	4.4	Noted 4.5dB gain in Analogue Bypass paths	5, 16, 52, 54, 56	PH
01/03/16	4.5	Correction to recommended power-down sequence	106-107	PH