# AMMP-6120
## 8-24 GHz x2 Frequency Multiplier

## Data Sheet

**Avago TECHNOLOGIES**
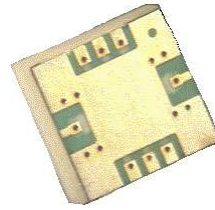
### Description

Agilent's AMMP-6120 is an easy-to-use integrated frequency multiplier (x2) in a surface mount package designed for commercial communication systems. The MMIC takes a 4 to 12 GHz input signal and doubles it to 8 to 24 GHz. It has integrated amplification, matching, harmonic suppression, and bias networks. The input/output are matched to 50 Ω and fully DC blocked. The MMIC is fabricated using PHEMT technology.

The backside of the package is both RF and DC ground. This helps simplify the assembly process and reduces assembly related performance variations and costs. The surface mount package allows elimination of "chip & wire" assembly for lower cost. This MMIC is a cost effective alternative to hybrid (discrete-FET), passive, and diode doublers that require complex tuning and assembly processes.

### Features

- 5x5mm Surface Mount Package
- Frequency Range : 8-24 GHz output (Useable to 26 GHz)
- Broad input power range: -11 to +5 dBm
- Output Power : +16 to +18 dBm
- Harmonic Suppression : 20 dBc (Fundamental)
- DC requirements : -1.4V and 5V, 112 mA @ Pin= +3dBm

### Applications

- Microwave Radio systems
- Satellite VSAT and DBS systems
- Commercial grade military
- 802.16 & 802.20 WiMax BWA systems
- WLL and MMDS loops



top view
package base: RF and DC GND
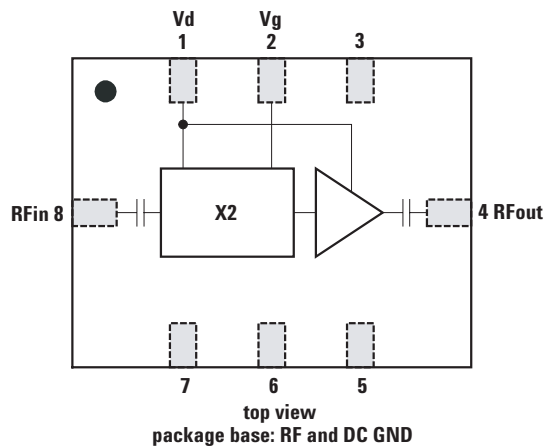
| Pin | Function |
|-----|----------|
| 1 | Vd |
| 2 | Vg |
| 3 | |
| 4 | RF Out |
| 5 | |
| 6 | |
| 7 | |
| 8 | RF In |

## AMMP-6120 Absolute Maximum Ratings[1]

| Symbol | Parameters/Conditions | Unit | Minimum | Maximum |
|--------|----------------------|------|---------|---------|
| Vd | Positive Drain Voltage | V | | 7 |
| Vg | Gate Supply Voltage | V | -3.0 | +0.5 |
| Id | Drain Current | mA | | 120 |
| Pin | CW Input Power | dBm | | 15 |
| Tch | Operating Channel Temp. | °C | | +150 |
| Tstg | Storage Case Temp. | °C | -65 | +150 |
| Tmax | Maximum Assembly Temp.(60 sec. max.) | °C | | +300 |

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

## AMMP-6120 DC Specifications/Physical Properties [1]

| Symbol | Parameters and Test Conditions | Units | Typ. | Maximum |
|--------|-------------------------------|-------|------|---------|
| Id | Drain Supply Current (under any RF power drive and temperature) (Vd=5V) | mA | 85 | 110 |
| Ig | Gate Current | mA | 9 | |
| $\Theta$ch-b | Thermal Resistance [2] (Backside temperature, Tb = 25°C) | °C/W | 34 | |

Notes:
1. Ambient operational temperature TA=25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance ($T_{channel}$ (Tc) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

## RF Specifications [3,4] ($T_A$=25°C, Vd=5V, Vg=-1.4V, $Id_{(Q)}$=85mA, Zin=Zout=50$\Omega$)

| Symbol | Parameters and Test Conditions | Units | Minimum | Typ. |
|--------|-------------------------------|-------|---------|------|
| Pout | Output Power [5] | dBm | 13 | 16 |
| Rlin | Input Return Loss | dB | | -15 |
| RLout | Output Return Loss | dB | | -10 |
| IP-1dB | Input Power @ 1dB Gain Comp | dBm | | 2 |
| Sup | Fundamental Suppresion [5] | dBc | 18 | 25 |
| Sup3 | 3rd Harmonic Suppression | dBc | | 25 |
| Sup4 | 4th Harmonic Suppression | dBc | | 35 |
| SSBPN | Single Side Band Phase Noise (@100kHz offset) | dBc Hz | -140 (fout=15.6GHz) | |

Notes:
3. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C.
4. Pre-assembly into package performance verified 100% on-wafer.
5. This final package part performance is verified by a functional test correlated to actual performance at Fout=10GHz output, Pin=+3dBm.

## AMMP-6120 Typical Performances

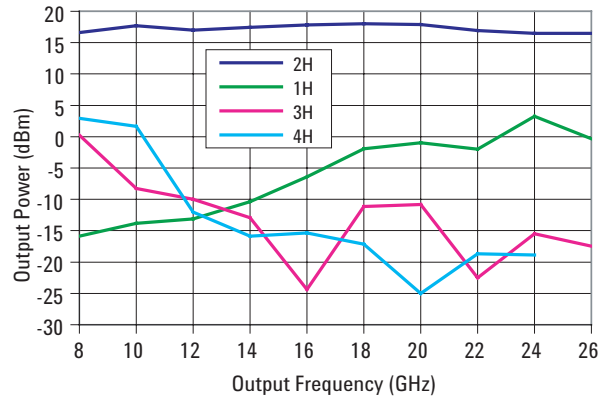($T_A$ = 25°C,$Z_{in}$ = $Z_{out}$ = 50 Ω, Vd=5V, Vg=-1.4V)



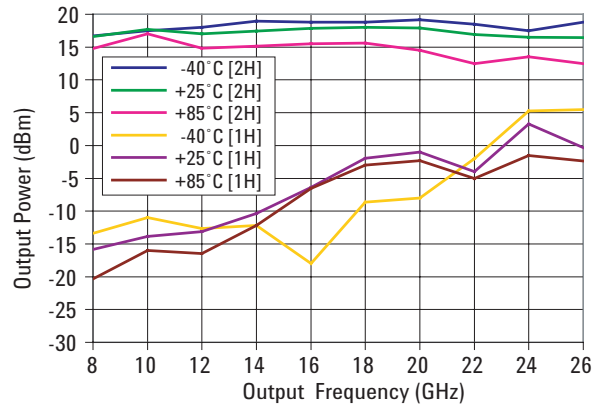Figure 1. Output Power vs. Output Freq. @ Pin=+3dBm



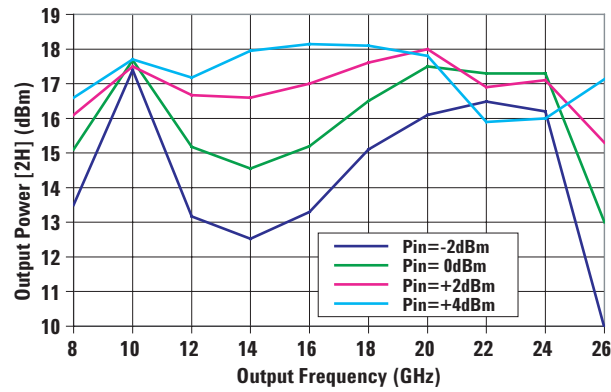Figure 2. Output Power vs. Output Freq. over temp @ Pin=+3dBm



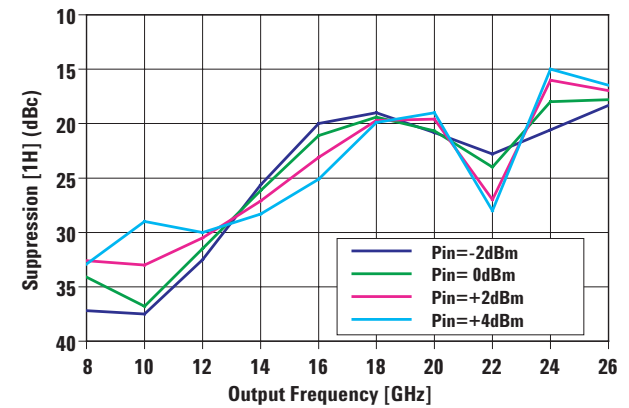Figure 3. Output Power [2H] vs. Output Freq. at variable Pin
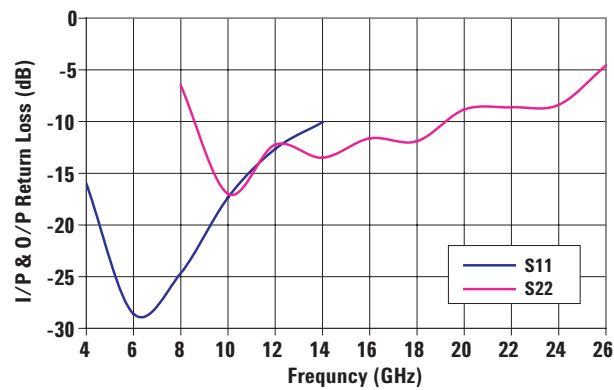


Figure 4. Fundamental Suppression at variable Pin

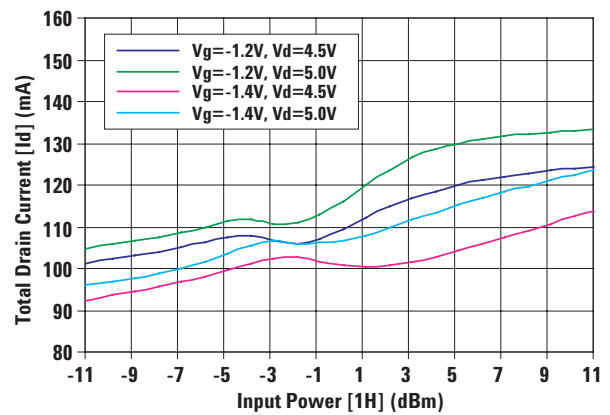

Figure 5. Input and Output Return Loss



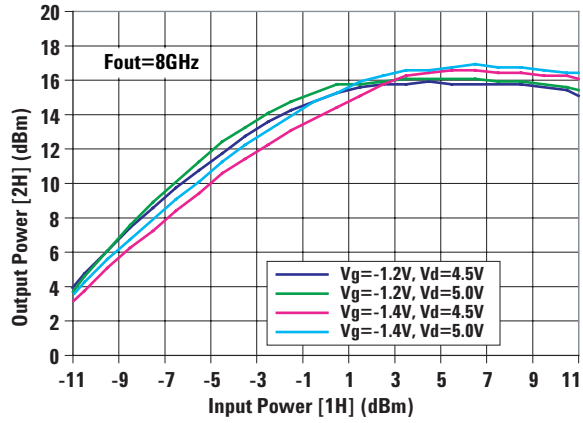Figure 6. Variation of total drain current with input power
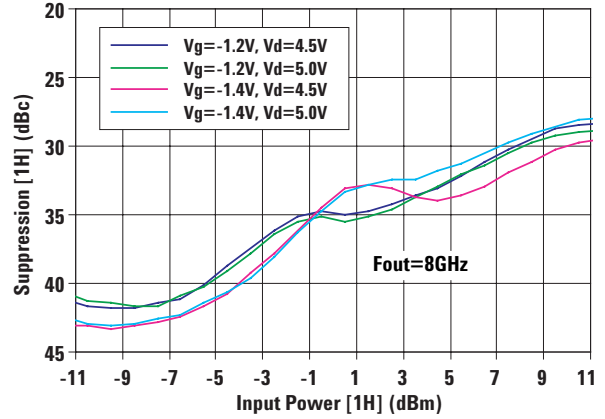
3

**Figure 7. 2H Output Power Vs Input Power @ Fout=8GHz**



**Figure 8. Fundamental Supp. Vs Input Power @ Fout=8GHz**
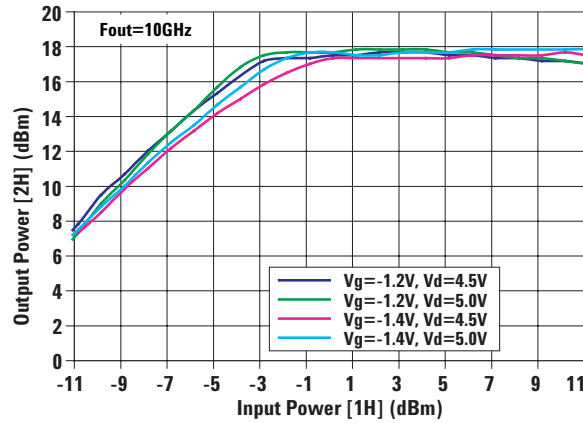
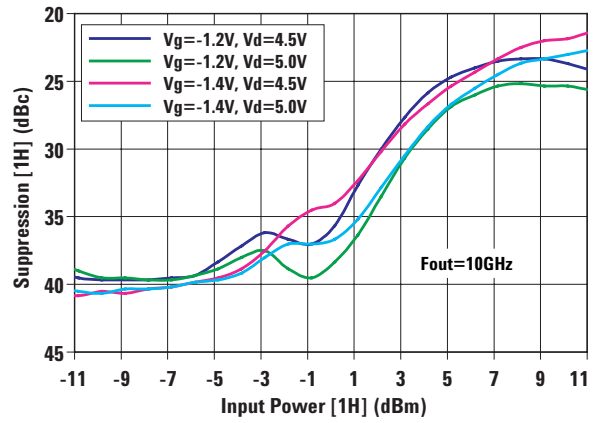

**Figure 9. 2H Output Power Vs Input Power @ Fout=10GHz**



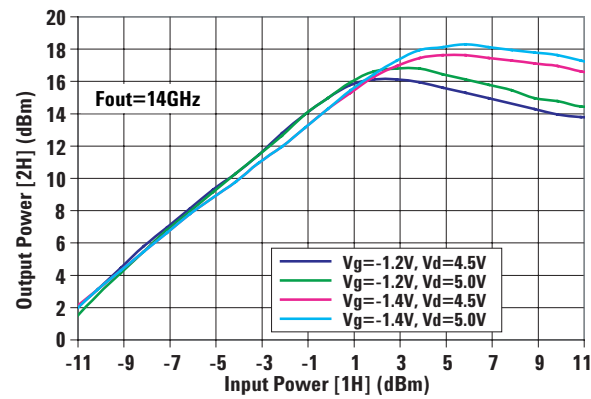**Figure 10. Fundamental Supp. Vs Input Power @ Fout=10GHz**



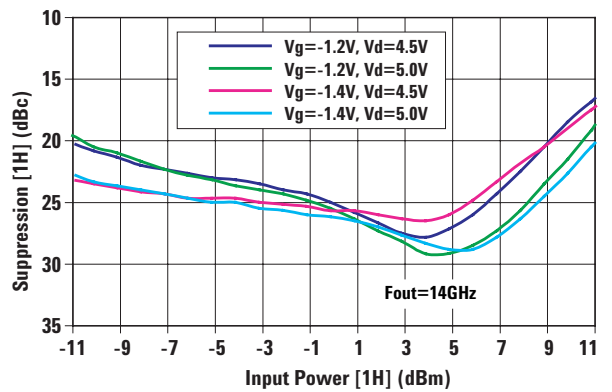**Figure 11. 2H Output Power Vs Input Power @ Fout=14GHz**



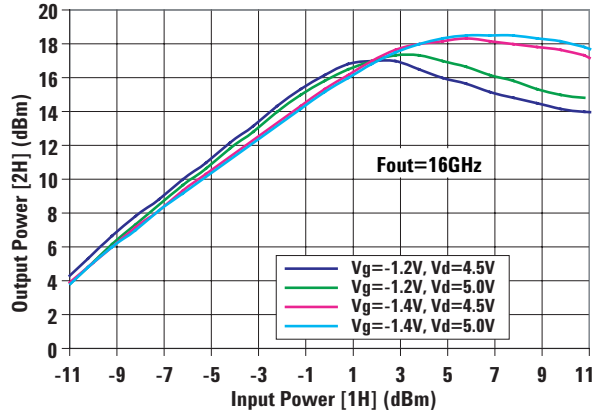**Figure 12. Fundamental Supp. Vs Input Power @ Fout=14GHz**

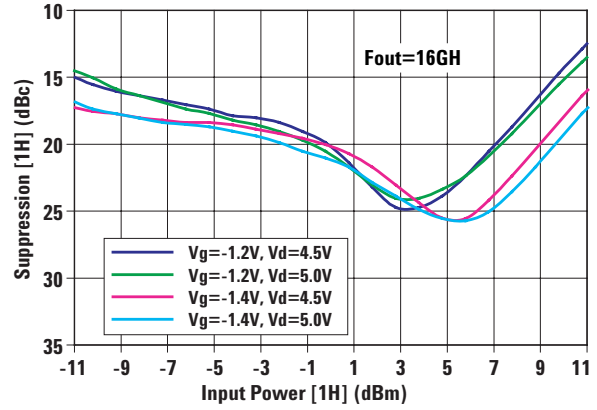Figure 13. 2H Output Power Vs Input Power @ Fout=16GHz



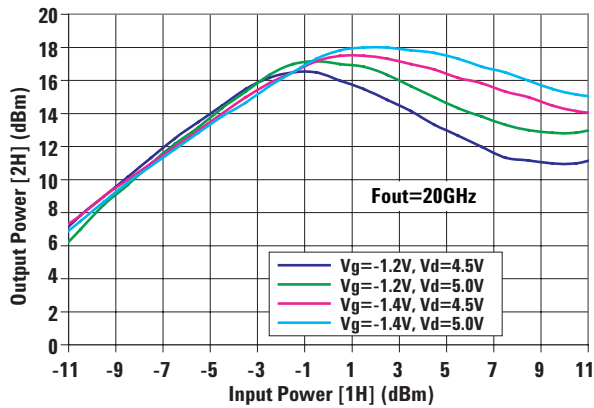Figure 14. Fundamental Supp. Vs Input Power @ Fout=16GHz



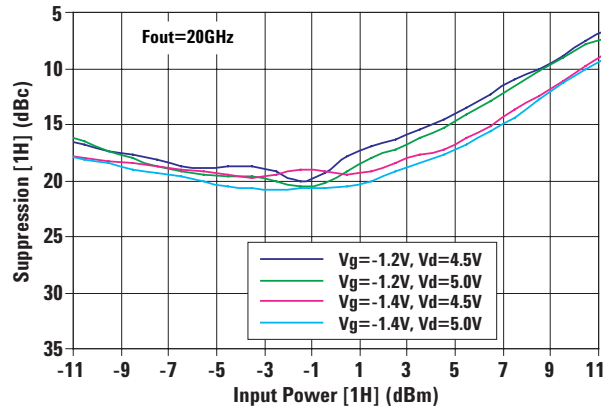Figure 15. 2H Output Power Vs Input Power @ Fout=20GHz



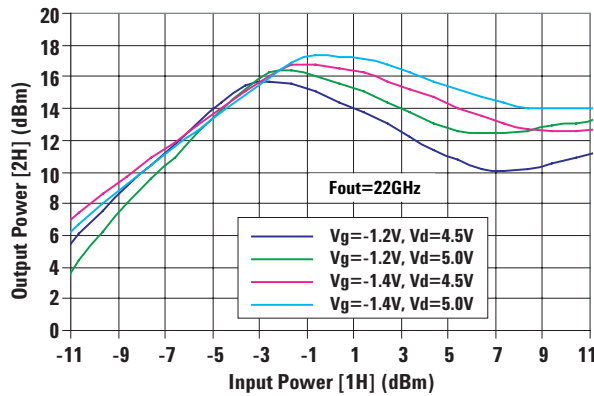Figure 16. Fundamental Supp. Vs Input Power @ Fout=20GHz



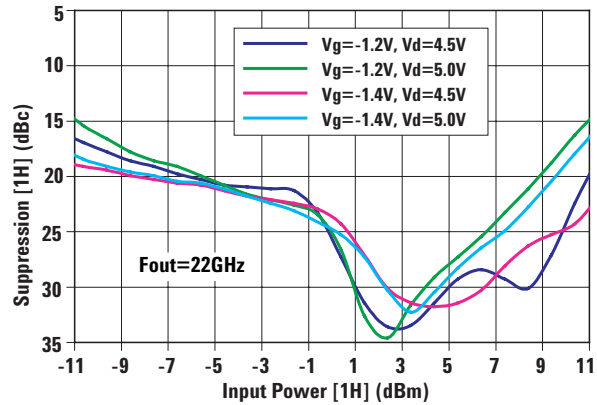Figure 17. 2H Output Power Vs Input Power @ Fout=22GHz



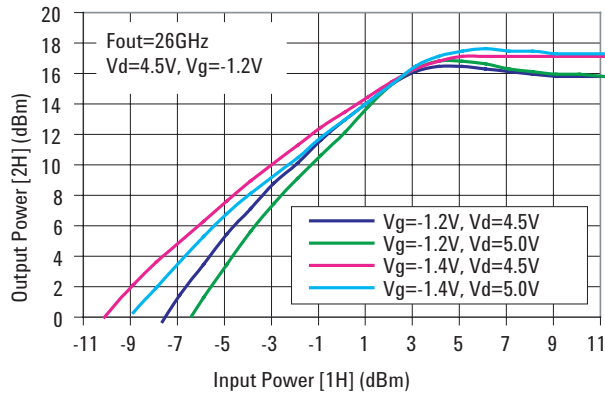Figure 18. Fundamental Supp. Vs Input Power @ Fout=22GHz

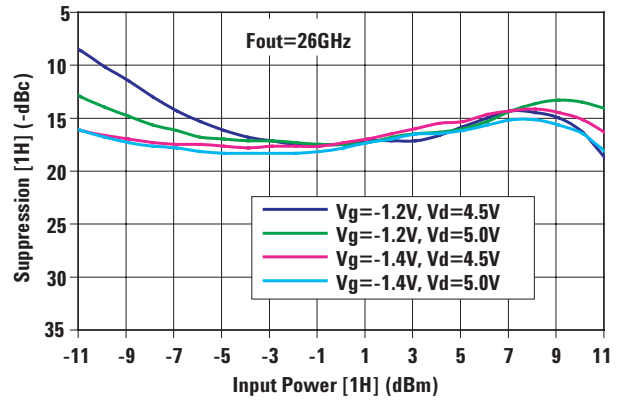Figure. 19  2H Output Power Vs Input Power @ Fout=26GHz



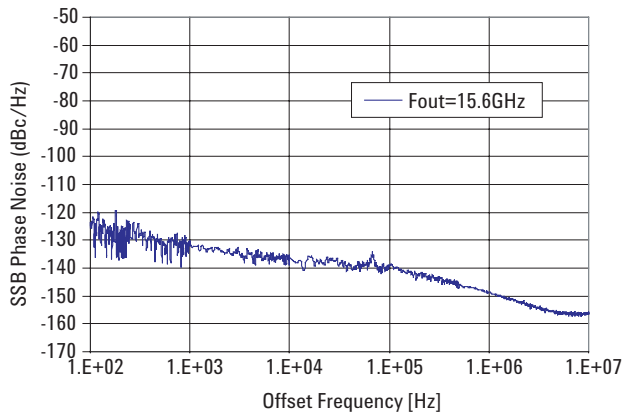Figure. 20  Fundamental Supp. Vs Input Power @ Fout=26GHz



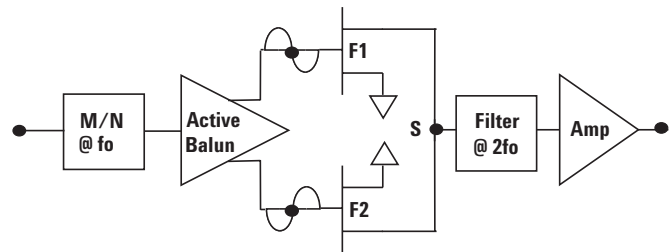Figure.21  SSB Phase Noise of frequency doubler
(Pin=+2dBm, fout=15.6GHz)



Figure 22. Top Level Schematic of Frequency doubler

## Biasing and Operation

The frequency doubler MMIC consists of a balun. The outputs of this balun feed the gates of balanced FETs and the drains are connected to form the single-ended output. This results in fundamental frequency & odd harmonics cancellation. The even harmonic drain currents are in phase and thus add in phase. The input matching network (M/N) is designed to provide good match at fundamental frequencies and produces high impedance mismatch to higher harmonics.

The AMMP-6120 is biased with a single positive drain supply Vdd and a single negative gate supply using separate bypass capacitors. It is normally biased with the drain supply connected to Vd and the gate supply connected to Vg. For most applications it is recommended to use a Vg =-1.2V to -1.4V and Vd=4.5V to 5.0V.

The RF input and output ports are AC coupled thus no DC voltage is present at either port. The ground connection is made via the package base."

The AMMP-6120 performance changes with Drain Voltage (Vd) and Gate bias (Vg) as shown in the previous graphs. Improvements in output power or fundamental suppression performance are possible by optimizing the Vg from -1.2V to -1.4V and/or Vd from 4.5 to 5.0V.

A simplified schematic of the frequency multiplier is shown in figure 22. The active balun circuit and the output amplifier of the circuit are self biased. The Vg negative bias (below pinch off) is only applied to FETs 'F1' and 'F2'. FETs 'F1' and 'F2' have no significant contribution to total drain current therefore Vg cannot be used to set drain current. It should only be used to optimize the output power and fundamental & higher harmonics suppression of the doubler.
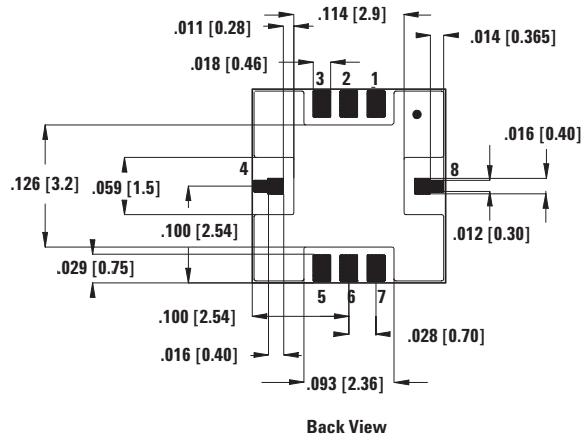
Refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

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## Outline Drawing



Front View      Side View
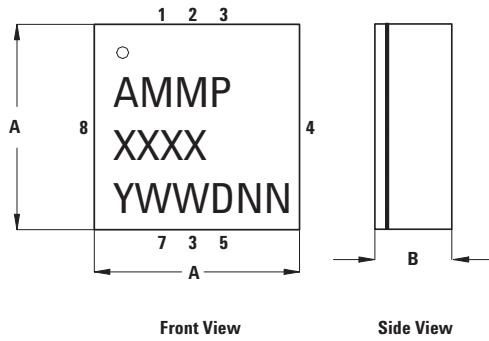
| Symbol | Min | Max |
|--------|------|------|
| A | 0.198 (5.03) | 0.213 (5.4) |
| B | 0.0685 (1.74) | 0.088 (2.25) |

Dimensions are in inches (mm)



**Back View**

Dimensional Tolerance for back view: 0.002" (0.05mm)

Notes:
1. * Indicates Pin 1
2. Dimensions are in inches [millimeters]
3. All Grounds must be soldered to PCB RF Ground

## Recommended SMT Attachment

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available from www.agilent.com/view/rf or upon request from Agilent Application Engineering.

## Evaluation Test Circuit (Demo Board)

(Available to customer on qualified request)
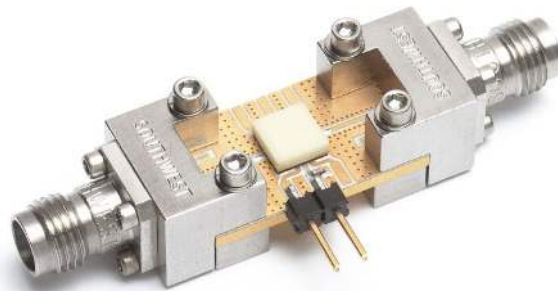


## Suggested PCB Material and Land Pattern
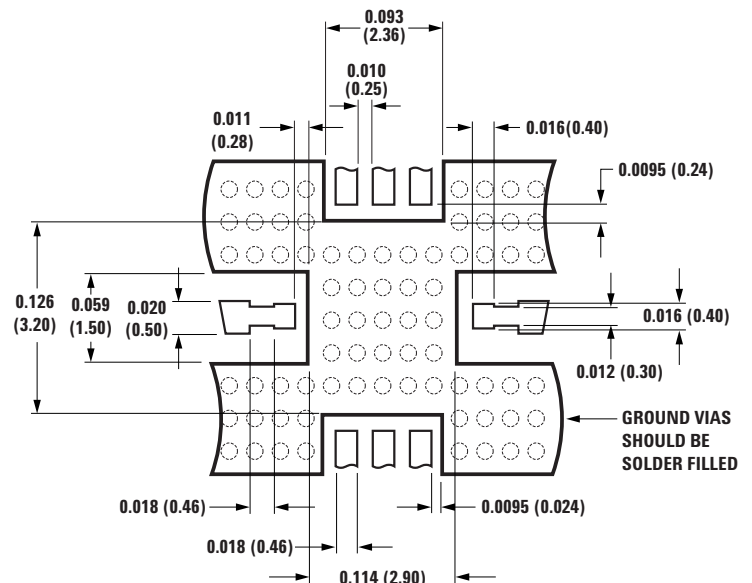


INCHES (MILLIMETERS).
MATERIAL IS ROGERS RO4350, 0.010-INCH THICK.

## Manual Assembly

1. Follow ESD precautions while handling packages.

2. Handling should be along the edges with tweezers.

3. Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Conductive epoxy is *not* recommended. Hand soldering is *not* recommended.

4. Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.

5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temperature to avoid damage due to thermal shock.

6. Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

## Solder Reflow Profile

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 23. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.
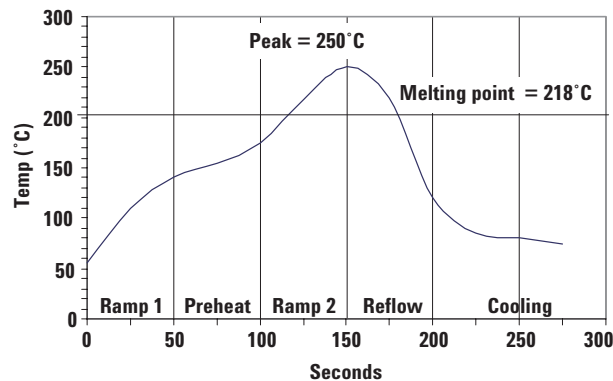
## Recommended solder reflow profile



Figure 23. Suggested lead-free reflow profile for SnAgCu solder paste.

## Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 24. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

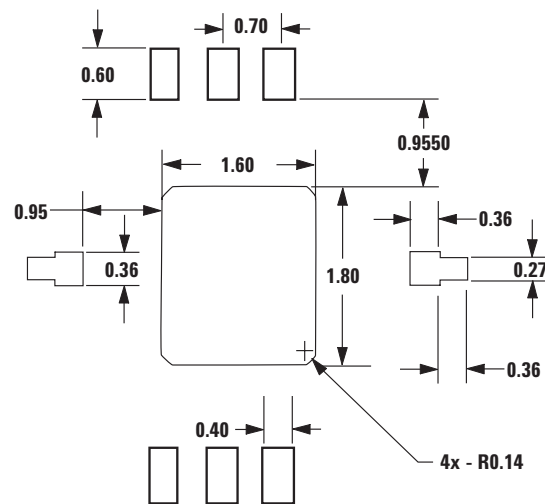The combined PCB and stencil layout is shown in below**.**
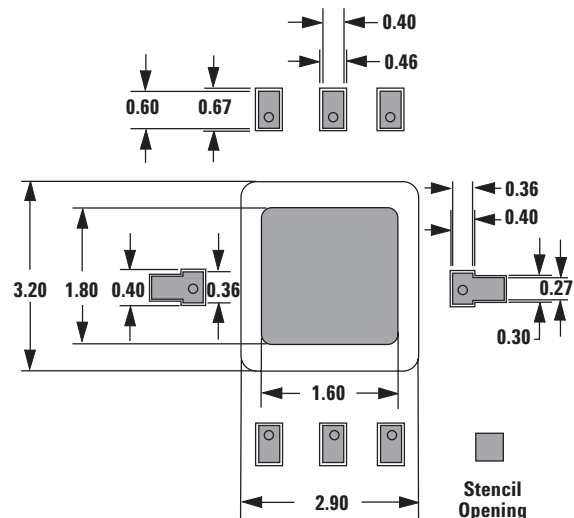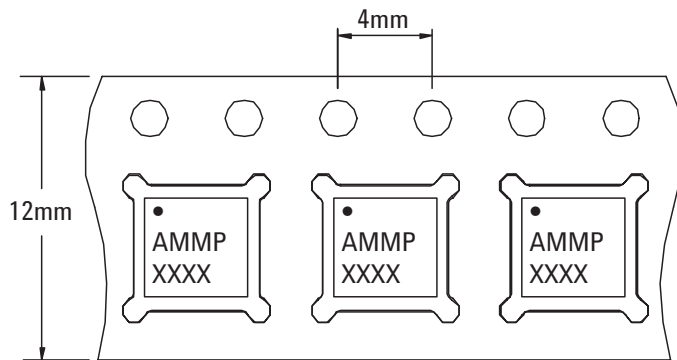


Figure 24. Stencil outline drawing (mm).



Figure 25. Combined PCB and stencil layouts (mm).

## AMMP-6120 Part Number Ordering Information

| Part Number | Devices Per Container | Container |
|---|---|---|
| AMMP-6120-BLK | 10 | Antistatic bag |
| AMMP-6120-TR1 | 100 | 7" Reel |
| AMMP-6120-TR2 | 500 | 7" Reel |

## Device Orientation (Top View)



## Carrier Tape and Pocket Dimensions



SECTION B-B

SECTION A-A

Notes:
1. Ao & Bo measure at 0.3mm above base of pocket
2. 10 pitches cumulative tol. ±0.2mm

| Item | Ao | Bo | Ko |
|---|---|---|---|
| Min. | 5.20 | 5.20 | 2.10 |
| Nom. | 5.30 | 5.30 | 2.20 |
| Max. | 5.40 | 5.40 | 2.30 |

Ao: 5.30
Bo: 5.30
Ko: 2.20
Pitch: 8.00
Width: 12.00