DAC11001B 20-Bit, Low-Noise, Ultra-Low Harmonic Distortion, Fast-Settling, High-Voltage-Output, Digital-to-Analog Converter (DAC)

1 Features

- 20-bit monotonic: 1-LSB DNL (max)
- Integral linearity: 1-LSB INL (max)
- Low noise: 7 nV/√Hz
- Code independent low glitch: 1 nV-s
- Excellent THD:
  –118 dB at 20-kHz f_{OUT}, 1-MHz f_{DAC}
- Fast settling: 1 µs
- Flexible output ranges: V_{REFPF} to V_{REFNF}
- Integrated, precision feedback resistors
- 50-MHz, 4-wire SPI-compatible interface
  - Readback
  - Daisy-chain
- Temperature range: –40°C to +125°C
- Package: 48-pin TQFP

2 Applications

- Lab and field instrumentation
- Spectrometer
- Analog output module
- Battery Test
- Semiconductor test
- Arbitrary waveform generator (AWG)
- MRI
- X-ray systems
- Professional audio amplifier (rack mount)

3 Description

The 20-bit DAC11001B is a highly accurate, low-noise, voltage-output, single-channel, digital-to-analog converter (DAC). The DAC11001B is specified monotonic by design, and offers excellent linearity across all output ranges.

The unbuffered voltage output offers low noise performance (7 nV/√Hz) in combination with a fast settling time (1 µs), making this device an excellent choice for low-noise, fast control-loop, and waveform-generation applications. The DAC11001B integrates an enhanced deglitch circuit with code-independent ultra-low glitch (1 nV-s) to enable clean waveform ramps with ultra-low total harmonic distortion (THD).

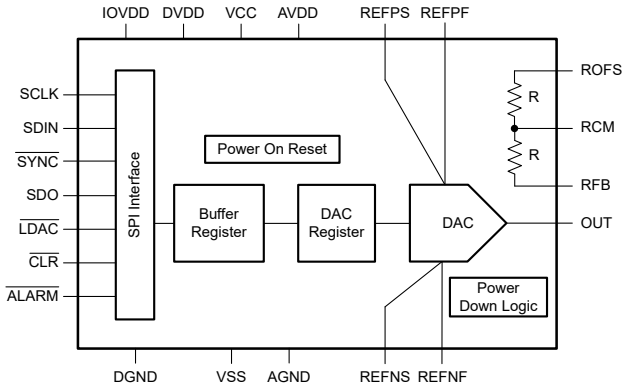
The DAC11001B device incorporates a power-on-reset (POR) circuit so that the DAC powers on with known values in the registers. With external references, DAC output ranges from V_{REFPF} to V_{REFNF} can be achieved, including asymmetric output ranges.

The DAC11001B uses a versatile 4–wire serial interface that operates at clock rates of up to 50 MHz.

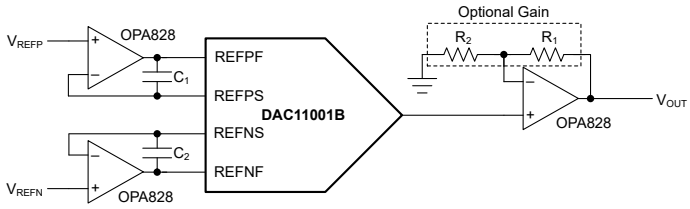
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DAC11001B	TQFP (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Functional Block Diagram



Arbitrary Waveform Generation Circuit

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4 Revision History

DATE	REVISION	NOTES
December 2021	*	Initial Release

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5 Pin Configuration and Functions

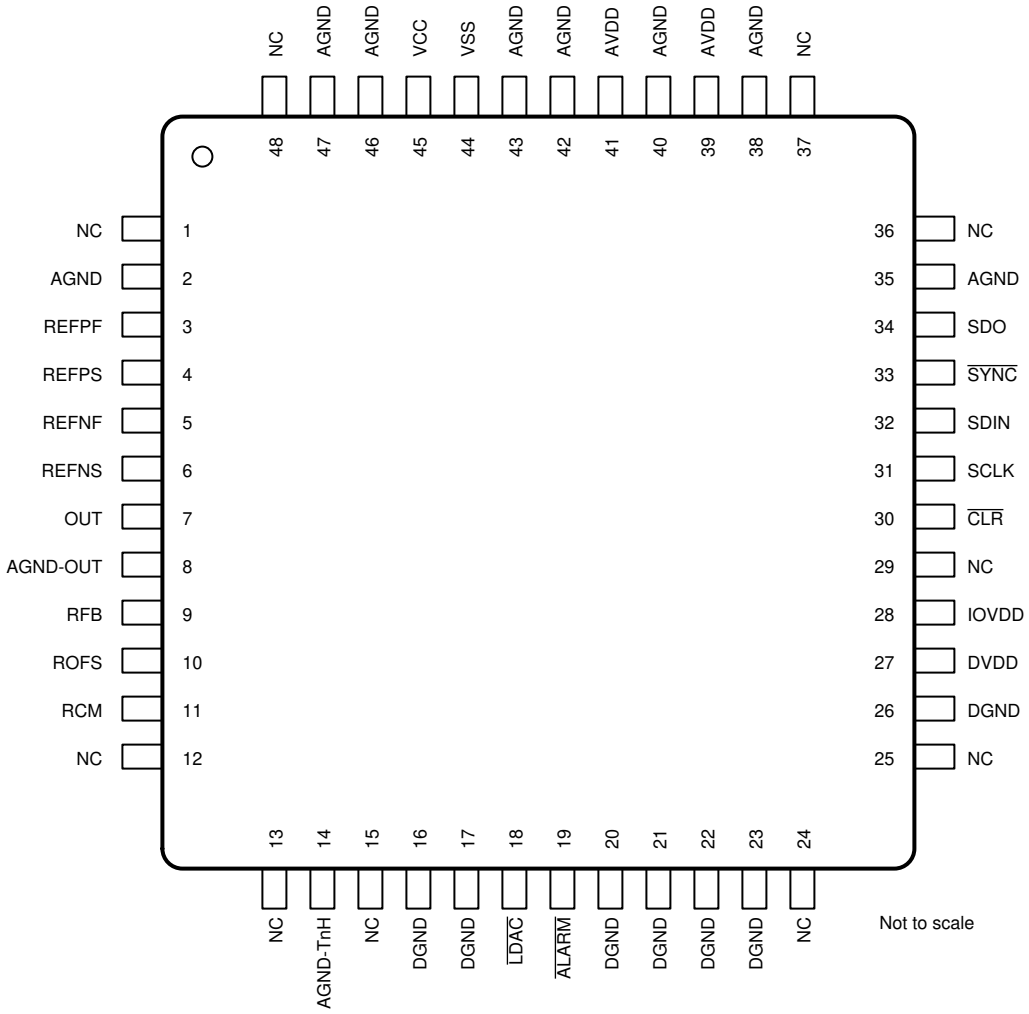

Figure 5-1. PFB Package, 48-Pin TQFP, Top View

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Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	2, 35, 38, 40, 42, 43, 46, 47	Analog ground	Connect to 0 V.
AGND-OUT	8	Analog ground	Connect to 0 V. Measure DAC output voltage with respect to this node.
AGND-TnH	14	Analog ground	Connect to 0 V. Integrated deglitcher clock ground.
$\overline{\text{ALARM}}$	19	Output	Alarm output
AVDD	39, 41	Power	Positive low voltage analog power supply
$\overline{\text{CLR}}$	30	Input	DAC registers clear pin, active low
DGND	16, 17, 20, 21, 22, 23, 26	Digital ground	Connect to 0 V.
DVDD	27	Power	Digital power supply pin
RFB	9	Input	Integrated precision resistor feedback node
IOVDD	28	Power	Interface power supply pin
$\overline{\text{LDAC}}$	18	Input	Load DAC pin, active low
NC	1, 12, 13, 15, 24, 25, 29, 36, 37, 48	—	No connection, leave floating
OUT	7	Output	Unbuffered voltage output
RCM	11	Input	Integrated precision resistor common-mode node
REFNF	5	Input	External negative reference input. Connect to 0 V for unipolar DAC output.
REFNS	6	Input	External negative reference sense node
REFPF	3	Input	External positive reference input
REFPS	4	Input	External positive reference sense node
ROFS	10	Input	Integrated precision resistor offset node
SCLK	31	Input	Serial clock input of serial peripheral interface (SPI). Schmitt-trigger logic input. Data are transferred at rates of up to 50 MHz.
SDIN	32	Input	Serial data input. Schmitt-trigger logic input. Data are clocked into the input shift register on the falling edge of the serial clock input.
SDO	34	Output	Serial data output. Data are valid on the falling edge of SCLK.
$\overline{\text{SYNC}}$	33	Input	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{SYNC}}$ is low. When $\overline{\text{SYNC}}$ is high, the SDO pin is in high-impedance status.
VCC	45	Power	Analog positive power supply
VSS	44	Power	Analog negative power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Positive supply voltage	AV_{DD} to AGND	–0.3	7	V
		V_{CC} to V_{SS}	–0.3	40	
		V_{CC} to AGND	–0.3	40	
	Negative supply voltage	V_{SS} to AGND	–19	0.3	V
	Digital and IO supply voltage	DV_{DD}, IOV_{DD} to DGND	–0.3	7	V
	Positive reference voltage	V_{REFPF} to V_{REFNF}	–0.3	40	V
		V_{REFPF} to V_{CC}	–0.3	V_{CC} + 0.3	
		V_{REFPF} to AGND	–0.3	40	
	Negative reference voltage	V_{REFNF} to AGND	–19	0.3	V
		V_{REFNF} to V_{SS}	V_{SS} – 0.3	0.3	
	Digital input(s) to DGND		DGND – 0.3	IOV_{DD} + 0.3	V
	OUT, RFB, RCM, ROFS pin voltage	to AGND (V_{SS} = AGND)	V_{SS}	V_{CC}	V
		to V_{SS}	0	V_{CC}	
	Alarm pin voltage, $\overline{ALARM}$ to DGND		–0.3	DV_{DD} + 0.3	V
	Digital output, SDO to DGND		–0.3	DV_{DD} + 0.3	V
	Current into any pin		–10	10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	AV_{DD} to AGND	4.5		5.5	V
	V_{SS} to AGND	–18		–3	V
	V_{CC} to AGND	8		33	V
	V_{CC} to V_{SS}	11		36	V
	DV_{DD} to DGND	2.7		5.5	V
	IOV_{DD} to DGND	1.7		5.5	V
	AGND to DGND	–0.3		0.3	V
	V_{IH} digital input high voltage	0.7 × IOV_{DD}			V
	V_{IL} digital input low voltage			0.3 × IOV_{DD}	V
	V_{REFPF} to AGND	3		15	V
	V_{REFNF} to AGND	–15		0	V
	V_{REFPF} to V_{REFNF}	3		30	V
T_A	Operating temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DAC11001B PFB (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution		20			Bits
INL	Relative accuracy(2) (3)	T_A = 0°C to 70°C(4) V_{REFPF} = 10 V and V_{REFNF} = 0 V V_{REFPF} = +5 V and V_{REFNF} = –5 V	–1		1	LSB
		T_A = 0°C to 70°C(4)	–1.25		1.25	
		T_A = –40°C to +125°C	–2		2	
	Relative accuracy drift over time(2)	T_A = 25°C, 1000 hrs		±0.1		LSB
DNL	Differential nonlinearity(2) (3)	T_A = –40°C to +125°C	–1		1	LSB
	Zero code error(4)	T_A = 0°C to 70°C, code 0d into DAC, unipolar ranges only	–4		4	LSB
		T_A = –40°C to +125°C, code 0d into DAC, unipolar ranges only	–4		4	
		T_A = 25°C, unipolar ranges only		±2		
	Zero code error temperature coefficient	T_A = 0°C to 70°C, code 0d into DAC, unipolar ranges only		±0.04		ppm FSR/°C
		T_A = –40°C to +125°C, code 0d into DAC, unipolar ranges only		±0.04		
	Gain error(2) (4)	T_A = 0°C to 70°C	–8		8	ppm of FSR
		T_A = –40°C to +125°C	–10		10	
		T_A = 25°C		±2		
	Gain error temperature coefficient	T_A = 0°C to 70°C		±0.04		ppm FSR/°C
		T_A = –40°C to +125°C		±0.04		
	Positive full-scale error(4)	T_A = 0°C to 70°C, code 1048575d into DAC	–8		8	LSB
		T_A = –40°C to +125°C, code 1048575d into DAC	–10		10	
		T_A = 25°C, code 1048575d into DAC		±2		
	Full-scale error temperature coefficient	T_A = 0°C to 70°C		±0.04		ppm FSR/°C
		T_A = –40°C to +125°C		±0.04		
OUTPUT CHARACTERISTICS						
	Headroom	From V_{REFPF} to V_{CC}	5			V
	Footroom	From V_{REFNF} to V_{SS}	5			V
	DC impedance	From ROFS to RCM		5		kΩ
		From RCM to RFB		5		
Z_O	DC output impedance			2.5		kΩ
	Power supply rejection ratio (dc)	V_{CC} = 15 V ±20%, V_{SS} = –15 V		1.5		µV/V
		V_{CC} = 15 V, V_{SS} = –15 V ±20%		1		
	Output voltage drift over time	T_A = 25°C, V_{OUT} = midscale, 1000 hr		1		ppm of FSR
VOLTAGE REFERENCE INPUT						
	Reference input impedance (REFPF)	DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		5.5		kΩ
	Reference input impedance (REFNF)	DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		7		

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6.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
t_s	Output voltage settling time(5)	Full-scale settling to 0.1%FSR, V_{REFPF} = 10 V, V_{REFNF} = 0 V		1		µs
		Full-scale settling to ±1 LSB, V_{REFPF} = 10 V, V_{REFNF} = 0 V		3		
		1-mV step settling to ±1 LSB, V_{REFPF} = 10 V, V_{REFNF} = 0 V		2.5		
SR	Slew rate(6)	Full-scale step, measured at OUT pin, V_{REFPF} = 10 V, V_{REFNF} = 0 V		30		V/µs
	Power-on glitch magnitude	Measured at unbuffered DAC voltage output, V_{REFPF} = 10 V, V_{REFNF} = 0 V		–0.2		V
V_n	Output noise	0.1-Hz to 10-Hz, DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		0.4		µVpp
		100-kHz bandwidth, DAC at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		3		µVrms
	Output noise density	Measured at 1 kHz, 10 kHz, 100 kHz, DAC at mid scale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		7		nV/√Hz
SFDR	Spurious free dynamic range(6)	DAC update rate = 768 kHz, f_{OUT} = 1 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 30-kHz output filter		–120		dB
		DAC update rate = 768 kHz, f_{OUT} = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 30-kHz output filter		–114		
		DAC update rate = 1 MHz, f_{OUT} = 100 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 150-kHz output filter		–92		
THD	Total harmonic distortion(6)	DAC update rate = 768 kHz, f_{OUT} = 1 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 30-kHz output filter		–118		dB
		DAC update rate = 768 kHz, f_{OUT} = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 30-kHz output filter		–118		
		DAC update rate = 1 MHz, f_{OUT} = 100 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = –4.5 V, sixth-order, low-pass, 150-kHz output filter		–96		
	Power supply rejection ratio (ac)	200-mV, 50-Hz or 60-Hz sine wave superimposed on V_{SS}, V_{CC} = 15 V		95		dB
		200-mV, 50 Hz or 60 Hz sine wave superimposed on V_{CC}, V_{SS} = –15 V		95		
	Code change glitch impulse	±1 LSB change around mid code (including feedthrough), V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at output of buffer op amp		1		nV-s
	Code change glitch impulse magnitude	±1 LSB change around mid code (including feedthrough), V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at output of buffer op amp		5		mV
	Reference feedthrough	V_{REFPF} = 10 V ± 10%, V_{REFNF} = 0 V, frequency = 100 Hz, DAC at zero scale		–90		dB
		V_{REFNF} = –10 V ± 10%, V_{REFPF} = 10 V, frequency = 100 Hz, DAC at full scale		–90		
	Digital feedthrough	SCLK = 1 MHz, DAC static at midscale, V_{REFPF} = 10 V, V_{REFNF} = 0 V		1		nV-s

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6.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{CC} = +15 V, V_{SS} = –15 V, AV_{DD} = 5.5 V, DV_{DD} = 3.3 V, IOV_{DD} = 1.8 V, see note(1) for V_{REFPF} and V_{REFNF}, OUT pin buffered with unity gain OPA827, ROFS, RCM, RFB unconnected, and all typical specifications at T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
	Hysteresis voltage			0.4		V
	Input current			±5		µA
	Pin capacitance	Per pin		10		pF
DIGITAL OUTPUTS						
V_{OL}	Low-level output voltage	Sinking 200 µA			0.4	V
V_{OH}	High-level output voltage	Sourcing 200 µA	IOV_{DD} – 0.5			V
	High impedance leakage			±5		µA
	High impedance output capacitance			10		pF
POWER						
I_{AVDD}	Current flowing into AV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			2.5	mA
I_{VCC}	Current flowing into V_{CC}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			15	mA
I_{VSS}	Current flowing into V_{SS}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			15	mA
I_{DVDD}	Current flowing into DV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code		0.5		mA
I_{IOVDD}	Current flowing into IOV_{DD}	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code, all digital input pins static at IOV_{DD}		0.1		mA
I_{REFPF}	Reference input current (V_{REFPF})	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			7	mA
I_{REFNF}	Reference input current (V_{REFNF})	V_{REFPF} = 10 V, V_{REFNF} = 0 V, midscale code			7	mA

(1) Specified for the following pairs: V_{REFPF} = 5 V and V_{REFNF} = 0 V; V_{REFPF} = 10 V and V_{REFNF} = 0 V; V_{REFPF} = 5 V and V_{REFNF} = –5 V; V_{REFPF} = 10 V and V_{REFNF} = –10 V.
(2) Calculated between code 0d to 1048575d.
(3) With device temperature calibration mode enabled and used.
(4) Specified by design, not production tested.
(5) Adaptive TnH mode. TnH action is disabled for large code steps. For small steps, TnH action happens with a hold time of 1.2 µs.
(6) OUT pin buffered with unity gain OPA828.

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6.6 Timing Requirements: Write, 4.5 V ≤ DV_{DD} ≤ 5.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency, 1.7 V ≤ IOV_{DD} < 2.7 V			33	MHz
	SCLK frequency, 2.7 V ≤ IOV_{DD} ≤ 5.5 V			50	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V	13			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	8			
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	23			ns
	$\overline{SYNC}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	18			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V	15			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	10			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V	55			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{SYNC}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	5			
t_{LDACSL}	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	50			ns
	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	50			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	20			ns
	$\overline{CLR}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			

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6.7 Timing Requirements: Write, 2.7 V ≤ DV_{DD} < 4.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency, 1.7 V ≤ IOV_{DD} < 2.7 V			20	MHz
	SCLK frequency, 2.7 V ≤ IOV_{DD} ≤ 5.5 V			25	
$t_{SCLKHIGH}$	SCLK high time, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
$t_{SCLKLOW}$	SCLK low time, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V	21			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	16			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V	21			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	16			
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	41			ns
	$\overline{SYNC}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	36			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V	25			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	20			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V	100			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	100			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V	10			ns
	SCLK falling edge to $\overline{SYNC}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	5			
t_{LDACSL}	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V	100			ns
	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	100			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	40			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	40			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V	40			ns
	$\overline{CLR}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V	40			

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6.8 Timing Requirements: Read and Daisy-Chain Write, 4.5 V ≤ DV_{DD} ≤ 5.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0			10	MHz
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1			20	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0			15	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1			30	
$t_{SCLKHIGH}$	SCLK high time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	50			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	25			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	33			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	16			
$t_{SCLKLOW}$	SCLK low time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	50			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	25			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	33			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	16			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V		13			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		8			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V		13			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		8			
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		30			ns
	$\overline{SYNC}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		20			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V		15			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		10			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V		55			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		50			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V		10			ns
	SCLK falling edge to $\overline{SYNC}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		5			
t_{LDACSL}	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		50			ns
	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		50			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		20			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		20			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		20			ns
	$\overline{CLR}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		20			
t_{SDODLY}	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0		0		35	ns
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0		0		25	
	SCLK falling edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1		0		35	
	SCLK falling edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1		0		25	
t_{SDOZ}	$\overline{SYNC}$ rising edge to SDO HiZ, 1.7 V ≤ IOV_{DD} < 2.7 V		0		20	ns
	$\overline{SYNC}$ rising edge to SDO HiZ, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		0		20	

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6.9 Timing Requirements: Read and Daisy-Chain Write, 2.7 V ≤ DV_{DD} < 4.5 V

all input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of IOV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0			8	MHz
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1			16	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0			10	
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1			20	
$t_{SCLKHIGH}$	SCLK high time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	62			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	31			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	50			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	25			
$t_{SCLKLOW}$	SCLK low time	1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0	62			ns
		1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1	31			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0	50			
		2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1	25			
t_{SDIS}	SDI setup, 1.7 V ≤ IOV_{DD} < 2.7 V		21			ns
	SDI setup, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		16			
t_{SDIH}	SDI hold, 1.7 V ≤ IOV_{DD} < 2.7 V		21			ns
	SDI hold, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		16			
t_{CSS}	$\overline{SYNC}$ falling edge to SCLK falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		41			ns
	$\overline{SYNC}$ falling edge to SCLK falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		36			
t_{CSH}	SCLK falling edge to $\overline{SYNC}$ rising edge, 1.7 V ≤ IOV_{DD} < 2.7 V		25			ns
	SCLK falling edge to $\overline{SYNC}$ rising edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		20			
t_{CSHIGH}	$\overline{SYNC}$ high time, 1.7 V ≤ IOV_{DD} < 2.7 V		100			ns
	$\overline{SYNC}$ high time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		100			
$t_{CSIGNORE}$	SCLK falling edge to $\overline{SYNC}$ ignore, 1.7 V ≤ IOV_{DD} < 2.7 V		10			ns
	SCLK falling edge to $\overline{SYNC}$ ignore, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		5			
t_{LDACSL}	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 1.7 V ≤ IOV_{DD} < 2.7 V		100			ns
	Synchronous update: $\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		100			
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		40			ns
	$\overline{LDAC}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		40			
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ IOV_{DD} < 2.7 V		40			ns
	$\overline{CLR}$ low time, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		40			
t_{SDODLY}	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 0		0		40	ns
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 0		0		30	
	SCLK rising edge to SDO valid data, 1.7 V ≤ IOV_{DD} < 2.7 V, FSDO = 1		0		40	
	SCLK rising edge to SDO valid data, 2.7 V ≤ IOV_{DD} ≤ 5.5 V, FSDO = 1		0		30	
t_{SDOZ}	$\overline{SYNC}$ rising edge to SDO HiZ, 1.7 V ≤ IOV_{DD} < 2.7 V		0		20	ns
	$\overline{SYNC}$ rising edge to SDO HiZ, 2.7 V ≤ IOV_{DD} ≤ 5.5 V		0		20	

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6.10 Timing Diagrams

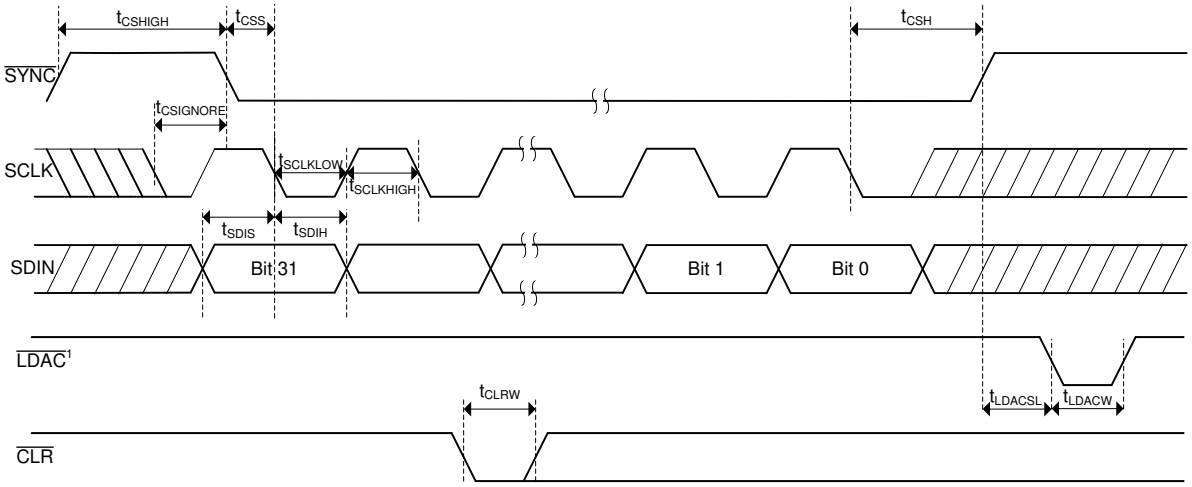

Figure 6-1. Serial Interface Write Timing: Standalone Mode

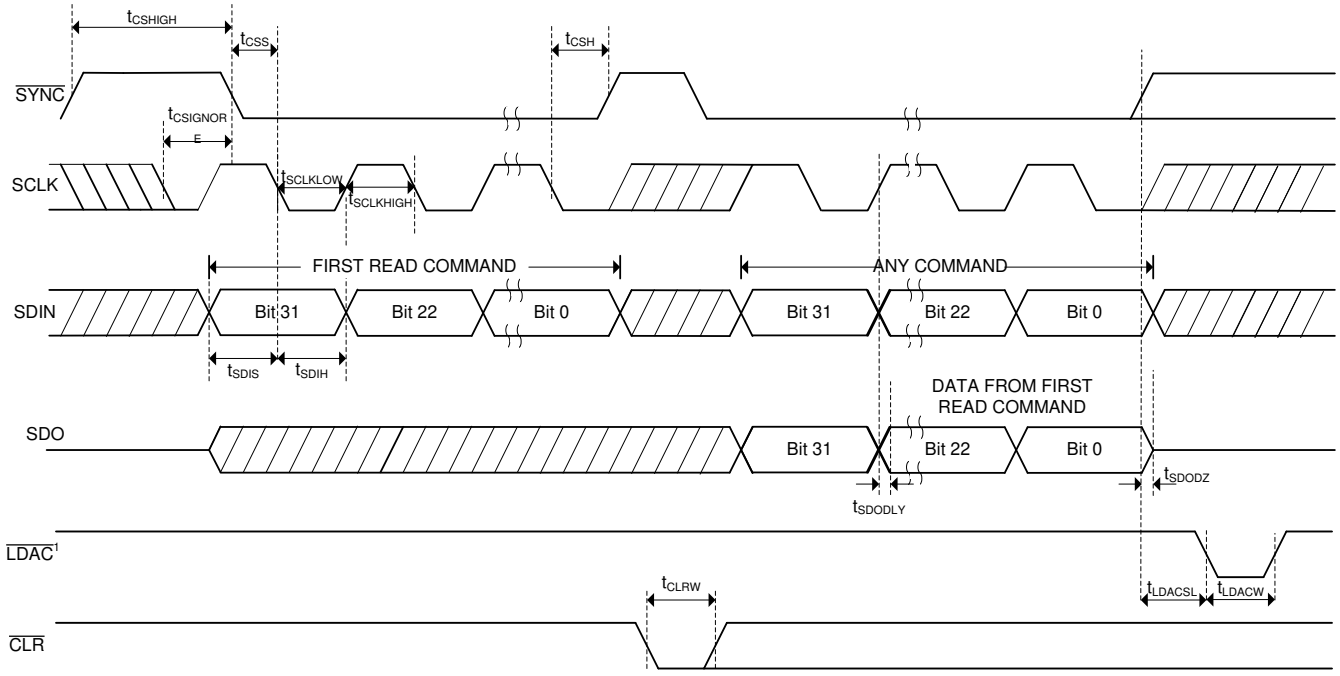

Figure 6-2. Serial Interface Read and Write Timing: Daisy-Chain Mode

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6.11 Typical Characteristics

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)

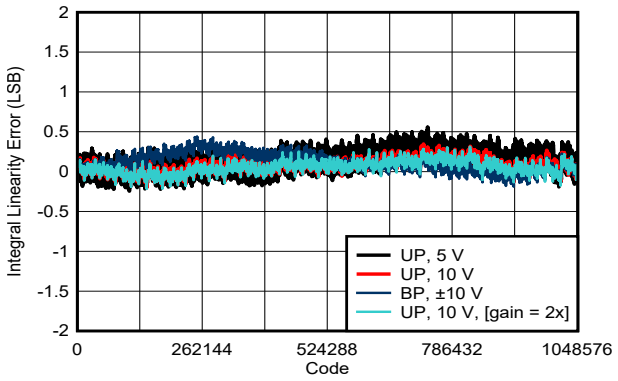


Figure 6-3. Integral Linearity Error vs Digital Input Code

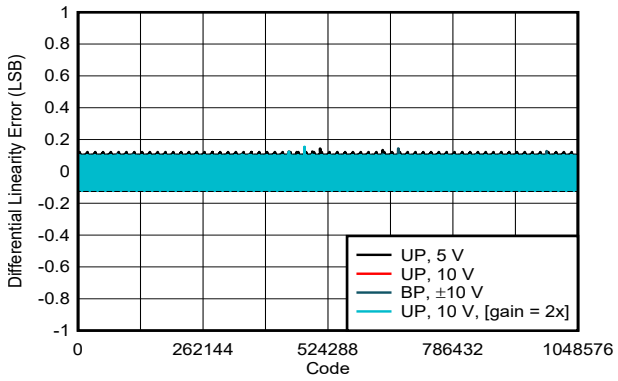
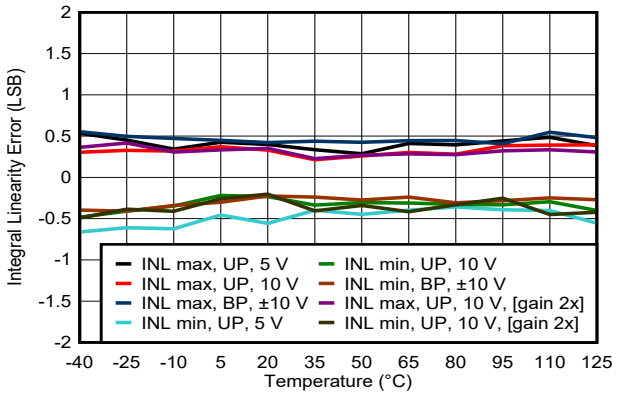
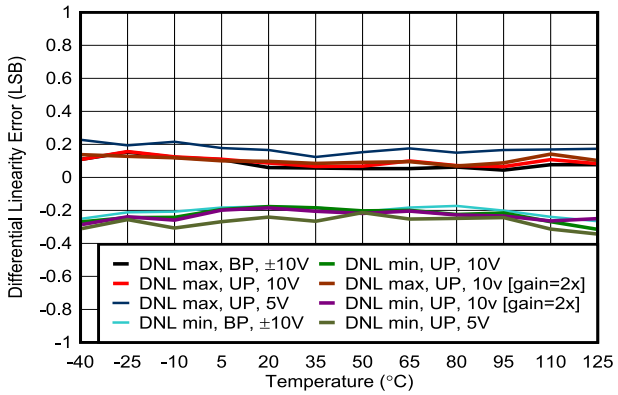


Figure 6-4. Differential Linearity Error vs Digital Input Code



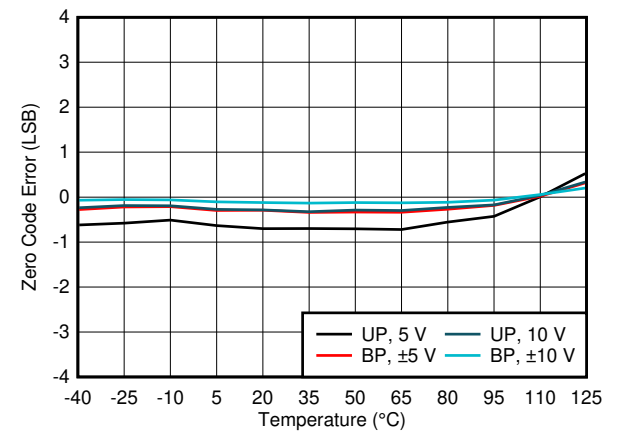
Temperature calibration enabled

Figure 6-5. Integral Linearity Error vs Temperature



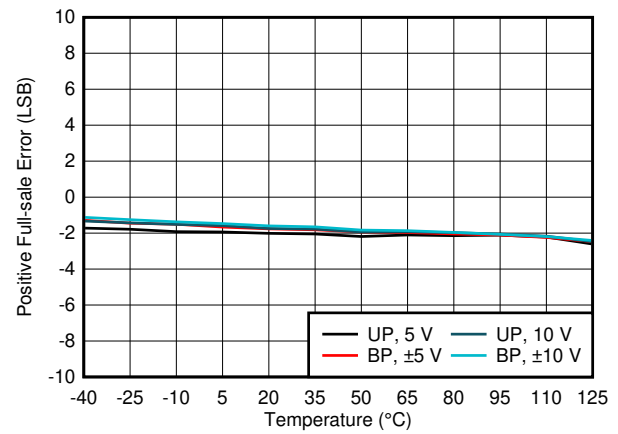
Temperature calibration enabled

Figure 6-6. Differential Linearity Error vs Temperature



Temperature calibration enabled

Figure 6-7. Zero Code Error vs Temperature



Temperature calibration enabled

Figure 6-8. Positive Full-Scale Error vs Temperature

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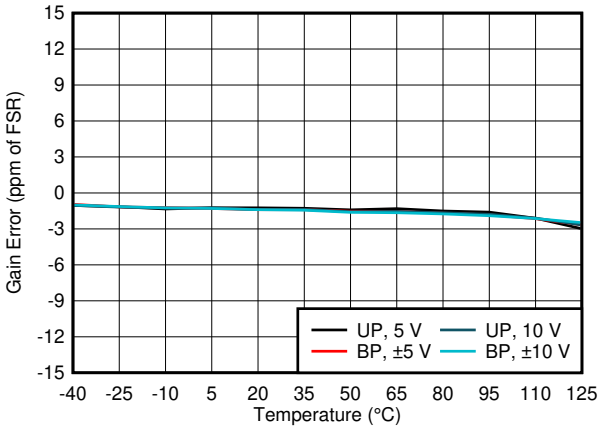
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



Temperature calibration enabled

Figure 6-9. Gain Error vs Temperature

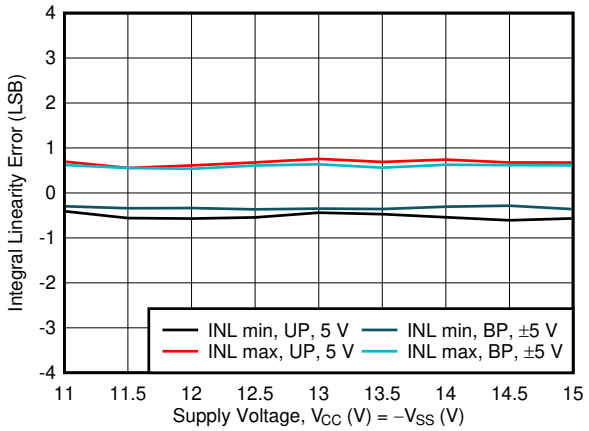


Figure 6-10. Integral Linearity Error vs Supply Voltage

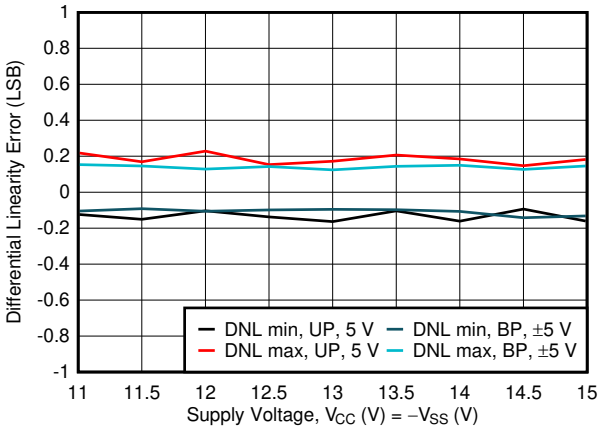


Figure 6-11. Differential Linearity Error vs Supply Voltage

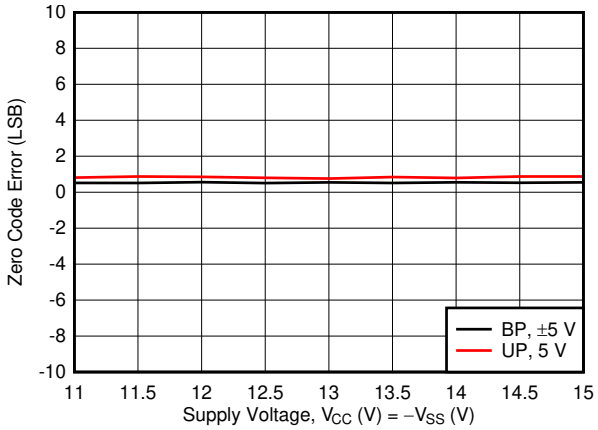


Figure 6-12. Zero Code Error vs Supply Voltage

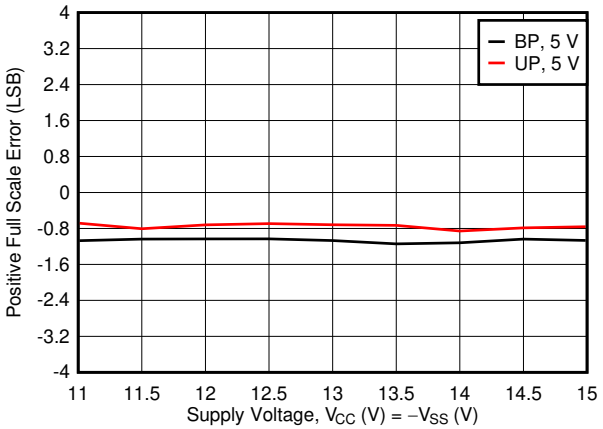


Figure 6-13. Positive Full-Scale Error vs Supply Voltage

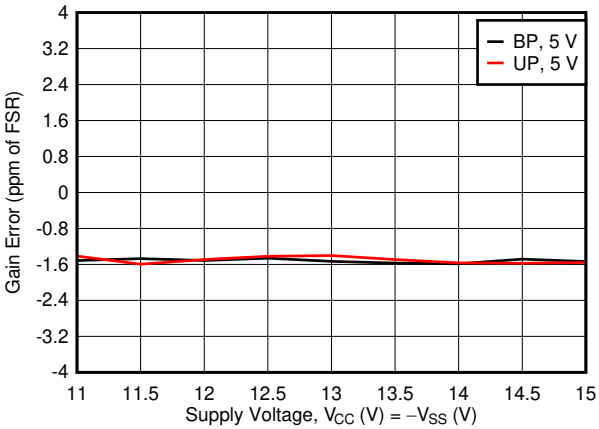


Figure 6-14. Gain Error vs Supply Voltage

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6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)

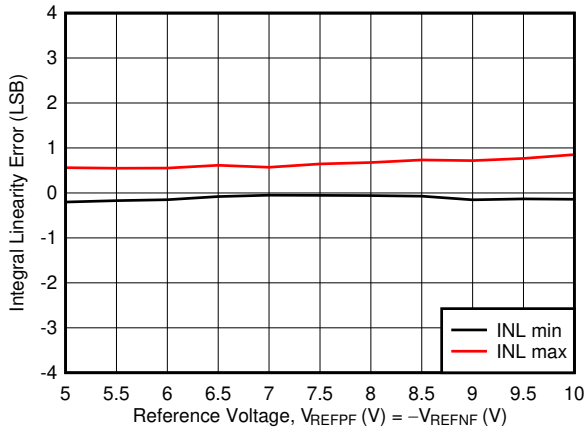


Figure 6-15. Integral Linearity Error vs Reference Voltage

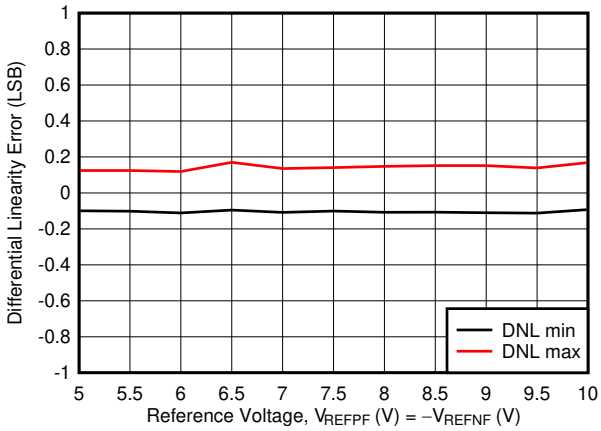


Figure 6-16. Differential Linearity Error vs Reference Voltage

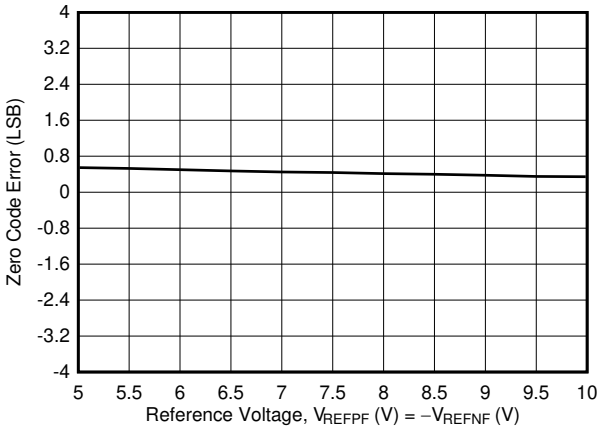


Figure 6-17. Zero Code Error vs Reference Voltage

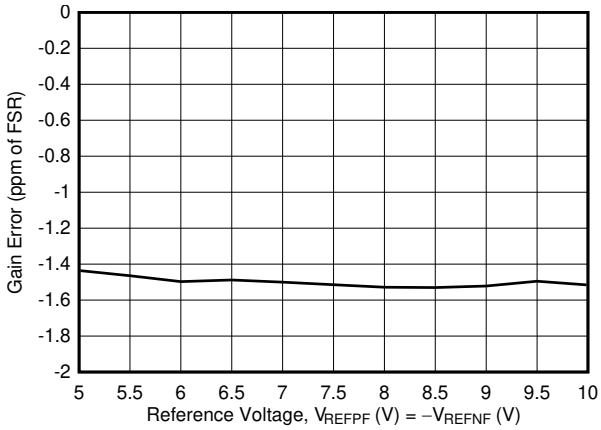


Figure 6-18. Gain Error vs Reference Voltage

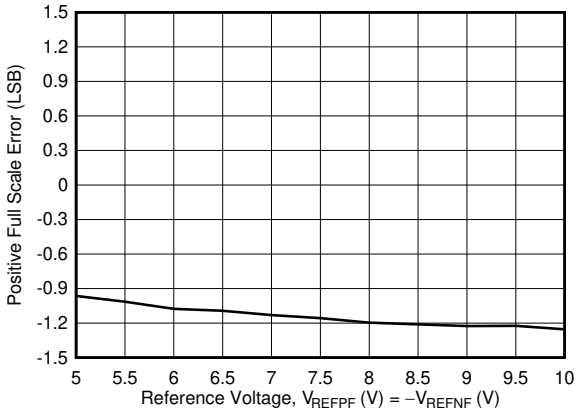
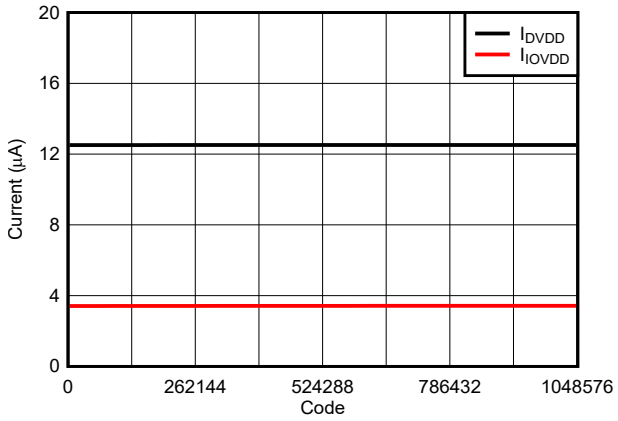


Figure 6-19. Positive Full-Scale Error vs Reference Voltage



V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-20. Supply Current (DV_{DD} and IOV_{DD}) vs Digital Input Code

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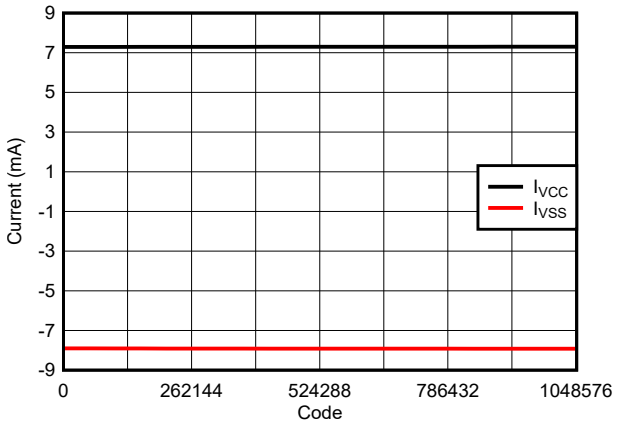
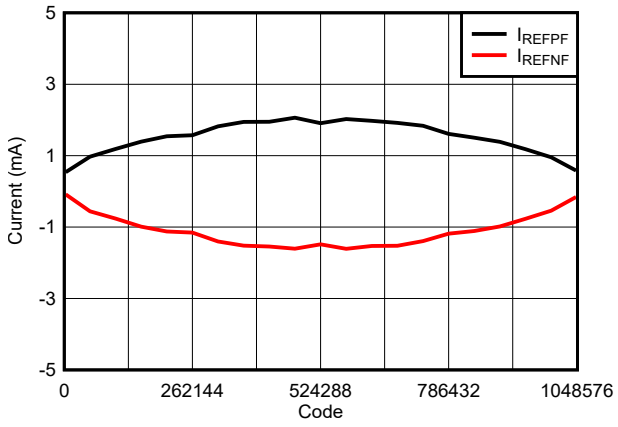
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



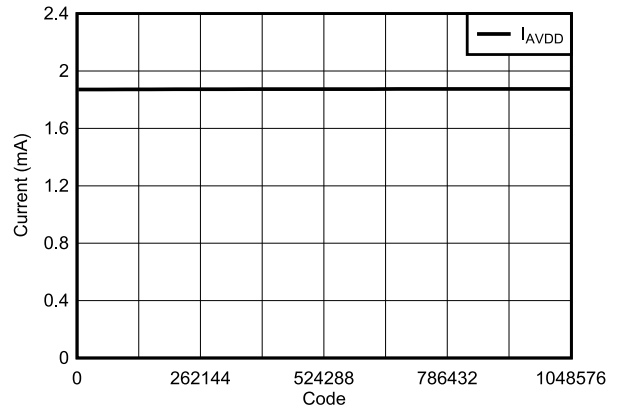
V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-21. Supply Current (V_{CC} and V_{SS}) vs Digital Input Code



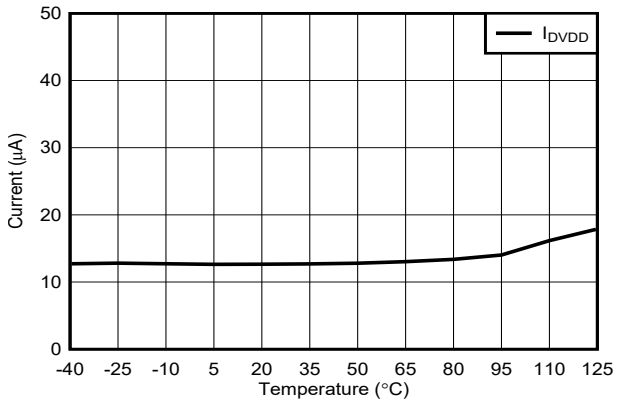
V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-22. Reference Current (V_{REFPF} and V_{REFNF}) vs Digital Input Code



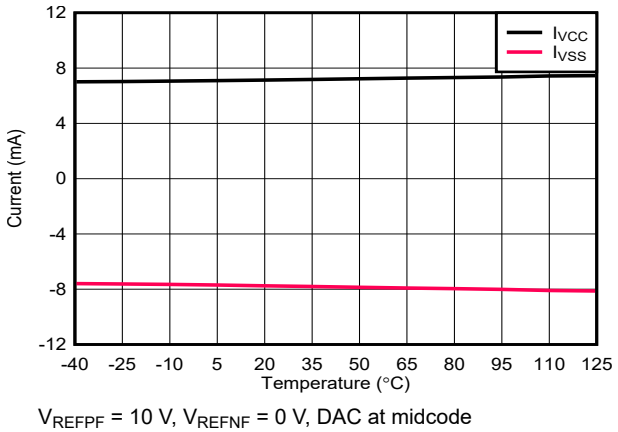
V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-23. Supply Current (AV_{DD}) vs Digital Input Code



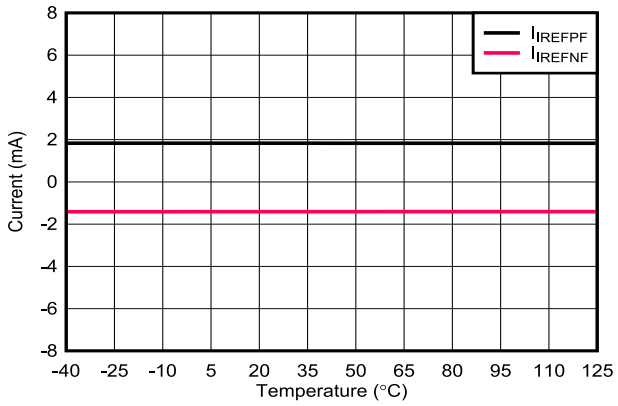
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-24. Supply Current (DV_{DD}) vs Temperature



V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-25. Supply Current (V_{CC} and V_{SS}) vs Temperature



V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-26. Reference Current (V_{REFPF} and V_{REFNF}) vs Temperature

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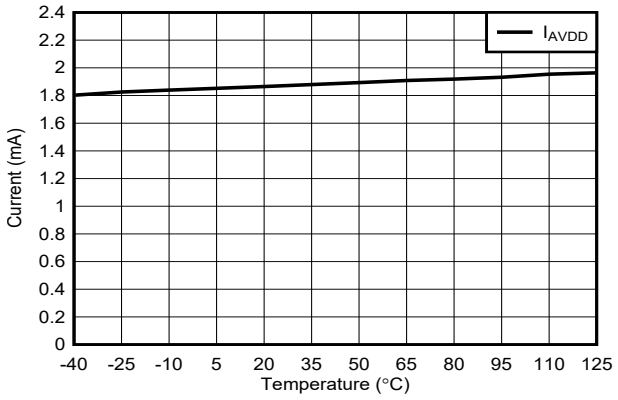
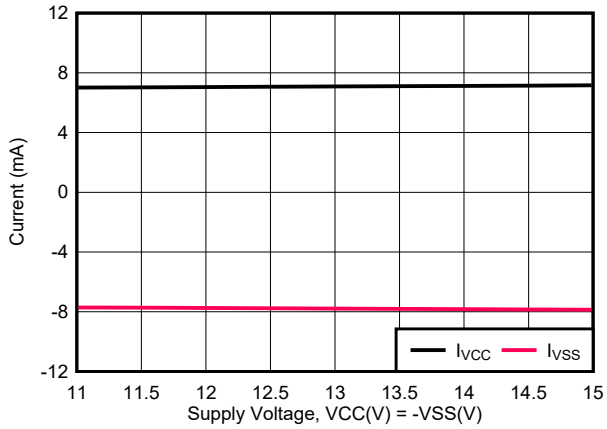
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



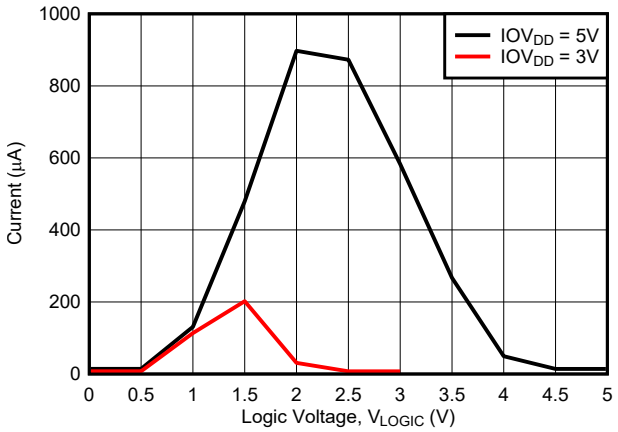
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-27. Supply Current (AV_{DD}) vs Temperature



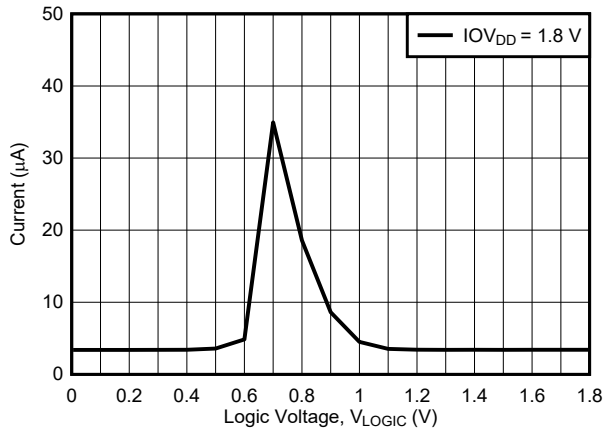
V_{REFPF} = 5 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-28. Supply Current (V_{CC} and V_{SS}) vs Supply Voltage



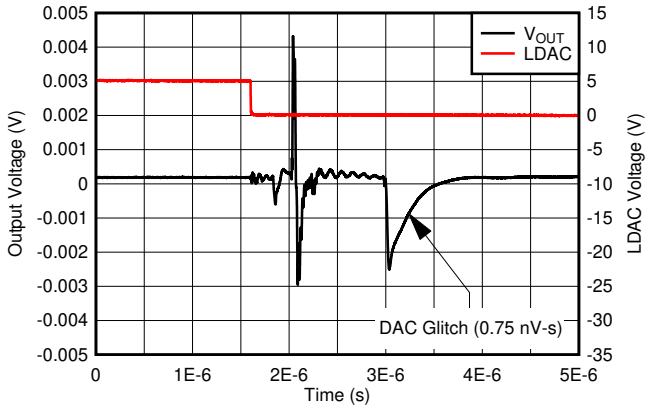
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-29. Supply Current (IOV_{DD}) vs Input Pin Logic Level



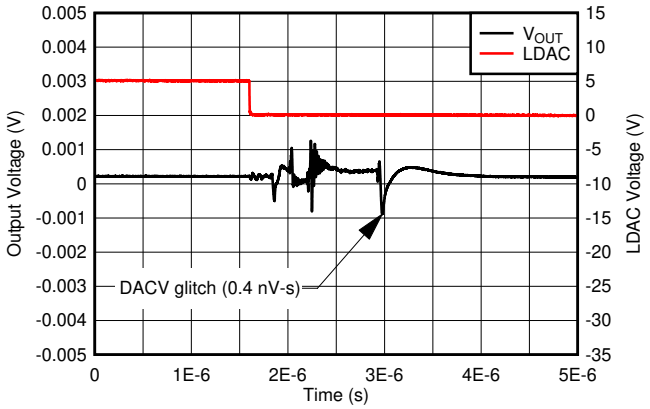
V_{REFPF} = 10 V, V_{REFNF} = 0 V, DAC at midcode

Figure 6-30. Supply Current (IOV_{DD}) vs Input Pin Logic Level



V_{REFPF} = 10 V, V_{REFNF} = –10 V,
DAC transition midcode – 1 to midcode

Figure 6-31. Glitch Impulse, Rising Edge, 1-LSB Step



V_{REFPF} = 10 V, V_{REFNF} = –10 V,
DAC transition midcode to midcode – 1

Figure 6-32. Glitch Impulse, Falling Edge, 1-LSB Step

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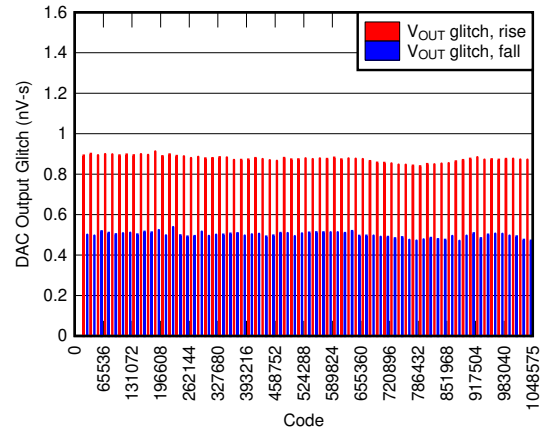
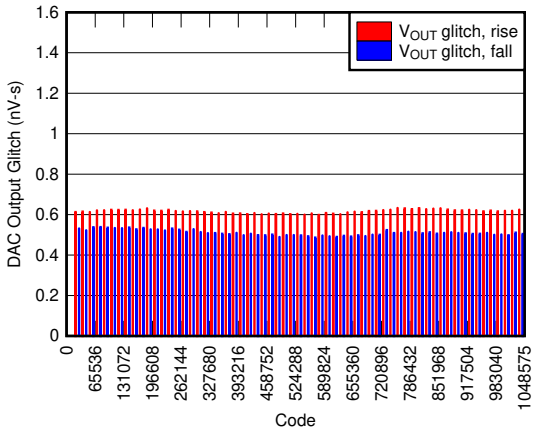
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



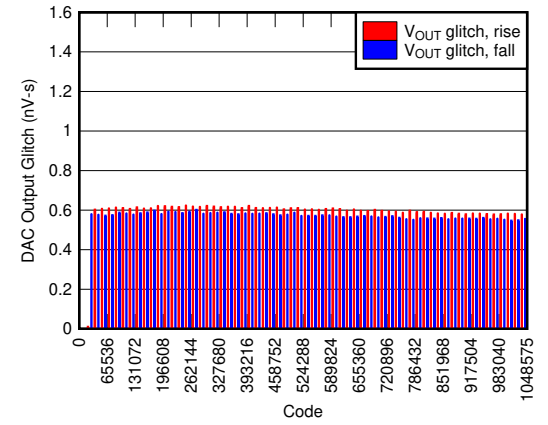
V_{REFPF} = 10 V, V_{REFNF} = –10 V

Figure 6-33. Segment Glitch Impulse, 1-LSB Step



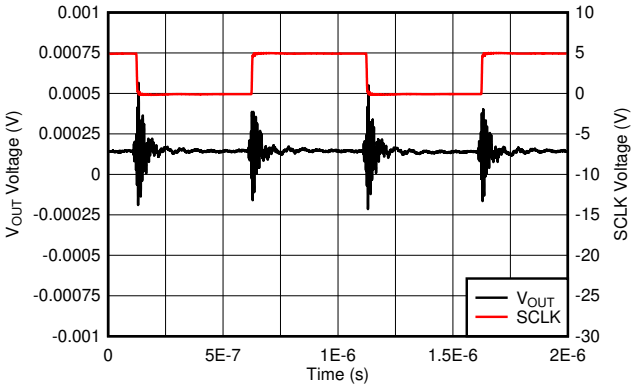
V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-34. Segment Glitch Impulse, 1-LSB Step



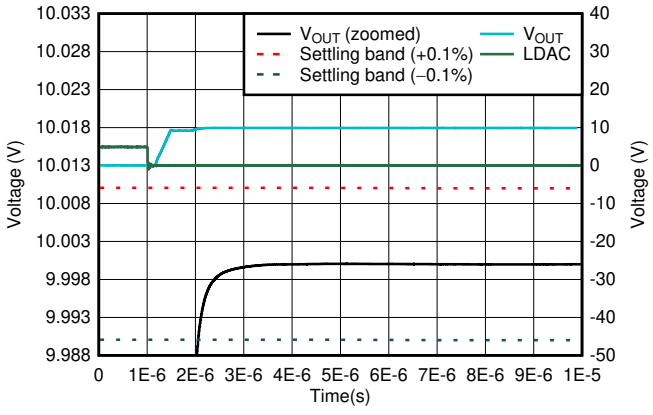
V_{REFPF} = 5 V, V_{REFNF} = 0 V

Figure 6-35. Segment Glitch Impulse, 1-LSB Step



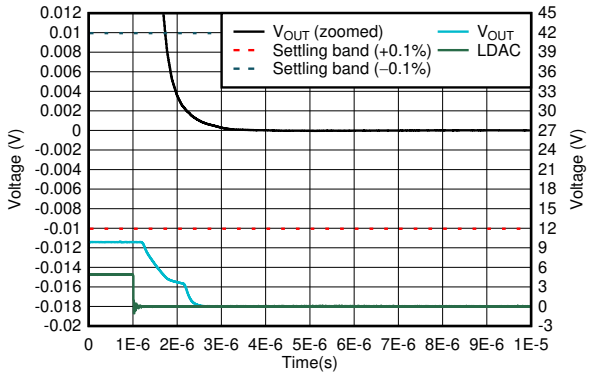
V_{REFPF} = 10 V, V_{REFNF} = 0 V,
DAC at midcode, measured at DAC output pin

Figure 6-36. Clock Feedthrough



V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-37. Full-Scale Settling Time, Rising Edge



V_{REFPF} = 10 V, V_{REFNF} = 0 V

Figure 6-38. Full-Scale Settling Time, Falling Edge

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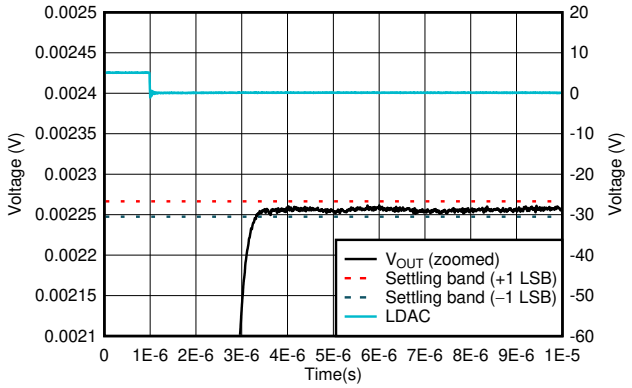
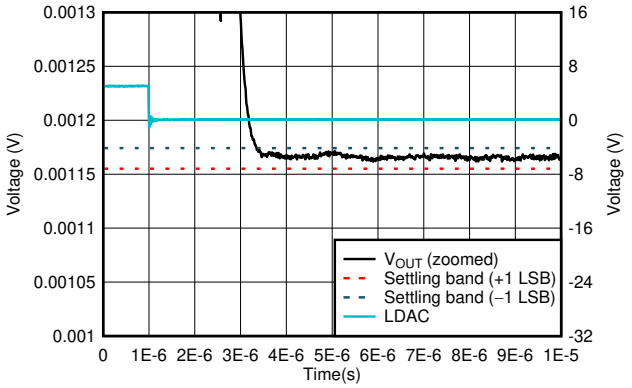
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



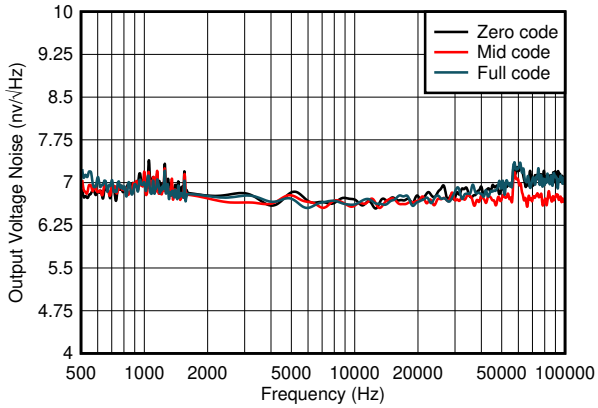
V_{REFPF} = 10 V, V_{REFNF} = 0 V,
DAC transitions 100 codes around midscale

Figure 6-39. 100 Codes Settling Time, Rising Edge



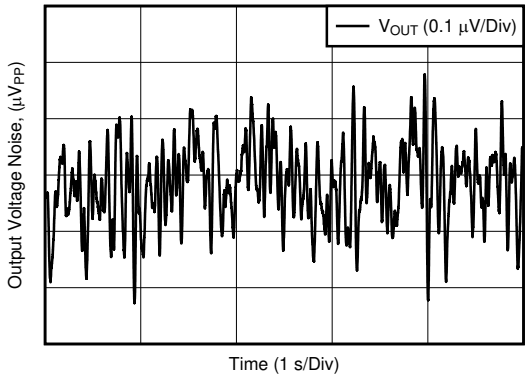
V_{REFPF} = 10 V, V_{REFNF} = 0 V,
DAC transitions 100 codes around midscale

Figure 6-40. 100 Codes Settling Time, Falling Edge



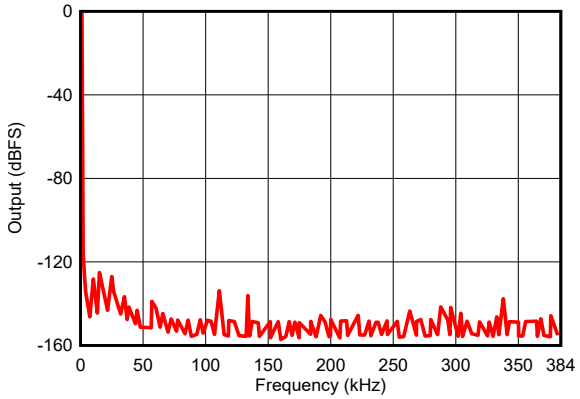
V_{REFPF} = 10 V, V_{REFNF} = 0 V, measured at DAC output

Figure 6-41. DAC Output Noise Spectral Density



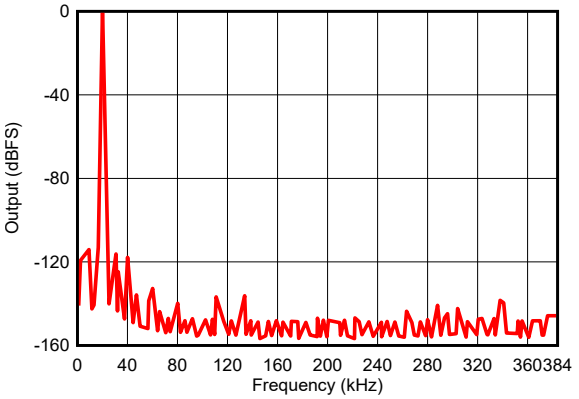
V_{REFPF} = 10 V, V_{REFNF} = 0 V,
DAC at midcode, measured at DAC output pin

Figure 6-42. DAC Output Noise: 0.1 Hz to 10 Hz



DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V,
sixth-order, low-pass, 30-kHz output filter

Figure 6-43. 1-kHz Spectrum vs Frequency



DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V,
sixth-order, low-pass, 30-kHz output filter

Figure 6-44. 20-kHz Spectrum vs Frequency

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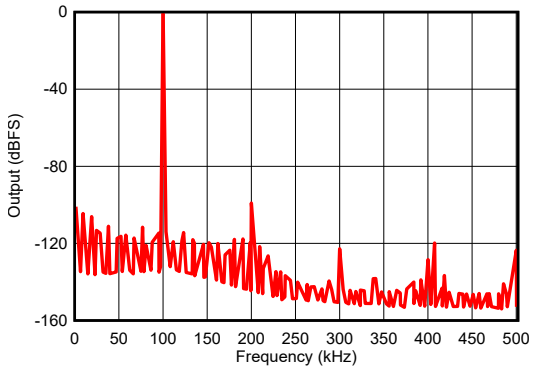
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)

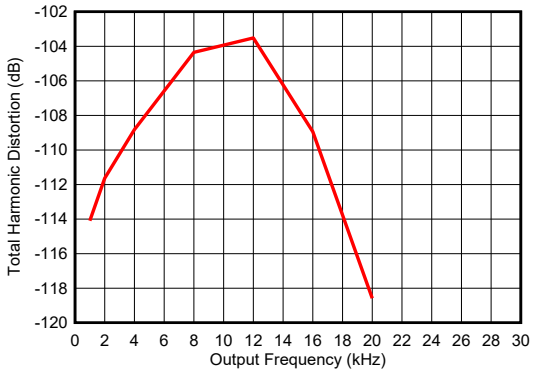


DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-45. 100-kHz Spectrum vs Frequency

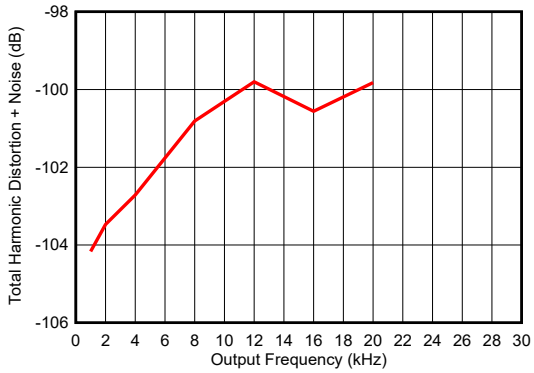
DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-46. Spurious Free Dynamic Range vs Output Frequency, f_{DAC} = 768 kHz



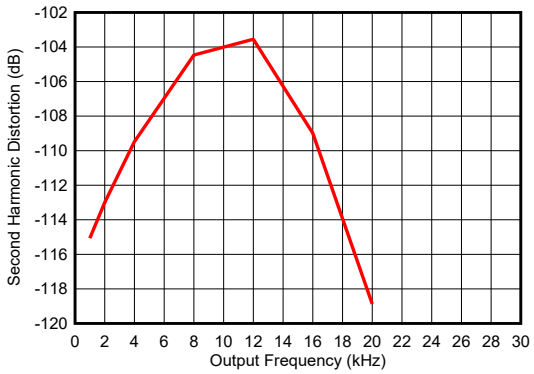
DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-47. Total Harmonic Distortion vs Output Frequency, f_{DAC} = 768 kHz



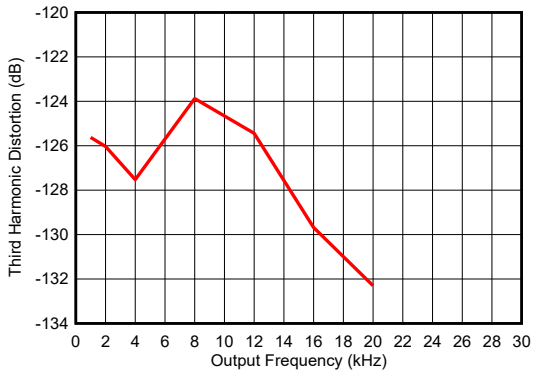
DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-48. Total Harmonic Distortion + Noise vs Output Frequency, f_{DAC} = 768 kHz



DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-49. Second Harmonic Distortion vs Output Frequency, f_{DAC} = 768 kHz



DAC update rate = 768 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-50. Third Harmonic Distortion vs Output Frequency, f_{DAC} = 768 kHz

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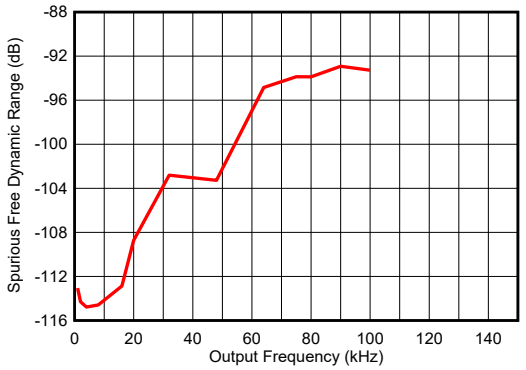
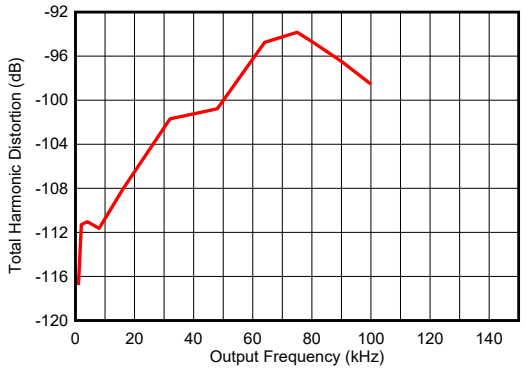
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



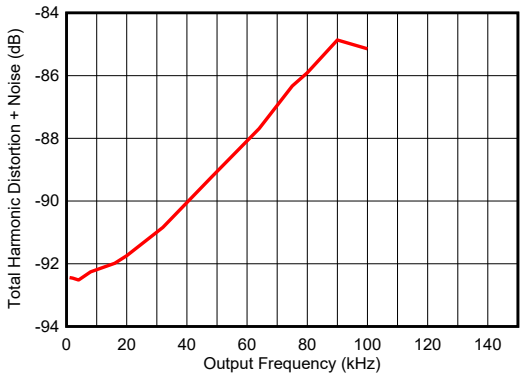
DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-51. Spurious Free Dynamic Range vs Output Frequency, f_{DAC} = 1 MHz



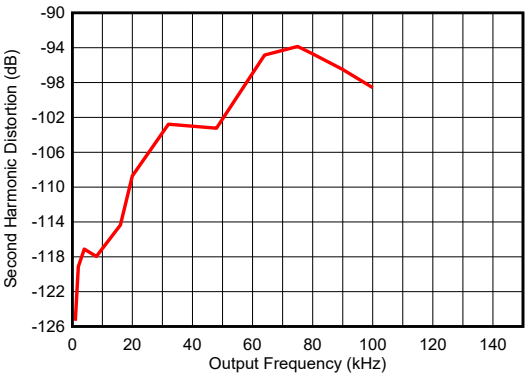
DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-52. Total Harmonic Distortion vs Output Frequency, f_{DAC} = 1 MHz



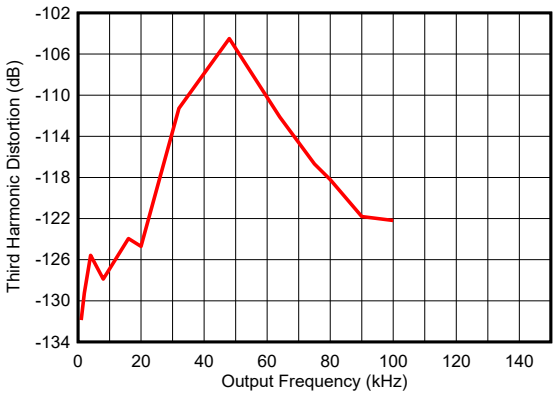
DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-53. Total Harmonic Distortion + Noise vs Output Frequency, f_{DAC} = 1 MHz



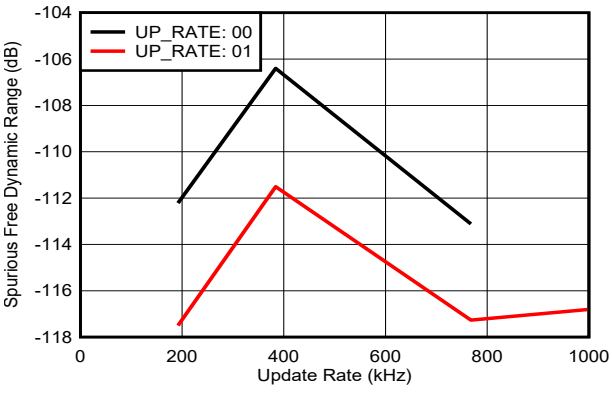
DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-54. Second Harmonic Distortion vs Output Frequency, f_{DAC} = 1 MHz



DAC update rate = 1 MHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 150-kHz output filter

Figure 6-55. Third Harmonic Distortion vs Output Frequency, f_{DAC} = 1 MHz



DAC output frequency = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-56. Spurious Free Dynamic Range vs Update Rate

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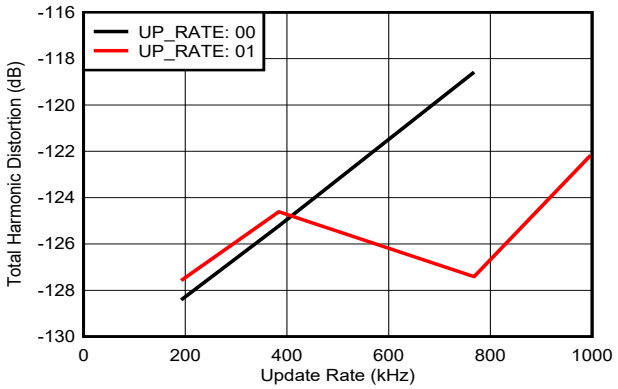
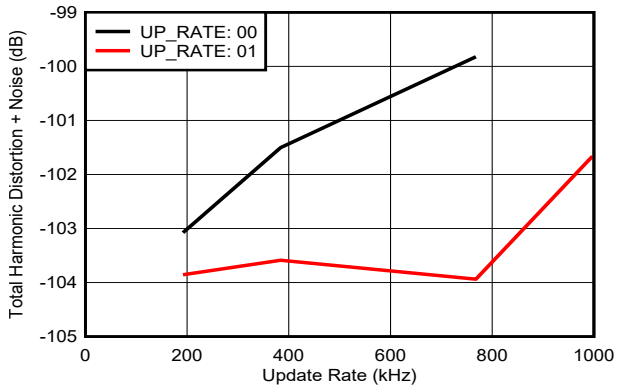
6.11 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 15 V, V_{SS} = –15 V, AV_{DD} = 5 V, IOV_{DD} = 1.8 V, gain resistors unconnected (gain = 1x), OPA827 used as reference amplifier, OPA828 used as output amplifier, UP = unipolar, BP = bipolar, and temperature calibration disabled (unless otherwise noted)



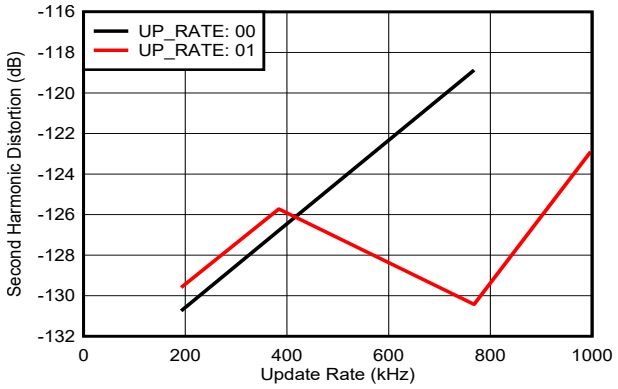
DAC output frequency = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-57. Total Harmonic Distortion vs Update Rate



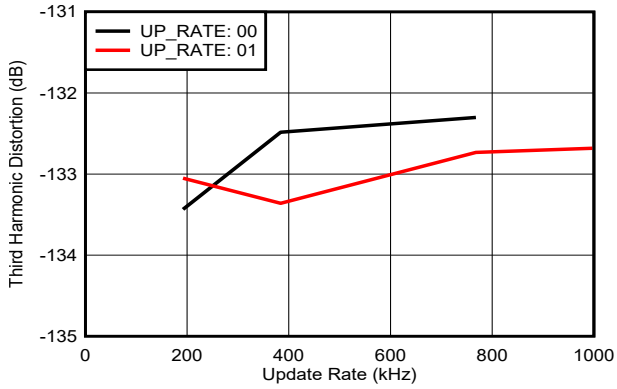
DAC output frequency = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-58. Total Harmonic Distortion + Noise vs Update Rate



DAC output frequency = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-59. Second Harmonic Distortion vs Update Rate



DAC output frequency = 20 kHz, V_{REFPF} = 4.5 V, V_{REFNF} = −4.5 V, sixth-order, low-pass, 30-kHz output filter

Figure 6-60. Third Harmonic Distortion vs Update Rate

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7 Detailed Description

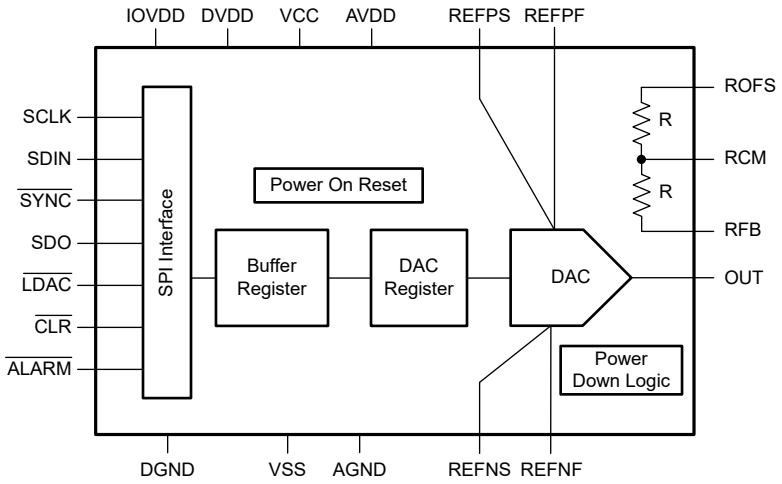
7.1 Overview

The 20-bit DAC11001B is a single-channel DAC. The unbuffered DAC output architecture is based on an R2R ladder that is designed to provide monotonicity and excellent linearity over wide reference and temperature ranges. This architecture provides a very low-noise (7 nV/$\sqrt{\text{Hz}}$) and fast-settling (1 µs) output. The DAC11001B also implements a deglitch circuit that enables low, code-independent glitch at the DAC output. The deglitch circuit is extremely useful for creating ultra-low, harmonic-distortion waveform generation.

The DAC11001B requires external reference voltages on REFPF and REFNF pins. The output of the DAC ranges from V_{REFNF} to V_{REFPF}. See Section 6.3 for $V_{REFPF}$and V_{REFNF} voltage ranges.

The DAC11001B also includes precision matched gain setting pins (ROFS, RCM, and RFB), Use these pins and an external op amp to scale the DAC output. The DAC11001B incorporates a power-on reset (POR) circuit to make sure that the DAC output powers up at zero scale, and remains at zero scale until a valid DAC command is issued. The DAC11001B uses a 4-wire serial interface that operates at clock rates of up to 50 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital-to-Analog Converter Architecture

The DAC11001B provides 20-bit monotonic outputs using an R2R ladder architecture. The DAC output ranges between VREFNF and VREFPF based on the 20-bit DAC data, as described in Equation 1:

$$V_{OUT} = (V_{REFPF} - V_{REFNF}) \times \frac{CODE}{2^N} + V_{REFNF} \quad (1)$$

where

- CODE is the decimal equivalent of the DAC-DATA loaded to the DAC.
- N is the bits of resolution.
- V_{REFPF}, V_{REFNF} is the reference voltage (positive and negative).

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7.3.2 External Reference

The DAC11001B requires external references (REFPF and REFNF) to operate. See *Section 6.3* for V_{REFPF} and V_{REFNF} voltage ranges.

The DAC11001B also contains dedicated sense pins, REFPS for REFPF and REFNS for REFNF. The reference pins are unbuffered; therefore, use a reference driver circuit for these pins. Set the VREFVAL bits (address 02h) as per a reference span equal to (V_{REFPF} – V_{REFNF}). For example, the VREFVAL bits must be set to 0100 for V_{REFPF} = 5 V and V_{REFNF} = –5 V.

Figure 7-1 shows an example reference drive circuit for the DAC11001B. Table 7-1 shows the op-amp options for the reference driver circuit.

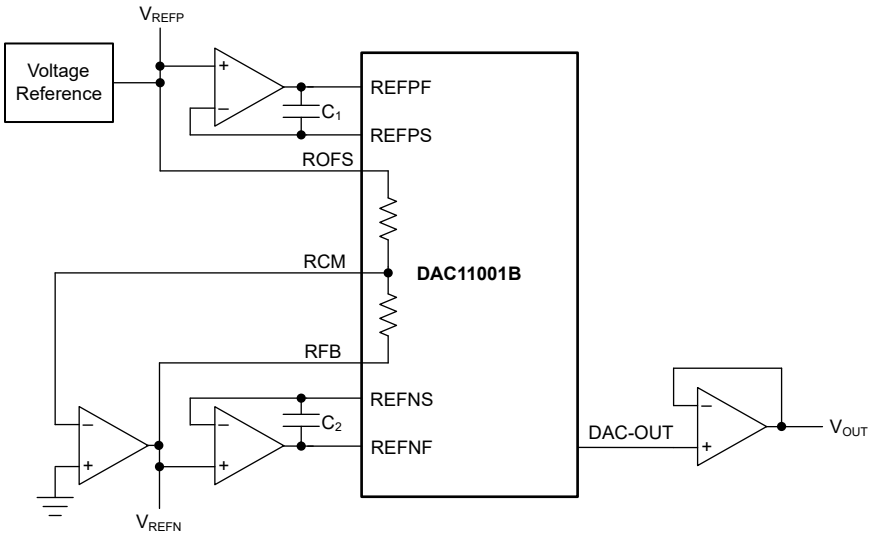

Figure 7-1. Reference Drive Circuit

Table 7-1. Reference Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low voltage and current noise	OPA211, OPA827, OPA828
Low offset and drift	OPA189

7.3.3 Output Buffers

The DAC11001B outputs are unbuffered. Use an external op amp to buffer the DAC output. The DAC output voltage ranges from V_{REFPF} to V_{REFNF}. Two gain-setting resistors are integrated in the DAC11001B. These resistors are used to scale the DAC output, minimize the bias current mismatch of the external op amp, and generate a negative reference for the REFNF pin. See *Section 8.3.3* for more information. Table 7-2 shows the op amp options for the output drive circuit.

Table 7-2. Output Op Amp Options

SELECTION PARAMETERS	OP AMPS
Low bias current	OPA827, OPA828
Low noise	OPA211, OPA828
Low offset and drift	OPA189
Fast settling and low THD	OPA828

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7.3.4 Internal Power-On Reset (POR)

The DAC11001B incorporates two internal POR circuits for the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, and V_{SS} supplies. The POR signals are ANDed together, so that all supplies must be at the minimum specified values for the device to *not* be in a reset condition. These POR circuits initialize internal registers, as well as set the analog outputs to a known state, all while the device supplies are ramping. All registers are reset to default values. The DAC11001B powers on with the DAC registers set to zero scale. The DAC output can be powered down by writing 1 to PDN (bit 4, address 02h). Typically, the POR function can be ignored as long as the device supplies power up and maintain the specified minimum voltage levels. However, a supply drop or brownout can trigger an internal POR reset event. Figure 7-2 represents the internal POR threshold levels for the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, and V_{SS} supplies.

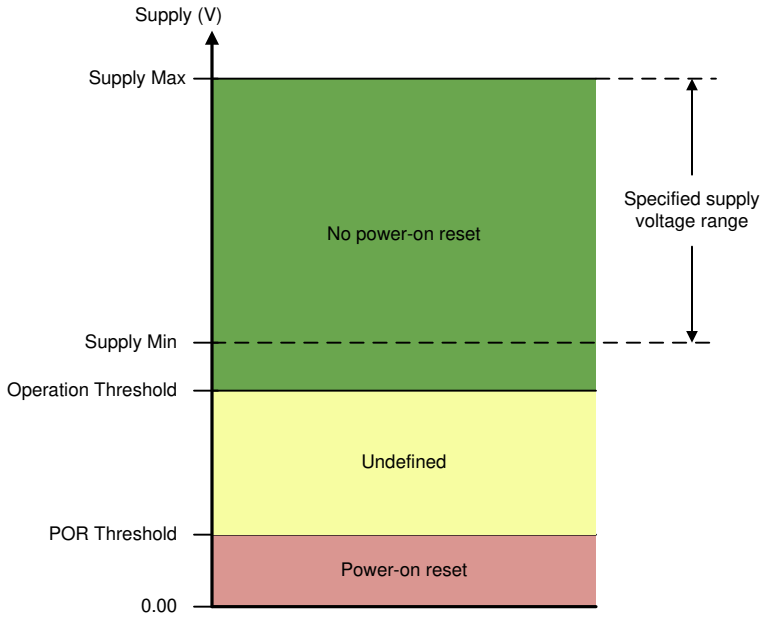

Figure 7-2. Relevant Voltage Levels for the POR Circuit

For the DV_{DD} supply, no internal POR occurs for nominal supply operation from 2.7 V (supply minimum) to 5.5 V (supply maximum). For a DV_{DD} supply region between 2.5 V (undefined operation threshold) and 1.6 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a DV_{DD} supply less than 1.6 V (POR threshold), the internal POR resets as long as the supply voltage is less than 1.6 V for approximately 1 ms.

For the AV_{DD} supply, no internal POR occurs for nominal supply operation from 4.5 V (supply minimum) to 5.5 V (supply maximum). For an AV_{DD} supply region between 4.1 V (undefined operation threshold) and 3.3 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For an AV_{DD} supply less than 3.3 V (POR threshold), the internal POR resets as long as the supply voltage is less than 3.3 V for approximately 1 ms.

For the V_{CC} supply, no internal POR occurs for nominal supply operation from 8 V (supply minimum) to 36 V (supply maximum). For V_{CC} supply voltages between 7.5 V (undefined operation threshold) to 6 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a V_{CC} supply less than 6 V (POR threshold), the internal POR resets as long as the supply voltage is less than 6 V for approximately 1 ms.

For the V_{SS} supply, no internal POR occurs for nominal supply operation from –3 V (supply minimum) to –18 V (supply maximum). For V_{SS} supply voltages between –2.7 V (undefined operation threshold) to –1.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For a V_{SS} supply greater than –1.8 V (POR threshold), the internal POR resets as long as the supply voltage is greater than –1.8 V for approximately 1 ms.

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For the IOV_{DD} supply, no internal POR occurs for nominal supply operation from 1.8 V (supply minimum) to 5.5 V (supply maximum). For IOV_{DD} supply voltages between 1.5 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For an IOV_{DD} supply less than 0.8 V (POR threshold), the internal POR resets as long as the supply voltage is less than 0.8 V for approximately 1 ms.

In case the DV_{DD}, AV_{DD}, IOV_{DD}, V_{CC}, or V_{SS} supply drops to a level where the internal POR signal is indeterminate, power cycle the device followed by a software reset.

7.3.5 Temperature Drift and Calibration

The DAC11001B includes a calibration circuit that significantly reduces the temperature drift on integrated and differential nonlinearities. By default, this feature is disabled. Enable the temperature calibration feature by writing 1 to the EN_TMP_CAL bit (address 02h, B23). After the EN_TMP_CAL bit is set, issue a calibration cycle by writing 1 to RCLTMP (address 04h, B8). At this point, the device enters a calibration cycle. Do not issue any DAC update command during this period. The device has the capability to indicate the end of calibration using two methods:

1. Read the status bit ALM (address 05h, B12) using SPI.
2. Issue an alarm on the $\overline{\text{ALARM}}$ pin by setting logic 0. To enable this feature, write 1 to ENALMP bit (address 02h, B12).

After the calibration cycle completes, update the DAC code to observe the impact at the DAC output. If the environmental temperature changes after calibration, then recalibrate the device.

7.3.6 DAC Output Deglitch Circuit

The DAC11001B includes a deglitch (track-and-hold) circuit at the output. This circuit is enabled by default. The deglitch circuit minimizes the code-to-code glitch at the DAC output at the expense of the DAC update rate. This circuit is disabled by writing 1 to DIS_TNH (bit 7, address 06h). Disable this circuit to enable faster update of the DAC output, but with higher code-to-code glitches.

7.4 Device Functional Modes

7.4.1 Fast-Settling Mode and THD

The DAC11001B R2R ladder and deglitch circuit reduce the harmonic distortion for waveform generation applications. The fast settling bit (FSET, bit 10, address 02h) is set to 1 by default, so that the DAC is configured for enhanced THD performance. The FSET bit can be reset to 0 using an SPI write to enable fast-settling mode. In this mode, the DAC deglitcher circuit can be configured using TNH_MASK (bits 19:18, address 02h). These bits disable the deglitch circuit for code changes specified in Table 7-7. These bits are only writable when FSET = 0 (fast settling enabled) and DIS_TNH = 0 (deglitch circuit enabled).

7.4.2 DAC Update Rate Mode

The DAC11001B maximum update rate can be configured up to 1 MHz by using UP_RATE (bits 5:4, address 06h). These bits change the hold time of the deglitch circuit. The bits are set to a 0.8-MHz DAC update rate by default for enhanced THD performance. Changing the maximum update rate of the DAC impacts THD performance.

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7.5 Programming

The DAC11001B is controlled through a flexible, four-wire serial interface that is compatible with serial interfaces used on many microcontrollers and DSP controllers. The interface provides read and write access to all registers of the DAC11001B. Additionally, the interface can be configured to daisy-chain multiple devices for write operations.

Each serial interface access cycle is exactly 32 bits long, as shown in Figure 7-3. A frame is initiated by asserting the $\overline{\text{SYNC}}$ pin low. The frame ends when the $\overline{\text{SYNC}}$ pin is deasserted high. The first bit is read/write bit B31. A write is performed when this bit is set to 0, and a read is performed when this bit is set to 1. The next seven bits are address bits B30 to B24. The next 20 bits are data. For all writes, data are clocked on the falling edge of SCLK. As Figure 7-4 shows, for read access and daisy-chain operation, the data are clocked out on the SDO terminal on the rising edge of SCLK.

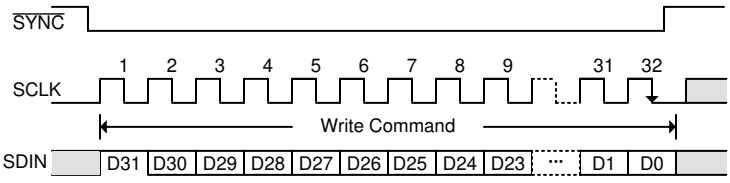

Figure 7-3. Serial Interface Write Bus Cycle: Standalone Mode

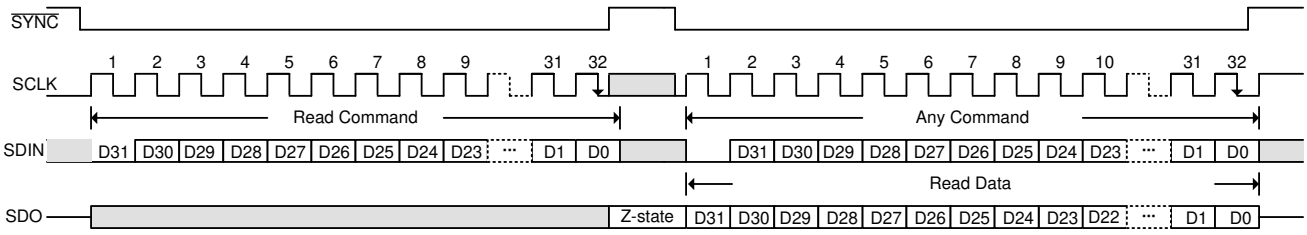

Figure 7-4. Serial Interface Read Bus Cycle

7.5.1 Daisy-Chain Operation

For systems that contain several DAC11001B devices, the SDO pin is used to daisy-chain the devices together. The daisy-chain feature is useful in reducing the number of serial interface lines. The first falling edge on the $\overline{\text{SYNC}}$ pin starts the operation cycle, as shown in Figure 7-5. SCLK is continuously applied to the input shift register while the $\overline{\text{SYNC}}$ pin is kept low. The DAC is updated with the data on rising edge of $\overline{\text{SYNC}}$ pin.

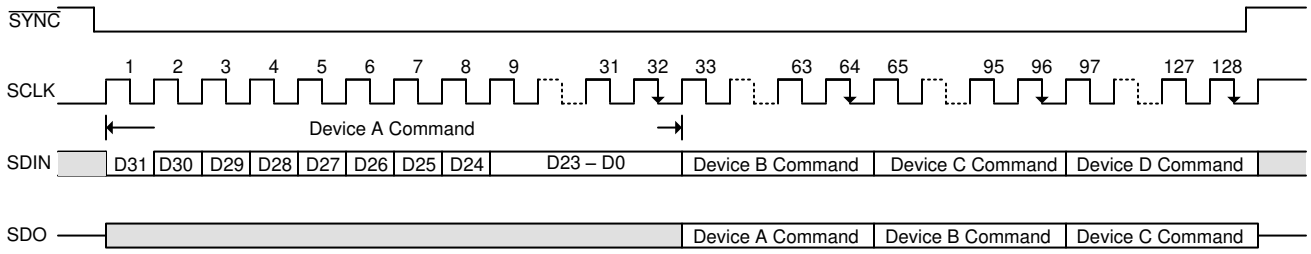

Figure 7-5. Serial Interface Daisy-Chain Write Cycle

If more than 32 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 32 clock pulses.

As a result, the total number of clock cycles must be equal to 32 × N, where N is the total number of devices in the daisy-chain. When the serial transfer to all devices is complete the $\overline{\text{SYNC}}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal register of each device in the daisy-chain and prevents any further data from being clocked into the input shift register. The DAC11001B implements a bit that

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enables higher speeds for clocking out data from the SDO pin. Enable this feature by setting FSDO (bit 13, address 02h) to 1.

7.5.2 $\overline{\text{CLR}}$ Pin Functionality and Software Clear

The $\overline{\text{CLR}}$ pin is an asynchronous input pin to the DAC. When activated, this level-sensitive pin clears the DAC buffers and DAC latches to the DAC-CLEAR-DATA bits (address 03h). The device exits clear mode on the $\overline{\text{SYNC}}$ rising edge of the next valid write to the device. If the $\overline{\text{CLR}}$ pin receives a logic 0 during a write sequence during normal operation, the clear mode is activated and the buffer and DAC registers are immediately cleared. The DAC registers can also be cleared using the SCLR bit (address 04h, B5); the contents are cleared at the rising edge of $\overline{\text{SYNC}}$.

7.5.3 Output Update (Synchronous and Asynchronous)

The DAC11001B offers both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for the DAC without disturbing the analog output. Data updates can be performed either in synchronous or in asynchronous mode, depending on the status of LDAC-MODE bit (address 02h, B14).

7.5.3.1 Synchronous Update

In synchronous mode (LDACMODE = 1), the $\overline{\text{LDAC}}$ pin is used as an active-low signal for simultaneous DAC updates. Data buffers must be loaded with the desired data before an $\overline{\text{LDAC}}$ low pulse. After an $\overline{\text{LDAC}}$ low pulse, the DAC is updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the DAC output remains unchanged after the $\overline{\text{LDAC}}$ pin is pulsed low.

7.5.3.2 Asynchronous Update

In asynchronous mode (LDACMODE = 0), data are updated with the rising edge of the $\overline{\text{SYNC}}$ (when daisy-chain mode is enabled, DSDO = 0), or at the 32nd falling edge of SCLK (When daisy-chain mode is disabled, DSDO = 1). For asynchronous updates, the $\overline{\text{LDAC}}$ pin is not required, and must be connected to 0 V permanently.

7.5.4 Software Reset Mode

The DAC11001B implements a software reset feature. The software reset function uses the SRST bit (address 04h, B6). When this bit is set to 1, the device resets to the default state.

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7.6 Register Map

Table 7-3. Register Map

REGISTER NAME	BIT																					
	31	30-24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3-0
NOP	$\overline{W}$	00h	NOP																				0h
DAC-DATA	R/$\overline{W}$	01h	DAC-DATA (20 bits, left-justified)																				0h
CONFIG1	R/$\overline{W}$	02h	EN_TMP_CAL	000			TNH_MASK	000				LDAC MODE	FSDO	ENALMP	DSDO	FSET	VREFVAL				0	PDN	0h
DAC-CLEAR-DATA	R/$\overline{W}$	03h	DAC-CLEAR-DATA (8 bits left justified)								000h												0h
TRIGGER	R/$\overline{W}$	04h	0000h															RCLTMP	0	SRST	SCLR	0	0h
STATUS	R	05h	000h											ALM	00h								0h
CONFIG2	R/$\overline{W}$	06h	0000h																DIS_TNH	1	UP_RATE		0h

Table 7-4. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1 NOP Register (address = 00h) [reset = 0x000000h for bits [23:0]]

Figure 7-6. NOP Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							NOP							
W	W							W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP												RESERVED			
W-000h												W-0h			

Table 7-5. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Write only register. Must be set to 0.
30-24	Address	W	N/A	00h
23-4	NOP	W	00000h	No operation; write 00000h
3-0	RESERVED	W	0h	These bits are reserved.

7.6.2 DAC-DATA Register (address = 01h) [reset = 0x000000h for bits [23:0]]

Figure 7-7. DAC-DATA Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							DAC-DATA (20-bit, left justified)							
W	W							R/W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAC-DATA (20-bit, left justified)												RESERVED			
R/W-000h												W-0h			

Table 7-6. DAC-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Read when set to 1 or write when set to 0
30-24	Address	W	N/A	01h
23-4	DAC-DATA[19:0]	R/W	00000h	Stores the 20-bit data to be loaded to the DAC in MSB-aligned, straight-binary format.
3-0	RESERVED	W	0h	These bits are reserved.

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7.6.3 CONFIG1 Register (address = 02h) [reset = 004C80h for bits [23:0]]

Figure 7-8. CONFIG1 Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							EN_ TMP_ CAL	RESERVED			TNH_MASK		RESERVED	
W	W							R/W-0h	W-0h			R/W-0h		W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	LDAC MODE	FSDO	ENALMP	DSDO	FSET	VREFVAL				RSVD	PDN	RESERVED			
W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-2h				W-0h	R/W-0h	W-0h			

Table 7-7. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Read when set to 1 or write when set to 0
30-24	Address	W	N/A	02h
23	EN_TMP_CAL	R/W	0h	Enables and disables the temperature calibration feature 0: Temperature calibration feature disabled (default) 1: Temperature calibration feature enabled
22-20	RESERVED	W	0h	These bits are reserved.
19-18	TNH_MASK	R/W	0h	Mask track and hold (TNH) circuit. This bit is writable only when FSET = 0 [fast-settling mode] and DIS_TNH = 0 [track-and-hold enabled] 00: TNH masked for code jump > 2^{14} (default) 01: TNH masked for code jump > 2^{15} 10: TNH masked for code jump > 2^{13} 11: TNH masked for code jump > 2^{12}
17-15	RESERVED	W	0h	These bits are reserved.
14	LDACMODE	R/W	1h	Synchronous or asynchronous mode select bit 0: DAC output updated on $\overline{\text{SYNC}}$ rising edge 1: DAC updated on $\overline{\text{LDAC}}$ falling edge (default)
13	FSDO	R/W	0h	Enable Fast SDO 0: Fast SDO disabled (Default) 1: Fast SDO enabled
12	ENALMP	R/W	0h	Enable $\overline{\text{ALARM}}$ pin to be pulled low, end of temperature calibration cycle 0: No alarm on the $\overline{\text{ALARM}}$ pin 1: Indicates end of temperature calibration cycle. $\overline{\text{ALARM}}$ pin pulled low.
11	DSDO	R/W	1h	Enable SDO (for readback and daisy-chain) 1: SDO enabled (default) 0: SDO disabled
10	FSET	R/W	1h	Fast-settling vs enhanced THD mode 0: Fast settling 1: Enhanced THD (default)
9-6	VREFVAL	R/W	2h	Reference span value bits 0000: Invalid 0001: Invalid 0010: Reference span = 5 V ± 1.25 V (default) 0011: Reference span = 7.5 V ± 1.25 V 0100: Reference span = 10 V ± 1.25 V 0101: Reference span = 12.5 V ± 1.25 V 0110: Reference span = 15 V ± 1.25 V 0111: Reference span = 17.5 V ± 1.25 V 1000: Reference span = 20 V ± 1.25 V 1001: Reference span = 22.5 V ± 1.25 V 1010: Reference span = 25 V ± 1.25 V 1011: Reference span = 27.5 V± 1.25 V 1100: Reference span = 30 V ± 1.25 V
5	RESERVED	W	0h	This bit is reserved.
4	PDN	R/W	0h	Powers down and power up the DAC 0: DAC power up (default) 1: DAC power down
3-0	RESERVED	W	0h	These bits are reserved.

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7.6.4 DAC-CLEAR-DATA Register (address = 03h) [reset = 000000h for bits [23:0]]

Figure 7-9. DAC-CLEAR-DATA Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							DAC-CLEAR-DATA (8 bits, left justified)							
W	W							R/W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RESERVED			
W-000h												W-0h			

Table 7-8. DAC-CLEAR-DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Read when set to 1 or write when set to 0
30-24	Address	W	N/A	03h
23-16	DAC-CLEAR-DATA	R/W	00h	Stores the 8-bit data to be loaded to the DAC in left-justified, straight-binary format. DAC data registers are updated with this value when the $\overline{CLR}$ pin is asserted low
15-4	RESERVED	W	000h	These bits are reserved.
3-0	RESERVED	W	0h	These bits are reserved.

7.6.5 TRIGGER Register (address = 04h) [reset = 000000h for bits [23:0]]

Figure 7-10. TRIGGER Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							RESERVED							
W	W							W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RCLTMP	RSVD	SRST	SCLR	RSVD	RESERVED			
W-00h							R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	W-0h			

Table 7-9. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Read when set to 1 or write when set to 0
30-24	Address	W	N/A	04h
23-9	RESERVED	W	0000h	These bits are reserved.
8	RCLTMP	R/W	0h	Trigger temperature recalibration DAC Codes 0: No temperature recalibration (default) 1: DAC codes recalibrated, $\overline{ALARM}$ pin pulled low (if ENALMP = 1) and ALM bit (address 05) set to 1 when calibration complete. Subsequent DAC codes use the latest calibrated coefficients.
7	RESERVED	W	0h	This bit is reserved.
6	SRST	R/W	0h	Software reset 0: No software reset (default) 1: Software reset initiated, device in default state
5	SCLR	R/W	0h	Software clear 0: No software clear (default) 1: Software clear initiated, DAC registers in clear mode, DAC code set by clear select register (address 03h). DAC output clears on 32nd SCLK falling (DSDO = 1) or $\overline{SYNC}$ rising edge (DSDO = 0)
4	RESERVED	W	0h	This bit is reserved.
3-0	RESERVED	W	0h	These bits are reserved.

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7.6.6 STATUS Register (address = 05h) [reset = 000000h for bits [23:0]]

Figure 7-11. STATUS Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							RESERVED							
R	W							W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ALM	RESERVED								RESERVED			
W-0h			R-0h	W-00h								W-0h			

Table 7-10. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	R	N/A	Read only register. Must be set to 1.
30-24	Address	W	N/A	05h
23-13	RESERVED	W	000h	These bits are reserved.
12	ALM	R	0	Alarm indicator bit, This bit is not masked by ENALMP bit 0: Temperature recalibration in progress 1: DAC codes recalibrated, $\overline{\text{ALARM}}$ pin is pulled low (if ENALMP = 1). Subsequent DAC codes will use latest calibrated coefficients. Reading back this register resets $\overline{\text{ALARM}}$ pin to 1 status.
11-4	RESERVED	W	00h	These bits are reserved.
3-0	RESERVED	W	0h	These bits are reserved.

7.6.7 CONFIG2 Register (address = 06h) [reset = 000040h for bits [23:0]]

Figure 7-12. CONFIG2 Register Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read/ Write	Address							RESERVED							
W	W							W-00h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DIS_TNH	RSVD	UP_RATE		RESERVED			
W-00h								R/W-0h	W-1h	R/W-0h		W-0h			

Table 7-11. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Read/Write	W	N/A	Read when set to 1 or write when set to 0
30-24	Address	W	N/A	06h
23-8	RESERVED	W	0000h	These bits are reserved.
7	DIS_TNH	R/W	0h	Disable track and hold: 0: Track and hold enabled (default) 1: Track and hold disabled
6	RESERVED	W	1h	This bit is reserved.
5-4	UP_RATE	R/W	0h	DAC output max update rate: 00: 0.8 MHz with 28-MHz SCLK, (default) 01: 1.05 MHz with 38.5-MHz SCLK 10: 0.7 MHz with 25.5-MHz SCLK 11: 0.95 MHz with 34.5-MHz SCLK
3-0	RESERVED	W	0h	These bits are reserved.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DAC11001B is targeted for high-precision applications where ultra-high dc accuracy, ultra-low noise, fast settling, or high total harmonic distortion (THD) are required. The DAC11001B provides 20-bit monotonic resolution and excellent linearity. The DAC11001B finds application in high-performance source measure unit (SMU), arbitrary waveform generation (AWG). The DAC11001B is an also excellent choice for closed-loop control applications such as microelectromechanical system (MEMS) actuators, linear actuators, precision motor control, lens autofocus control in precision microscopy, lens control in mass spectrometer, beam control in electron beam lithography, and so on.

8.2 Typical Application

8.2.1 Source Measure Unit (SMU)

A source measure unit (SMU) is a common building block in memory and semiconductor test equipment and bench-top source measure units. A DAC is used in an SMU to force a desired voltage or a current to a device-under-test (DUT). Figure 8-1 provides a simplified circuit diagram of the force-DAC in an SMU.

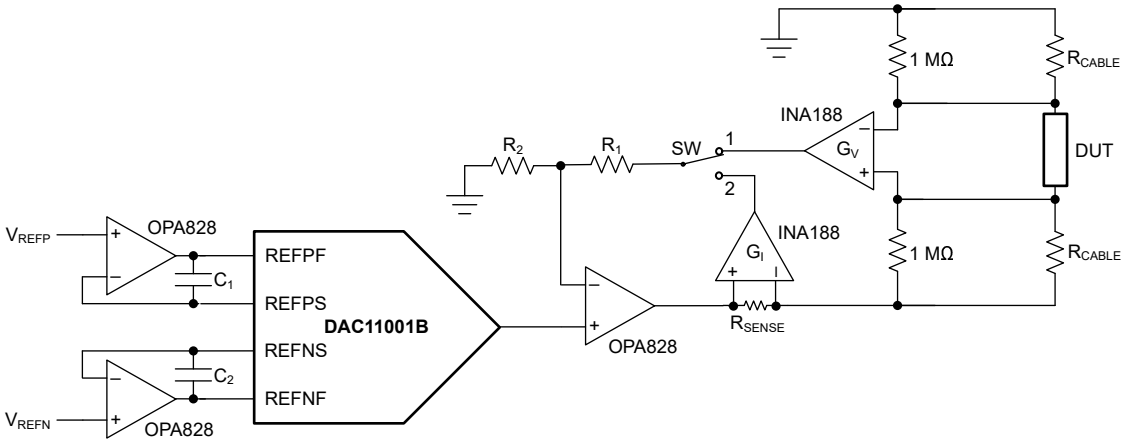

Figure 8-1. Source Measure Unit

8.2.1.1 Design Requirements

- Force voltage range: ±10 V
- Force current range: ±20 mA

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8.2.1.2 Detailed Design Procedure

The DAC11001B is an excellent choice for this application to meet the 20-bit resolution requirement. Switch SW is used to toggle between force-voltage and force-current modes, as shown in Figure 8-1. The OPA828 is a high-precision amplifier that provides a good balance between dc and ac performance, and can supply ±30-mA output current. The INA188 is a zero-drift instrumentation amplifier with gain selected with an external resistor. The external resistor is not shown in the drawing for simplicity. The gain resistor is not required for a gain of 1. Equation 2 shows the calculation of the voltage gain when switch SW is in position 1.

$$A_V = \frac{1}{G_V} x \left(1 + \frac{R_1}{R_2}\right) \tag{2}$$

Precision reference sources are available at 5 V or less. Use a ±5-V reference with a 2x gain configuration to get an output of ±10 V. The DAC output amplifier sets the gain at 2, assuming G_V = 1, as shown in Equation 3. R_1 and R_2 are 1-kΩ each. Equation 3 shows the calculation for the current gain when the switch is in the position 2.

$$A_V = \frac{1}{R_{SENSE} x G_I} x \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

In order to get ±20-mA output current range with $R_1 = R_2$, R_{SENSE}x G_I must be 500. Set G_I to 50 so that R_{SENSE} is 10-Ω. For a ±20-mA output current, the voltage drop across R_{SENSE} is ±200-mV. In case the design requires a lower voltage headroom, choose a higher value for G_I and a smaller resistance value for R_{SENSE}.

There is no equation to select C_1 and C_2. The values of C_1 and C_2 depend on the stability criteria of the reference buffers when driving the reference inputs of DAC11001B. The values are obtained through simulation. For the OPA828, use $C_1 = C_2$ = 100 pF. The 1-MΩ resistors in the circuit are used for making sure the amplifiers are not left in an open-loop state.

8.2.1.3 Application Curves

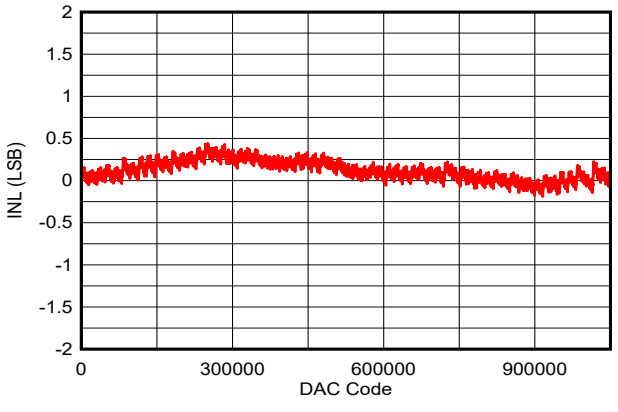

Figure 8-2. INL at ±10-V Output

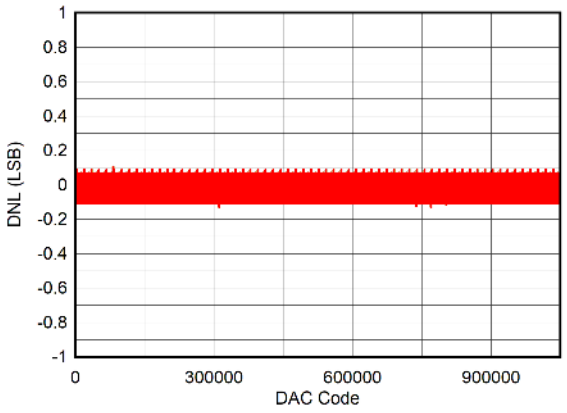

Figure 8-3. DNL at ±10-V Output

8.2.2 High-Precision Control Loop

High-precision control loops are used in precision motion-control applications, such as linear actuator control, servo motor control, galvanometer control, and more. The key requirements for such applications is resolution, monotonicity, settling time, and code-to-code glitch. Figure 8-4 provides a simplified circuit of a linear actuator control circuit, wherein the DAC11001B commands the set point and an analog loop controls the actuator.

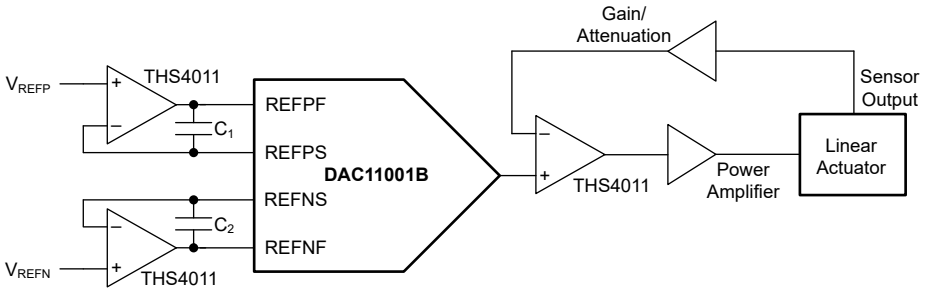

Figure 8-4. High-Precision Control Loop

8.2.2.1 Design Requirements

- DNL: ±1 LSB max at 20-bits
- Settling time: < 2 µs
- Code-to-code glltch: < 2 nV-s

8.2.2.2 Detailed Design Procedure

The DAC11001B provides 20-bit monotonic resolution at < ±1 LSB DNL. The device provides < 2-µs setting time and < 2-nV-s code-to-code glitch for major carry transition. The reference and output buffer used for this design is the THS4011, a high-speed amplifier with a 90-ns settling time. For the best settling response, use C_1 and C_2 between 10 pF to 50 pF.

8.2.2.3 Application Curves

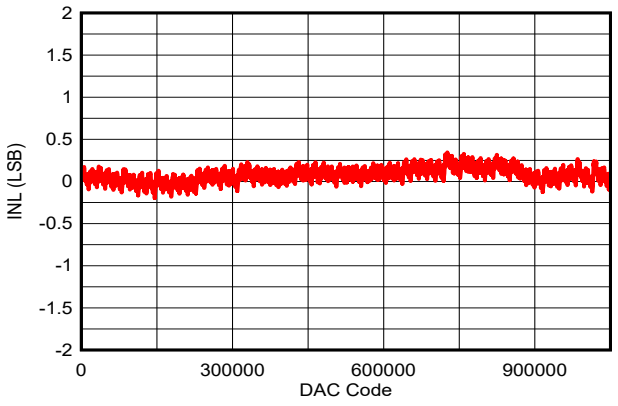

Figure 8-5. INL at ±5-V Output

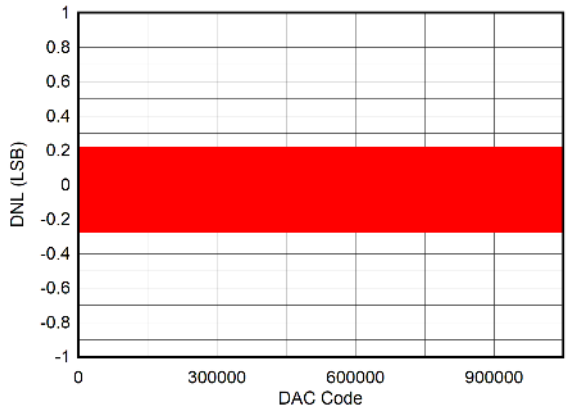

Figure 8-6. DNL at ±5-V Output

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8.2.3 Arbitrary Waveform Generation (AWG)

Arbitrary waveform generation circuits are common in memory and semiconductor test equipment. These circuits are used to generate reference ac waveforms to test semiconductor devices. The key performance parameters of such circuits are THD, SNR, and the update rate. Figure 8-7 shows the basic building block example of an AWG circuit using the DAC11001B.

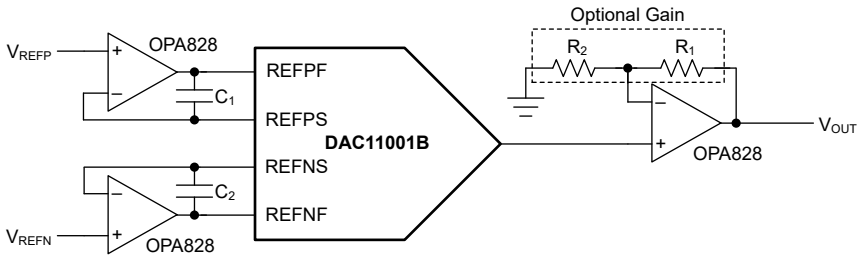

Figure 8-7. Arbitrary Waveform Generation

8.2.3.1 Design Requirements

- THD at 1 kHz: > –105 dB
- Update rate: 768 kHz

8.2.3.2 Detailed Design Procedure

The DAC11001B provides a THD of –115 dB at 1 kHz. The device provides update rates of up to 1 MHz, with marginal degradation in THD at higher frequencies. The OPA828 amplifier provides the best balance between the voltage and current noise densities, and is therefore an excellent choice to use as reference buffers. The OPA828 also offers low-distortion for high-THD applications.

8.2.3.3 Application Curves

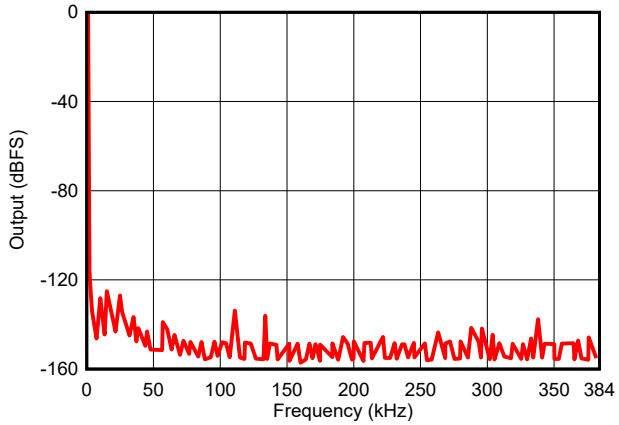

Figure 8-8. 1-kHz Spectrum vs Frequency

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8.3 System Examples

This section provides details on the digital interface and the embedded resistor configurations.

8.3.1 Interfacing to a Processor

The DAC11001B works with a 4-wire SPI interface. The digital interface of the device to a processor is shown in Figure 8-9. The DAC11001B has an $\overline{\text{LDAC}}$ input option for synchronous output update. In ac-signal-generation applications, the jitter in the $\overline{\text{LDAC}}$ signal contributes to signal-to-noise ratio (SNR). Therefore, the $\overline{\text{LDAC}}$ signal must be generated from a low-jitter timer in the processor. The $\overline{\text{CLR}}$ and $\overline{\text{ALARM}}$ pins are static signals, and therefore can be connected to general-purpose input-output (GPIO) pins on the processor. All active-low signals ($\overline{\text{SYNC}}$, $\overline{\text{LDAC}}$, $\overline{\text{CLR}}$, and $\overline{\text{ALARM}}$) must be pulled up to IOVDD using 10-kΩ resistors. $\overline{\text{ALARM}}$ is an output pin from the DAC; therefore, the corresponding GPIO on the processor must be configured as an input. Either poll the GPIO, or configure the GPIO as an interrupt to detect any failure alarm from the DAC. When using a high SCLK frequency, use source termination resistors, as shown in Section 8.3.1. Typically, 33-Ω resistors work on printed circuit boards (PCBs) with a 50-Ω trace impedance.

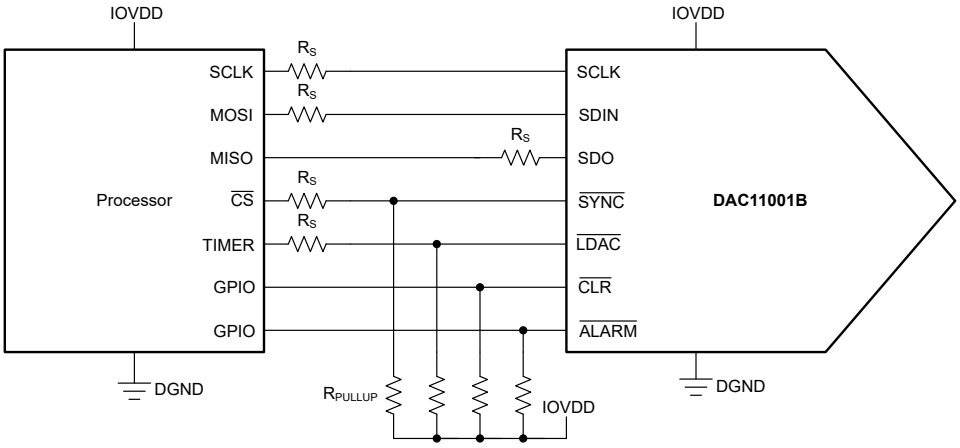

Figure 8-9. Interfacing to a Processor

8.3.2 Interfacing to a Low-Jitter $\overline{\text{LDAC}}$ Source

When the processor is not able to provide a low-jitter source for the $\overline{\text{LDAC}}$ signal, an external low-jitter LDAC source can be used, as shown in Figure 8-10. The processor can take the $\overline{\text{LDAC}}$ signal as an interrupt and trigger the SPI frame synchronously.

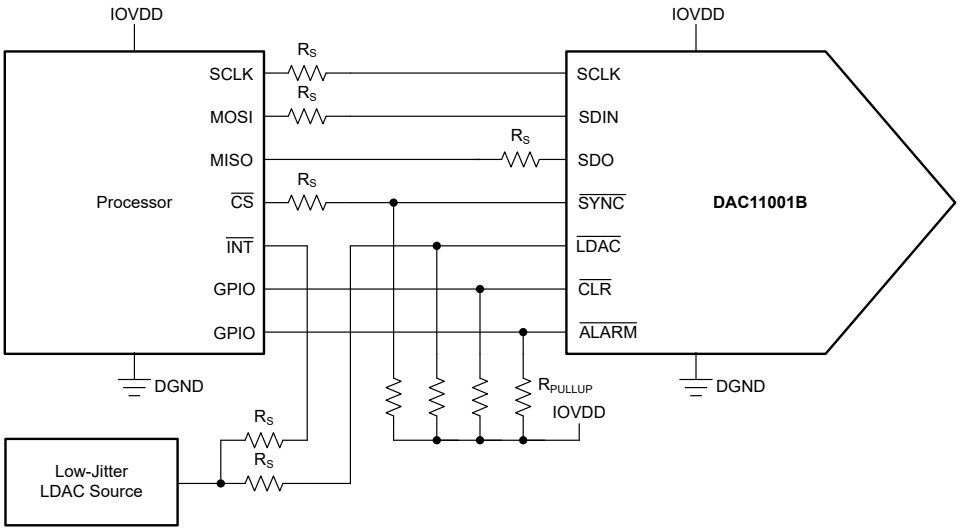

Figure 8-10. Interfacing to an External $\overline{\text{LDAC}}$ Source

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8.3.3 Embedded Resistor Configurations

The DAC11001B provides two embedded resistors with values that are double the value of the output impedance of the R2R ladder. These resistors can be used in various configurations, as shown in the following subsections.

8.3.3.1 Minimizing Bias Current Mismatch

The bias current mismatch in the output amplifier can lead to offset error at the output. To minimize mismatch, the amplifier must have a matching resistor to that of the R2R output impedance on the feedback path. The feedback resistors are used in parallel for this purpose, as shown in Figure 8-11. Some amplifiers may become unstable with a feedback resistor in the buffer configuration; therefore, a compensation capacitor (C_{COMP}) might be needed, as shown. The typical value of this capacitor is in the range of 22 pF to 100 pF, depending on the amplifier.

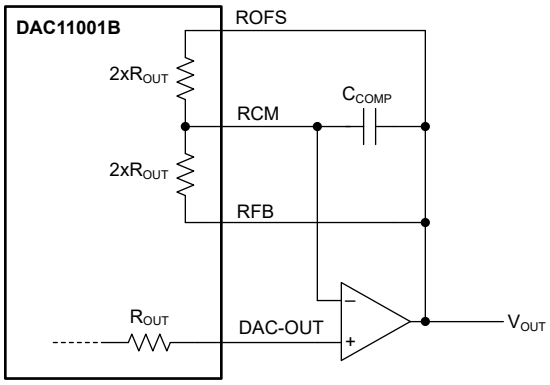

Figure 8-11. Minimizing Bias Current Mismatch

8.3.3.2 2x Gain Configuration

The circuit of Figure 8-11 can be configured for 2x gain by connecting one of the resistor ends to ground, as shown in Figure 8-12.

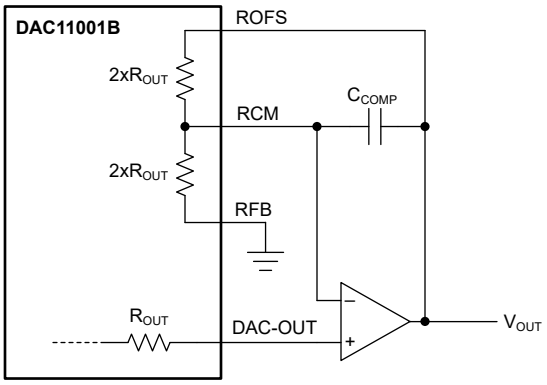

Figure 8-12. 2x Gain Configuration

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8.3.3.3 Generating Negative Reference

Generating a negative reference is a challenge because of the fact that the circuit needs an inverting amplifier involving resistors. The resistor mismatch and temperature drift can lead to inaccuracy. The embedded, matched resistors in DAC11001B can be used as shown in Figure 8-13, the inverting amplifier configuration, to generate an accurate negative reference voltage.

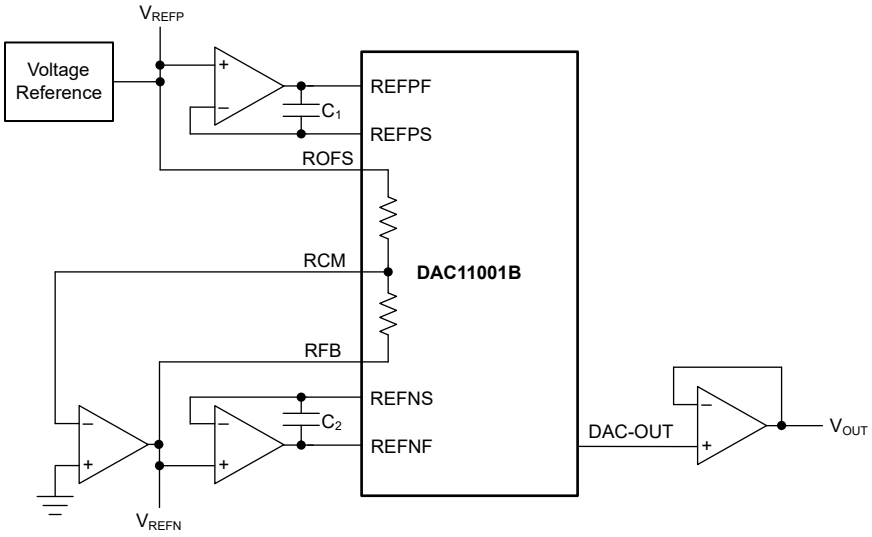

Figure 8-13. Generating Negative Reference

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8.4 What to Do and What Not to Do

8.4.1 What to Do

- Follow recommended grounding, decoupling, and layout schemes for achieving best accuracy.
- Use a low-jitter $\overline{\text{LDAC}}$ source for best ac performance.
- Choose the appropriate amplifiers depending on the application requirements as explained in above sections.

8.4.2 What Not to Do

- Do not apply the reference before the DAC power supplies are powered on.
- Do not use the reference source directly with the DAC reference inputs without using buffers. or else the accuracy drastically degrades.

8.5 Initialization Set Up

The following text shows the pseudocode to get started with the DAC11001B:

```
//SPI Settings
//Mode: Mode-1 (CPOL: 0, CPHA: 1)
//CS Type: Active Low, Per Packet
//Frame length: 32
//SYNTAX: WRITE <REGISTER (HEX ADDRESS>, <HEX DATA>
//Select VREF, TnH mode (Good THD), LDAC mode and power-up the DAC
WRITE CONFIG (0x02), 0x004C80
//Write zero code to the DAC
WRITE DACDATA (0x01), 0x000000
//Write mid code to the DAC
WRITE DACDATA (0x01), 0x7FFFF0
//Write full code to the DAC
WRITE DACDATA (0x01), 0xFFFFF0
```

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9 Power Supply Recommendations

To get the best performance out of the DAC11001B, the power supply, grounding, and decoupling are very important. Use a PCB with a ground-plane reference, which helps in confining the digital return currents. A low mutual inductance path is created just beneath the high-frequency digital traces causing the return currents to follow the respective signal traces, thus minimizing crosstalk. On the other hand, dc signals spread over the ground plane without being confined below the signal trace. Therefore, in precision dc applications, limiting the common-impedance coupling is very difficult unless the ground planes are physically separated. Figure 9-1 shows a method to divide the grounds so that there is no common-mode current flow between the grounds, while maintaining the same dc potential across all grounds. This circuit assumes that the REFGND and LOAD-GND are provided from isolated power sources, therefore, there is no common-mode current flow through the reference or the load.

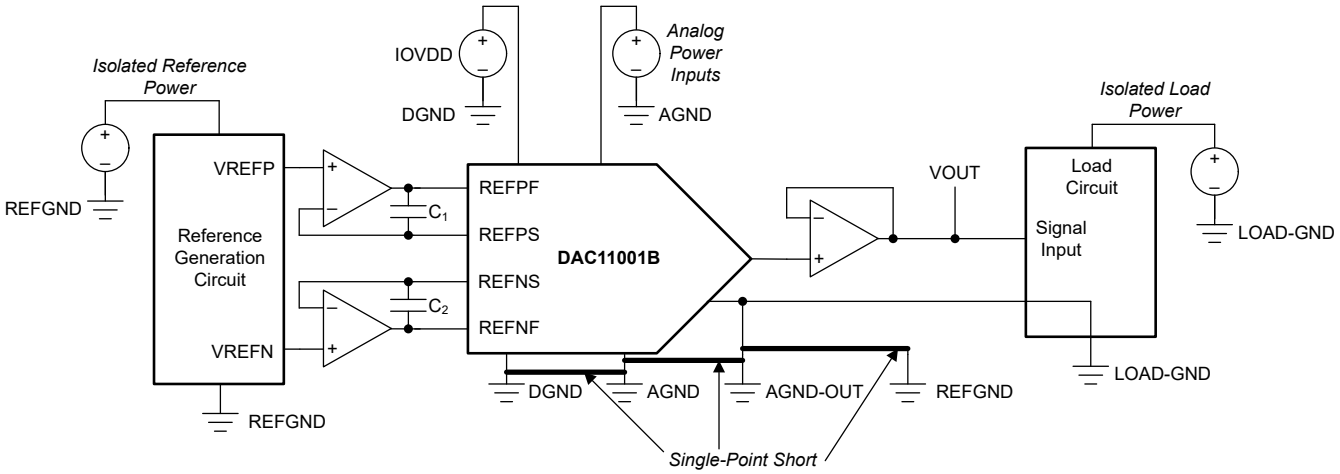

Figure 9-1. Power and Signal Grounding

When the load circuit is powered from a source referenced to AGND, and the LOAD-GND is shorted to AGND at the far end, the AGND-OUT must no longer be shorted to AGND locally near the DAC. The local shorting creates a ground loop, otherwise. The resulting connection that avoids the ground loop is shown in Figure 9-2.

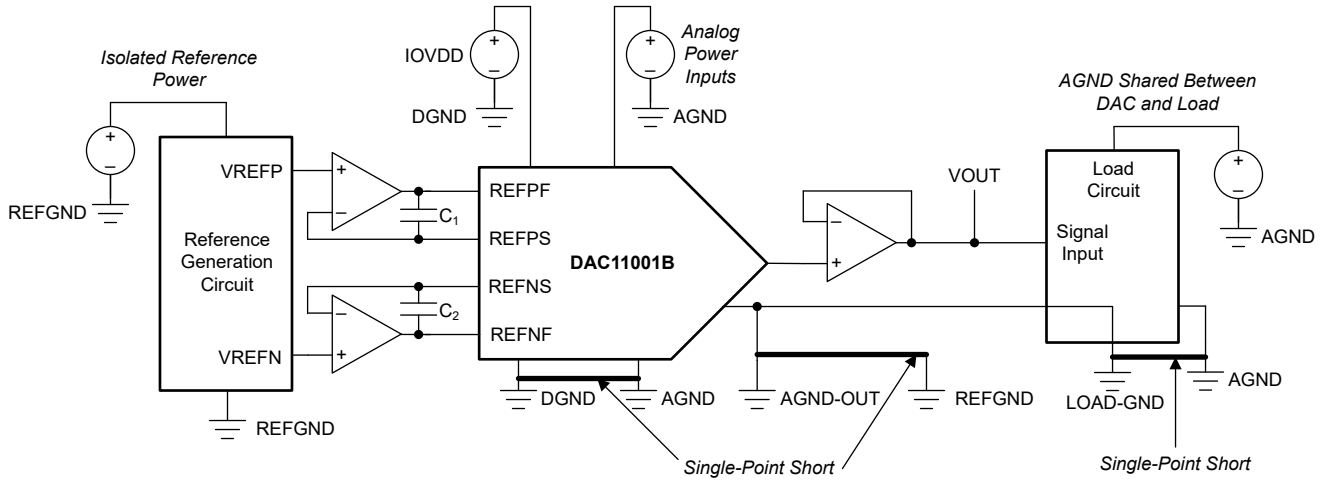

Figure 9-2. Grounding Scheme When AGND is Load Ground

When the reference source is powered from a power source with AGND as the ground, there is a possibility of common-impedance coupling causing a code-dependent shift in the reference voltage. To avoid undesired coupling, drive REFGND using a buffer that maintains the reference ground potential equals to that of AGND-OUT, as shown in Figure 9-3.

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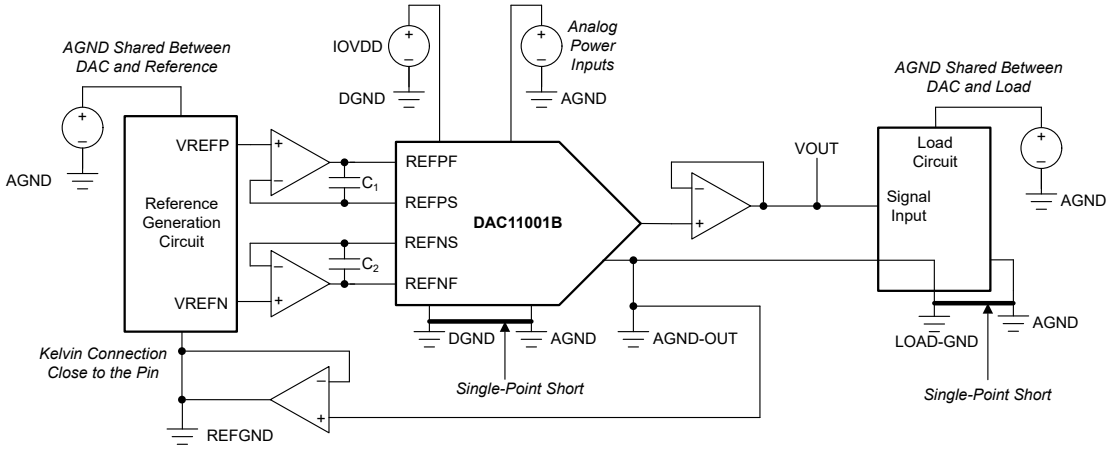

Figure 9-3. Connecting the Reference Ground

Channel-to-channel dc crosstalk is a major concern in multichannel applications, such as battery test equipment. While the DAC11001B is single-channel, the crosstalk problem can appear at a system level when using multiple DAC11001B devices. The problem becomes severe when the grounds of the loads are shorted together creating a possible ground loop. In such cases, avoid the local short between AGND and AGND-OUT. Use a single short between AGND and DGND for all the DACs. If the PCB layout allows for the digital signal and analog power supplies to be kept separate, DGND and AGND can be combined to a single ground plane. Figure 9-4 shows an example circuit for minimizing dc crosstalk across DAC channels in a system.

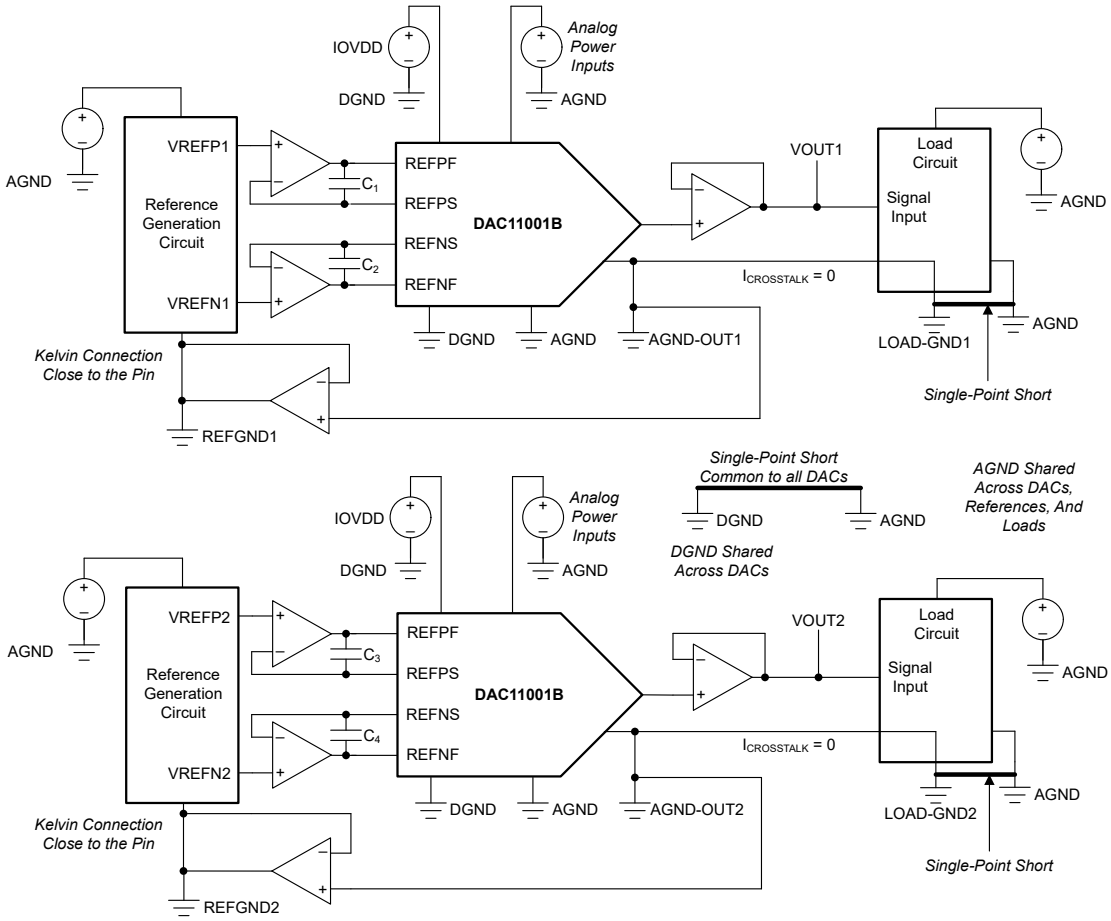

Figure 9-4. Minimizing Multichannel DC Crosstalk

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Power-supply bypassing and decoupling is key to keeping power supply noise, switching transients, and common-mode currents away from the DAC output. There are three main objective of power-supply bypassing:

- *Filtering*: Filter out noise and ripple from power supplies
- *Bypassing*: Supply switching or load transient currents locally by avoiding trace inductances
- *Decoupling*: Stop local transient currents from impacting other circuits

To achieve these objectives, use the following 3-element scheme. Place a decoupling capacitor close to every power supply pin to provide the local current path for load and circuit switching transients. This capacitor must be referenced to the respective load ground for best load transient suppression. Use a 0.1-µF to 1-µF, X7R, multilayer ceramic capacitor (MLCC) for this purpose. For analog power supplies, a 10-Ω series resistor provides the best decoupling. For filtering the power-supply noise and ripple, 10-µF capacitors work best when placed at the power entry point of the board. An example decoupling scheme is shown in Figure 9-5.

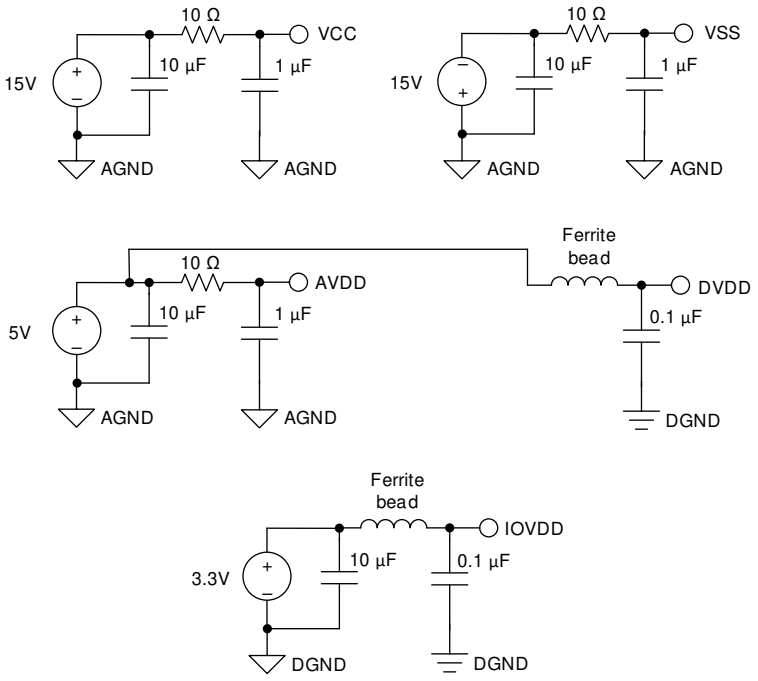

Figure 9-5. Power-Supply Decoupling

9.1 Power-Supply Sequencing

The DAC11001B does not require any power-supply sequence. However, the power supplies to the AVDD pin must be capable of providing 30-mA of current if V_{SS} ramps before AV_{DD}. This current is derived from the AVDD pin, and flows out of the VSS pin. This condition is transient, and the device stops consuming this current when the power supplies are ramped up. To avoid this condition, make sure to ramp AV_{DD} before V_{SS}.

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10 Layout

10.1 Layout Guidelines

PCB layout plays a significant role for achieving desired ac and dc performance from the DAC11001B. The DAC11001B has a pinout that supports easy splitting of the noisy and quiet grounds. The digital signals are available on two adjacent sides of the device; whereas, the power and analog signals are available separate sides. Figure 10-4 shows an example layout, where the different ground planes have been clearly demarcated. The figure also shows the best positions for the single-point shorts between the ground planes. For best power-supply bypassing, place the bypass capacitors close to the respective power pins as shown. Provide unbroken ground reference planes for the digital signal traces, especially for the SPI and $\overline{\text{LDAC}}$ signals.

10.1.1 PCB Assembly Effects on Precision

The printed-circuit board (PCB) assembly process, including reflow soldering, imparts thermal stresses on the device which can degrade the precision of the device and must be considered in the development of very-high-precision systems. Standard reflow guidelines must be followed to achieve the device specified performance. For more information please see Texas Instruments, *MSL Ratings and Reflow Profiles* application report.

Baking the PCBs after the assembly process can restore the precision of the device to pre-assembly values. Figure 10-1 to Figure 10-3 show the effect of reflow soldering on the typical distribution of INL of the device.

Figure 10-1 shows the INL distribution for a set of DAC11001B devices before the PCB assembly process. Exposing the devices to a JEDEC-standard thermal profile for reflow soldering produces the histogram shown in Figure 10-2 on another set of devices. The standard INL deviation increased due to the thermal stress imparted to the device from the reflow process. However, baking DAC11001B units for 60 minutes at 125°C after the reflow soldering process produced the distribution given in Figure 10-3. The post-reflow bake restored the INL standard deviation to pre-assembly levels.

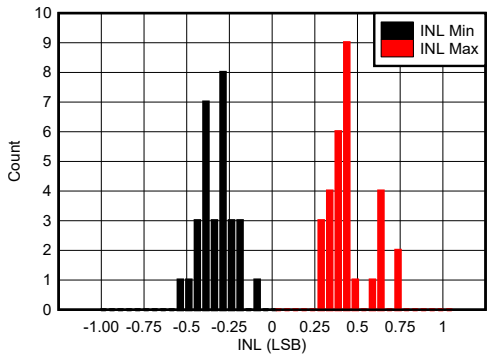

Figure 10-1. Typical INL Distribution Before Reflow Soldering

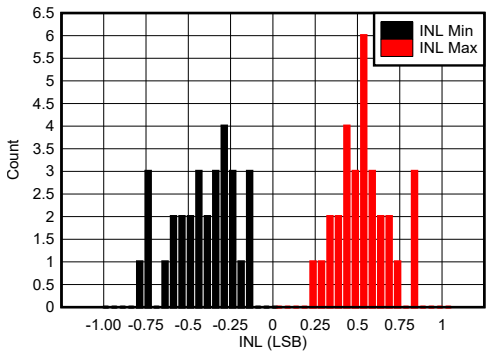

Figure 10-2. Typical INL Distribution After Reflow Soldering

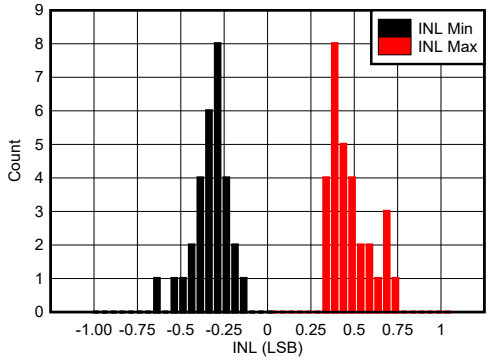

Figure 10-3. Typical INL Distribution Post-Reflow Units Baked at 125°C for 60 Minutes

10.2 Layout Example

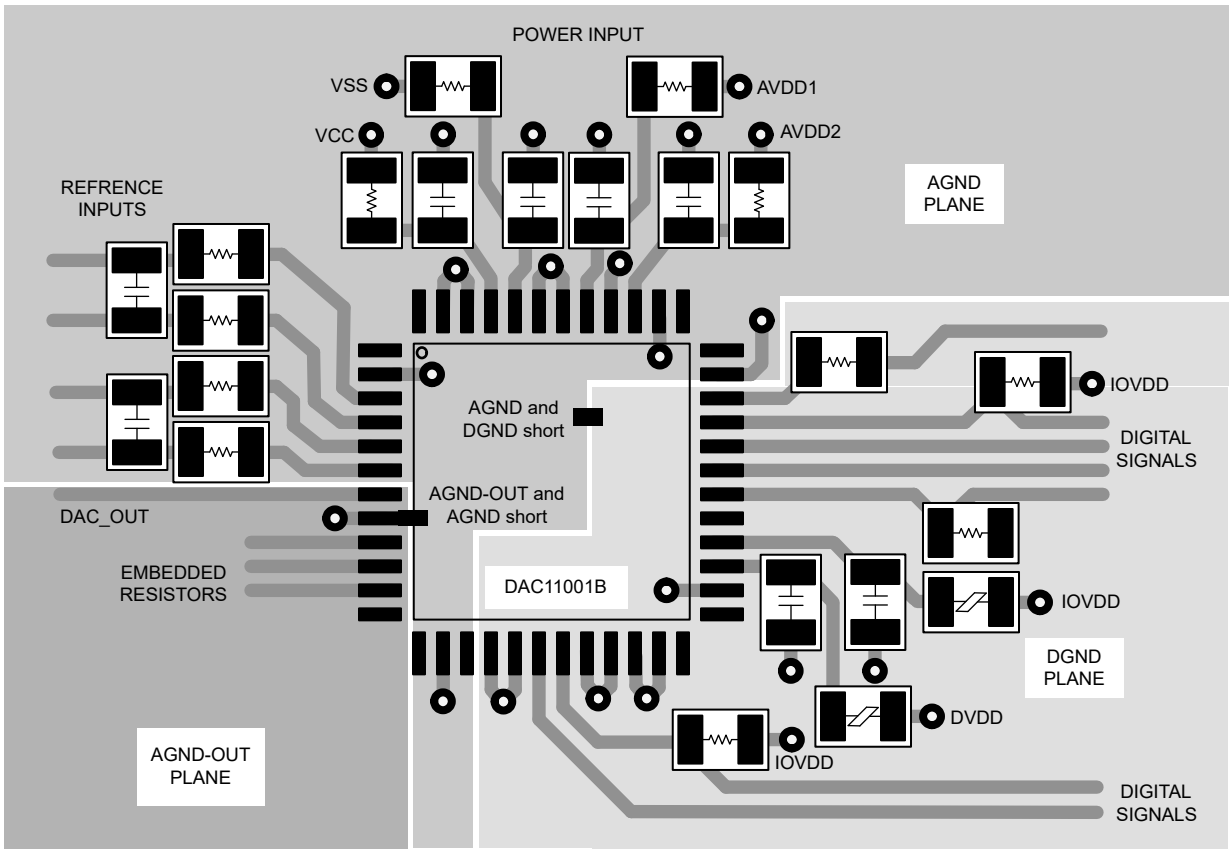

Figure 10-4. Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

BP-DAC11001 Evaluation Module

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *BP-DAC11001EVM* user's guide
- Texas Instruments, *Impact of Code-to-Code Glitch in Precision Applications* application brief

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC11001BPFBR	ACTIVE	TQFP	PFB	48	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC11001B	Samples
DAC11001BPFBT	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 125	DAC11001B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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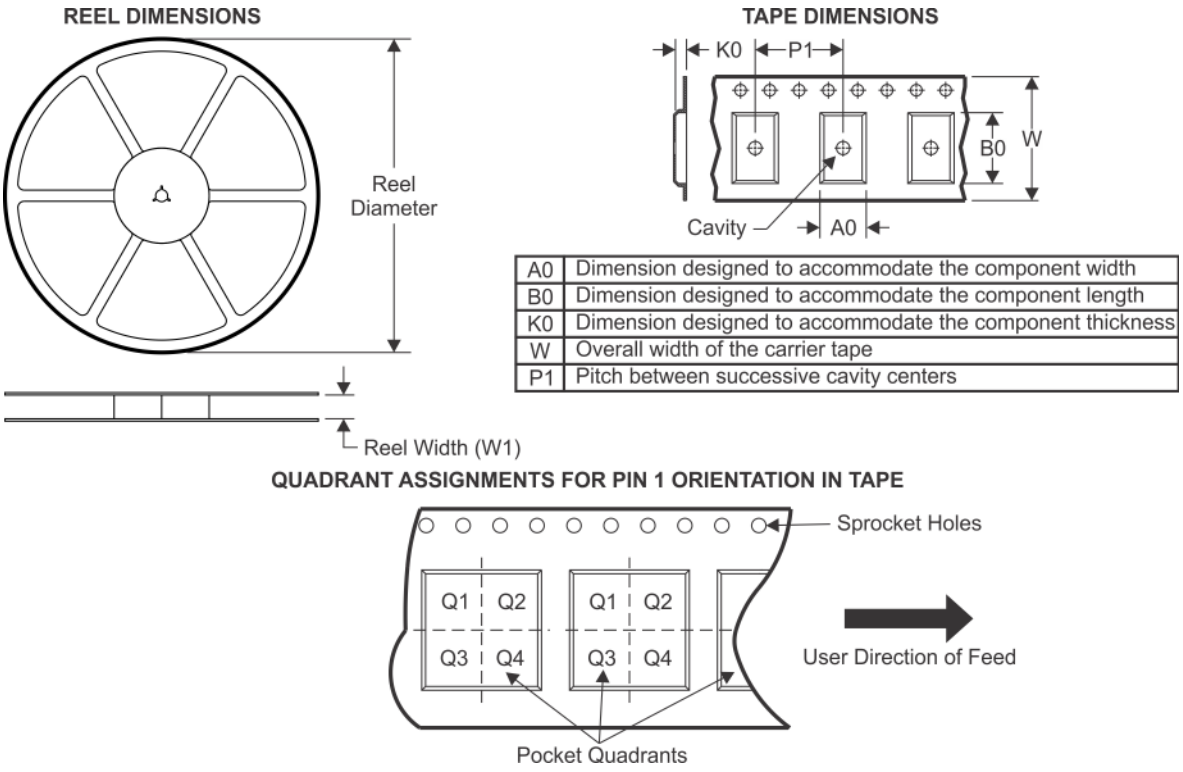
TAPE AND REEL INFORMATION

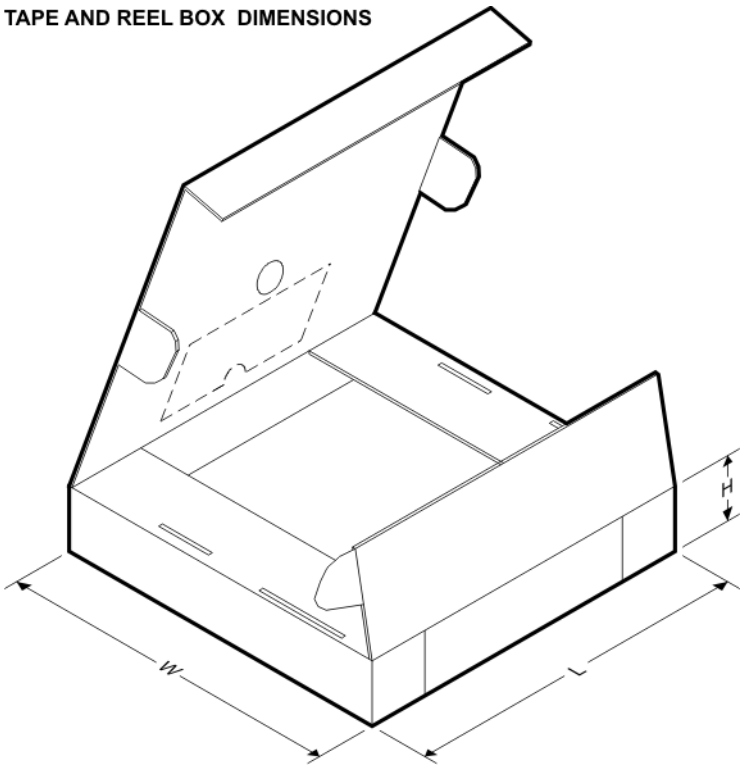


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC11001BPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DAC11001BPFBT	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

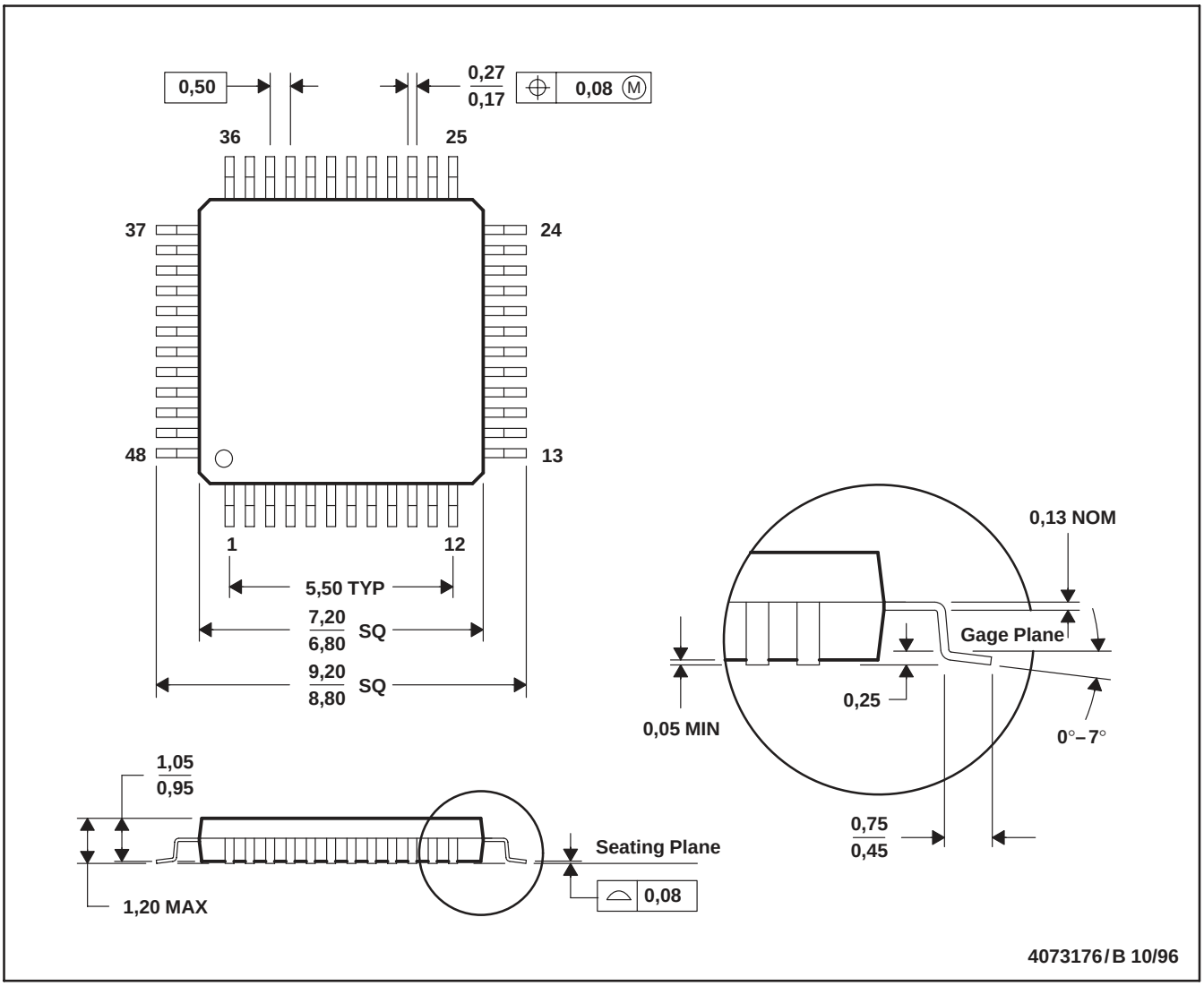


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC11001BPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
DAC11001BPFBT	TQFP	PFB	48	250	213.0	191.0	55.0

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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