

MC74AC273, MC74ACT273

Octal D Flip-Flop

The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 Has TTL Compatible Inputs

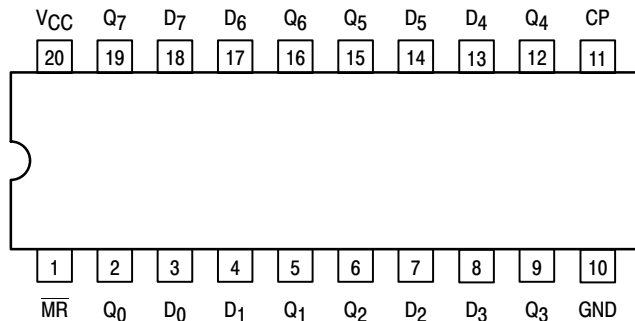


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

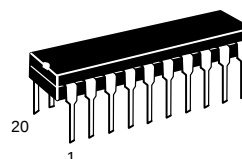
PIN ASSIGNMENT

PIN	FUNCTION
D ₀ –D ₇	Data Inputs
$\overline{\text{MR}}$	Master Reset
CP	Clock Pulse Input
Q ₀ –Q ₇	Data Outputs

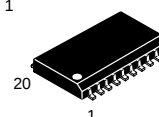


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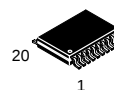
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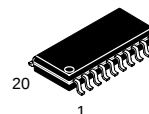
PDIP-20
N SUFFIX
CASE 738



SO-20
DW SUFFIX
CASE 751



TSSOP-20
DT SUFFIX
CASE 948E



EIAJ-20
M SUFFIX
CASE 967

ORDERING INFORMATION

Device	Package	Shipping
MC74AC273N	PDIP-20	18 Units/Rail
MC74ACT273N	PDIP-20	18 Units/Rail
MC74AC273DW	SOIC-20	38 Units/Rail
MC74AC273DWR2	SOIC-20	1000 Tape & Reel
MC74ACT273DW	SOIC-20	38 Units/Rail
MC74ACT273DWR2	SOIC-20	1000 Tape & Reel
MC74AC273DT	TSSOP-20	75 Units/Rail
MC74AC273DTR2	TSSOP-20	2500 Tape & Reel
MC74ACT273DT	TSSOP-20	75 Units/Rail
MC74ACT273DTR2	TSSOP-20	2500 Tape & Reel
MC74AC273M	EIAJ-20	40 Units/Rail
MC74AC273MEL	EIAJ-20	2000 Tape & Reel
MC74ACT273M	EIAJ-20	40 Units/Rail
MC74ACT273MEL	EIAJ-20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 221 of this data sheet.

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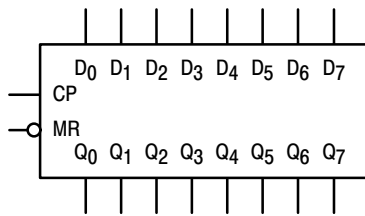


Figure 2. Logic Symbol

MODE SELECT-FUNCTION TABLE

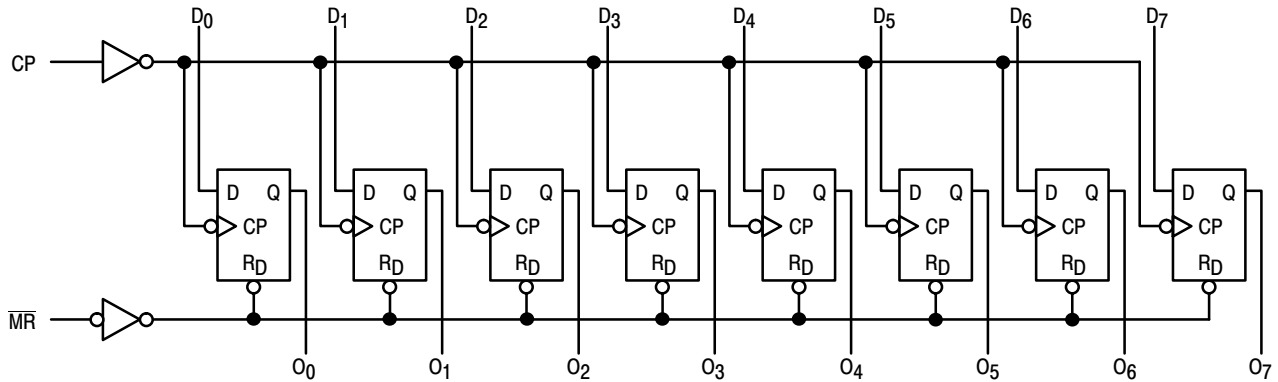
Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	$\uparrow$	H	H
Load '0'	H	$\uparrow$	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$\uparrow$ = LOW-to-HIGH Clock Transition



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0
		'ACT	4.5	5.0	5.5
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–
		V _{CC} @ 4.5 V	–	40	–
		V _{CC} @ 5.5 V	–	25	–
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–
		V _{CC} @ 5.5 V	–	8.0	–
T _J	Junction Temperature (PDIP)	–	–	140	°C
T _A	Operating Ambient Temperature Range	–40	25	85	°C
I _{OH}	Output Current – High	–	–	–24	mA
I _{OL}	Output Current – Low	–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	–	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
		4.5	–	3.86	3.76		
		5.5	–	4.86	4.76		
		5.5	–	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	–	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	–	0.36	0.44		
		5.5	–	0.36	0.44		
		5.5	–	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175	– –	75 125	– –	Mhz	3–3
t _{PLH}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.5	12.5 9.0	3.0 2.5	14.0 10.0	ns	3–6
t _{PHL}	Propagation Delay Clock to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.5 11.0	ns	3–6
t _{PHL}	Propagation Delay MR to Output	3.3 5.0	4.0 3.0	7.0 5.0	13.0 10.0	3.5 2.5	14.0 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = –40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3–9
t _h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	–2.0 –1.0	0 1.0	0 1.0	ns	3–9
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3–6
t _w	$\overline{\text{MR}}$ Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.0 4.5	ns	3–6
t _{rec}	Recovery Time $\overline{\text{MR}}$ to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0	ns	3–9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Unit	Conditions
			T _A = +25°C		T _A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 µA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 µA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	µA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	–	1.5	mA	V _I = V _{CC} – 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	–	–	–75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	µA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	125	200	–	125	–	MHz	3–3
t _{PHL}	Propagation Delay Clock to Output	5.0	3.0	6.0	10	2.5	11.0	ns	3–6
t _{PLH}	Propagation Delay Clock to Output	5.0	3.0	6.5	11	2.5	12.0	ns	3–6
t _{PHL}	Propagation Delay MR to Output	5.0	3.0	7.0	11	2.5	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW Data to CP	5.0	3.0	4.5	5.0	ns	3–9
t _h	Hold Time, HIGH or LOW Data to CP	5.0	–2.5	2.0	2.0	ns	3–9
t _w	Clock Pulse Width HIGH or LOW	5.0	2.5	4.0	4.5	ns	3–6
t _w	$\overline{\text{MR}}$ Pulse Width HIGH or LOW	5.0	2.5	4.0	4.5	ns	3–6
t _{rec}	Recovery Time $\overline{\text{MR}}$ to CP	5.0	–1.0	2.0	3.0	ns	3–6

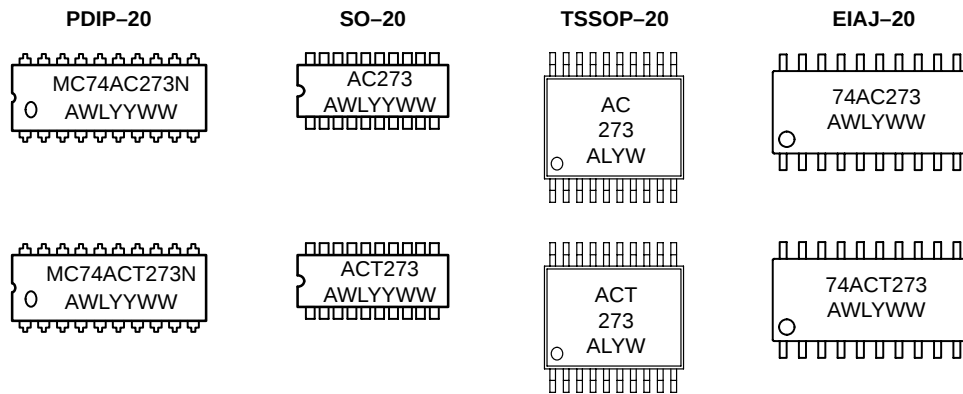
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week