CL8800

Sequential Linear LED Driver

Features

- Minimal component count (base config: CL8800 + 6 resistors + diode bridge)
- No magnetics, no capacitors
- Up to 7.5W output (13W w/ heat sink)
- >110Lm/W using efficient LEDs
- 85% typical electrical efficiency
- >0.95 power factor
- <20% THD line current
- Low conducted EMI w/o filters
- 85% LED luminous utilization
- Phase dimmer compatible with an RC network

Applications

- Fluorescent tube retrofit
- Incandescent & CFL bulb replacement
- General LED lighting

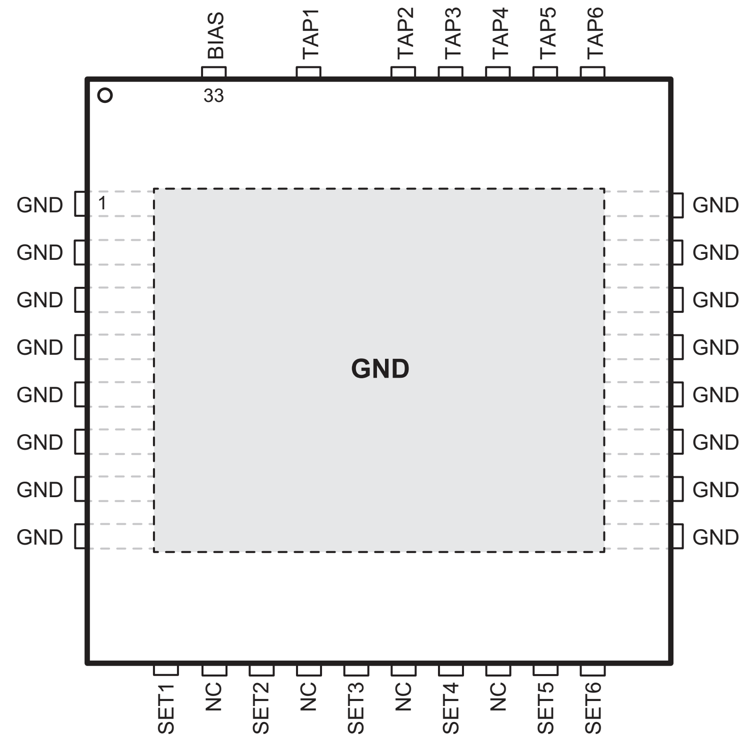
Description

CL8800 is designed to drive a long string of inexpensive, low-current LEDs directly from the AC mains. A basic driver circuit consists of CL8800, six resistors, and a bridge rectifier. Two to four additional components are optional for various levels of transient protection. No capacitors, EMI filters, or power factor correction circuits are needed.

A string of series/parallel LEDs is tapped at six locations. Six linear current regulators sink current at each tap and are sequentially turned on and off. Thereby tracking the input sine wave voltage. Voltage across each regulator is minimized when conducting, providing high efficiency. Output current at each tap is individually resistor-adjustable. Cross-regulation, as the CL8800 switches from one regulator to another, provides smooth transitions. The current waveform can be tailored to optimize for input voltage range, line/load regulation, output power/current, efficiency, power factor, THD, dimmer compatibility, and LED utilization.

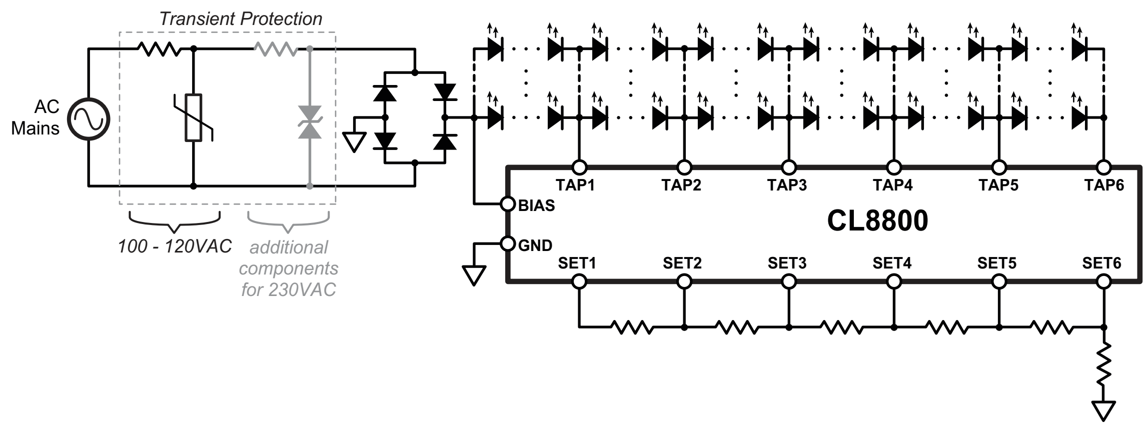
With the addition of an RC network, the driver is compatible with phase dimming.

Package Type



See Table 2-1 for pin information

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{BIAS}, V_{TAP1} .... -0.5V to +550V
V_{TAP2-6} .... -50V to +320V
V_{SET1-6} 4.0V
Operating temperature .... -55°C to +125°C
Storage temperature, T_S .... -65°C to +150°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{OUT}	Output Current	TAP1			60	mA	
		TAP2			90	mA	
		TAP3			115	mA	
		TAP4			115	mA	
		TAP5			115	mA	
		TAP6			115	mA	
V_{OUT}	Output Voltage	TAP1			400	V	Non-conducting
		TAP2-6			300	V	Non-conducting
		TAP1-6			varies[1]	V	Conducting
V_{BIAS}	Applied BIAS voltage				440	V	

1 Voltage capability is determined by power dissipation (V * I).

TABLE 1-2: ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{BIAS}	BIAS pin input current			250	410	µA	V_{BIAS} = 340V
$I_{TAP(ON)}$	Output current, on	TAP1	60			mA	V_{TAP1} = 30V, V_{SET1-6} = GND
		TAP2	90			mA	V_{TAP2} = 17V, V_{SET1-6} = GND
		TAP3	115			mA	V_{TAP3}= 17V, V_{SET1-6} = GND
		TAP4	115			mA	V_{TAP4} = 17V, V_{SET1-6} = GND
		TAP5	115			mA	V_{TAP5} = 17V, V_{SET1-6} = GND
		TAP6	115			mA	V_{TAP6} = 17V, V_{SET1-6} = GND
$I_{TAP(OFF)}$	Output current, off			0	10	µA	Tap 1-5, V_{BIAS} = 312V
V_{REG}	Regulation voltage at SET pins	SET1-5	1.80	2.00	2.20	V	
		SET6	1.89	2.10	2.31	V	

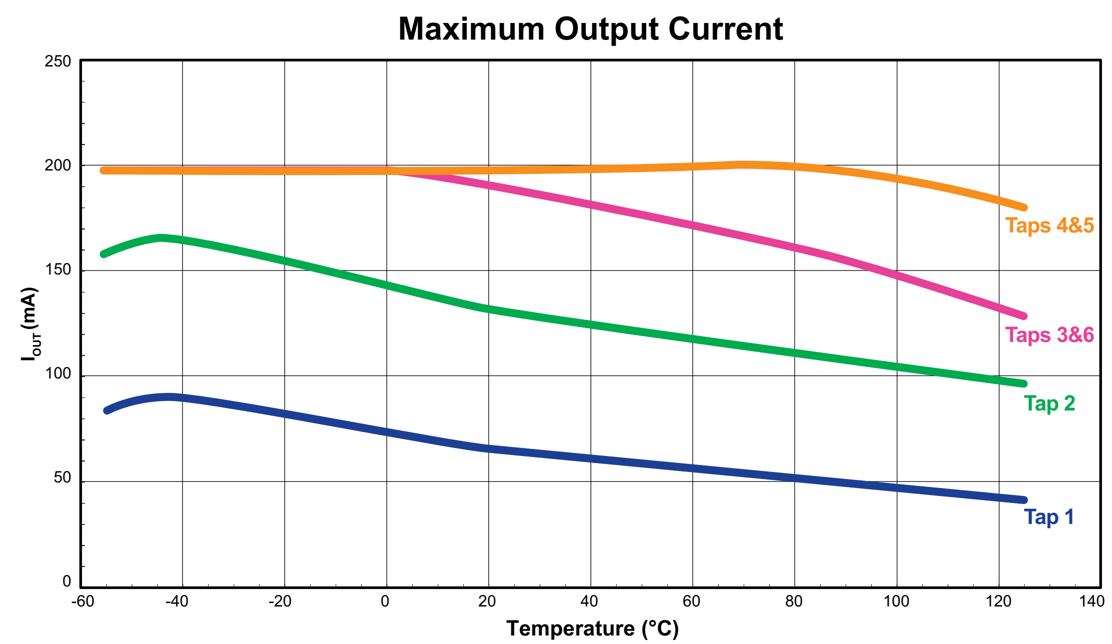
1 Over recommended operating conditions at 25°C, unless specified otherwise.

TABLE 1-3: THERMAL RESISTANCE

Package	θ_{ja}[1]	θ_{jc}[2]
33-Lead QFN	24°C/W	2.5°C/W

1 1.0 oz Cu 4-layer board, 3x4” PCB with thermal pad and thermal via array.
2 Junction to exposed heat slug.

FIGURE 1-1: OUTPUT CURRENT THERMAL CHARACTERISTICS



2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION

Pin #	Function	Description
1 - 8	GND	Circuit common (use for heat sink ground plane pass through).
9	SET1	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
10	NC	No internal connection.
11	SET2	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
12	NC	No internal connection.
13	SET3	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
14	NC	No internal connection.
15	SET4	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
16	NC	No internal connection.
17	SET5	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
18	SET6	Current sense for linear current regulators for each tap. Resistors on these pins sets the tap currents.
19 - 20	GND	Circuit common (use for heat sink ground plane pass through).
21	GND	Circuit common. Connect to bridge rectifier return (use for heat sink ground plane pass through).
22 - 26	GND	Circuit common (use for heat sink ground plane pass through).
27	TAP6	Current regulator outputs. Connect to taps along the LED string.
28	TAP5	
29	TAP4	
30	TAP3	
31	TAP2	
32	TAP1	
33	BIAS	Provides bias for driver. Connect to rectified AC.
Underside plate (GND)		For heat sinking purposes, it should be soldered to a 4.0cm2 exposed copper area. It should also be electrically connected to circuit common (GND).

3.0 APPLICATION INFORMATION

3.1 Overview

Designing a driver to meet particular requirements may be a difficult task considering the 18 design variables: tap current (6), number of series-connected LEDs per segment (6), and the number of parallel-connected LEDs per segment (6). Manually selecting values will provide light, but the chosen values may be far from optimal in regards to efficiency, LED utilization, and line regulation.

Contact your nearest Microchip Field Applications Engineer for design assistance.

In addition to configuring the driver, several circuits may be employed to increase reliability, performance, and cost. The following sections briefly describe these circuits.

3.2 Transient Protection

The driver circuits have no need for capacitors that could otherwise absorb transient energy, nor is there a need for EMI filters that would block transients. Therefore, the full burden of transient protection is borne by the protection circuit. The two-stage approach in the following schematics provide 2.5kV protection, both pulse and ring per EN 61000-4-5 and EN 61000-4-12, six hits each.

FIGURE 3-1: 100 TO 120 VAC TRANSIENT PROTECTION

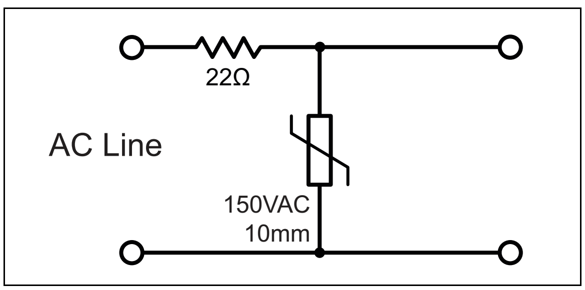
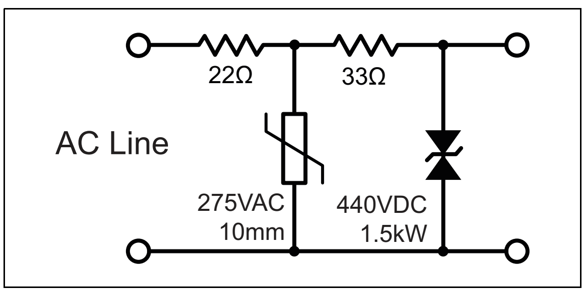


FIGURE 3-2: 230VAC TRANSIENT PROTECTION



3.3 Zener Diode Substitution

Zener diodes may be substituted for LEDs in the bottom stages of the design. The last 1 or 2 stages of LEDs contribute little to the light output - they are mainly present to off-load the adjacent upstream regulator at high line voltages to minimize losses. The advantages of Zener substitution includes minimizing unlit LEDs at low line for better light uniformity, better line regulation at high line, fewer LEDs for lower cost and less PCB area, and fewer board-to-board connections. Disadvantages include slightly-reduced efficiency at high line, and additional heat load on the driver board.

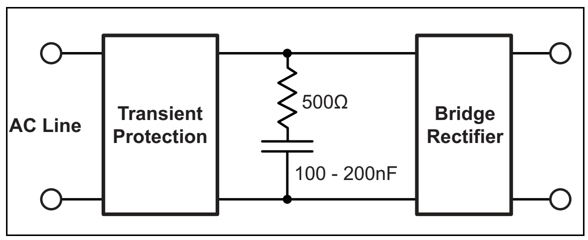
3.4 Phase Dimming

As with any light load, the LED lamp might not draw enough current to ensure proper dimmer operation. This is especially true for 230VAC dimmers. Triodes for Alternating Current (TRIAC) used in dimmers require a minimum latching current when triggered to place the TRIAC in the latched-on state. Once latched, a minimum holding current is required to maintain the TRIAC in the on state. Latching current is many times greater than the holding current, and is the main concern with dimmer compatibility.

Higher latching current can be provided by a simple series RC network across the AC line. A short time constant provides a current spike at the turn-on edge.

Less common is inadequate holding current. The minimum dimmer holding current is typically 10-20mA. Tap1 at 60mA (max) exceeds the minimum.

FIGURE 3-3: PHASE DIMMING



3.5 Strobing

Twice per AC line cycle the line voltage crosses zero volts, during which time there is no light output.

The circuit in Figure 3-4 can provide 5-10% valley fill. It has little effect on input current wave shape (THD, PF) and efficiency.

This circuit is intended to prevent the output from reaching zero. It will not significantly reduce output ripple.

3.6 Power Boost

Higher output power can be achieved by off-loading a portion of the power dissipation from the CL8800 to external Field-Effect Transistors (FET). The circuit below drops most of the tap voltage across the FETs, thereby shifting the bulk of the dissipation to the FET.

FIGURE 3-4: POWER BOOST

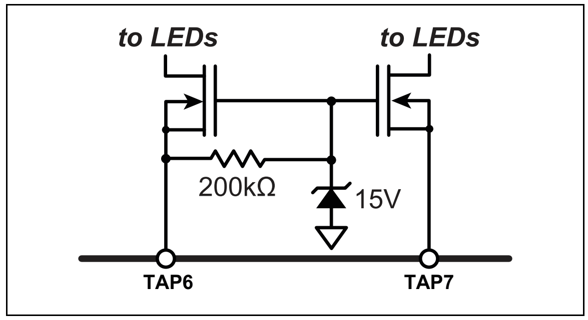


FIGURE 3-5: VALLEY FILL CIRCUIT

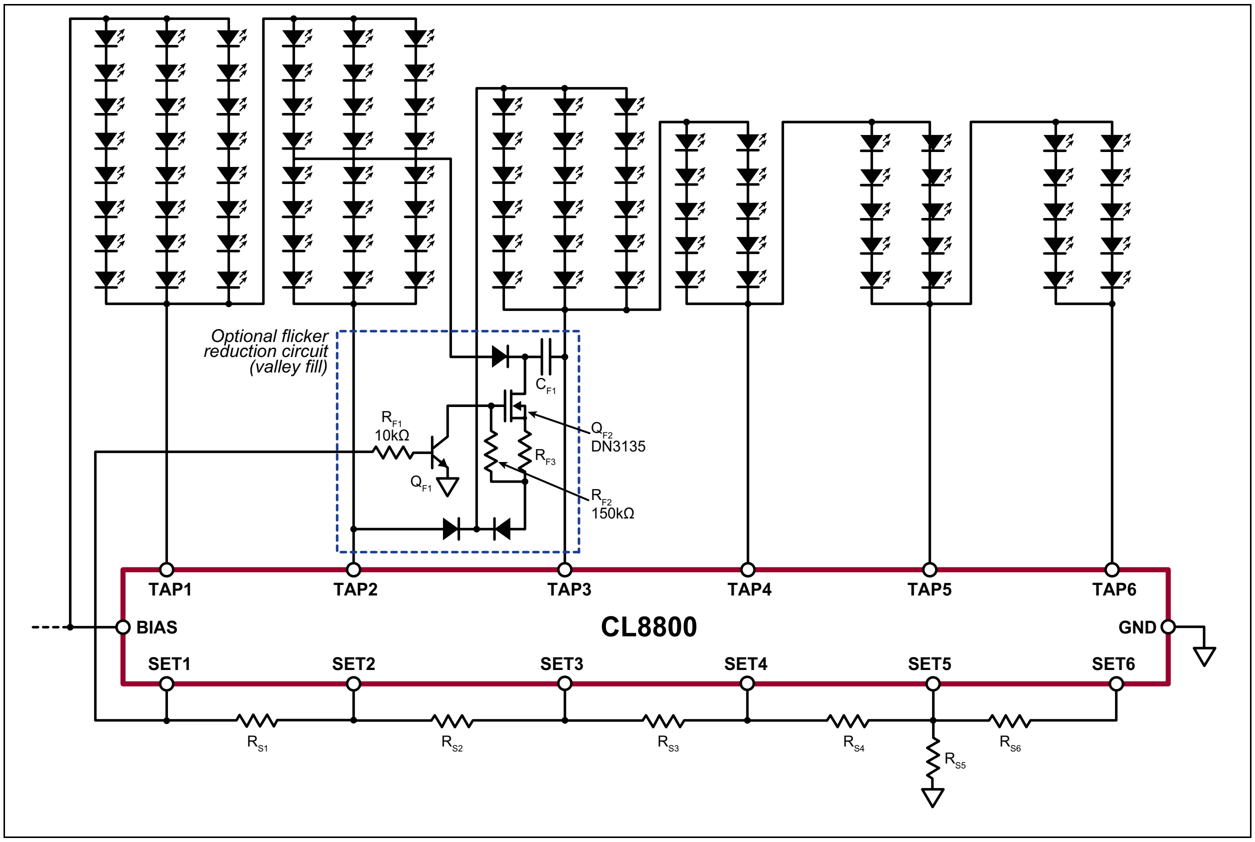
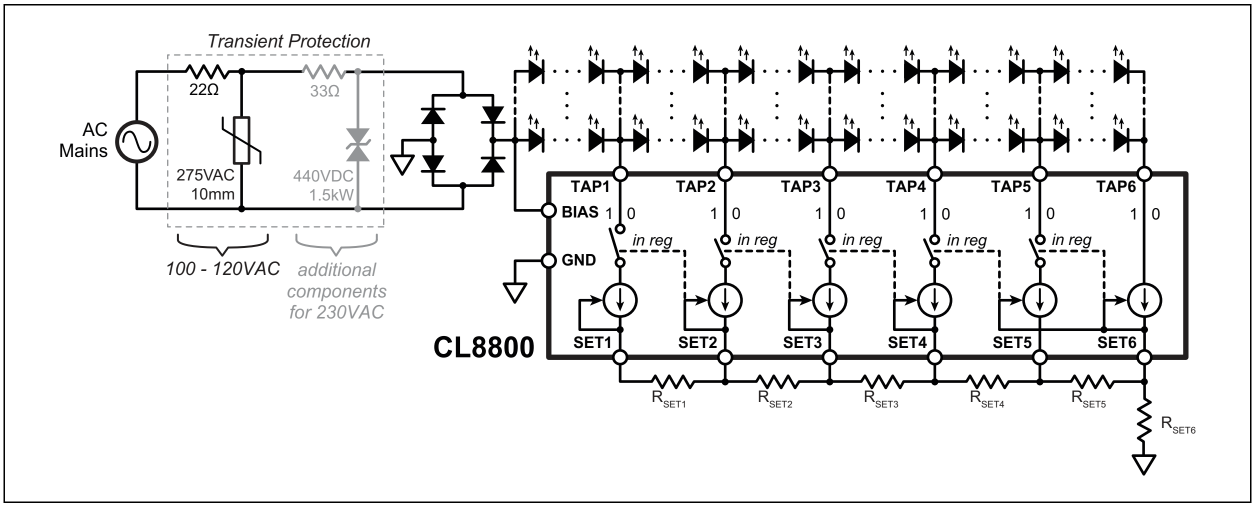


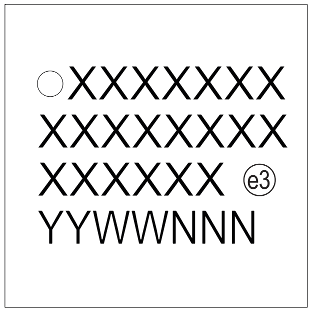
FIGURE 3-6: SIMPLIFIED BLOCK DIAGRAM



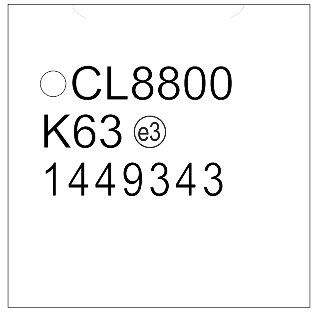
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

33-lead QFN



Example

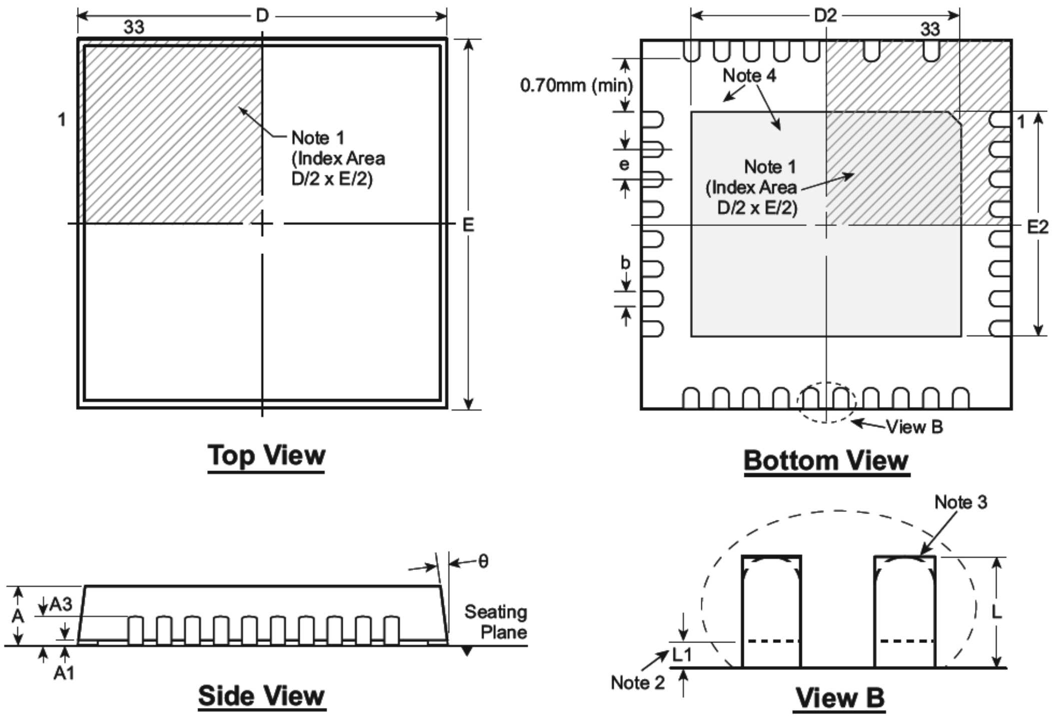


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

33-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*
4. *There will be an exposed DAP. A minimum of 0.7mm spacing will be maintained between the leads and the DAP.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85	4.00	5.85	3.60	0.50 BSC	0.30	0.00	0
	NOM	0.90	0.02		0.25	6.00	4.15	6.00	3.75		0.40	-	-
	MAX	1.00	0.05		0.30	6.15	4.25	6.15	3.85		0.50	0.15	14

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (January 2015)

- Update file to new format

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	CL8800	=	Sequential Linear LED Driver
Package:	K6(3)	=	QFN (6x6 mm body), 33-lead
Environmental	G	=	Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	=	490/Tray
	M935	=	3000/Reel

Examples:

a) CL8800K63-G: 33-lead QFN package, 490/Tray.

b) CL8800K63-G-M935 33-lead QFN package, 3000/Reel

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