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### Evaluating the ADA8282 Radar Receive Path AFE

#### **FEATURES**

Ready SPI interface for setup and control Easy connection to test equipment

#### **EVALUATION KIT CONTENTS**

ADA8282CP-EBZ evaluation board 6 V, 2 A switching power source

#### **EQUIPMENT NEEDED**

PC running Windows® USB 2.0 port SDP-B

#### **SOFTWARE NEEDED**

Analysis control evaluation (ACE) software

#### **GENERAL DESCRIPTION**

The ADA8282CP-EBZ is designed to aid in the evaluation of the ADA8282 radar receive path analog front-end (AFE). The board connects to the system demonstration platform (SDP) for easy configuration of registers through a serial peripheral interface (SPI) using the ACE evaluation software. The board provides headers to allow configuration using other platforms. It also includes on-board options to provide manual reset capability to the part.

This user guide provides quick start instructions for working with the board.

Full specifications for the ADA8282 are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.



#### **DIGITAL PICTURE OF THE BOARD**

Figure 1.

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#### **REVISION HISTORY**

7/15—Revision 0: Initial Version

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### EVALUATION BOARD HARDWARE POWER SUPPLY

The ADA8282CP-EBZ comes with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. The supply may be connected to the rated 100 V ac to 240 V ac to provide power to the board.

The ADA8282 requires 3.3 V for both analog (AVDD) and digital (VIO) power. The evaluation board has an on-board ADP7118 (U3) regulator for this purpose. U3 directly supplies the power for AVDD. The user may opt to use U3 to provide power to VIO by placing a header at VIO\_3V3.

The SDP requires a 5 V supply to properly control the board. This supply is derived from the on-board ADP7105 (U2). The 5V\_EN header allows the user to enable or disable this supply. Positions for the shunt to enable or disable are indicated on the board. U2 may be disabled if a different external controller is used.

#### **ANALOG INPUTS**

Each input is configured with SMA ports, +JINx and –JINx (where x stands for Channel A, Channel B, Channel C, or Channel D), and terminated with 50  $\Omega$  for easy interfacing to source equipment. The inputs are ac-coupled through 0.1  $\mu F$  capacitors to the ADA8282. Use P1INx (where x stands for Channel A, Channel B, Channel C, or Channel D) to short any two differential lines together.

The inputs of the ADA8282 are intended to be driven by a differential signal source. The output signal swing is reduced by a factor of 2 when driven by a single-ended source.

#### ANALOG OUTPUTS

Each output is configured with SMA ports, +JOUTx and –JOUTx (where x stands for Channel A, Channel B, Channel C, or Channel D), which allows easy interfacing to equipment. Components are included for high-pass filtering at the output.

#### **RESET LOGIC INPUT**

A switch to control the RESET pin of the ADA8282 is available on the board. The switch position to reset the board is indicated on the evaluation board.

#### **DIGITAL LINES**

The SDP-B is used to provide digital signals to configure the ADA8282. Short the SPI headers to use the SDP. If an external controller is used to generate the digital signals, the signals can be ported through the SPI header.

#### JUMPER CONFIGURATIONS

The jumper settings/link options on the evaluation board for the required operating modes are described in Table 1. Figure 2 shows the default jumper settings.

Table 1. Jumper Descriptions	Table	1. Jum	per Des	scriptions
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Jumper	Description
SPI	SPI lines. Short all jumpers to configure the registers via the SDP.
VIO_3V3	Digital supply pin, VIO. Short the jumper to supply the VIO pin of the ADA8282 with the on-board regulator supply of 3.3 V.
5V_ENBL	5 V supply enable. Place a shunt at Position 1 to enable the 5 V on-board regulator. Place the shunt at Position 3 to disable the 5 V on-board regulator. Correct positions are indicated on the board.
RESET	This switch provides the required logic level to reset the device through hardware. To reset, follow the indicated position on the board.



Figure 2. Default Evaluation Board Configuration Rev. 0 | Page 3 of 16

# **EVALUATION BOARD SOFTWARE QUICK START PROCEDURES**

This section provides quick start procedures and software information for using the ADA8282CP-EBZ board.

#### **EVALUATION BOARD SOFTWARE**

To use the board with the SDP-B, make sure that the ACE software is available on your computer. The software installer and a comprehensive user guide for the tool are available on the ACE Wiki.

### QUICK START PROCEDURES

Figure 6 shows the typical evaluation board setup for the ADA8282CP-EBZ. Complete the following steps to enable functionality testing of the part:

- 1. Configure the jumpers as shown in Figure 2.
- 2. Connect the SDP connector on the ADA8282CP-EBZ to Connector A of the SDP-B.
- 3. Connect the 6 V power supply to the board at P2 and connect to a power source.
- 4. Plug the USB cable into the USB port.
- 5. Run the ACE software.
- 6. Upon running the software, the hardware should automatically be detected (see Figure 3).

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Figure 3. ACE Executable

7. Double-click the ADA8282 evaluation board plug-in to navigate to the ACE board view (see Figure 4).



#### Figure 4. ADA8282 ACE Board View

8. Double-click the ADA8282 component on the board to navigate to the chip view (see Figure 5). Click the tabs to select a previous or different view.

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	all and and	
	and the second second second	
	COLUMN 1	
		The Proceed to Memory Map

Figure 5. ADA8282 ACE Chip View

- 9. Write a data byte of 0x0F to Register 0x17 to enable all channels of the device, using any of the configuration methods discussed in the Configuring the ADA8282 through ACE section.
- 10. Power up the signal generator and check the waveform through the oscilloscope. The default gain is 18 dB for all channels.



Figure 6. Typical Evaluation Setup Rev. 0 | Page 4 of 16

#### **CONFIGURING THE ADA8282 THROUGH ACE**

The ACE software provides several views or interfaces for configuring the ADA8282 via the SDP-B. Raw SPI writes and reads may be done through the register debugger. The chip view provides a more graphical approach to configuring the ADA8282, while the memory map provides users with the option to change register settings bit by bit.

#### USING THE REGISTER DEBUGGER

Raw SPI data writes and reads may be performed on the device using the register debugger.

To write to the device, complete the following steps:

1. Select the address from the **Address** drop-down menu on the register debugger (see Figure 7).

ADA828	2				
Address:	0x				Ŧ
Data:	0x	0000	0 : intf	_confa	-
	0x	0003	1 : soft	_reset	
History		0004	4 : chip	o_id1	-
R/W	Add	0003	5 : chip	o_id2	
		0000	5 : revi	sion	-
		0010	):Ina	offset	)
		001	1 : Ina_	offset1	L
		0012	2 : Ina_	offset2	2
		4	- 18		1

Figure 7. Register Debugger Drop-Down Menu

2. Enter the data to be written to the device in the **Data** text box and click **Write** (see Figure 8).

ADA828	32		
Address:	0x	0015:	pga_gain 🔻
Data:	Qx	01	Write
	0x	0	Read
History			
R/W	Add	iress	Data
147	001	-	01

Figure 8. Writing Data to the ADA8282

To read from the device, complete the following steps:

- 1. Select the address from the Address drop-down menu,
- 2. Click **Read** (see Figure 9).



#### Figure 9. Reading Data from the ADA8282

#### USING THE ACE SOFTWARE CHIP VIEW

The ACE software provides a chip view for the ADA8282. This allows the user to configure the part graphically. Enabling or disabling channels, along with gain manipulation, can be accomplished using the chip view.

To enable or disable a channel, click the channel of interest. An enabled channel is highlighted in blue, while a disabled channel is grayed out. In Figure 10, Channel A is enabled, while the rest of the channels are disabled.



Figure 10. Enabled and Disabled Channels

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To manipulate the gain of a channel, type in the desired gain on the corresponding channel that should be changed in the **PGA** section. Note that only the gain of enabled channels may be changed (see Figure 11).



Figure 11. Manipulating Gain

To write the preferred settings to the registers of the device, click **Apply Changes** on the toolbar (see Figure 12).

Start A	system A	ADAOZ	OZ EVAI D	Jaru A	ADA0202	
Apply Changes	Read All	Reset Chip	Diff	Softwa Defaul	re ts	
		10000000000		0.000.000.000		

Figure 12. Chip View Toolbar

#### USING THE ACE MEMORY MAP

The memory map for the ADA8282 can be accessed by clicking the **Proceed to Memory Map** found on the lower right portion of the chip view (see Figure 5). The memory map view can show either the register fields or the bit fields of the device.

The register view allows the user to manipulate the bits one by one. Each register may be expanded to show its corresponding bit fields for easier configuration.

Clicking a bit toggles its value (see Figure 13).



Figure 13. Register Field View

The bit field view allows the user to configure the ADA8282 by modifying its control values. The hexadecimal data is displayed in the **Data (Hex)** column.

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filter View	ins, amorti	12	2.2
hunctional Groups	majofiset2	11	
KOACIEC Mening Man	We shut!	12	1.
	safeiti	10	
	autoria.	15	- A
	ange, bran, set		
	exee	a.	
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Figure 14. Bit Field View

As with the chip view, the desired setting of the registers is only written to the ADA8282 when **Apply Changes** is clicked.

For more detailed information on using the ACE software, see the ACE Wiki.

#### ADA8282 REGISTER SUMMARY

The register settings for the ADA8282 are given in the register section of the ADA8282 data sheet. An abbreviated register summary is shown in Table 2.

Table 2.	ADA8282	Register	Summary	ÿ
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Register Address	Register Name
0x00	INTF_CONFA
0x01	SOFT_RESET
0x04	CHIP_ID1
0x05	CHIP_ID2
0x06	Revision
0x10	LNA_OFFSET0
0x11	LNA_OFFSET1
0x12	LNA_OFFSET2
0x13	LNA_OFFSET3
0x14	BIAS_SEL
0x15	PGA_GAIN
0x17	EN_CHAN
0x18	EN_BIAS_GEN
0x1D	SPAREWRO
0x1E	SPARERDO

## **EVALUATION BOARD SCHEMATICS AND ARTWORK**



Figure 15. Input Schematic

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Figure 16. Output Schematic



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Figure 18. Power Section Schematic Rev. 0 | Page 11 of 16

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Figure 19. SDP Schematic





Figure 21. Evaluation Board Layout, Layer 2

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Figure 23. Evaluation Board Layout, Layer 4

### **ORDERING INFORMATION**

### **BILL OF MATERIALS**

Table	Table 3.					
Item	Qty	Reference Designator	Description	Manufacturer	Part Number	
1	1	U1	IC 32 kB serial EEPROM	Microchip Technology	24LC32A-I/ST	
2	1	U2	500 mA, low noise regulator	Analog Devices, Inc.	ADP7105ARDZ-5.0	
3	1	U3	Low noise linear regulator	Analog Devices, Inc.	ADP7118ARDZ-3.3	
4	1	U4	IC-TTL bus buffer	NXP Semiconductors	74HC1G125GW	
5	1	U5	4-channel LNA and PGA	Analog Devices, Inc.	ADA8282WBCPZ	
6	8	+JINA, +JINB, +JINC, +JIND, -JINA, -JINB, -JINC, -JIND	End launch SMA	Johnson	142-0701-801	
7	8	+JOUTA, +JOUTB, +JOUTC, +JOUTD, –JOUTA, –JOUTB, –JOUTC, –JOUTD	Straight SMA	Johnson	142-0701-201	
8	1	5V_EN	3-pin header	Samtec	TSW-103-08-G-S	
9	2	C1, C7	10 μF, 100 V tantalum capacitor	Kemet	T491D106K025AT	
10	14	C2 to C6, C10, C1INA, C1INB, C1INC, C1IND, C2INA, C2INB, C2INC, C2IND	0.1 μF, X7R, 50 V, 0805 capacitor	Kemet	C0805C104J5RACTU	
11	1	C12	1 μF, 25 V, 0805 capacitor	Murata	NFM21PC105B1C3B	
12	4	C8, C9, C13, C14	1 μF, X5R, 6.8 V, 0603 capacitor	Murata	GRM188R61E105KA12D	
13	4	C1OUTA, C1OUTB, C1OUTC, C1OUTD	5 pF, C0G, 2.2 V, 0805 capacitor	Murata	GQM2195C2A5R0CB01D	
14	8	C2OUTA, C2OUTB, C2OUTC, C2OUTD, C3OUTA, C3OUTB, C3OUTC, C3OUTD	1 μF, X7R, 0805 capacitor	AVX	08051C104JAT2A	
15	1	C39	10 μF, 13.2 V tantalum capacitor	AVX	TAJA106K010RNJ	
16	1	C40	1 μF, X8R, 0603 capacitor	TDK	C1608X8R1E104K	
17	1	CR1	Zener	Micro Commercial Components	SMBJ5342B-TP	
18	2	DS1, DS2	LED	Lumex	SML-LX0603GW-TR	
19	1	E1	Ferrite bead, 330 Ω, 0805	Murata	BLM21PG331SN1D	
20	1	F1	Fuse, 50 V	Littelfuse	1210L050YR	
21	12	P1INA, P1INB, P1INC, P1IND, P1OUTA, P1OUTB, P1OUTC, P1OUTD, P2OUTA, P2OUTB, P2OUTC, P2OUTD	2-pin header	Berg	69157-102	
22	1	P2	Power jack	CUI Inc.	PJ-002A-SMT	
23	8	R1INA, R1INB, R1INC, R1IND, R2INA, R2INB, R2INC, R2IND	SM, 49.9 Ω, 1%, 1/10 W, 0805 resistor	Panasonic	ERJ-6ENF49R9V	
24	10	R5, R7, R1OUTA, R1OUTB, R1OUTC, R1OUTD, R2OUTA, R2OUTB, R2OUTC, R2OUTD	SM, 0 Ω, 1%, 1/16 W, 0805 resistor	Panasonic	ERJ-6GEY0R00V	
25	2	R2, R3	SM, 100 kΩ, 1%, 1/10 W, 0603 resistor	Panasonic	ERJ-3EKF1003V	
26	8	R3OUTA, R3OUTB, R3OUTC, R3OUTD, R4OUTA, R4OUTB, R4OUTC, R4OUTD	SM, 5 kΩ, 0805 resistor	Vishay	PNM0805E5001BST5	
27	1	R4	SM, 1 kΩ, 0603 resistor	Panasonic	ERJ-3EKF1001V	
28	1	R6	SM, 165 Ω, 0603 resistor	Panasonic	ERJ-3EKF1650V	
29	4	R60 to R63	SM, 33 Ω, 0603 resistor	Multicomp	MC 0.063W 0603 1% 33R	
30	1	R71	SM, 49.9 kΩ, 0603 resistor	Panasonic	ERJ-3EKF4992V	
31	1	RESET	Slide switch	Secma	09-03-201-02	
32	1	SDP	SDP connector	Hirose	FX8-120S-SV(21)	
33	1	SPI	8-pin header	Samtec	TSW-104-08-G-D	
34	1	TP_VIO	Test point	Vector	K24A	
35	1	VIO_3V3	2-pin header	Samtec	TSW-102-08-G-S	

### NOTES



#### circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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