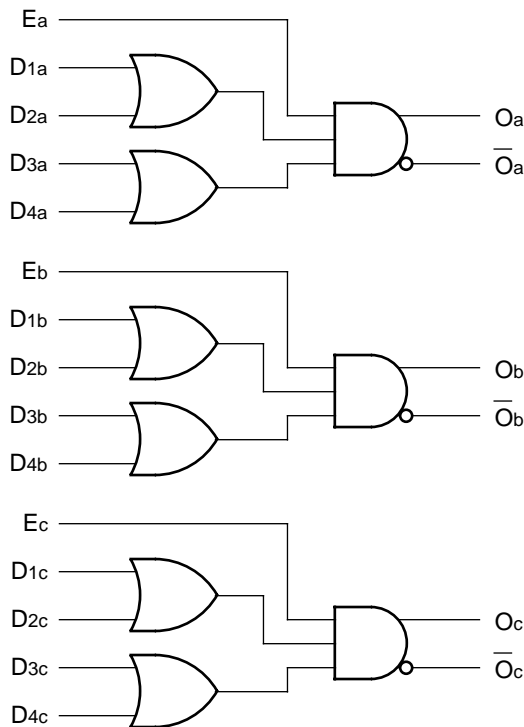
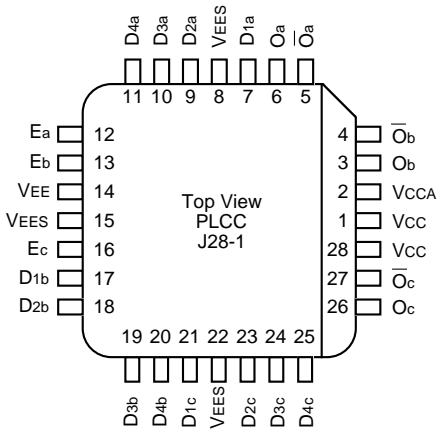


- Max. propagation delay of 900ps
- IEE min. of -48mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- Approximately 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

The SY100S317 is a set of ultra-fast, triple 2-wide OR/AND gates designed for use in high-performance ECL systems. This device offers both true and complement outputs. The inputs on this device have 75kΩ pull-down resistors.



Pin	Function
Dna - Dnc	Data Inputs (n = 1...4)
Ea - Ec	Enable Inputs
Oa - Oc	Data Outputs
$\bar{O}a - \bar{O}c$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs



**28-Pin PLCC (J28-1)**

### Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S317JC	J28-1	Commercial	SY100S317JC	Sn-Pb
SY100S317JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S317JC	Sn-Pb
SY100S317JZ <sup>(2)</sup>	J28-1	Commercial	SY100S317JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S317JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S317JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

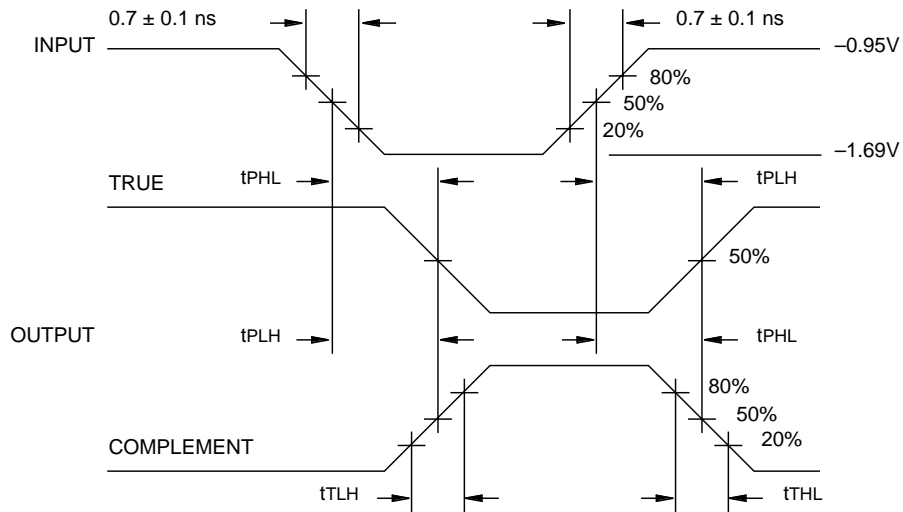
1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current, All Inputs	—	—	200	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
I <sub>EE</sub>	Power Supply Current	-48	-32	-22	mA	Inputs Open

$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

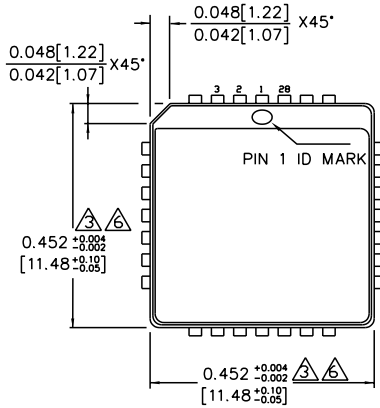
Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	300	900	300	900	300	900	ps	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Enable to Output	300	700	300	700	300	700	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	



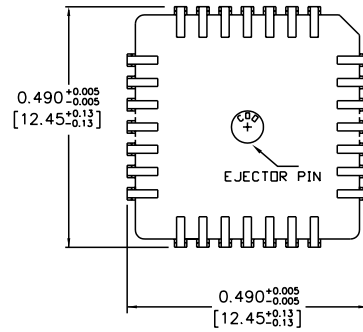
**Propagation Delay and Transition Times**

**Note:**

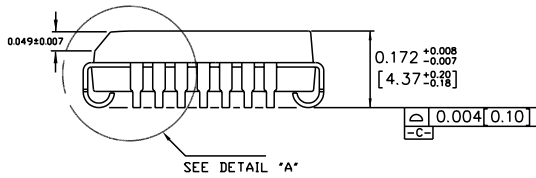
$V_{EE} = -4.2V$  to  $-5.5V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$



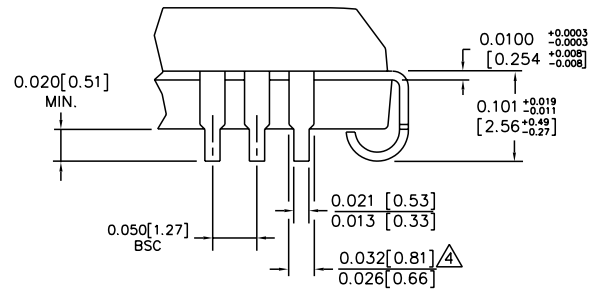
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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