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Evaluating the ADG5404F Fault Protection and Detection, 10 Ω R_{ON}, 4-Channel Multiplexer

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LED for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board low dropout (LDO) regulator for digital supply and control if required

ONLINE RESOURCES

- Evaluation Kit Contents
  - EVAL-ADG5404F
- Documents Needed
  - ADG5404F data sheet

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital voltage source: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as digital multimeter (DMM)

GENERAL DESCRIPTION

This user guide describes the evaluation board for the ADG5404F, which is a 4-channel multiplexer. The ADG5404F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered state.

Figure 1 shows the EVAL-ADG5404FEBZ in a typical setup. The ADG5404F is soldered to the center of the board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, with a fourth terminal used to provide a user defined digital voltage, if required. Alternatively, an LDO regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

TYPICAL SETUP

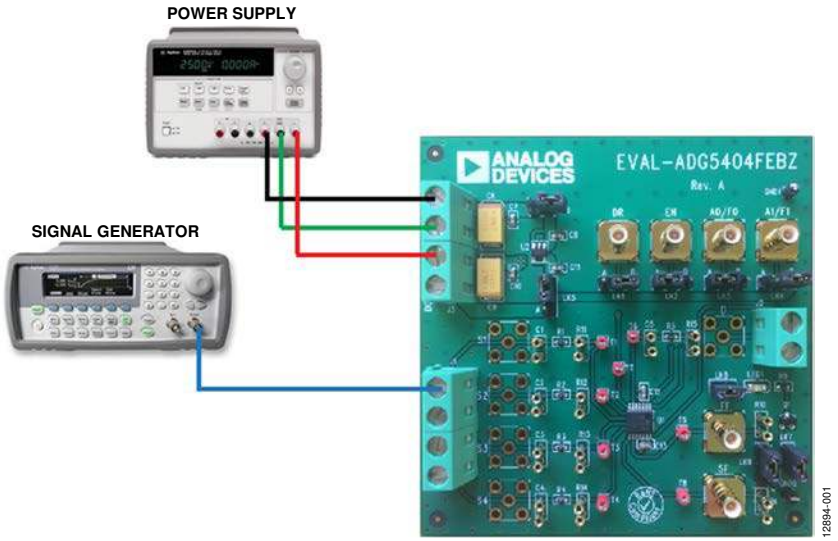

Figure 1. EVAL-ADG5404FEBZ, Power Supply, and Signal Generator

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REVISION HISTORY

9/15—Rev. 0 to Rev. A

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Added Ordering Information Section, Bill of Materials, and Table 3 ... 10

2/15—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5404FEBZ board operates independently and does not require any additional evaluation boards or software. An on-board LDO regulator provides digital control and the supply voltage.

Supply the evaluation board with a dual power source of up to ±22 V or a single supply of up to 44 V. For single-supply operation, connect VSS to GND using J3.

Set up a functionality test as follows:

- Connect a power supply to J3. For single-supply operation, connect VSS to GND using J3.
- Insert a header at LK6 to use the on-board LDO regulator, and set the header at LK5 to Position B.
- LK2 through LK4 control the digital signals for each switch on the ADG5404F.
  - When these three links are in Position A, the switches are open (off).
  - When these three links are in Position B, the S4 switch is closed (on), and it has a resistance of approximately 10 Ω.
- When LK9 is in Position A, LED1 lights up to indicate that no faults were detected at any of the source pins.

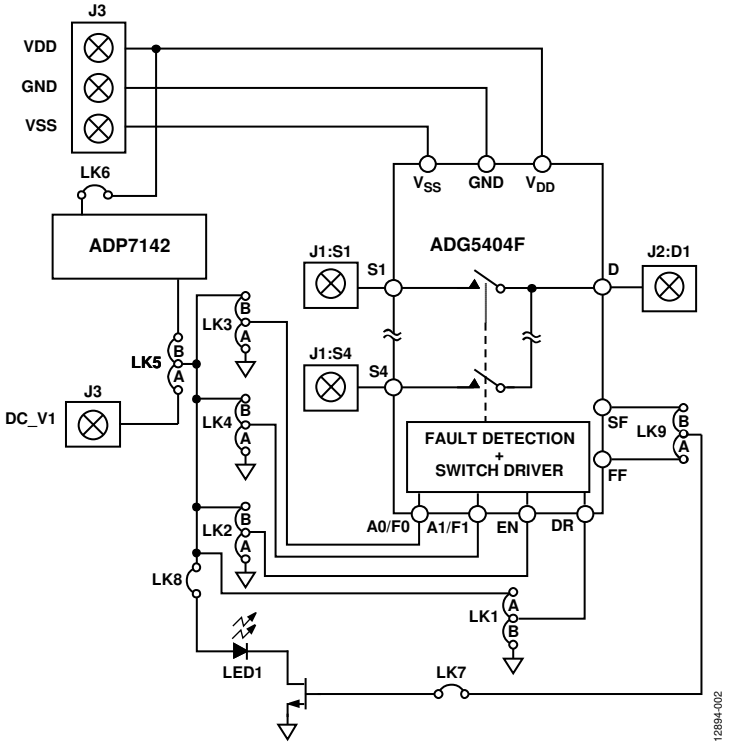

Figure 2. EVAL-ADG5404FEBZ Block Diagram

EVALUATION BOARD HARDWARE

Use the EVAL-ADG5404FEBZ to evaluate the ADG5404F. Figure 1 shows a typical setup where only a power supply and signal generator are required. Figure 2 shows a block diagram of the main components of the evaluation board.

The connectors on the board pass signals through the ADG5404F switch. The source pins have fault detection circuitry that reacts to an overvoltage. During an overvoltage event, the switch turns off and the FF pin pulls low. The SF pin pulls low when the source where the overvoltage occurs is the one selected by the A0/F0 and A1/F1 pins. See the ADG5404F data sheet for further details.

POWER SUPPLIES

Connector J3 provides access to the supply pins of the ADG5404F. VDD, GND, and VSS link to the appropriate pins on the ADG5404F. For dual-supply voltages, power the evaluation board from ±5 V to ±22 V. For single-supply voltages, connect the GND and V_{SS} terminals and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator provides for digital control voltage. If necessary, connect a secondary voltage source to DC_V1 and use it as the digital control voltage. To use DC_V1, set the header at LK5 to Position A.

INPUT SIGNALS

Two screw connectors connect the source and drain pins of the ADG5404F. If extra connections are required, additional Subminiature Version B (SMB) connector pads are laid out.

The ADG5404F is overvoltage protected on the source side, and the maximum voltage that can be applied to S1 through S4 is −55 V or +55 V. See the ADG5404F data sheet for more details.

Each trace on the source and drain side includes two sets of gold pin connectors for placing a load on the signal path to ground. Place a 0 Ω resistor in the signal path, or it can be replaced with a user defined value. Use the resistor combined with the gold pin connectors to create a simple resistor/capacitor (RC) filter.

Use parallel interface channels (A0/F0 and A1/F1) to control the operation of the ADG5404F switches. Use the headers on LK2 through LK4 to manually control the operation of the switches, or connect an external controller directly to the control pins by using the SMB connectors (A0/F0, A1/F1, and EN) and by removing the link headers on LK2 through LK4.

OUTPUT SIGNALS

The ADG5404F has two outputs. The FF pin indicates when the device operates normally or whether there is an overvoltage fault on one of the source pins. The SF pin also indicates when an overvoltage occurs on one of the source pins and transitions low only when an overvoltage occurs on the channel selected by the A0/F0 and A1/F1 inputs. For visual indication, an LED is mounted on the evaluation board. Use LK8 to connect the LED circuit. When the device operates normally, the FF pin remains high, and the LED turns on. If an overvoltage occurs at any of the source pins, the FF pin pulls low, and the LED turns off.

The LK9 selector allows the user to choose which output controls the LED. Setting the header to Position A allows the FF pin to control the LED. Setting the header to Position B, the SF pin controls the LED.

SMB connectors can interface the evaluation board with external controllers, and two gold pin connectors can connect a pull-up resistor between the FF and SF signals and the digital supply.

The DR pin allows the user to choose the state of the drain pin when the device deactivates during an overvoltage. The LK1 selector allows the user to choose between open circuit and pulling to the rails.

JUMPER SETTINGS

LINK HEADERS

Use the link headers to control the ADG5404F manually, to configure the digital control voltage, and to isolate the LED from the system. Table 2 lists the link header descriptions, and how the links can be used on the evaluation board.

Use LK3 and LK4 to control the switches of the ADG5404F. Use LK2 to enable or disable the device.

Position A ties to GND and sets the logic low, whereas Position B ties to DC_V1 and sets the logic high.

Table 1. ADG5404F Truth Table

LK2 (EN)	LK3 (A0)	LK4 (A1)	Connected Sx
A	X[1]	X[1]	All switches off
B	A	A	S1
B	B	A	S2
B	A	B	S3
B	B	B	S4

[1] X = don't care.

LK1 allows the user to configure the drain state during an overvoltage condition.

LK6 connects the on-board LDO regulator to the V_{DD} supply. Remove the header to protect the LDO regulator from voltages higher than 28 V or to use an alternative digital control voltage. Change the header on LK5 to Position B to connect to DC_V1.

LK8 connects the LED to the digital power supply, and LK7 connects the FF pin or the SF pin of the ADG5404F to the LED.

SMB CONNECTORS

Control the parallel interface of the ADG5404F manually by using the link headers of LK2 through LK4, or access the interface by using the SMB connectors (A0/F0, A1/F1, and EN). To use the SMB connectors, remove the link headers of LK2 through LK4. Use the FF/SF SMB connectors to access the FF/SF digital outputs from the ADG5404F.

Table 2. Link Header Descriptions

Link Header	Position	Description
LK1	A	VDD or VSS during an overvoltage
	B	Open circuit during an overvoltage
LK2	A	All switches off (disabled)
	B	Device enabled (EN pin), switch function set by A0/F0 and A1/F1 pins
LK3	A	Logic 0 on A0/F0 pin
	B	Logic 1 on A0/F0 pin
LK4	A	Logic 0 on A1/F1 pin
	B	Logic 1 on A1/F1 pin
LK5	A	DC_V1 digital voltage
	B	On-board LDO regulator digital voltage
LK6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
LK7	Inserted	FF/SF pins connected to LED
	Removed	FF/SF pins disconnected from LED
LK8	Inserted	LED powered up
	Removed	LED unpowered
LK9	A	FF pin controls the LED
	B	SF pin controls the LED

EVALUATION BOARD SCHEMATICS AND ARTWORK

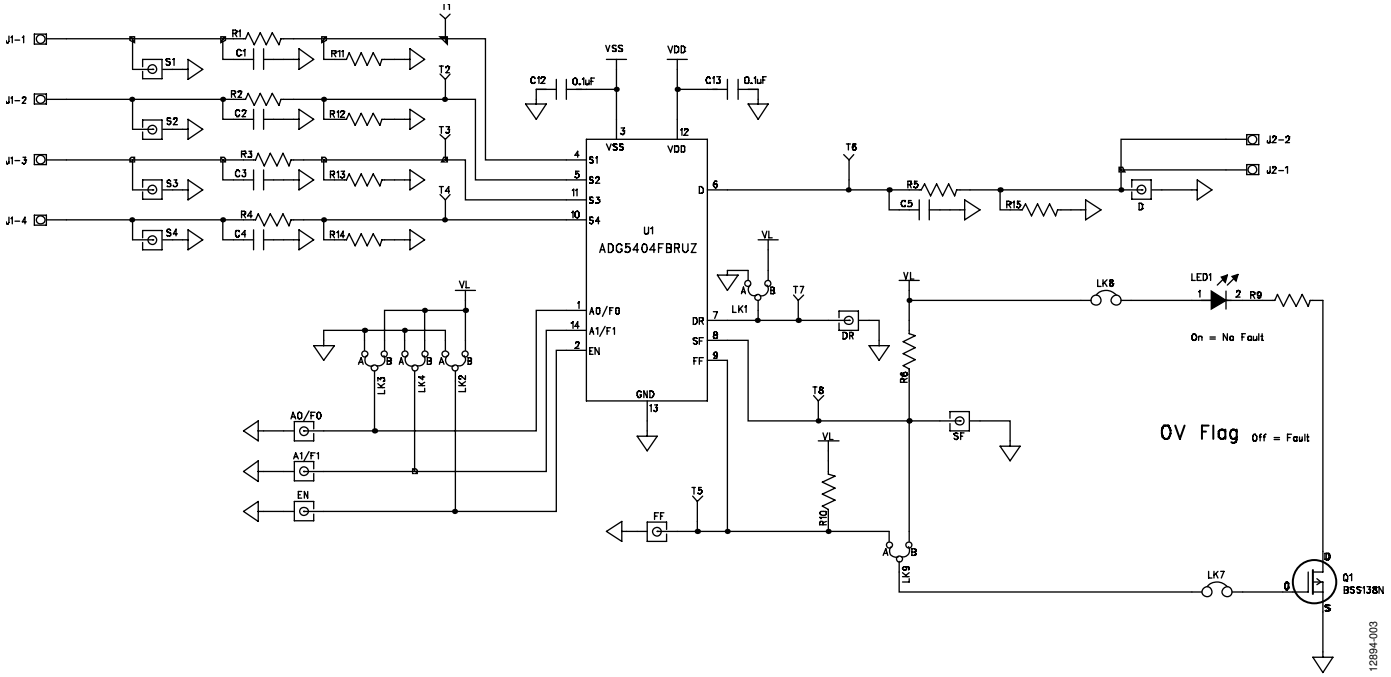

Figure 3. EVAL-ADG5404FEBZ Evaluation Board Schematic (Part 1)

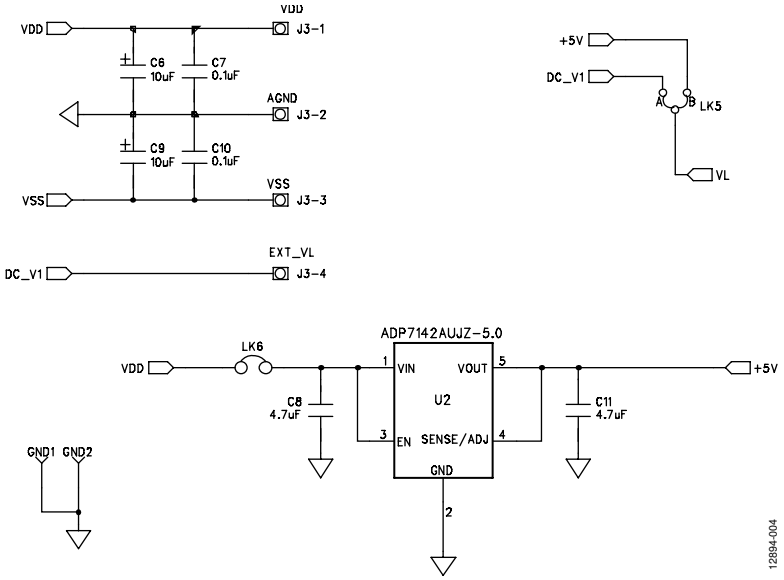

Figure 4. EVAL-ADG5404FEBZ Evaluation Board Schematic (Part 2)

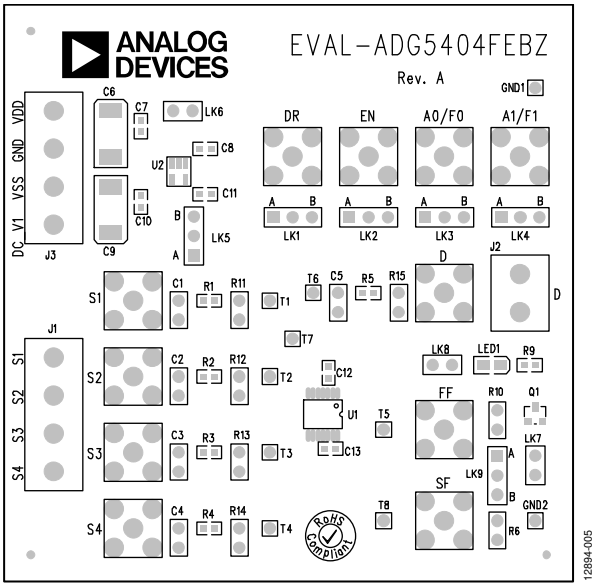

Figure 5. EVAL-ADG5404FEBZ Silkscreen

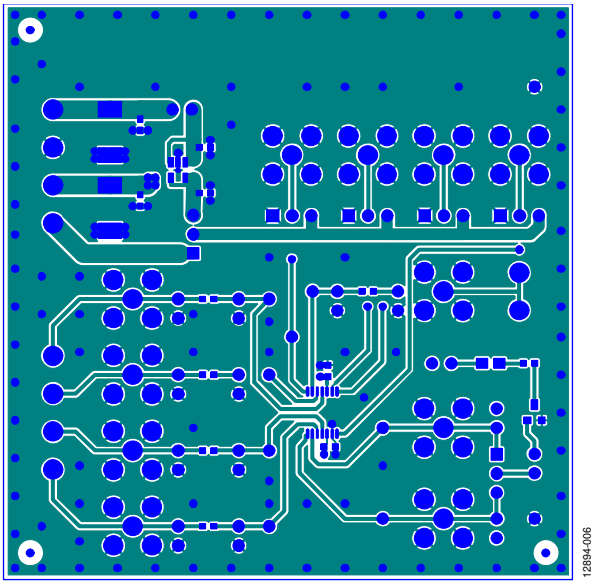

Figure 6. EVAL-ADG5404FEBZ Top Layer

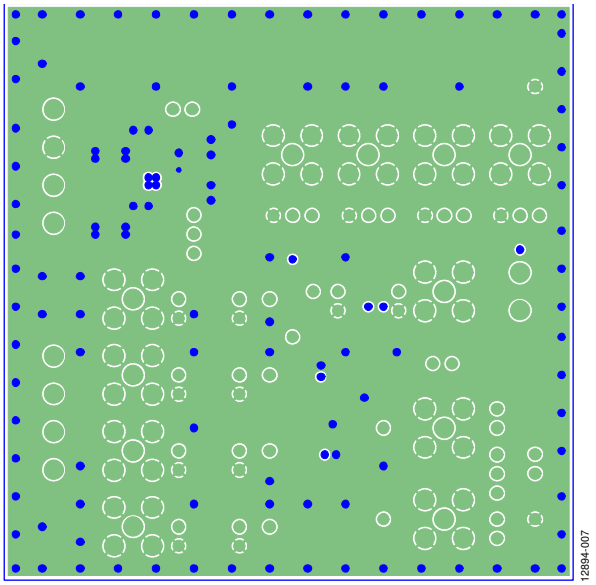

Figure 7. EVAL-ADG5404FEBZ Layer 2

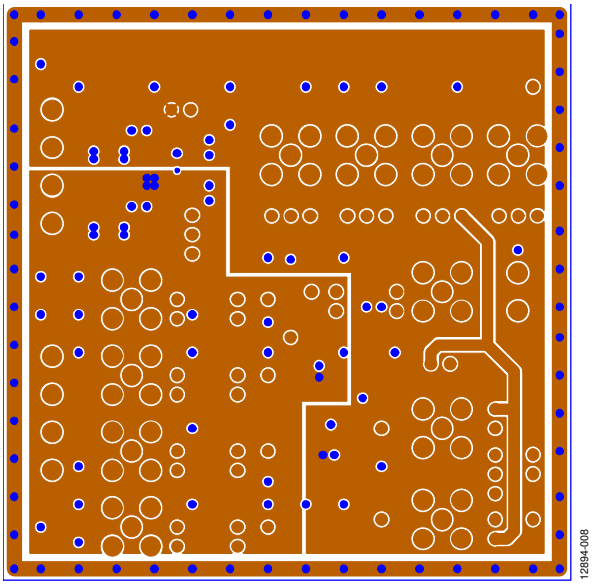

Figure 8. EVAL-ADG5404FEBZ Layer 3

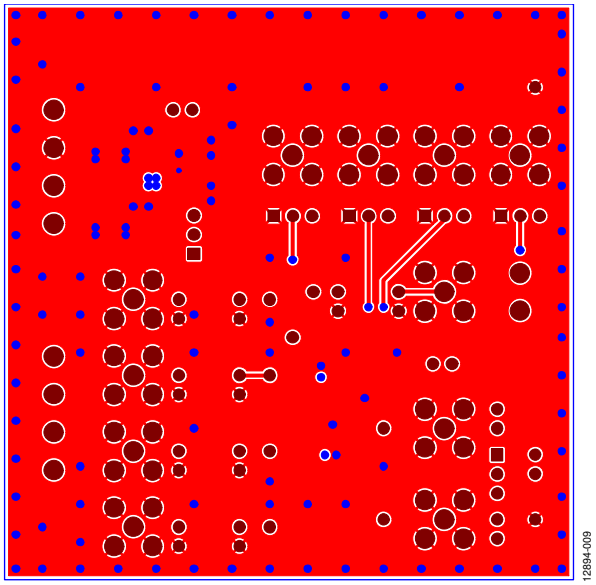

Figure 9. EVAL-ADG5404FEBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	MFR Part Number	Stock Code
A0/F0, A1/F1, D, DR, EN, FF, SF	50 Ω SMB socket	SMB1251B1-3GT30G-50	FEC 1111349
C1 to C5, R6, R10 to R15	Socket pin, PCB, PK100 (2 pins only)	66-3472	FEC 329563
C6, C9	10 µF, 50 V tantalum capacitors, D size	TAJD106K050RNJ	FEC 143-2387
C7, C10, C12, C13	0.1 µF, 50 V, X7R, multilayer ceramic capacitors, 0603 size	GRM188R71H104KA93D	FEC 882-0023
C8, C11	Capacitors, MLCC, X5R, 4.7 µF, 35 V, 0603 size	GRM188R6YA475KE15D	FEC 2426960
GND1, GND2	Black test points	20-2137	FEC 873-1128
J1, J3	4-pin terminal blocks (5 mm pitch)	CTB5000/4	FEC 151791
J2	2-pin terminal block (5 mm pitch)	CTB5000/2	FEC 151789
LED1	LED, SMD, green, 0805	KP-2012SGC	FEC 1318243
LK1	2-way solder bridge, solder in Position B	Not applicable	Do not insert
LK2 to LK5, LK9	3-pin SIL headers and shorting link	M20-9990345, M7567-05	FEC 1022248, 150410
LK6 to LK8	2-pin (0.1" pitch) headers and shorting shunt	M20-9990246	FEC 1022247, 150-411
Q1	Transistor, N-MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R5	Resistors, 0603 1%, 0 Ω	MC0063W06030R	FEC 9331662
R9	Resistor, 1 kΩ, 0.063 W, 1%, 0603 size	MC0063W060311K	FEC 9330380
S1 to S4	50 Ω SMB sockets	SMB1251B1-3GT30G-50	Do not insert
T1 to T8	Red test points	20-313137	FEC 873-1144
U1	Fault protection and detection, 10 Ω R_{ON}, 4-channel multiplexer	ADG5404FBRUZ	ADG5404FBRUZ
U2	40 V, 200 mA, low noise, CMOS LDO	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7