

Am25LS22

8-Bit Serial/Parallel Register with Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322

GENERAL DESCRIPTION

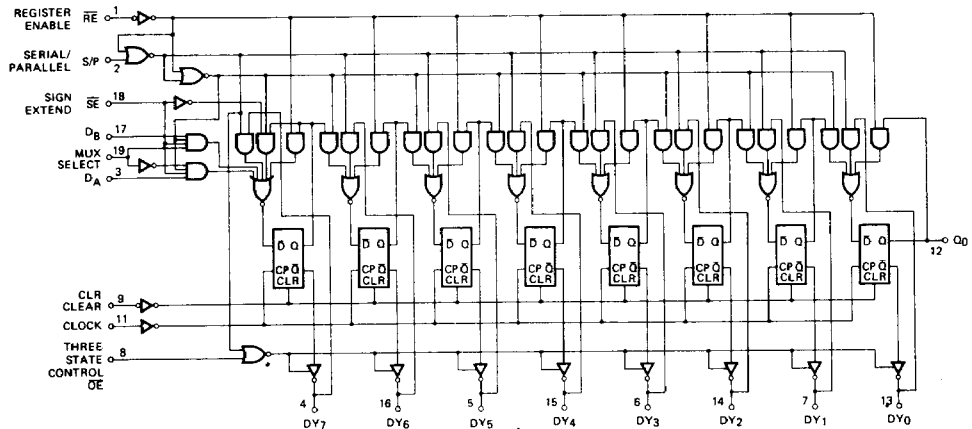
The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B . A serial output, Q_0 is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extended function required for this device.

When the Register Enable (\overline{RE}) input is HIGH, the register will retain its current contents. Synchronous parallel loading

is accomplished by applying a LOW to \overline{RE} and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of \overline{OE} and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend (\overline{SE}) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever \overline{SE} is LOW when the SHIFT mode is selected. When \overline{SE} is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

BLOCK DIAGRAM

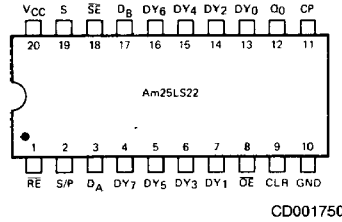


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RELATED PRODUCTS

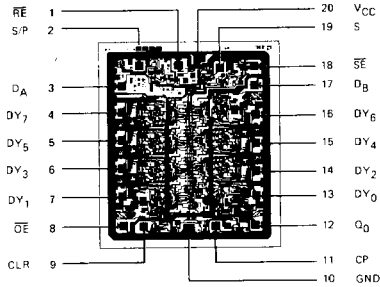
| Part No. | Description |
|----------|------------------------------|
| Am25LS23 | 8-Bit Shift/Storage Register |

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.096" x 0.112"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS22

D

C

B

- Screening Option
 - Blank - Standard processing
 - B - Burn-in
- Temperature (See Operating Range)
 - C - Commercial (0°C to +70°C)
 - M - Military (-55°C to +125°C)

- Package
 - D- 20-pin Cerdip
 - F- 20-pin flatpak
 - P- 20-pin plastic DIP
 - X- Dice

Device type
8-Bit Serial/Parallel Register
with Sign Extend

| Valid Combinations | |
|--------------------|------------------------------|
| Am25LS22 | PC DC, DM FM XC, XM |

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---------|---------------------------------|-----|---|
| | DY _i | I/O | The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, $i = 0$ through 7. |
| 12 | Q ₀ | O | The continuous output from the Q ₀ flip-flop of the register. This output is used for serial shifting. |
| 1 | RE | I | Register Enable. When RE is LOW, the register functions are enabled. When RE is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited. |
| 2 | S/P | I | Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the OE input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition. |
| 18 | SE | I | Sign Extend. When the SE input is LOW, the contents of the Q ₇ flip-flop will be repeated in the Q ₇ flip-flop as the register is shifted right. When SE is HIGH, the two-input multiplexer (D _A and D _B) is enabled to enter data during the serial shift right. The Q ₇ flip-flop (DY ₇) is normally considered the MSB of the register for arithmetic definitions. |
| 3, 17 | D _A , D _B | I | The serial inputs to the device. |
| 19 | S | I | Multiplexer Select. When S is LOW, the D _A serial input is selected. When S is HIGH, the D _B serial input is selected. |
| 9 | CLR | I | Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function. |
| 11 | CP | I | Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse. |
| 8 | OE | I | Output Control. When the OE input is HIGH, the eight DY _i outputs are in the high-impedance state. When OE is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW. |

FUNCTION TABLE

| Mode | Inputs | | | | | | | Outputs | | | | | | | | |
|---------------|--------|-----------------|-----------------|-------------|------------|-----|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| | Clear | Register Enable | Serial/Parallel | Sign Extend | Mux Select | OE* | Clock | DY ₇ | DY ₆ | DY ₅ | DY ₄ | DY ₃ | DY ₂ | DY ₁ | DY ₀ | Q ₀ |
| Clear | L | H | X | X | X | L | X | L | L | L | L | L | L | L | L | L |
| | L | L | H | X | X | L | X | L | L | L | L | L | L | L | L | L |
| | L | L | L | X | X | L | X | Z | Z | Z | Z | Z | Z | Z | Z | Z |
| | L | X | X | X | X | H | X | Z | Z | Z | Z | Z | Z | Z | Z | Z |
| Parallel Load | H | L | L | X | X | X | ↑ | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ | D ₀ |
| Shift Right | H | L | H | H | L | L | ↑ | D _A | Y _{7n} | Y _{6n} | Y _{5n} | Y _{4n} | Y _{3n} | Y _{2n} | Y _{1n} | Y _{1n} |
| | H | L | H | H | H | L | ↑ | D _B | Y _{7n} | Y _{6n} | Y _{5n} | Y _{4n} | Y _{3n} | Y _{2n} | Y _{1n} | Y _{1n} |
| Sign Extend | H | L | H | L | X | L | ↑ | Y _{7n} | Y _{7n} | Y _{6n} | Y _{5n} | Y _{4n} | Y _{3n} | Y _{2n} | Y _{1n} | Y _{1n} |
| Hold | H | H | X | X | X | L | ↑ | NC | NC | NC | NC | NC | NC | NC | NC | NC |

L = LOW

↑ = Clock LOW-to-HIGH Transition

X = Don't Care

H = HIGH

NC = No Change

Z = High-Impedance Output State

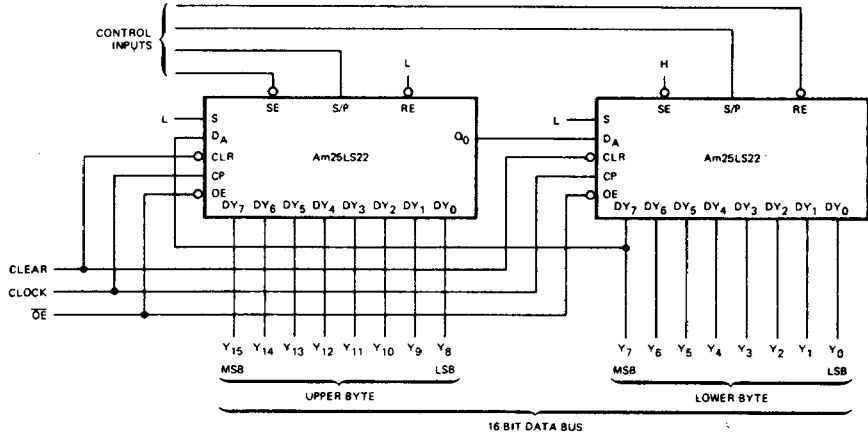
*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D₇, D₆...D₀ = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q₀) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady-state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n}...Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

APPLICATION



AF001190

| System Operation | Am25LS22 Upper Byte | | | | Am25LS22 Lower Byte | | | | Function |
|--|---------------------|-----|----|----|---------------------|-----|----|----|--|
| | SE | S/P | RE | OE | SE | S/P | RE | OE | Description |
| Load lower byte and extend lower byte sign to upper byte | H | H | L | X | X | L | L | X | Load from Bus |
| | L | H | L | H | X | X | H | H | 7 clock cycles to extend sign |
| Load upper byte and extend upper byte sign while shifting value to lower byte position | X | L | L | X | X | X | X | X | Load from Bus |
| | H | H | L | H | H | H | L | H | 8 clock cycles to extend upper byte sign and shift upper byte into lower byte position |
| Read 16-bit word to Bus | X | X | X | L | X | X | X | L | Unload |

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -85°C to +150°C
 (Ambient) Temperature Under Bias -55°C to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5V to +7.0V
 DC Voltage Applied to Outputs For
 HIGH Output State -0.5V to +V_{CC} max
 DC Input Voltage (OE, S/P, RE,
 CP, CLR) -0.5V to +7.0V
 DC Input Voltage (Others) -0.5V to +5.5V
 DC Output Current, Into Outputs 30mA
 DC Input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
 Temperature 0°C to +70°C
 Supply Voltage +4.75V to +5.25V
 Military (M) Devices
 Temperature -55°C to +125°C
 Supply Voltage +4.5V to +5.5V
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions (Note 2) | Min | Typ (Note 1) | Max | Units |
|-----------------|--|---|-------------------------|------------------|-------|-------|
| V _{OH} | Output HIGH Voltage | V _{CC} = MIN V _{IN} = V _{IH} or V _{IL} | MIL | 2.5 | | Volts |
| | | | COM'L | 2.7 | | |
| | | | MIL | 2.4 | | |
| | | | COM'L | 2.4 | | |
| V _{OL} | Output LOW Voltage | V _{CC} = MIN V _{IN} = V _{IH} or V _{IL} | I _{OL} = 4.0mA | | 0.4 | Volts |
| | | | I _{OL} = 8.0mA | | 0.45 | |
| V _{IH} | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | 2.0 | | | Volts |
| V _{IL} | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | 0.7 | Volts |
| V _I | Input Clamp Voltage | V _{CC} = MIN, I _{IN} = -18mA | | | -1.5 | Volts |
| I _{IL} | Input LOW Current | V _{CC} = MAX, V _{IN} = 0.4V | SE | | -1.08 | mA |
| | | | S | | -0.72 | |
| | | | Others | | -0.36 | |
| I _{IH} | Input HIGH Current | V _{CC} = MAX, V _{IN} = 2.7V (Except DY _i) | SE | | 60 | μA |
| | | | S | | 40 | |
| | | | Others | | 20 | |
| I _I | Input HIGH Current | V _{CC} = MAX, (Except DY _i) | V _{IN} = 7.0V | OE,S/P,RE,CP,CLR | 0.1 | mA |
| | | | V _{IN} = 5.5V | SE | 0.3 | |
| | | | S | 0.2 | | |
| | | | Others | 0.1 | | |
| I _{OZ} | Off state (High-Impedance) Output Current (DY _i) | V _{CC} = MAX | V _O = 2.4 | | 40 | mA |
| | | | V _O = 0.4V | | -100 | |
| I _{SC} | Output Short Circuit Current (Note 3) | V _{CC} = MAX | -15 | | -85 | mA |
| I _{CC} | Power Supply Current | V _{CC} = MAX | | 40 | 65 | mA |

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 2. For conditions shown as MIN, or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

| Parameters | Description | Test Conditions | Min | Typ | Max | Units |
|--------------------|---------------------------|--|------|------|-----|-------|
| t_{PLH} | Clock to DY_i | $R_L = 2.0\text{k}\Omega$, $C_L = 15\text{pF}$ | | 16.5 | 24 | ns |
| t_{PHL} | | | | 18 | 26 | |
| t_{PHL} | Clear to DY_i | | | 23 | 30 | ns |
| t_{PLH} | Clock to Q_0 | | | 16.5 | 24 | |
| t_{PHL} | | | | 18 | 26 | |
| t_{PHL} | Clear to Q_0 | | | 23 | 30 | ns |
| t_{ZH} | \overline{OE} to DY_i | $R_L = 2.0\text{k}\Omega$, $C_L = 5\text{pF}$ | | 13 | 21 | |
| t_{ZL} | | | | 18 | 26 | |
| t_{HZ} | | | | 13 | 21 | |
| t_{LZ} | SER/PAR to DY_i | $R_L = 2.0\text{k}\Omega$, $C_L = 15\text{pF}$ | | 18 | 26 | ns |
| t_{ZH} | | | | 23 | 32 | |
| t_{ZL} | | | | 18 | 26 | |
| t_{HZ} | | | | 23 | 32 | |
| t_s | RE to Clock | $R_L = 2.0\text{k}\Omega$, $C_L = 15\text{pF}$ | 20 | | | ns |
| t_s | SE to Clock | | 10 | | | |
| t_s | S to Clock | | 15 | | | |
| t_s | D_A and D_B to Clock | | 15 | | | |
| t_s | DY_i (Load) to Clock | | 15 | | | |
| t_s | Clear Recovery to Clock | | 8.0 | | | |
| t_s | S/P to Clock | | 15 | | | ns |
| t_h | Any Input | | 0 | | | |
| t_h | Clear Hold | | 0 | | | ns |
| t_{pw} | Clock | | HIGH | 8.0 | | |
| | | LOW | 8.0 | | | |
| t_{pw} | Clear | | 20 | | | ns |
| f_{max} (Note 1) | Maximum Clock Frequency | | 35 | 50 | | MHz |

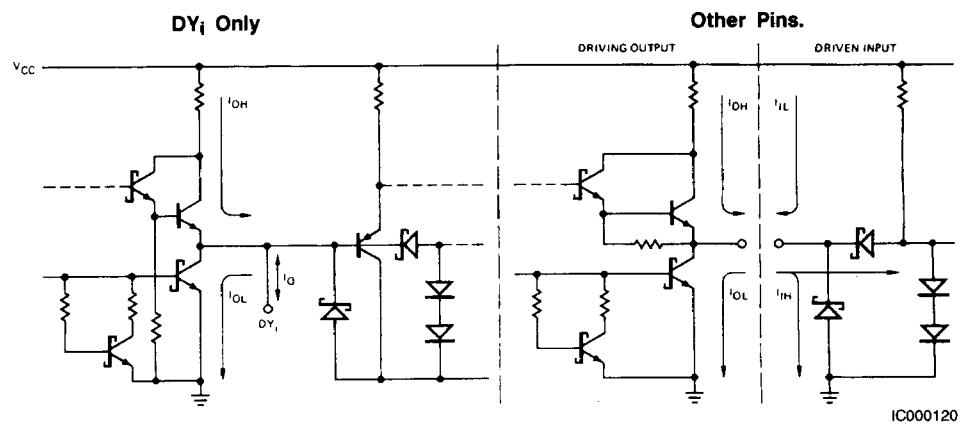
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

| Parameters | Description | Test Conditions | COMMERCIAL | | MILITARY | | Units | |
|---------------------------|--|---|--|-----|----------|-----|-------|-----|
| | | | Am25LS | | Am25LS | | | |
| | | | Min | Max | Min | Max | | |
| t _{PLH} | Clock to DY _i | C _L = 50pF R _L = 2.0kΩ | | 35 | | 41 | ns | |
| t _{PHL} | | | | 38 | | 44 | | |
| t _{PHL} | Clear to DY _i | | | 43 | | 50 | ns | |
| t _{PLH} | Clock to Q ₀ | | | 35 | | 41 | | |
| t _{PHL} | | | | 38 | | 44 | | |
| t _{PHL} | Clear to Q ₀ | | | 43 | | 50 | ns | |
| t _{ZH} | OE to DY _i | | C _L = 5.0pF R _L = 2.0kΩ | | 32 | | | 36 |
| t _{ZL} | | | | | 38 | | 44 | |
| t _{HZ} | | | | | 28 | | 31 | |
| t _{LZ} | | | | | 34 | | 39 | |
| t _{ZH} | SER/PAR to DY _i | C _L = 50pF R _L = 2.0kΩ | | 38 | | 44 | ns | |
| t _{ZL} | | | | 46 | | 53 | | |
| t _{HZ} | | | | 34 | | 39 | | |
| t _{LZ} | | | | 42 | | 48 | | |
| t _s | RE to Clock | C _L = 50pF R _L = 2.0kΩ | 30 | | 35 | | ns | |
| t _s | SE to Clock | | 17 | | 20 | | | |
| t _s | S to Clock | | 24 | | 27 | | | |
| t _s | D _A and D _B to Clock | | 24 | | 27 | | | |
| t _s | DY _i (Load) to Clock | | 24 | | 27 | | | |
| t _s | Clear Recovery to Clock | | 15 | | 17 | | | |
| t _s | S/P to Clock | | 24 | | 27 | | | |
| t _h | Any Input | | 4 | | 5 | | | |
| t _h | Clear Hold | | 4 | | 5 | | | |
| t _{pw} | Clock | | HIGH | 15 | | 17 | | |
| | | | LOW | 15 | | 17 | | |
| t _{pw} | Clear | | 30 | | 35 | | | |
| f _{max} (Note 1) | Maximum Clock Frequency | | 26 | | 23 | | | MHz |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.