



ELECTRICAL MODEL DOCUMENTATION

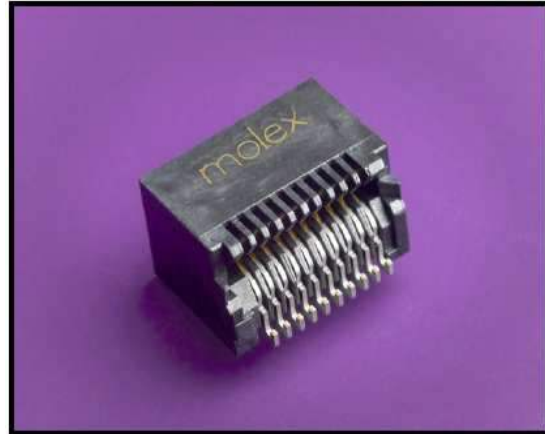
MODEL SUMMARY

An SFP+ application, defined by SFF-8431, could be an electrical-to-optical module or an electrical-to-electrical device such as a passive cable. SFP+ applications are intended to support Datacom applications. Examples of these applications are 10Gbps Ethernet, 8.5 Gbps Fibre Channel, 10.51 Gbps Fibre Channel, 10 Gbps Ethernet with FEC and Telecom (SONET OC-192 and G.709 "OTU-2").

The SFF-8083 specification defines the SFP/SFP+ host connector. It includes both the dimensional requirements and the high-speed signal integrity requirements.

The SFF-8432 specification defines the requirements for the improved SFP+ cage and modules in order to address EMC compliance.

Small Form-Factor Pluggable (SFP+)



Further information regarding this connector product line and other related Molex SFP+ products can be found at <http://www.molex.com/product/sfp-plus.html>

MODEL TYPE: S-parameter	MODEL FORMAT: Touchstone (*.snp)
MODEL FILENAME: SP-74441-001_revA.s8p	DATA FORMAT: Real/Imaginary
MODEL BASIS: Analytical 3-D field solution	MODEL SOURCE: Ansoft HFSS version 14.0.0
BANDWIDTH: DC –20.48 GHz	RESOLUTION: 10 MHz steps
REFERENCE: 50 ohms	NUMBER OF POINTS: 2049 (2048 + 1 DC)
NUMBER OF CHANNELS: 2 differential	NUMBER OF PORTS: 8 single-ended/model
CHANNEL TYPE: Coupled pairs + reference	VALIDATION:
MODEL APPLICATION: SFP/SFP+	DATA RATE: 11.10Gbps

APPLICABLE PART NUMBER(S): 74441

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REVISION: A	ECN INFORMATION: EC No: UCP2013-0034 DATE: 2012/07/05	TITLE: SFP+ Connector Electrical Model Documentation MOLEX CONFIDENTIAL	SHEET No. 1 of 8
DOCUMENT NUMBER: EE-74441-001	CREATED / REVISED BY: K. Wang	REVIEWED BY: P. Casher	APPROVED BY: P. Casher



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MODEL DESCRIPTION

This model contains 2 differential pairs (and their associated grounds) arranged in a G-S-S-G format circuit board interfaces, which results in an 8-port, single-ended S-parameter matrix. Two power pins are not part of the ports. The signal path represented by the model consists of a surface-mount host card, and an edge card connector inserted into one side of the connector.

The electrical model was simulated using Ansoft HFSS in the Frequency domain. The frequency range of this simulation is from 0 GHz to 20.48GHz. With Ansoft HFSS the DC values of the S-parameters are extrapolated from the lowest solved frequency (10 MHz).

CONDUCTOR TO PORT MAPPING TABLE

SIGNAL PATHS

Terminals (Host Board)	Ports (Host Board)	Ports (Edge Card)
12	1	2
13	3	4
18	5	6
19	7	8

Non-available Signal Paths

Terminals
1,2,3,4,5,6,7,8,9,10 11,14,15,16,17,20

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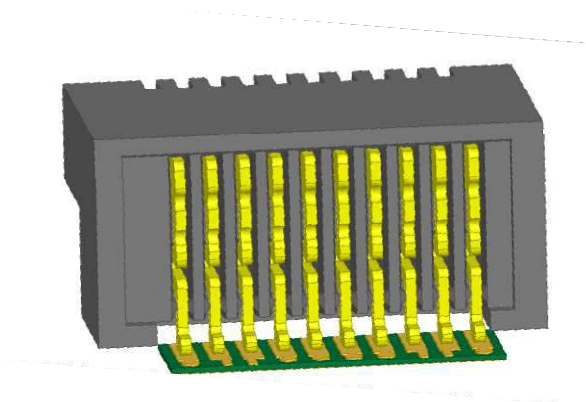
PART ILLUSTRATIONS

Connector

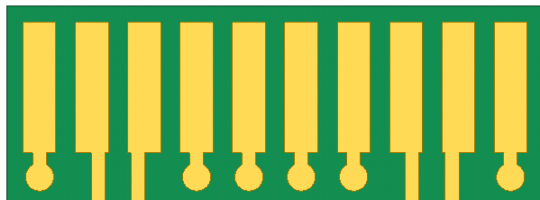
Side



Perspective



Host Card



Edge Card



Host Board Construction Details

Thickness: 0.148mm
 Layers: 2 (Microstrip & Ground)
 Board Material: Dk=3.8, Df=0.015
 Copper: 1.5 oz. (.05mm)

Edge Card Pads

Pitch: 0.8 mm
 Ground: 3.0 x 0.6 mm
 Signal: 2.2 x 0.6 mm

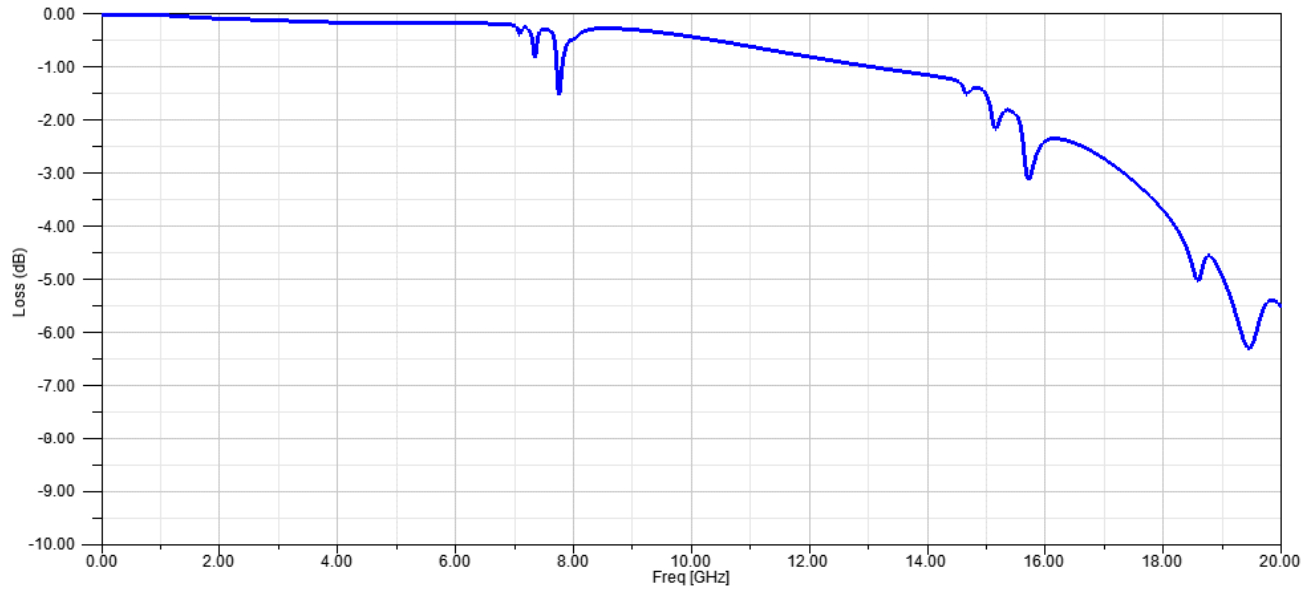
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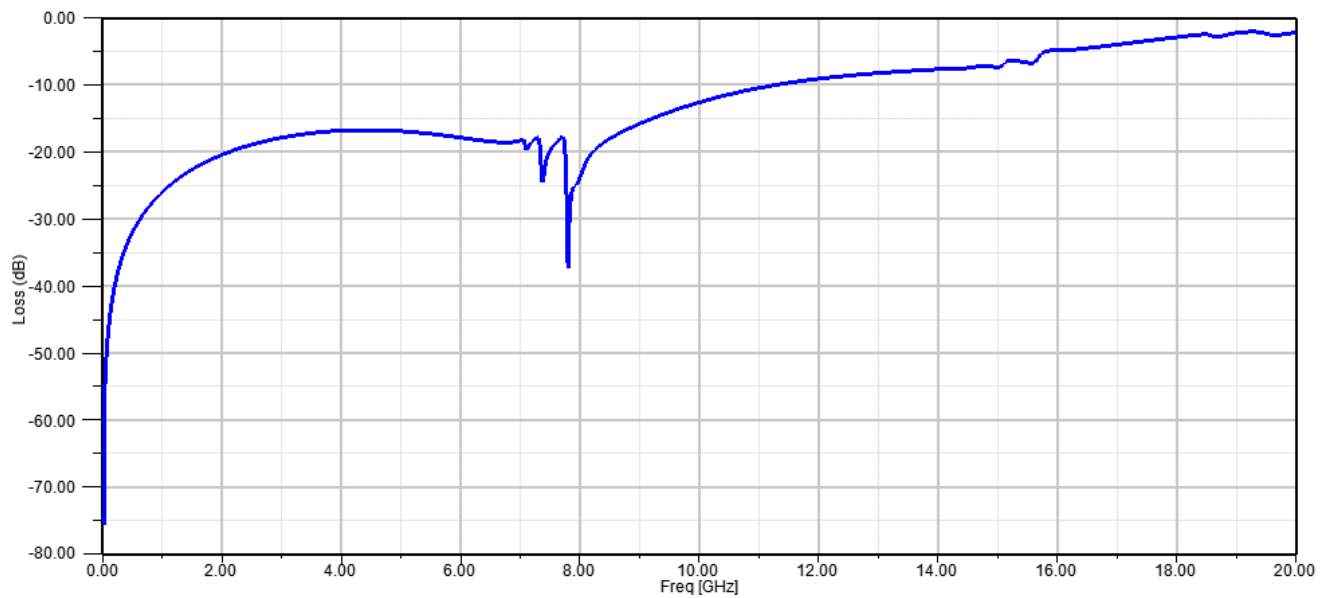
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REFERENCE RESULTS

Differential Insertion Loss



Differential Return Loss



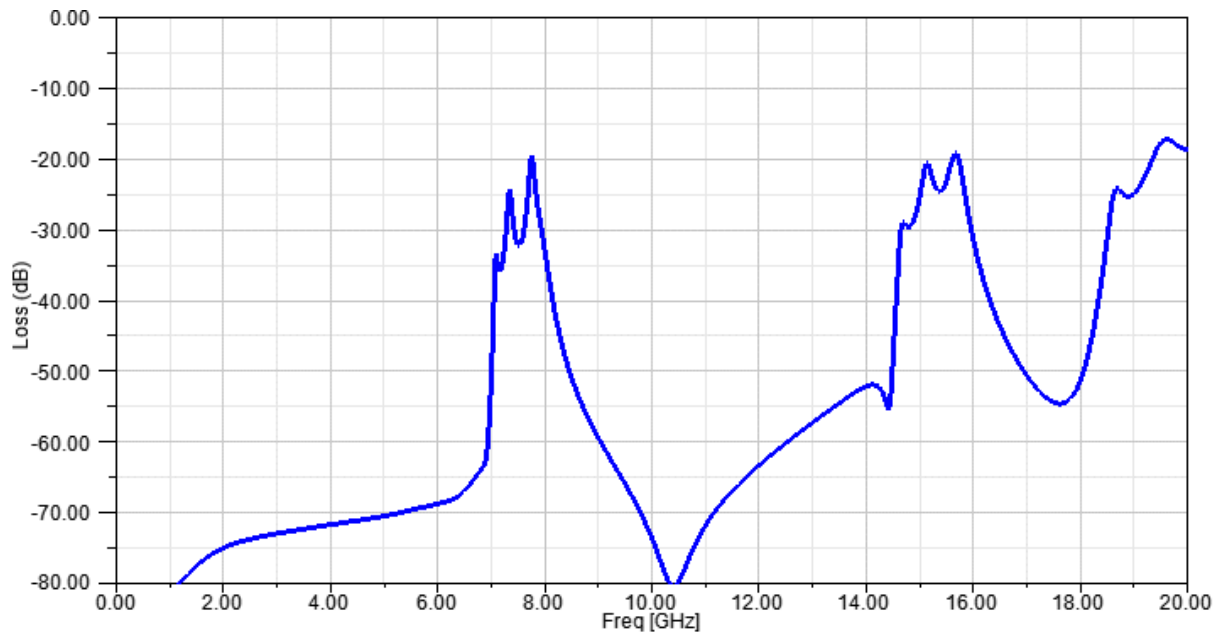
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REFERENCE RESULTS

Near-end Differential Crosstalk



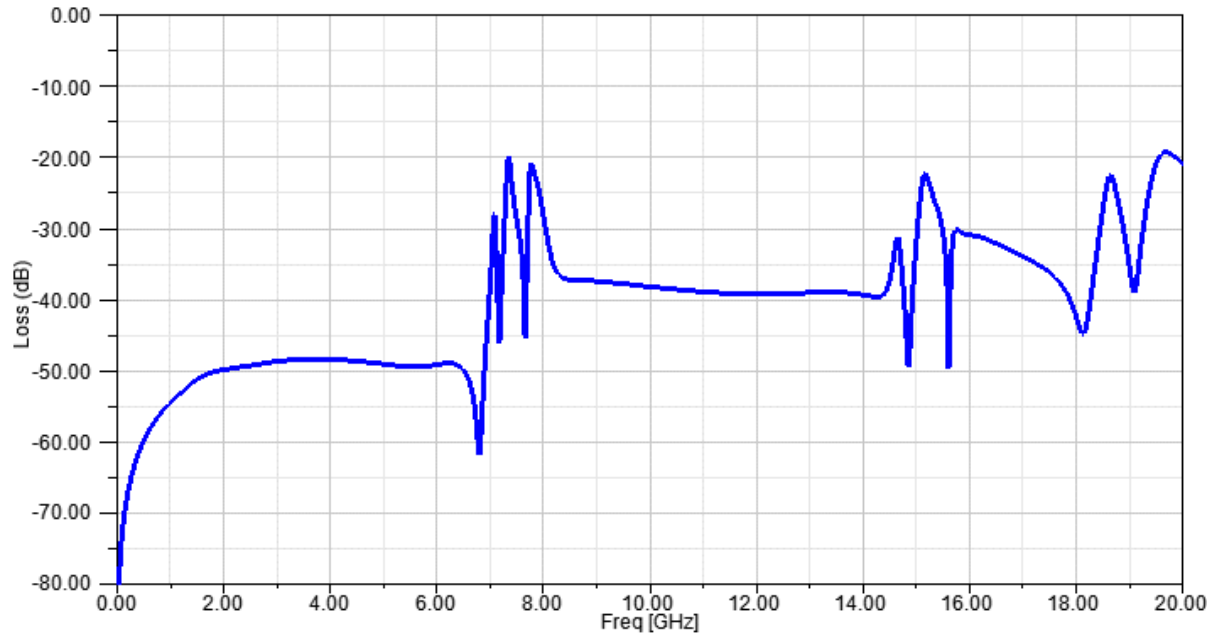
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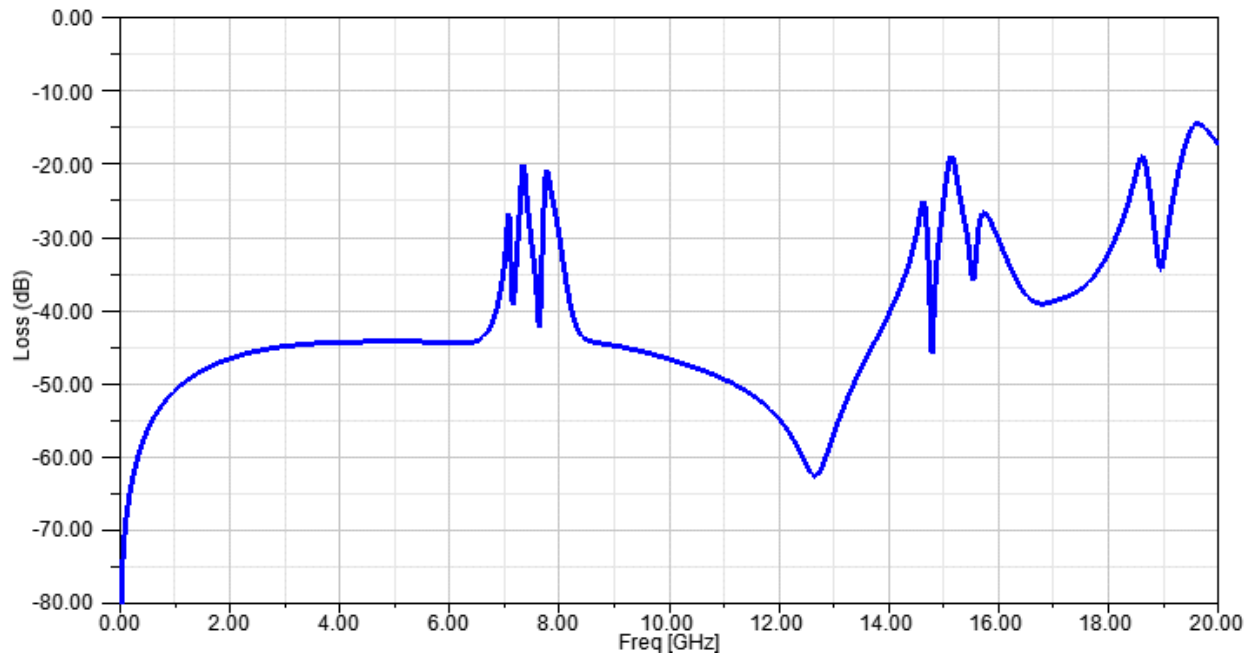
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REFERENCE RESULTS

Mode Conversion – Thru



Mode Conversion – Reflected



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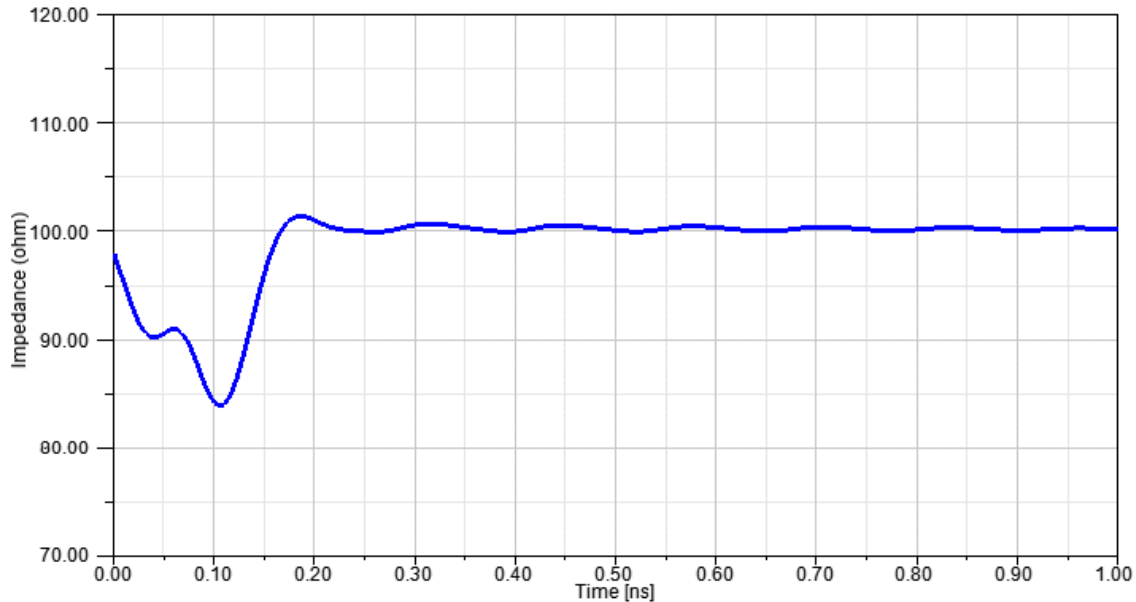


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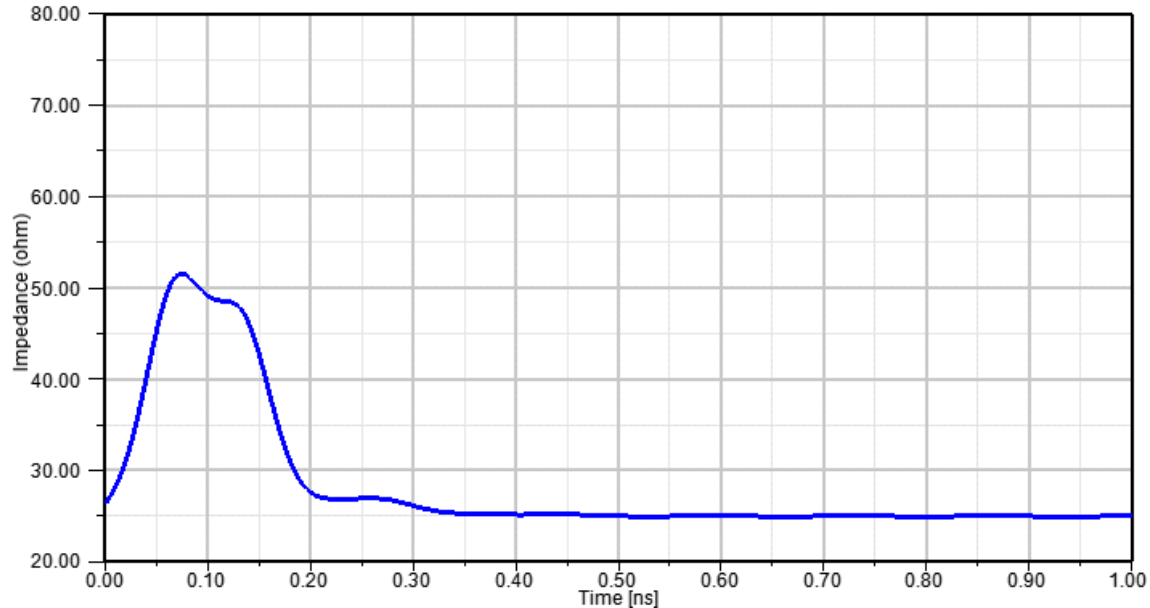
Differential TDR Response

- Rise-time of 35ps (10-90%), representative of 10.0 Gbps applications



Common Mode TDR Response

- Rise-time of 35ps (10-90%), representative of 10.0 Gbps applications

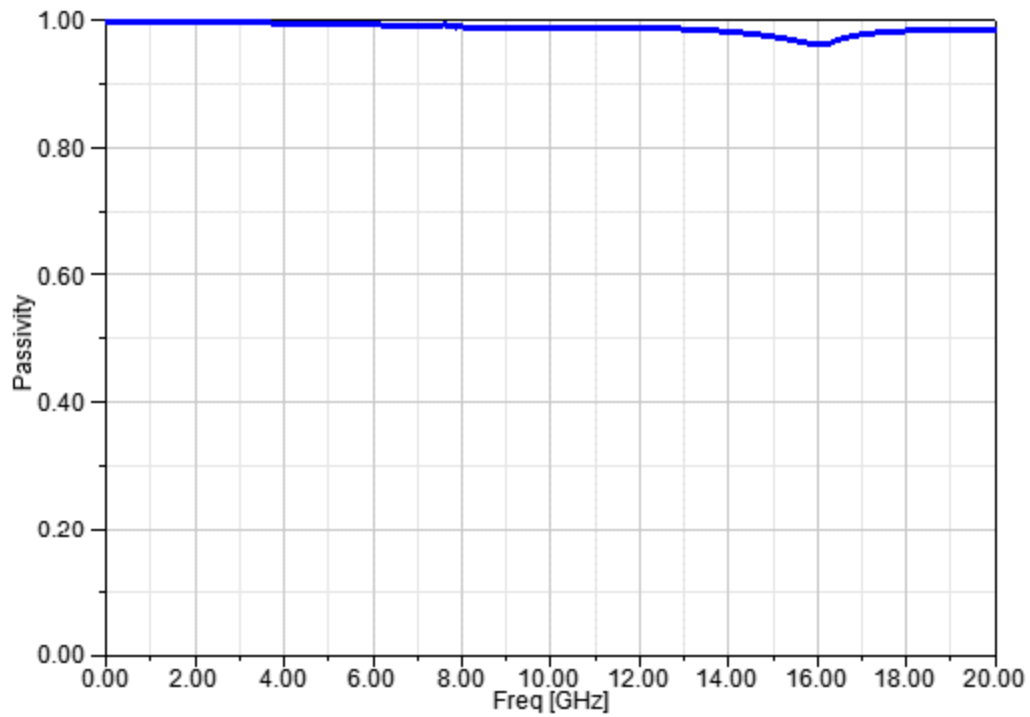


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Model Passivity



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