

LTC3311-0.85

3.3V to 0.85V at 12.5A, 2MHz Automotive Low EMI Buck Regulator in a 1.04cm² Solution

DESCRIPTION

Demonstration Circuit 3059A features the [LTC®3311-0.85](#), fixed 0.85V, 12.5A synchronous step-down Silent Switcher® operating as a 2MHz, 3V to 3.6V input, 0.85V/12.5A output buck regulator. The LTC3311-0.85 supports fixed 0.85V output voltage with operating frequencies from 500kHz up to 5MHz. The LTC3311-0.85 is a compact, ultralow emission, high efficiency, and high speed synchronous monolithic step-down switching regulator. The LTC3311-0.85 has Active Voltage Positioning (AVP) where the output voltage is dependent on load current. At light loads the output voltage is regulated above the nominal value. At full load the output voltage is regulated below the nominal value. The DC load regulation is adjusted to improve transient performance and reduce required output capacitance.

DC3059A is set up to run in forced continuous mode with a 2MHz switching frequency but can be configured to run at different switching frequencies, or in pulse skip mode. The LTC3311-0.85 oscillator can also synchronize to an external clock using MODE/SYNC turret, with the DC3059 default setup. Figure 5 shows the efficiency and power loss of the DC3059A with a 3.3V input in both operation modes.

The DC3059A is optimized for keeping its output within ±3% of the target voltage during a 4A to 8A, 4A/μs load step transient. A fast load step transient circuit is placed on the back of the demo board to measure the load step response of the converter.

The DC3059A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the VIN EMI terminal. The EMI performance of the board is shown in the EMI Test Results section. The red lines in the EMI performance graphs illustrate the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3311-0.85 data sheet gives a complete description of the part and its application information. The data sheet must be read in conjunction with this demo manual. The LTC3311-0.85 is assembled in a 3mm × 3mm LQFN package with exposed pads for low thermal resistance. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet section Low EMI PCB Layout.

[Design files for this circuit board are available.](#)

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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN} /V _{IN EMI}	DC3059A Input Voltage Range		3		3.6	V
V _{OUT}	DC3059A Output Voltage Range		0.827	0.85	0.871	V
I _{OUT}	DC3059A Output Current				12.5	A
f _{SW}	Switching Frequency		1.8	2	2.2	MHz
EFF	Efficiency	V _{IN} = 3.3V, I _{OUT} = 5A		90		%

BOARD PHOTO

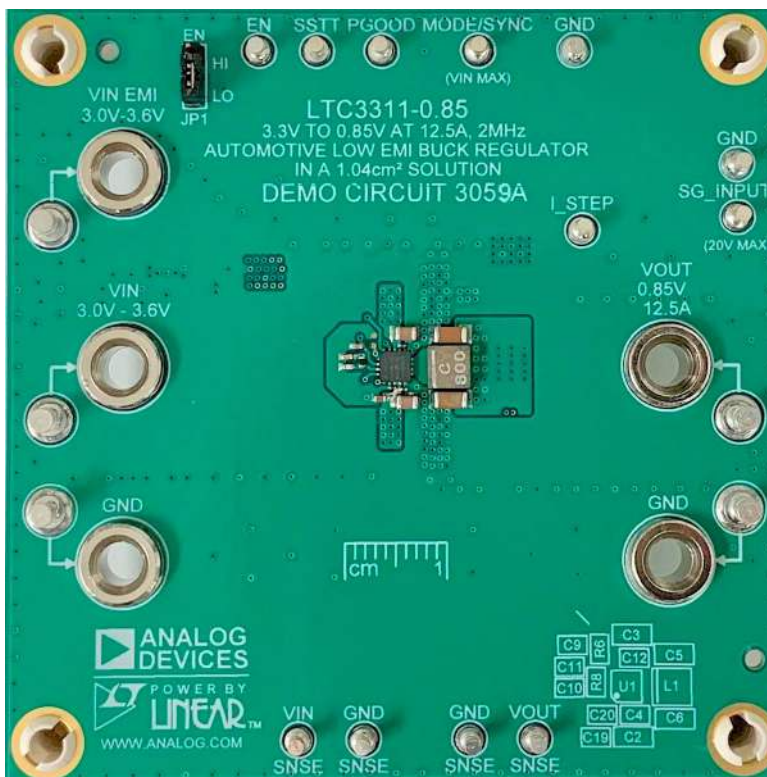


Figure 1. DC3059A Board Photo

QUICK START PROCEDURE

Refer to Figure 2 for the proper measurement equipment setup and follow the procedure below:

NOTE: For accurate V_{IN} , V_{OUT} and efficiency measurements, measure V_{IN} at the VIN SNSE and GND SNSN turrets, and measure V_{OUT} at the VOUT SNSE and GND SNSE turrets as illustrated as VM1 and VM2 in Figure 2. When measuring the input or output ripple, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Set the JP1 Jumper to the HI position.
2. With power off, connect the input power supply to VIN and GND. If the input EMI filter is desired, connect the input power supply to VIN EMI and GND.
3. Set power supply PS1 current limit to 10A. Set the electronic load LD1 to CC mode and 0A current. Slowly increase PS1 to 1.0V. If PS1 output current reads less than 20mA, increase PS1 to 3.3V. Verify that VM1

reads 3.3V and VM2 reads around 0.86V. Check VM1, VM2, VM3, PS1 output current and LD1 input current. Connect an oscilloscope voltage probe as shown in Figure 3. Set Channel to AC-coupled, voltage scale to 20mV and time base to 10µs. Check VOUT ripple voltage. Verify that PGOOD voltage is above 3V.

4. Increase the load by 1A intervals up to 12.5A and observe the voltage output regulation, ripple voltage, and the voltage on the SSTT turret. Calculate Die temperature using the formula below:

$$T_J(^{\circ}\text{C}) = \frac{V_{\text{SSTT}}}{4\text{mV}} - 273 \quad (1)$$

5. If pulse skipping mode is desired, set PS1 to 0V. Install a 0Ω resistor in the R5 location and remove R3. Repeat steps 1 through 4. In step 4, observe that the

QUICK START PROCEDURE

switching waveform is now in pulse skipping mode at light load.

- Optional: To change the frequency, remove R4 and R5, if installed. Install the desired RT resistor in the R6 location. Note that the MODE/SYNC pin should have high impedance to GND and VIN. Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output. Refer to the LTC3311-0.85 data sheet and [LTPowerCAD](#) for more information on choosing the required components.
- To test the transient response with a base load, add the desired resistor to produce a minimum load between VOUT and I_STEP turrets (RL shown on Figure 2). Note that the total load resistance will be RL plus R10

(20mΩ). Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.

- Measure the I_STEP voltage to observe the current, $V_{I_STEP} / 20m\Omega$. Adjust the amplitude of the pulse to provide the desired transient. Connect signal generator SG1 between SG_INPUT and GND turrets. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Figure 7 shows a load step from 4A to 8A. Refer to the following equations:

$$I_{OUT} = \frac{V_{I_STEP}}{20m\Omega} \quad (1)$$

$$V_{GS} = V_{SG_INPUT} - V_{I_STEP} \quad (2)$$

- When done, turn off SG1, PS1 and Load. Remove all the connections to the demo board.

TEST SETUP

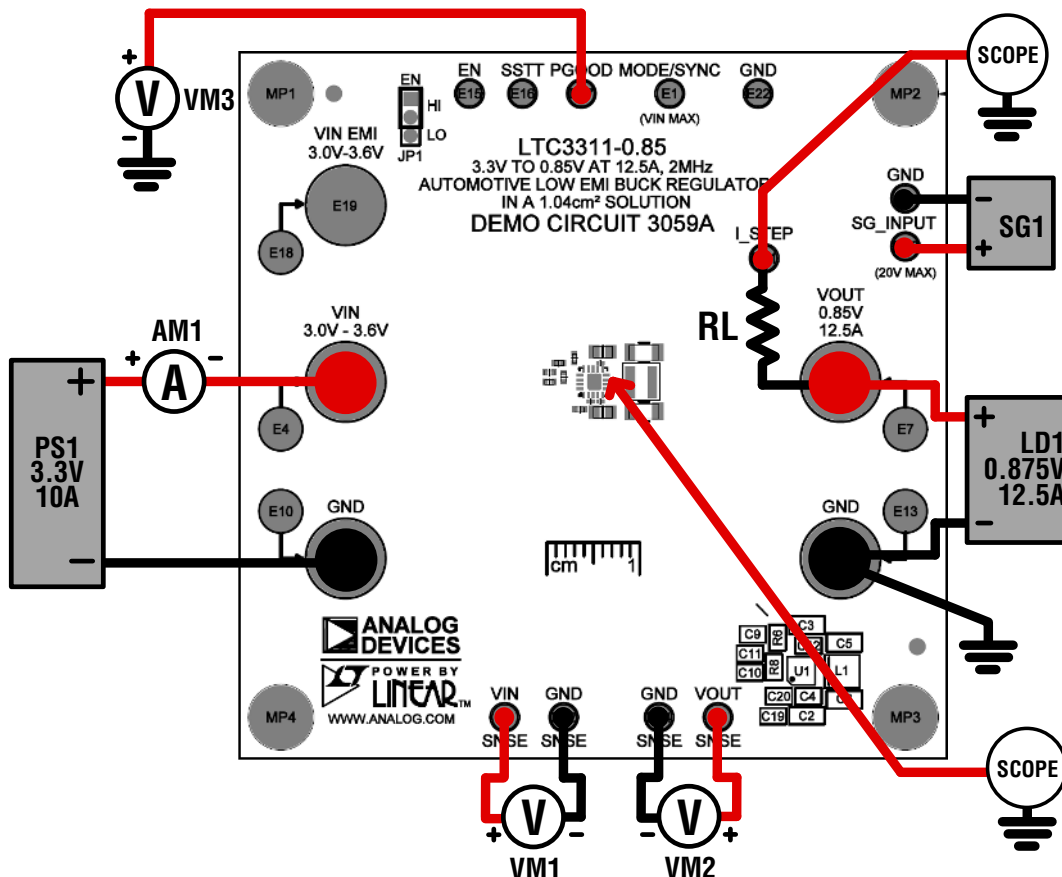


Figure 2. Test Setup for DC3059A Demo Board

TEST SETUP

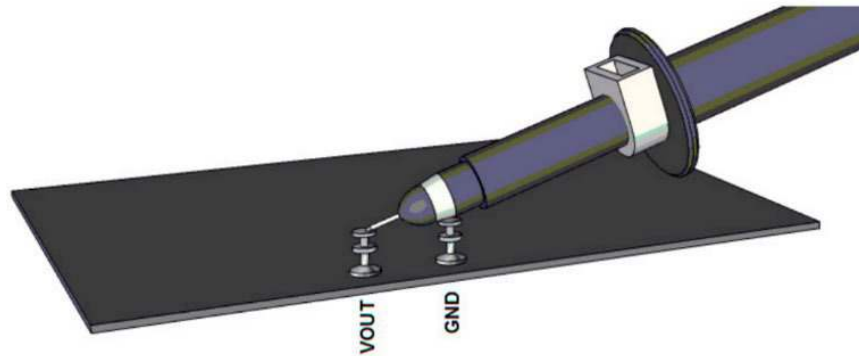


Figure 3. Technique for Measuring Output Ripple and Step Response

TYPICAL PERFORMANCE CHARACTERISTICS

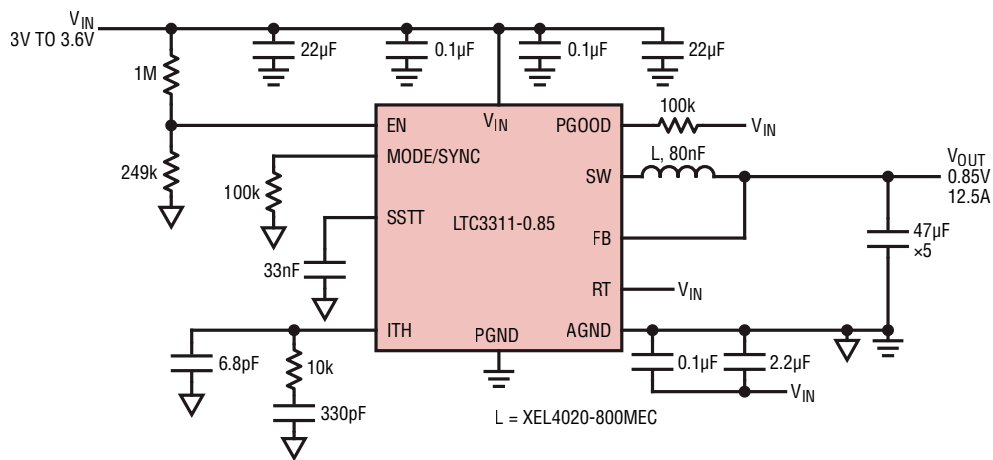


Figure 4. DC3059A, 0.85V/12.5A Step-Down Converter Typical Solution Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

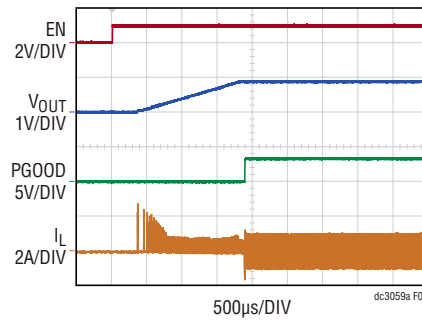


Figure 5. Start-Up Waveforms with Light Load

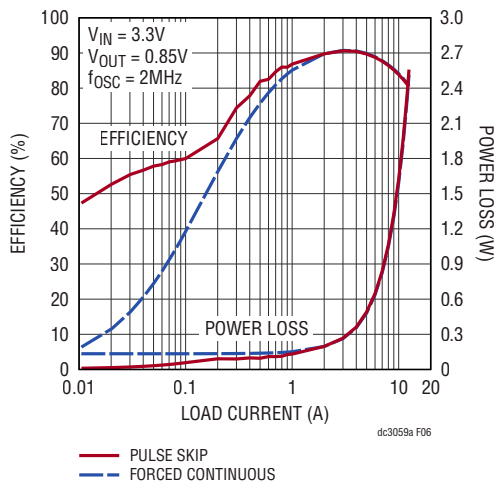


Figure 6. Efficiency vs Load Current

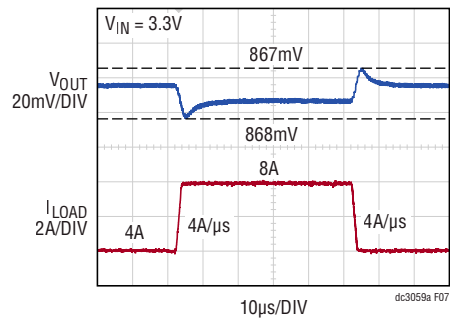
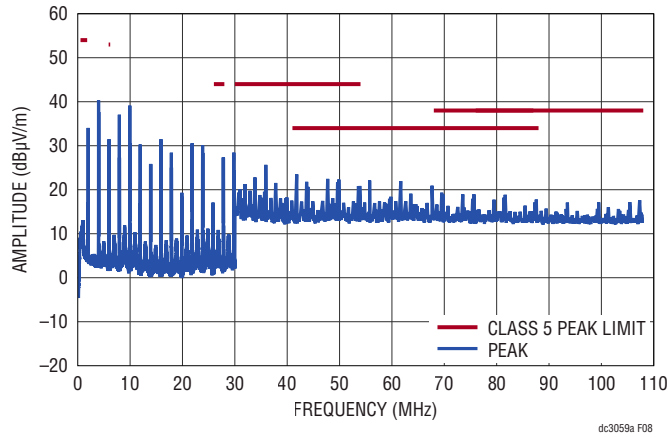


Figure 7. Load Step Response

EMI TEST RESULTS

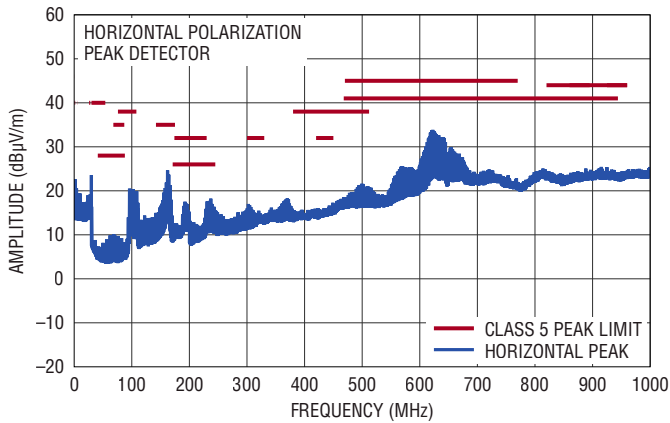
CISPR25 Conducted Emission Test with Class 5 Peak Limits (Voltage Method)



DC3059A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 0.85V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

Figure 8. DC3059A CISPR25 Conducted Emission with Class 5 Peak Limits (Voltage Method)

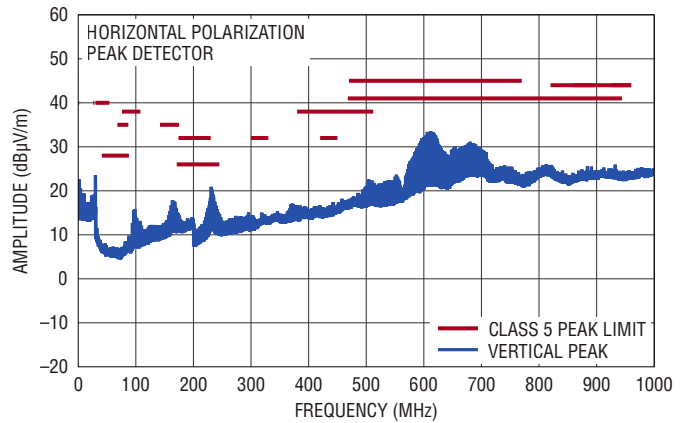
CISPR25 Radiated Emission with Class 5 Peak Limits (Horizontal)



DC3059A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 0.85V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

Figure 9. DC3059A CISPR25 Radiated Emission (Horizontal)

CISPR25 Radiated Emission with Class 5 Peak Limits (Vertical)



DC3059A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 0.85V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

Figure 10. DC3059A CISPR25 Radiated Emission (Vertical)

THEORY OF OPERATION

Introduction to the DC3059A

The DC3059A demonstration circuit features the LTC3311-0.85, a low voltage synchronous step-down Silent Switcher. The LTC3311-0.85 is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current, at which the top switch turns off, is controlled by the voltage on the ITH node. The error amplifier servos the ITH node by comparing the voltage on the internal VFB node with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference, leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous bottom power switch turns on until the next clock cycle begins. In pulse skip mode, the bottom switch also turns off when inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

If the EN pin is low, the LTC3311-0.85 is in shutdown state with low quiescent current. When the EN pin is above its threshold, the switching regulator will be enabled.

The MODE/SYNC pin synchronizes the switching frequency to an external clock. It can be a clock output for multi-phase operation. It also sets the regulator operation modes. The operation modes are either forced continuous or pulse skipping. See the LTC3311-0.85 data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of

V_{OUT} to V_{IN} and the inductance of the output inductor. The maximum allowable operating frequency may be calculated in the formula below.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot t_{ON(MIN)}} \quad (3)$$

Select an operating switching frequency below $f_{SW(MAX)}$. Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3311-0.85 operating load, 12.5A. Use the formulas below to calculate the inductor value to obtain a 30% (3A) inductor ripple for the operating frequency.

$$L \geq \frac{V_{OUT}}{3.75A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5 \quad (4)$$

$$L \geq \frac{0.25 \cdot V_{IN(MAX)}}{3.75A \cdot f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (5)$$

When determining the compensation components, C10, C11 and R8, controlling the loop stability and transient response are the two main considerations. The LTC3311-0.85 has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces required output capacitance to meet the desired transient voltage range. The mid-band gain of the loop increases with R8 and the bandwidth of the loop increases with decreasing C11. C10 along with R8 provides a high frequency pole to reduce the high frequency gain.

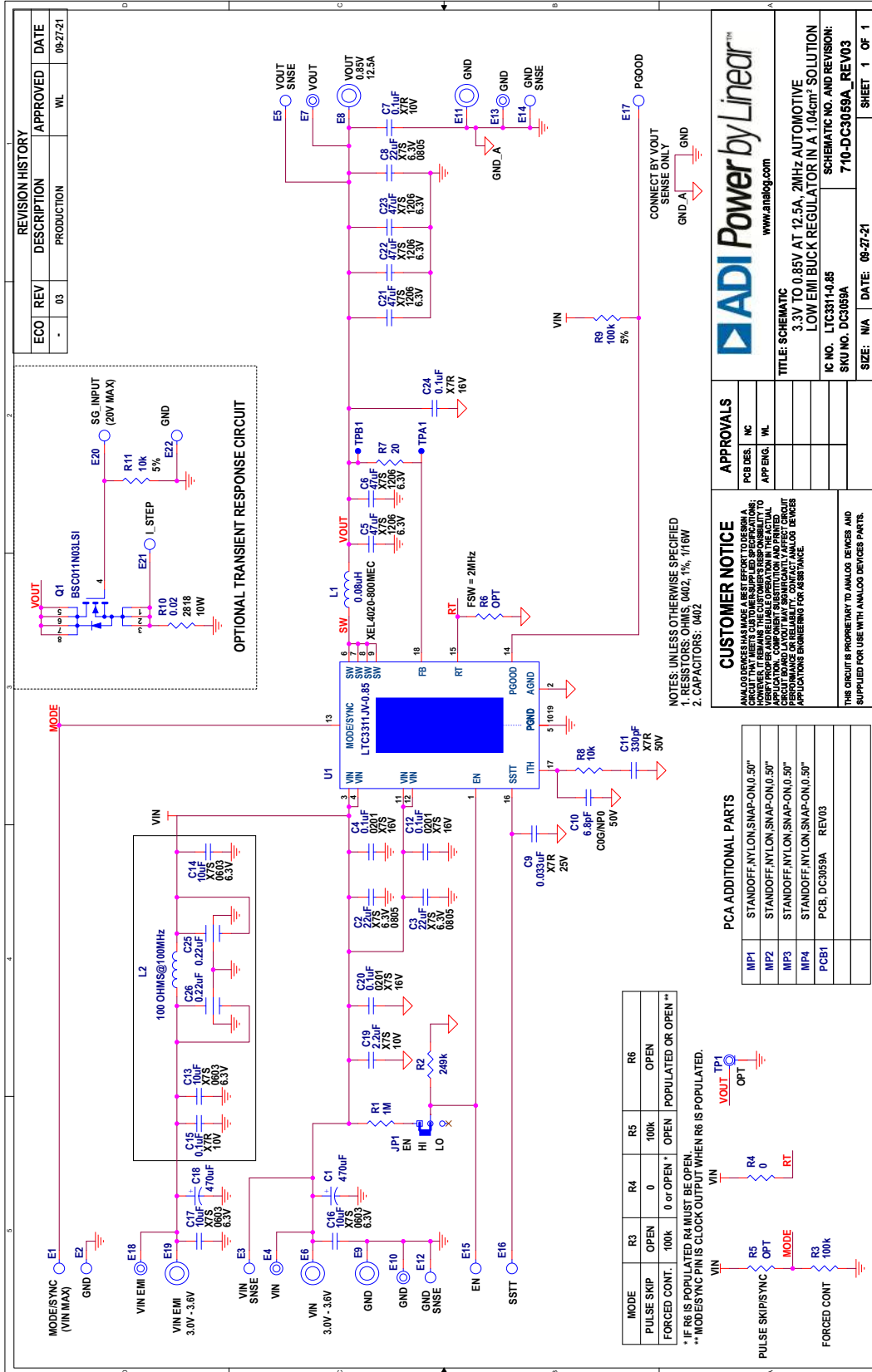
Loop stability is generally measured using the Bode Plot method of plotting loop gain in dB and phase shift in degrees. The 0dB crossover frequency should be less than 1/6 of the operating frequency to reduce the effects of added phase shift of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

DEMO MANUAL DC3059A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C2, C3	CAP., 22 μ F, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
2	3	C4, C12, C20	CAP., 0.1 μ F, X7S, 16V, 10%, 0201	MURATA, GRM033C71C104KE14D
3	5	C5, C6, C21-C23	CAP., 47 μ F, X7S, 6.3V, 20%, 1206	TDK, C3216X7S0J476M160AC
4	1	C9	CAP., 0.033 μ F, X7R, 25V, 10%, 0402	KEMET, C0402C333K3RACTU
5	1	C10	CAP., 6.8pF, C0G/NPO, 50V, \pm 0.5pF, 0402	AVX, 04025A6R8DAT2A
6	1	C11	CAP., 330pF, X7R, 50V, 10%, 0402, AEC-Q200	TDK, CGA2B2X7R1H331K050BA
7	1	C19	CAP CER 2.2 μ F 10V X7S 0402	MURATA ELECTRONICS, GRT155C71A225KE13D
8	1	C24	CAP., 0.1 μ F, X7R, 16V, 10%, 0402, AEC-Q200	MURATA, GCM155R71C104KA55D
9	1	L1	IND., 0.08 μ H, PWR, 20%, 21.4A, 1.8m Ω , 4mm x 4mm, AEC-Q200	COILCRAFT, XEL4020-800MEC
10	1	R8	RES., 10k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0FKED
11	1	U1	IC, LOW VOLTAGE SYNCH STEP-DOWN Reg, LQFN-18, PRELIM-PART NOT FOR PRODUCTION	ANALOG DEVICES, LTC3311JV-0.85#PBF
Additional Demo Board Circuit Components				
1	2	C1, C18	CAP., 470 μ F, TANT, POSCAP, 6.3V, 20%, 7343, 10m Ω , TCF	PANASONIC, 6TCF470MAH
2	2	C7, C15	CAP., 0.1 μ F, X7R, 10V, 10%, 0402, AEC-Q200	MURATA, GCM155R71A104KA55D
3	1	C8	CAP., 22 μ F, X7S, 6.3V, 20%, 0805	TDK, C2012X7S0J226M125AC
4	4	C13, C14, C16, C17	CAP., 10 μ F, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
5	2	C25, C26	CAP., 0.22 μ F, X7R, 6.3V, 20%, 0603	JOHANSON DIELECTRICS, 6R3X14W224MV4T
6	1	L2	IND., 100 Ω AT 100MHZ, FERRITE BEAD, 25%, 8A, 6m Ω , 1812	WURTH ELEKTRONIK, 74279226101
7	1	Q1	XSTR., MOSFET, N-CH, 30V, 37A, PG-TDSON-8	INFINEON, BSC011N03LSI
8	1	R1	RES., 1M, 1%, 1/16W, 0402, AEC-Q200	STACKPOLE ELECTRONICS, INC., RMCFO402FT1M00
9	1	R2	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F2493TRF
10	2	R3, R9	RES., 100k, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J104TRF
11	1	R4	RES., 0 Ω , 1/16W, 0402, AEC-Q200	NIC, NRC04Z0TRF
12	1	R7	RES., 20 Ω , 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F20R0TRF
13	1	R10	RES., 0.02 Ω , 1%, 10W, 2818, HP, METAL, SENSE, AEC-Q200	VISHAY, WSHP2818R0200FEA
14	1	R11	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J103TRF
15	0	TP1	CONN., U.FL, RECEPT, ST SMD, 0Hz TO 6GHz 50 Ω	HIROSE ELECTRIC, U.FL-R-SMT-1(10)
Hardware: For Demo Board Only				
1	12	E1-E3, E5, E12, E14-E17, E20-E22	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	5	E4, E7, E10, E13, E18	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E6, E8, E9, E11, E19	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	KEYSTONE, 8833
6	1	XJP1	CONN., SHUNT, FEMALE, 2-POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM





ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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