SL28647

Clock Generator for Intel®CK505

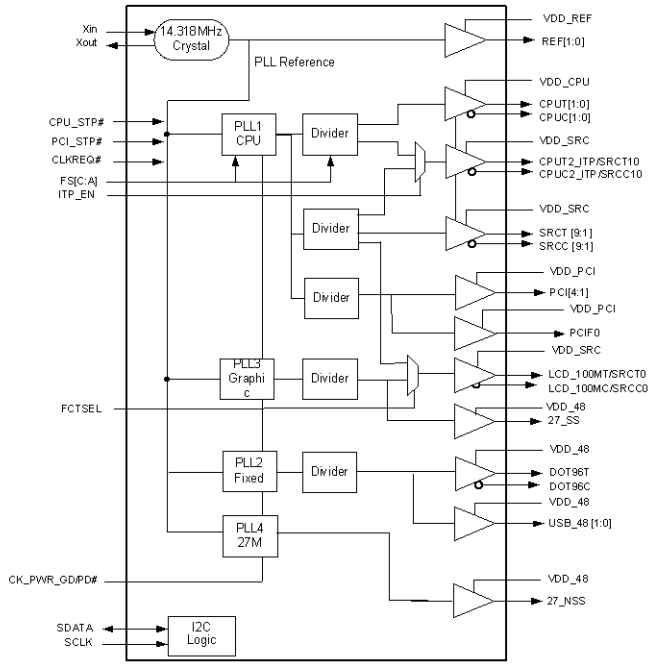
Features

- **Compliant to Intel® CK505**
- **Selectable CPU frequencies**
- **Low power differential CPU clock pairs**
- **100-MHz low power differential SRC clocks**
- **96-MHz low power differential dot clock**
- **27-MHz Spread and Non-spread video clock**
- **48-MHz USB clock**
- **SRC clocks independently stoppable through CLKREQ#[1:9]**
- **100-MHz low power spreadable differential video clock**
- **33-MHz PCI clocks**
- **Buffered Reference Clock 14.318 MHz**
- **Low-voltage frequency select inputs**
- **I^2C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V power supply**
- **72-pin QFN package**

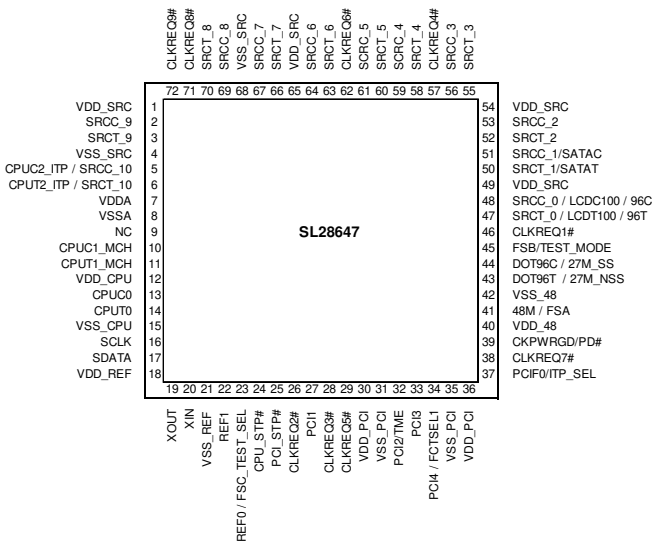
Table 1. Output Confguration Table

CPU	SRC	PCI	REF	DOT96	USB_48M	LCD	27M
x2/x3	x9/11	x5	x 2	x 1	x 1	x1	x2

Block Diagram



Pin Configuration



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Pin Description

Pin No.	Name	Type	Description
1, 49, 54, 65	VDD_SRC	PWR	3.3V power supply for outputs.
2, 3, 52, 53, 55, 56, 58, 59, 60, 61, 63, 64, 66, 67, 69, 70	SRCT/C[2:9]	O, DIF	100-MHz Differential serial reference clocks.
4, 68	VSS_SRC	GND	Ground for outputs.
5, 6	CPUT2_ITP/SRCT10, CPUC2_ITP/SRCC10	O, DIF	Selectable differential CPU or SRC clock output. ITP_SEL = 0 @ pin 39 assertion = SRC10 ITP_SEL = 1 @ pin 39 assertion = CPU2
7	VDDA	PWR	3.3V power supply for PLL.
8	VSSA	GND	Ground for PLL.
9	NC	NC	No Connect Pin
10, 11	CPUC1_MCH, CPUT1_MCH	O, DIF	Differential CPU clock output to MCH
12	VDD_CPU	PWR	3.3V power supply for outputs.
13, 14	CPU[T/C]0	O, DIF	Differential CPU clock output
15	VSS_CPU	GND	Ground for outputs.
16	SCLK	I	SMBus-compatible SCLOCK.
17	SDATA	I/O, OD	SMBus-compatible SDATA.
18	VDD_REF	PWR	3.3V power supply for outputs.
19	XOUT	O, SE	14.318-MHz crystal output.
20	XIN	I	14.318-MHz crystal input.
21	VSS_REF	GND	Ground for outputs.
22	REF1	O	Fixed 14.318-MHz clock output.
23	REF0/FSC_TESTSEL	I/O	Fixed 14.318 clock output/3.3V-tolerant input for CPU frequency selection/Selects test mode if pulled to V_{IMFS_C} when pin 39 is asserted LOW. *Refer to DC Electrical Specifications table for* V_{ILFS_C},V_{IMFS_C},V_{IHFS_C} *specifications.*
24	CPU_STP#	I	3.3V LVTTL input for CPU_STP# active LOW During direct clock off to M1 mode transition, a serial load of BSEL data is driven on this pin and sampled on the rising edge of PCI_STP#. See Figure 14.for more information.
25	PCI_STP#	I	3.3V LVTTL input for PCI_STP# active LOW During direct clock off to M1 mode transition, a serial load of BSEL data is driven on CPU_STP# and sampled on the rising edge of this pin. See Figure 14. for more information.
26, 28, 29, 38, 46, 57, 62, 71, 72	CLKREQ[1:9]#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
27	PCI1	I/O, SE	33MHz clock output
30, 36	VDD_PCI	PWR	3.3V power supply for outputs.
31, 35	VSS_PCI	GND	Ground for outputs.

Pin Description (continued)

Pin No.	Name	Type	Description
32	PCI2/TME	I/O, PU, SE	33-MHz clock output/Trusted Mode Enable Strap Strap at pin 39 assertion to determine if the part is in trusted mode or not. Internal pull-up resistor of 100K to 3.3V, use 10K resistor to pull it low externally if needed 0 = Normal mode 1= Trusted mode (default)
33	PCI3	O, SE	33MHz clock output / 3.3V-tolerant input select pin to select termination scheme for differential clocks.
34	PCI4/FCTSEL1	I/O, PD	33-MHz clock output/3.3V LVTTL input for selecting pins 47,48 (SRC[T/C]0, 100M[T/C]) and pins 43,44 (DOT96[T/C] and 27M Spread and Non-spread) (sampled on pin 39 assertion). Internal pull-down resistor of 100K to GND
37	ITP_SEL/PCIF0	I/O, PD, SE	3.3V LVTTL input to enable SRC10 or CPU2_ITP/33-MHz clock output. (sampled on pin 39 assertion). Internal pull-down resistor of 100K to GND 1 = CPU2_ITP, 0 = SRC10
39	CKPWRGD/PD#	I	3.3V LVTTL input. This pin is a level sensitive strobe. When asserted, it latches data on the FSA, FSB, FSC, FCTSEL1 and ITP_SEL pins. After assertion, it becomes a real time input for controlling power down.
40	VDD_48	PWR	3.3V power supply for outputs.
41	48M/FSA	I/O	Fixed 48-MHz clock output/3.3V-tolerant input for CPU frequency selection *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
42	VSS_48	GND	Ground for outputs.
43, 44	DOT96T/ 27M_NSS DOT96C/ 27M_SS	O, DIF	Fixed 96-MHz clock output or 27 Mhz Spread and Non-spread output Selected via FCTSEL1 at pin 39 assertion.
45	FSB/TEST_MODE	I	3.3V-tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
47, 48	SRC[T/C]0/ LCD100M[T/C]	O,DIF	100-MHz differential serial reference clock output/Differential 96/100-MHz SS clock for flat-panel display Selected via FCTSEL1 at pin 39 assertion.
50, 51	SRCT_1/SATAT, SRCC_1/SATAC	O, DIF	100-MHz Differential serial reference clocks.

FCTSEL1	Pin 43	Pin 44	Pin 47	Pin 48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_NSS	27M_SS	SRCT0	SRCC0

Frequency Select Pins (FSA, FSB, and FSC)

Host clock frequency selection is achieved by applying the appropriate logic levels to FSA, FSB, FSC inputs prior to CK_PWRGD assertion (as seen by the clock synthesizer). Upon CK_PWRGD being sampled HIGH by the clock chip (indicating processor CK_PWRGD voltage is stable), the clock chip samples the FSA, FSB, and FSC input values. For all logic levels of FSA, FSB, and FSC, CK_PWRGD employs a one-shot functionality in that once a valid HIGH on CK_PWRGD has been sampled, all further CK_PWRGD, FSA, FSB, and FSC transitions will be ignored, except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h)

Table 2. Frequency Select Table FSA, FSB, and FSC

FSC	FSB	FSA	CPU	SRC	PCIF/PCI	27MHz	REF	DOT96	USB
0	0	0	266 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
1	0	1	100 MHz						
0	0	1	133 MHz						
0	1	1	166 MHz						
0	1	0	200 MHz						
1	0	0	333 MHz						
1	1	0	400 MHz						
1	1	1	Reserved						

Table 3. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0 Control Register 0

Bit	@Pup	Name	Description
7	0	RESEREVD	RESERVED
6	0	RESEREVD	RESERVED
5	0	RESEREVD	RESERVED
4	0	iAMT_EN	Set via SMBus or by combination of PD, CPU_STP and PCI_STP 0 = Legacy mode, 1 = iAMT enable
3	0	RESEREVD	RESERVED
2	0	RESEREVD	RESERVED
1	0	RESEREVD	RESERVED
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

Byte 1 Control Register 1

Bit	@Pup	Name	Description
7	1	SRC7_OE	SRC7 Output Enable 0 = Disabled, 1 = Enabled
6	1	SRC6_OE	SRC[6 Output Enable 0 = Disabled, 1 = Enabled
5	1	SRC5_OE	SRC5 Output Enable 0 = Disabled, 1 = Enabled
4	1	SRC4_OE	SRC4 Output Enable 0 = Disabled, 1 = Enabled
3	1	SRC3_OE	SRC3 Output Enable 0 = Disabled, 1 = Enabled
2	1	SRC2_OE	SRC2 Output Enable 0 = Disabled, 1 = Enabled
1	1	SRC1_OE	SRC1 Output Enable 0 = Disabled, 1 = Enabled
0	1	SRC0 /LCD_96/100M_OE	SRC0/LCD_96/100M Output Enable 0 = Disabled, 1 = Enabled

Byte 2 Control Register 2

Bit	@Pup	Name	Description
7	1	PCIF0_OE	PCIF0 Output Enable 0 = Disabled, 1 = Enabled
6	1	27M_non_SS/DOT_96_OE	27M Non-spread and DOT_96 MHz Output Enable 0 = Disable, 1 = Enabled
5	1	48M_OE	48-MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0_OE	REF0 Output Enable 0 = Disabled, 1 = Enabled
3	1	REF1_OE	REF1 Output Enable 0 = Disabled, 1 = Enabled
2	1	CPU1_OE	CPU[T/C]1 Output Enable 0 = Disabled, 1 = Enabled
1	1	CPU0_OE	CPU[T/C]0 Output Enable 0 = Disabled, 1 = Enabled
0	1	CPU, SRC, PCI, PCIF Spread Enable	PLL1 (CPU PLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 3 Control Register 3

Bit	@Pup	Name	Description
7	1	PCI4_OE	PCI4 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI3_OE	PCI3 Output Enable 0 = Disabled, 1 = Enabled
5	1	PCI2_OE	PCI2 Output Enable 0 = Disabled, 1 = Enabled
4	1	PCI1_OE	PCI1 Output Enable 0 = Disabled, 1 = Enabled
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	CPU2/SRC10_OE	CPU2/SRC10 Output Enable 0 = Disabled, 1 = Enabled
0	1	RESERVED	RESERVED

Byte 4 Control Register 4

Bit	@Pup	Name	Description
7	0	SRC7_STP_CTRL	Allow control of SRC7 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
6	0	SRC6_STP_CTRL	Allow control of SRC6 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
5	0	SRC5_STP_CTRL	Allow control of SRC5 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
4	0	SRC4_STP_CTRL	Allow control of SRC4 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC3_STP_CTRL	Allow control of SRC3 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC2_STP_CTRL	Allow control of SRC2 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC1_STP_CTRL	Allow control of SRC1 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#

Byte 4 Control Register 4 (continued)

Bit	@Pup	Name	Description
0	0	SRC0_STP_CTRL	Allow control of SRC0 with assertion of PCI_STP# or SW PCI_STP 0 = Free running, 1 = Stopped with PCI_STP#

Byte 5 Control Register 5

Bit	@Pup	Name	Description
7	0	LCD_96/100M_PD_Drive_Mode	LCD_96/100 PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
6	0	DOT96_PD_Drive_Mode	DOT96 PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	PCIF0_STP_CTRL	Allow control of PCIF0 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	1	CPU2_STP_CTRL	Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
1	1	CPU1_STP_CTRL	Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU0_STP_CTRL	Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 6 Control Register 6

Bit	@Pup	Name	Description
7	0	SRC_STP_Drive_Mode	SRC Stop Drive Mode 0 = Driven when PCI_STP# asserted 1 = Tri-state when PCI_STP# asserted
6	0	CPU2_STP_Drive_Mode	CPU2 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted
5	0	CPU1_STP_Drive_Mode	CPU1 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted
4	0	CPU0_STP_Drive_Mode	CPU0 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted
3	0	SRC_[9:1]_PD_Drive_Mode	SRC[9:1] PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
2	0	CPU2_PD_Drive_Mode	CPU2 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
1	0	CPU1_PD_Drive_Mode	CPU1 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
0	0	CPU0_PD_Drive_Mode	CPU0 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted

Byte 7 Control Register 7

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 0 = Tri-state, 1 = REF/N Clock

Byte 7 Control Register 7 (continued)

Bit	@Pup	Name	Description
6	0	TEST_MODE	Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Tri-state mode,
5	1	REF1 Bit0	REF1 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
4	1	REF0 Bit0	REF0 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
3	1	PCI, PCIF and SRC clock outputs except those set to free running	SW PCI_STP Function 0 = SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	HW	FSC	FSC Reflects the value of the FSC pin sampled on power up 0 = FSC was low during CK_PWRGD assertion
1	HW	FSB	FSB Reflects the value of the FSB pin sampled on power up 0 = FSB was low during CK_PWRGD assertion
0	HW	FSA	FSA Reflects the value of the FSA pin sampled on power up 0 = FSA was low during CK_PWRGD assertion

Byte 8 Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	1	Revision Code Bit 1	Revision Code Bit 1
4	0	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Byte 9 Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	48M Bit0	48M Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
1	1	RESERVED	RESERVED
0	1	PCIF0 Bit0	PCIF0 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High

Byte 10 Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED

Byte 10 Control Register 10 (continued)

Bit	@Pup	Name	Description
5	0	S1	27M_SS/LCD 96_100M SS Spread Spectrum Selection table: S[1:0] SS% '00' = –0.5%(Default value) '01' = –1.0% '10' = –1.5% '11' = –2.0%
4	0	S0	
3	1	RESERVED	RESERVED
2	1	27M_SS_OE	27M_SS Output Enable 0 =Disabled, 1 = Enabled
1	1	27M_SS/LCD_96M/100M Spread Enable	27M_SS/LCD_96/100M Spread spectrum enable. 0 = Spread Disabled, 1 = Spread Enabled
0	0	RESERVED	RESERVED

Byte 11 Control Register 11

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	SRC9_OE	SRC9 Output Enable 0 = Disabled, 1 = Enabled
4	1	SRC8_OE	SRC8 Output Enable 0 = Disabled, 1 = Enabled
3	0	RESERVED	RESERVED
2	0	SRC10_STP_CTRL	Allow control of SRC10 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC9_STP_CTRL	Allow control of SRC9 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC8_STP_CTRL	Allow control of SRC8 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 12 Control Register 12

Bit	@Pup	Name	Description
7	0	DIAG_EN	Diagnostic Bits Enabled 0 = Reset (default) setting bit 6, 5, 4, 2, 0 to zero 1 = DIAG mode enabled
6	HW	CPU PLL Status	CPU_PLL status 0 = PLL not locked; 1 = PLL locked
5	HW	Video PLL Status	Video_PLL status 0 = PLL not locked; 1 = PLL locked
4	HW	Fixed PLL Status	Fixed_PLL status 0 = PLL not locked; 1 = PLL locked
3	HW	PCIe PLL Status	PCIe_PLL status 0 = PLL not locked; 1 = PLL locked
2	HW	Frequency Accuracy	Primiary PLL or external crystal Frequency Accuracy 0=Frequency not accurate, 1=Frequency Accurate
1	1	Byte 0 Access	Byte 0 Access Control 0 = Disabled, 1 = Enabled

Byte 12 Control Register 12

Bit	@Pup	Name	Description
0	HW	PWRGOOD	Power on reset status bit 0 = All of the below conditions are not meet 1 = Valid voltage levels exist on VDD_SRC/CPU, VDD_REF, VDDA, VDD_48, VDD_PCI and CKPWRGD is asserted and external crystal is detected.

Byte 13 Control Register 13

Bit	@Pup	Name	Description
7	0	CLKREQ#9	CLKREQ#9 Input Enable 0 = Disabled, 1 = Enabled
6	0	CLKREQ#8	CLKREQ#8 Input Enable 0 = Disabled, 1 = Enabled
5	0	CLKREQ#7	CLKREQ#7 Input Enable 0 = Disabled, 1 = Enabled
4	0	CLKREQ#6	CLKREQ#6 Input Enable 0 = Disabled, 1 = Enabled
3	0	CLKREQ#5	CLKREQ#5 Input Enable 0 = Disabled, 1 = Enabled
2	0	CLKREQ#4	CLKREQ#4 Input Enable 0 = Disabled, 1 = Enabled
1	0	CLKREQ#3	CLKREQ#3 Input Enable 0 = Disabled, 1 = Enabled
0	0	CLKREQ#2	CLKREQ#2 Input Enable 0 = Disabled, 1 = Enabled

Byte 14 Control Register 14

Bit	@Pup	Name	Description
7	0	CLKREQ#1	CLKREQ#1 Input Enable 0 = Disabled, 1 = Enabled
6	1	LCD _96/100M Clock Speed	LCD 96_100M Clock Speed 0 = 96 MHz, 1 = 100 MHz
5	1	27M_SS Bit 0	27M SS Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
4	1	27M_non-SS Bit 0	27M non-SS Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
3	1	PCI4 Bit 0	PCI4 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
2	1	PCI3 Bit 0	PCI3 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
1	1	PCI2 Bit 0	PCI2 Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = High
0	1	PCI1 Bit 0	PCI1Slew Rate Control Bit 0, *See Table 6 for more detail* 0 = Low, 1 = Highh

Byte 15 Control Register 15

Bit	@Pup	Name	Description
7	HW	TME_STRAP	Trusted mode enable strap status, 0 = Normal 1 = No overclocking (default)
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED

Byte 15 Control Register 15

Bit	@Pup	Name	Description
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	IO_VOUT2	IO_VOUT[2,1,0] 000 = 0.30V 001 = 0.40V 010 = 0.50V 011 = 0.60V 100 = 0.70V 101 = 0.80V (Default) 110 = 0.90V 111 = 1.00V
1	0	IO_VOUT1	
0	1	IO_VOUT0	

Byte 16 Control Register 16

Bit	@Pup	Name	Description
7	1	PCI4 Bit 1	PCI4 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
6	1	PCI3 Bit 1	PCI3 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
5	1	PCI2 Bit 1	PCI2 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
4	1	PCI1 Bit 1	PCI1 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
3	1	PCIF0 Bit 1	PCIF0 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
2	1	48M Bit 1	48M Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
1	1	27M_SS Bit 1	27M_SS Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
0	1	27M_non-SS Bit 1	27M_non-SS Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High

Byte 17 Control Register 17

Bit	@Pup	Name	Description
7	1	27M_SS Bit 2	27MHz_SS Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
6	1	27M_non_SS Bit 2	27MHz_non_SS Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
5	1	REF1 Bit 1	REF1 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
4	1	REF0 Bit 1	REF0 Slew Rate Control Bit 1, *See Table 6 for more detail* 0=Low, 1 = High
3	1	REF1 Bit 2	REF1 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
2	1	REF0 Bit 2	REF0 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 18 Control Register 18

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 19 Control Register 19

Bit	@Pup	Name	Description
7	1	PCI4 Bit 2	PCI4 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
6	1	PCI3 Bit 2	PCI3 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
5	1	PCI2 Bit 2	PCI2 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
4	1	PCI1 Bit 2	PCI1 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
3	1	PCIF0 Bit 2	PCIF0 Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
2	1	48M Bit 2	48M Slew Rate Control Bit 2, *See Table 6 for more detail* 0=Low, 1 = High
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Table 6. Slew Rate Control Table

	Slew Rate Control Bit [2:0]			Slew Rate
	Bit2	Bit1	Bit0	
Default	1	1	1	Fastest
	1	1	0	
	1	0	1	
	1	0	0	
	0	1	1	
	0	1	0	
	0	0	1	
	0	0	0	Slowest

Table 7. Crystal Recommendation

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SL28647 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the SL28647 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency

shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

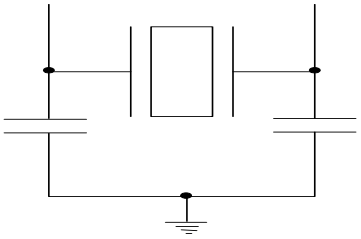


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

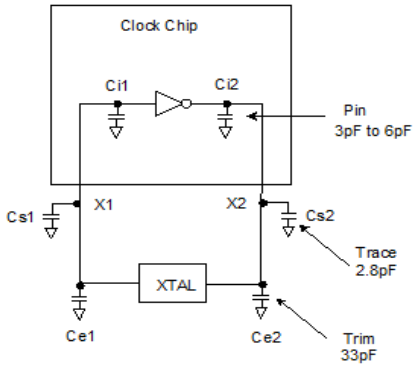


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL.....Crystal load capacitance

CLe..... Actual loading seen by crystal using standard value trim capacitors

Ce..... External trim capacitors

Cs.....Stray capacitance (terraced)

Ci .....Internal capacitance (lead frame, bond wires etc.)

CLK_REQ# Description

The CLKREQ# signals are active LOW inputs used for clean enabling and disabling selected SRC outputs. The outputs controlled by CLKREQ# are determined by the settings in register byte 8. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of SRCC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

CLK_REQ[1:9]# Assertion (CLKREQ# -> LOW)

All differential outputs that were stopped are to resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs must be driven HIGH within 10 ns of CLKREQ# deassertion to a voltage greater than 200 mV.

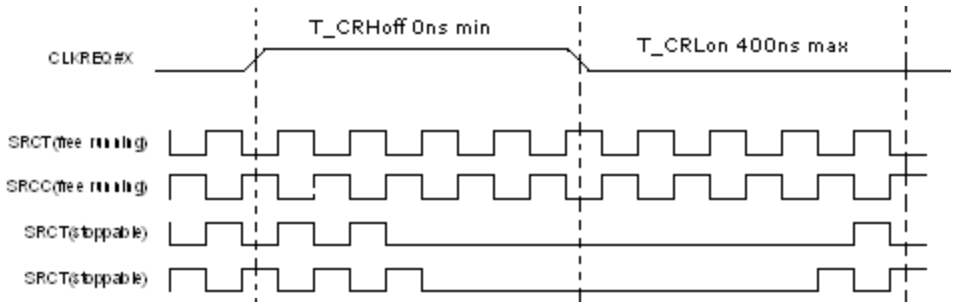


Figure 3. CLK_REQ#[1:9] Deassertion/Assertion Waveform

CLK_REQ[1:9]# Deassertion (CLKREQ# -> HIGH)

The impact of deasserting the CLKREQ# pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of CLKREQ# are to be stopped after their next transition. The final state of all stopped SRC clocks is Low/Low.

PD (Power-down) Clarification

The CK_PWRGD/PD# pin is a dual-function pin. During initial power-up, the pin functions as CK_PWRGD. Once CK_PWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD# is sampled LOW by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must be held HIGH or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock outputs are held with "Diff clock" pin driven HIGH, and "Diff clock#" tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are tri-state. Note that *Figure 4* shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, and 200 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 µs after asserting CK_PWRGD. It should be noted that 96_100_SSC will follow the DOT waveform when selected for 96 MHz and the SRC waveform when in 100-MHz mode.

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 µs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up. It should be noted that 96_100_SSC will follow the DOT waveform when selected for 96 MHz and the SRC waveform when in 100-MHz mode.

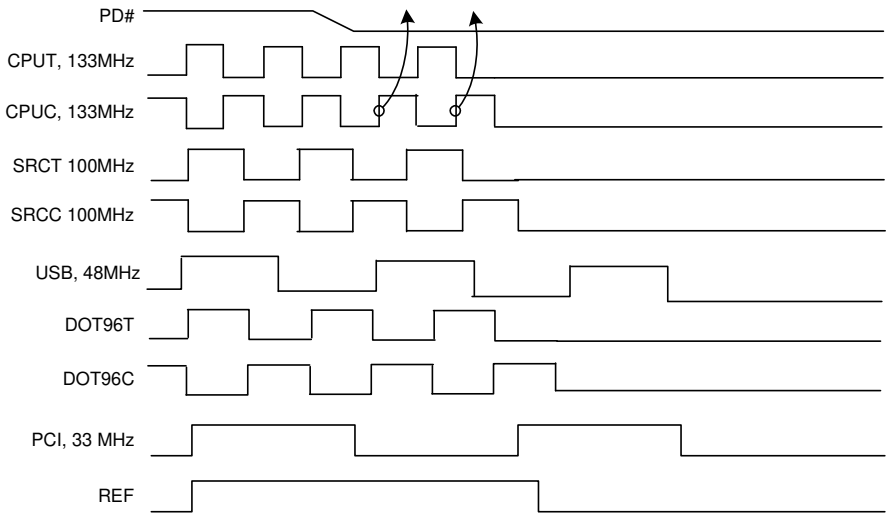


Figure 4. Power-down Assertion Timing Waveform

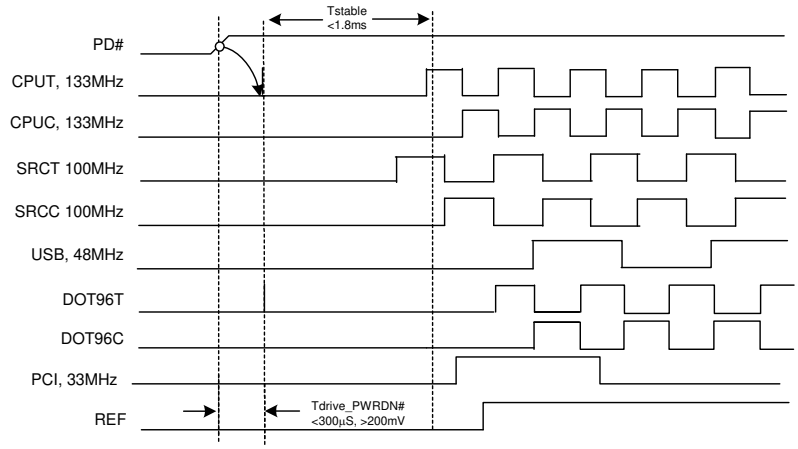


Figure 5. Power-down Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final state of all stopped CPU clocks is High/Low when driven, Low/Low when tri-stated.

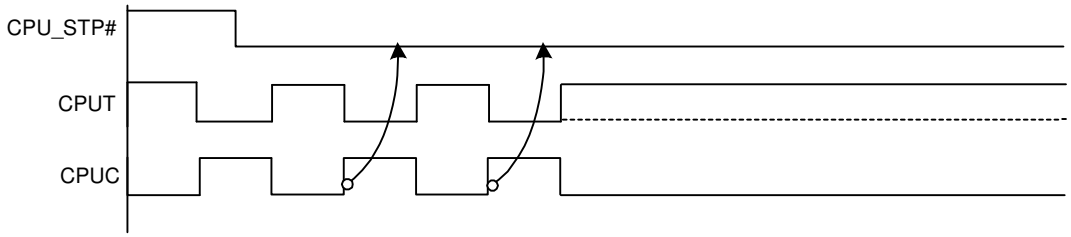


Figure 6. CPU_STP# Assertion Waveform

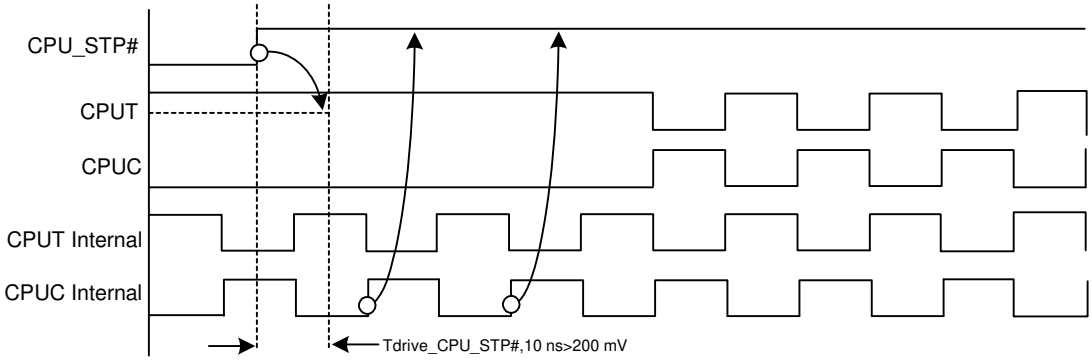


Figure 7. CPU_STP# Deassertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs and SRC outputs if they are set to be stoppable in SMbus while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 9*.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running. All stopped PCI outputs are driven Low, SRC outputs are High/Low if set to driven and Low/Low if set to tri-state.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level.

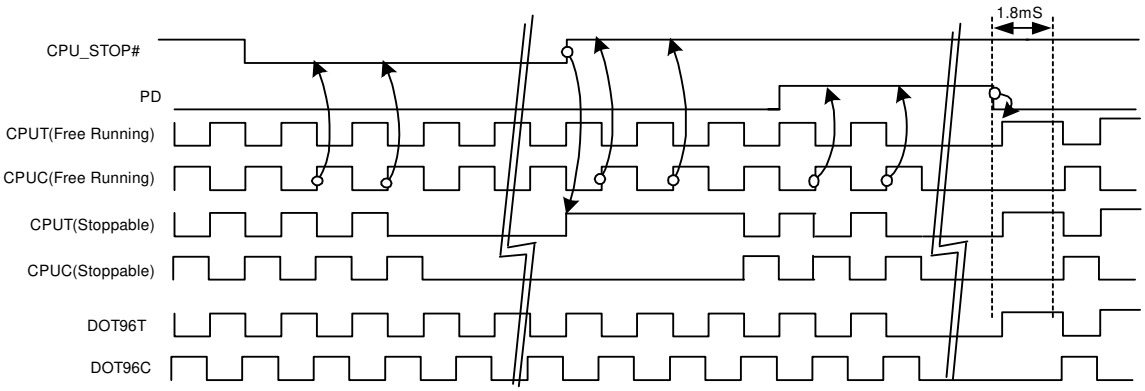


Figure 8. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

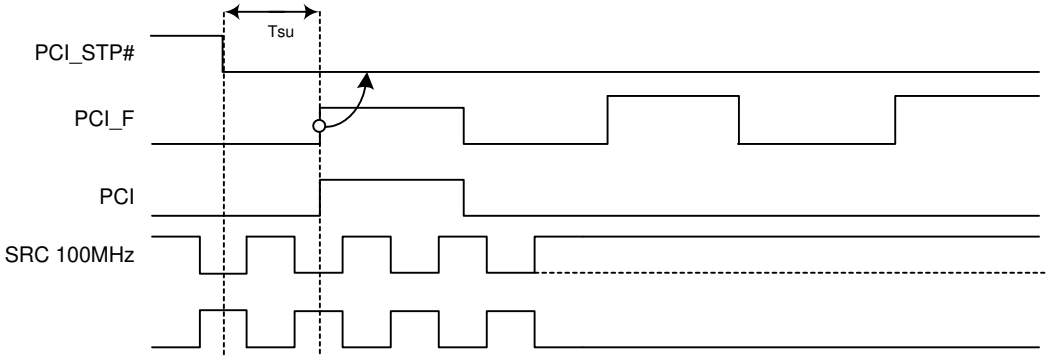


Figure 9. PCI_STP# Assertion Waveform

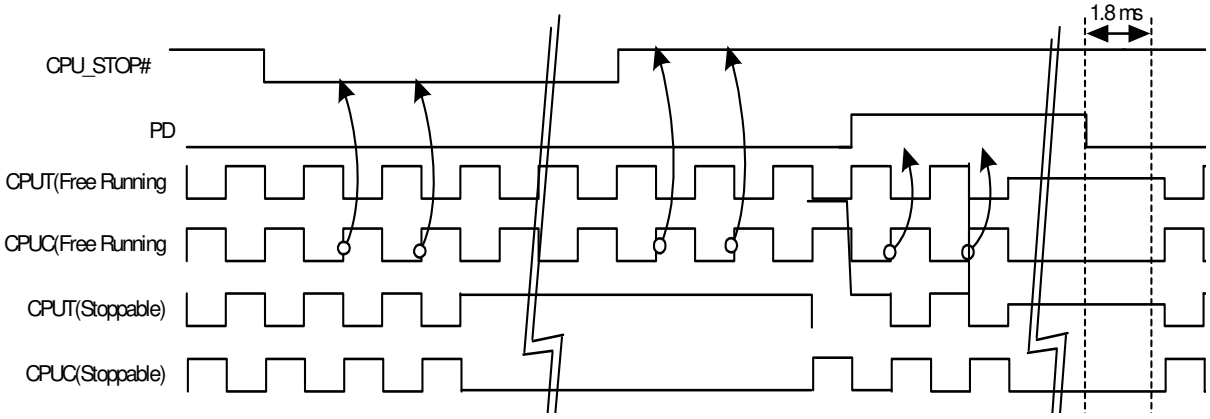


Figure 10. CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven

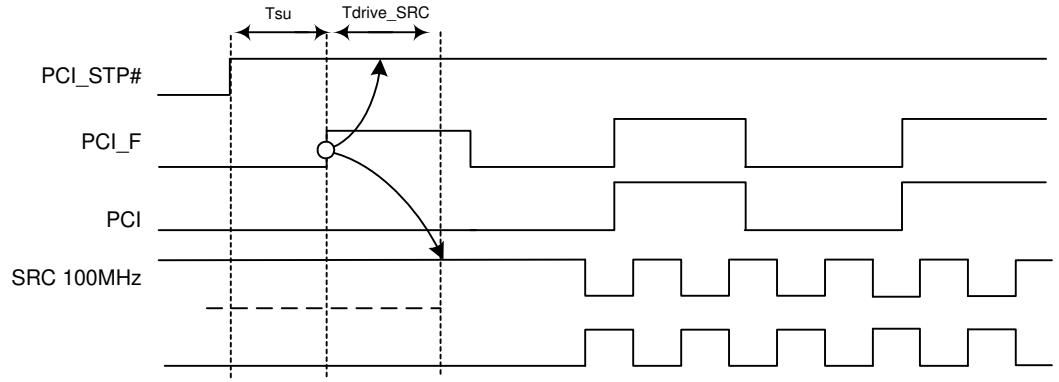


Figure 11. PCI_STP# Deassertion Waveform

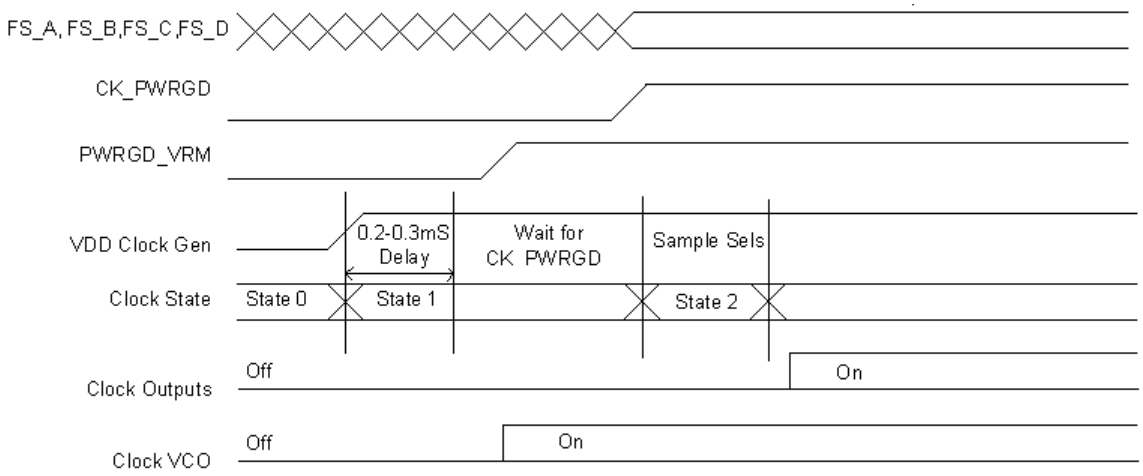


Figure 12. CK_PWRGD Timing Dlagram

Table 8. Default Condition for Output Driver Status

		PCI_STOP# Asserted	CPU_STOP# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Driven Low	Running	Driven Low
	Non Stoppable	Running	Running	
Differential Clocks	Stoppable	Clock Drive High Clock# Driven Low	Clock Drive High Clock# Driven Low	Driven Low or 20K pulldown
	Non Stoppable	Running	Running	

Table 9. Default Condition for Output Driver Status

	All Single-ended Clocks		All Differential Clocks except CPU1		CPU1	
	w/o Strap	w/Strap	Clock	Clock#	Clock	Clock#
Latches Open State	Low	Hi-Z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
Powerdown (PD#)	Low	Hi-Z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
M1	Low	Hi-Z	Low or 20K pulldown	Low	Running	Running

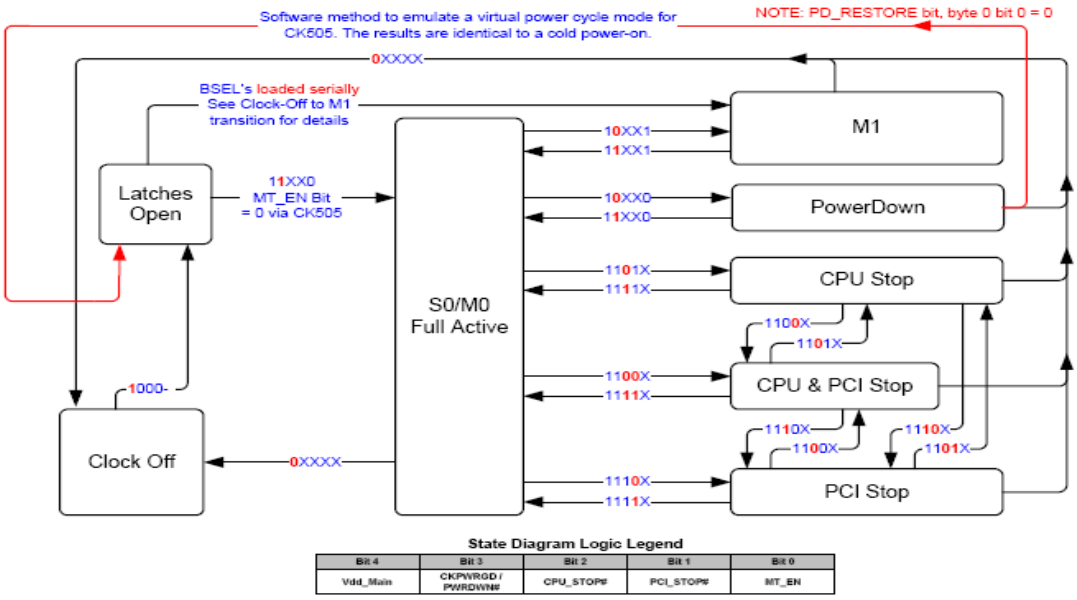


Figure 13. SL28647 State Diagram

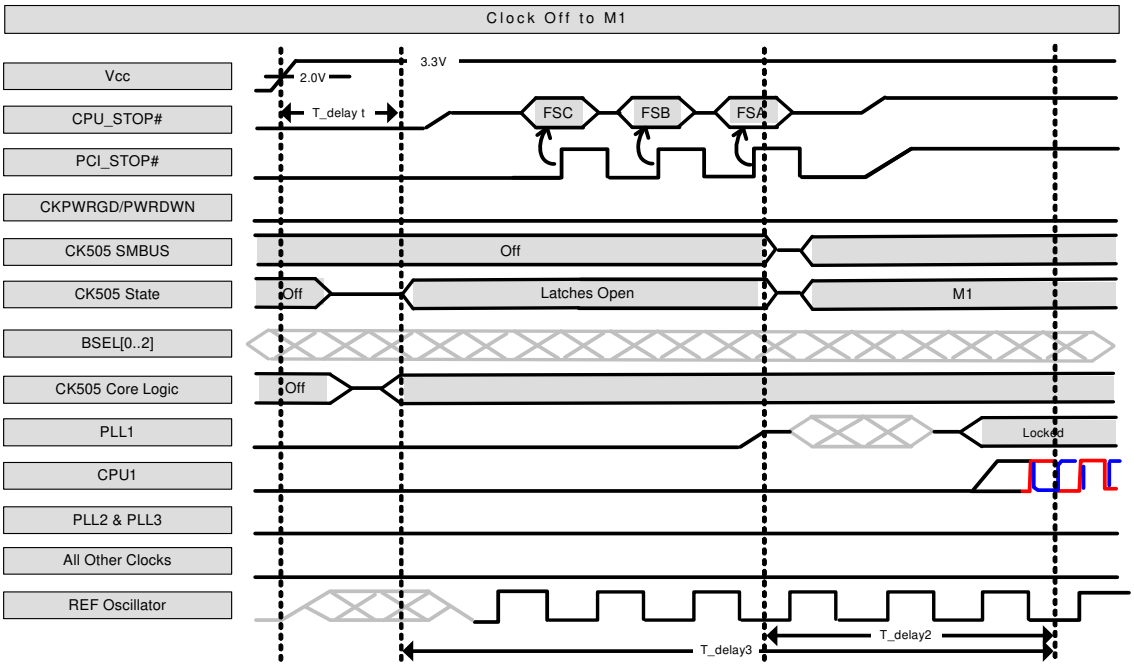


Figure 14. BSEL Serial Latching

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–	4.6	V
V_{DD_A}	Analog Supply Voltage		–	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		2		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All VDDs	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	V_{DD} + 0.5	V
V_{ILFS_C}	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IMFS_C}	FS_C Input Middle Voltage		0.7	1.7	V
V_{IHFS_C}	FS_C Input High Voltage		2.0	V_{DD} + 0.5	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	5	µA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current		–	250	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Driven	–	30	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-state	–	5	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
CPU					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at 0V differential at 0.1s	45	55	%
T_{PERIOD}	100 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
T_{PERIOD}	133 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	7.49925	7.50075	ns
T_{PERIOD}	166 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	5.99940	6.00060	ns
T_{PERIOD}	200 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	4.99950	5.00050	ns
T_{PERIOD}	266 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	3.74963	3.75038	ns
T_{PERIOD}	333 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	2.99970	3.00030	ns
T_{PERIOD}	400 MHz CPUT and CPUC Period	Measured at 0V differential at 0.1s	2.49975	2.50025	ns
$T_{PERIODSS}$	100 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODSS}$	133 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	7.51804	7.51955	ns
$T_{PERIODSS}$	166 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	6.01444	6.01564	ns
$T_{PERIODSS}$	200 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	5.01203	5.01303	ns
$T_{PERIODSS}$	266 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	3.75902	3.75978	ns
$T_{PERIODSS}$	333 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	3.00722	3.00782	ns
$T_{PERIODSS}$	400 MHz CPUT and CPUC Period, SSC	Measured at 0V differential at 0.1s	2.50601	2.50652	ns
$T_{PERIODAbs}$	100 MHz CPUT and CPUC Absolute period	Measured at 0V differential at 1 clock	9.91400	10.0860	ns
$T_{PERIODAbs}$	133 MHz CPUT and CPUC Absolute period	Measured at 0V differential at 1 clock	7.41425	7.58575	ns
$T_{PERIODAbs}$	166 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	5.91440	6.08560	ns
$T_{PERIODAbs}$	200 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	4.91450	5.08550	ns
$T_{PERIODAbs}$	266 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	3.66463	3.83538	ns
$T_{PERIODAbs}$	333 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	2.91470	3.08530	ns
$T_{PERIODAbs}$	400 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	2.41475	2.58525	ns
$T_{PERI-ODSSAbs}$	100 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	9.91406	10.1362	ns
$T_{PERI-ODSSAbs}$	133 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	7.41430	7.62340	ns
$T_{PERI-ODSSAbs}$	166 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	5.91444	6.11572	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERI-ODSSAbs}$	200 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	4.91453	5.11060	ns
$T_{PERI-ODSSAbs}$	266 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	3.66465	3.85420	ns
$T_{PERI-ODSSAbs}$	333 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	2.91472	3.10036	ns
$T_{PERI-ODSSAbs}$	400 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	2.41477	2.59780	ns
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_{SKEW}	CPU0 to CPU1 Clock Skew	Measured at 0V differential	–	100	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at 0V differential	–	150	ps
T_R / T_F	CPU Rising/Falling Slew rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential @ 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential @ 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential @ 1 clock	9.87400	10.1260	ns
$T_{PERI-ODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential @ 1 clock	9.87406	10.1762	ns
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
DOT96 at 0.7V					
T_{DC}	DOT96 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96 Period	Measured at 0V differential at 0.1s	10.4156	10.4177	ns
$T_{PERIODAbs}$	DOT96 Absolute Period	Measured at 0V differential at 0.1s	10.1656	10.6677	ns
T_{CCJ}	DOT96 Cycle to Cycle Jitter	Measured at 0V differential at 1 clock	–	250	ps
L_{ACC}	DOT96 Long Term Accuracy	Measured at 0V differential at 1 clock	–	100	ppm
T_R / T_F	DOT96 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
LCD_100_SSC at 0.7V					
T_{DC}	LCD_100 Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz LCD_100 Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz LCD_100 Period, SSC -0.5%	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz LCD_100 Absolute Period	Measured at 0V differential at 1 clock	9.74900	10.25100	ns
$T_{PERIODSSAbs}$	100 MHz LCD_100 Absolute Period, SSC	Measured at 0V differential @ 1 clock	9.74906	10.3012	ns
T_{CCJ}	LCD_100 Cycle to Cycle Jitter	Measured at 0V differential	–	250	ps
L_{ACC}	LCD_100 Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	LCD_100 Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99700	30.00300	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	30.08421	30.23459	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49700	30.50300	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.56617	30.58421	ns
T_{HIGH}	Spread Enabled PCIF and PCI high time	Measurement at 2V	12.27095	16.27995	ns
T_{LOW}	Spread Enabled PCIF and PCI low time	Measurement at 0.8V	11.87095	16.07995	ns
T_{HIGH}	Spread Disabled PCIF and PCI high time	Measurement at 2.V	12.27365	16.27665	ns
T_{LOW}	Spread Disabled PCIF and PCI low time	Measurement at 0.8V	11.87365	16.07665	ns
T_R / T_F	PCIF/PCI Rising/Falling Slew Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	1000	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measurement at 1.5V	–	100	ppm
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2V	8.216563	11.15198	ns
T_{LOW}	48_M Low time	Measurement at 0.8V	7.816563	10.95198	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measurement at 1.5V	–	100	ppm
27M_NSS/27M_SS at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{PERIOD}	Spread Disabled 27M Period	Measurement at 1.5V	37.03594	37.03813	ns
	Spread Enabled 27M Period	Measurement at 1.5V	37.012986	37.13172	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	200	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	50	ppm
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.82033	69.86224	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.83429	70.84826	ns
T_{HIGH}	REF High time	Measurement at 2V	29.97543	38.46654	ns
T_{LOW}	REF Low time	Measurement at 0.8V	29.57543	38.26654	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	100	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For Single-ended Signals and Reference

The following diagram shows test load configurations for the single-ended PCI, USB, and REF output signals.

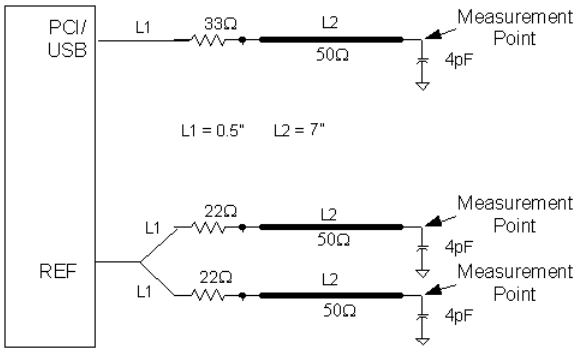


Figure 15.Single-ended Load Configuration Low Drive Option

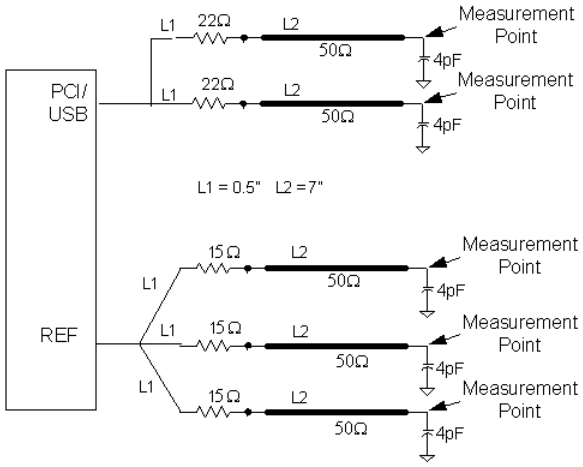


Figure 16. Single-ended Load Configuration High Drive Option

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

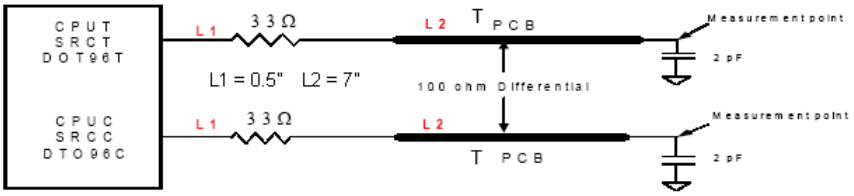


Figure 17. 0.8V Differential Load

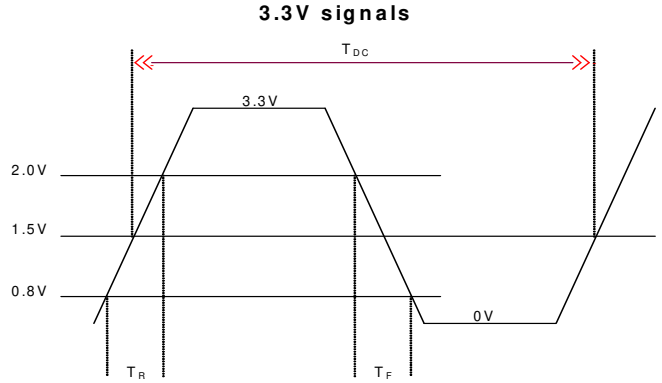
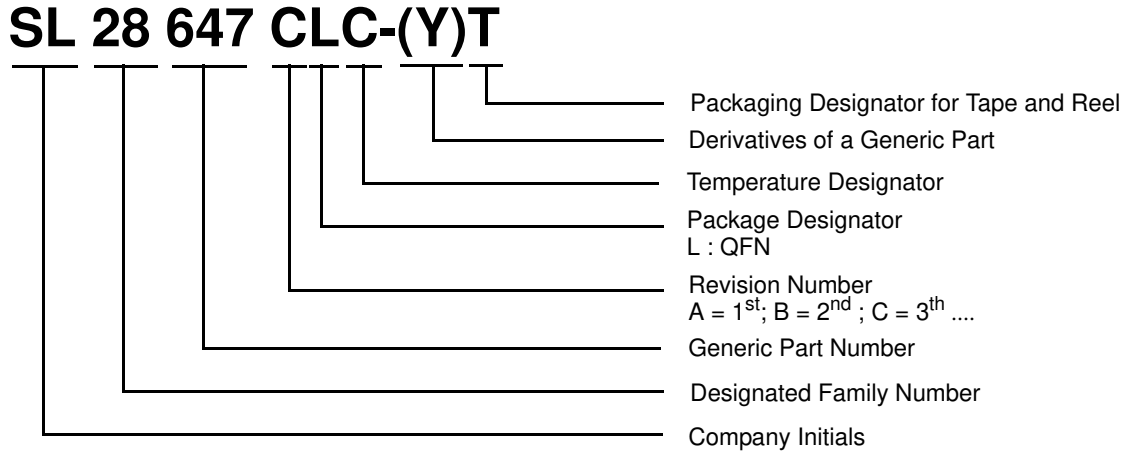


Figure 18. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

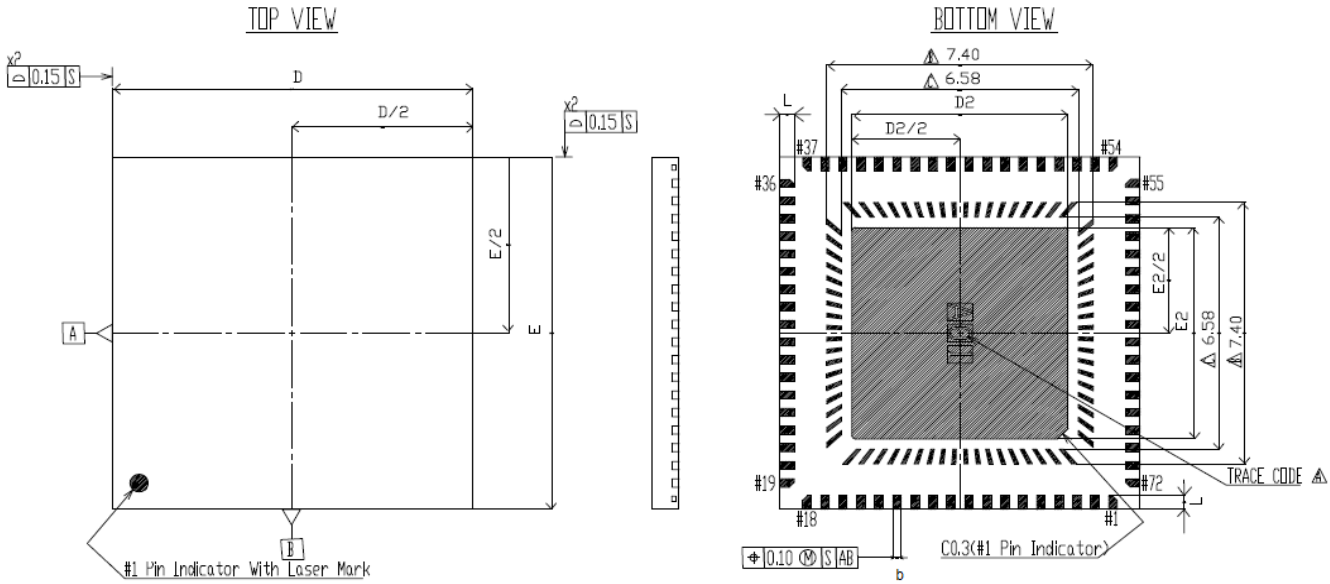
Part Number	Package Type	Product Flow
Lead-free		
SL28647CLC	72-pin QFN	Commercial, 0° to 85°C
SL28647CLCT	72-pin QFN–Tape and Reel	Commercial, 0° to 85°C



This device is Pb free and RoHS compliant. Parts supporting extended temperature is available upon request.

Package Diagram

72-Lead QFN 10 x 10 mm (Saw Version)



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.18	0.23	0.28
D	9.90	10.00	10.10
D2	5.85	6.00	6.15
E	9.90	10.00	10.10
E2	5.85	6.00	6.15
e		0.50 BSC.	
L	0.30	0.40	0.50

NOTES)
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.10.
3.THE SURFACE OF THE PACKAGE SHALL BE RZ 1-BIEM.
4.PROTRUSIONS AT PKG.OUTLINE SHALL NOT EXCEED 0.10.
5.DIMENSIONS IN PARENTHESIS ARE REFERENCE VALUES.

Document History Page

Document Title: SL28647 Clock Generator for Intel®CK505 Document Number: 001-05103			
REV.	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0	7/29/08	JMA	New data sheet
1.1	3/30/09	JMA	1. Updated Package Diagram 2. Updated 27MHz Slew Rate Measurement Window 3. Updated TPeriod for CPU at 100MHz 4. MSL 1 to 2 5. Updated package drawing to be Saw 6. Updated Lead Width parameter b to be more visible