User's Guide
SLVU495B – July 2011 – Revised January 2012

600-kHz Synchronous Switch-Mode Li-Ion and Li-Polymer Host-Controlled Battery Charger With Integrated MOSFETs

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- Input Operating Range 5.5 V–17 V
- LED Indication for Charge Status
- Test Points for Key Signals Available for Testing Purpose—Easy Probe Hook-up
- Jumpers Available—Easy to Change Setting

1.2 General Description

The bq24130 is highly integrated host-controlled Li-ion and Li-polymer switch-mode battery charge controllers with two integrated N-channel power MOSFETs. It offers a constant-frequency synchronous PWM controller with high accuracy regulation of charge current and voltage. It also provides charge status monitoring.

The bq24130 automatically enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage. The bq24130 charges one, two or three cell (selected by CELL pin), supporting up to 4A charge current. The bq24130 is available in a 20-pin, 3.5×4.5 mm^2 thin QFN package.

For details, see bq24130 data sheet (SLUSAN2).

1.3 I/O Description

Table 1. I/O Description

Jack	Description
J1 – VIN	Positive input
J1 – PGND	Negative input
J2 – VBAT	Connected to charger output
J2 – PGND	Ground
J3 – CMOD	Charge mode selection
J3 – $\overline{CE}$	Charge enable
J3–TS_EXT	Temperature qualification voltage Input

1.4 Control and Key Parameters Setting

Table 2. Control and Key Parameters Setting

Jack	Description	Factory Setting
JP1	Select external TS input or internal valid TS setting 1-2 : External TS input 2-3 : Internal valid TS setting	Jumper ON 1-2 (external TS)
JP2	The pull-up power source supplies the LED when JP5 ON. LED has no power source when JP5 OFF.	Jumper ON (LED power available)
JP3	CELL selection 2-3 : CELL-GND, 1CELL 2-1 : CELL-VREF, 3CELL OPEN: CELL- FLOAT, 2CELL	Jumper ON 2-1 (3 CELL)
JP4	Charge mode selection: ON: CMOD-GND for pre-charge set by ISET2 OFF: CMOD-VREF for fast charge set by ISET1	Jumper ON (Pre-charge setting)

Table 2. Control and Key Parameters Setting (continued)

Jack	Description	Factory Setting
JP5	Charger enable/disable setting. ISET is pulled to GND and the charger is disabled when JP5 OPEN; charger is enable when JP5 ON.	Jumper OPEN (disable charger)

1.5 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
Supply voltage, V_{BUS}	Input voltage	5.5		17	V	
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J2	0		12.6	V	
Supply current	Maximum input current	0		4	A	
Charge current, I_{chrg}	Battery charge current	0	2	4	A	
Operating junction temperature range, T_J		0		125	°C	

The bq24130 EVM board requires a regulated supply approximately 1V minimum above the regulated voltage of the battery pack to a maximum input voltage of 17 VDC. The bq24130 uses CELL pin to select number of cells with a fixed 4.2V/cell. Connecting CELL to AGND gives 1 cell, floating CELL pin gives 2 cell configure, and connecting to VREF gives 3 cells configure. CELL pin adjusts internal resistor voltage divider from BAT pin to AGND pin for voltage feedback and regulate to internal 2.1V voltage reference.

CELL Pin	Voltage Regulation
AGND	4.2V
Floating	8.4V
VREF	12.6V

The default setting is 12.6V for BAT voltage.

A low-level signal on the CMOD pin forces the IC to charge at the pre-charge rate set on the ISET2 pin. A high-level signal forces charge at fast-charge rate as set by the ISET1 pin. If the battery reaches the voltage regulation level, the IC transitions to voltage regulation phase regardless of the status of the CMOD input.

The ISET1 input sets the maximum charging current. Battery current is sensed by current sensing resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is **40mV max**. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET1}}{20 \times R_7} \quad (1)$$

The precharge current is determined by the voltage on the ISET2 pin according to the formula

$$I_{PRECHARGE} = \frac{V_{ISET2}}{100 \times R_7} \quad (2)$$

The default setting is 2ADC for fast charge current and 0.2ADC for pre-charge current.

2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA624 evaluation board. On the test procedure the following naming conventions are followed.

VXX:	External voltage supply name (VIN, VBAT, VTS)
LOADW;	External load name (LOADR, LOADI)
V(TPyYy):	Voltage at internal test point TPyyy. For example, V(TP1) means the voltage at TP1.
V(Jxx):	Voltage at jack terminal Jxx.
V(TP(XXX)):	Voltage at test point "XXX". For example, V(REGN) means the voltage at the test point which is marked as "REGN".
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON:	Internal jumper Jxx terminals are shorted
Jxx OFF:	Internal jumper Jxx terminals are open
Jxx (-YY-) ON:	Internal jumper Jxx adjacent terminals marked as "YY" are shorted
Measure → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Safety

- Safety Glasses are to be worn.
- This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.
- ESD precautions must be followed while handling electronic assemblies while performing this test.
- Precautions should be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

2.3 Quality

- Test data shall be made available upon request by Texas Instruments.

2.4 Apparel

- Electrostatic smock
- Electrostatic Gloves or finger cots
- Safety Glasses
- Ground ESD wrist strap

2.5 Equipment

- Power Supplies
  Power Supply #1 (PS#1): a power supply capable of supplying 30-V at 5-A is required.
- Loads
  LOAD #1 A 20V (or above), 3A (or above) electronic load that can operate at constant current and constant voltage mode.
- Meters
  Five Fluke 75 multi-meters, (equivalent or better)

Or: Four equivalent voltage meters and three equivalent current meters.
The current meters must be capable of measuring 5A+ current.

2.6 Equipment Setup

- Set the power supply #1 (PS#1) for 16V ± 200mV, 2A ± 0.1A current limit and then turn off supply.
- Connect the output of PS#1 in series with a current meter (multi-meter) to J1 (VIN, GND).
- Connect a voltage meter across J1 (VIN, PGND).
- Connect Load #1 in series with a current meter to J2 (VBAT, PGND). Turn off Load #1.
- Connect a voltage meter across J2 (VBAT, PGND).
- Check all jumper shunts. JP1: connect 1-2 (External TS); JP2: ON; JP3: connect 1-2 (3-cell); JP4: ON; JP5: OPEN.

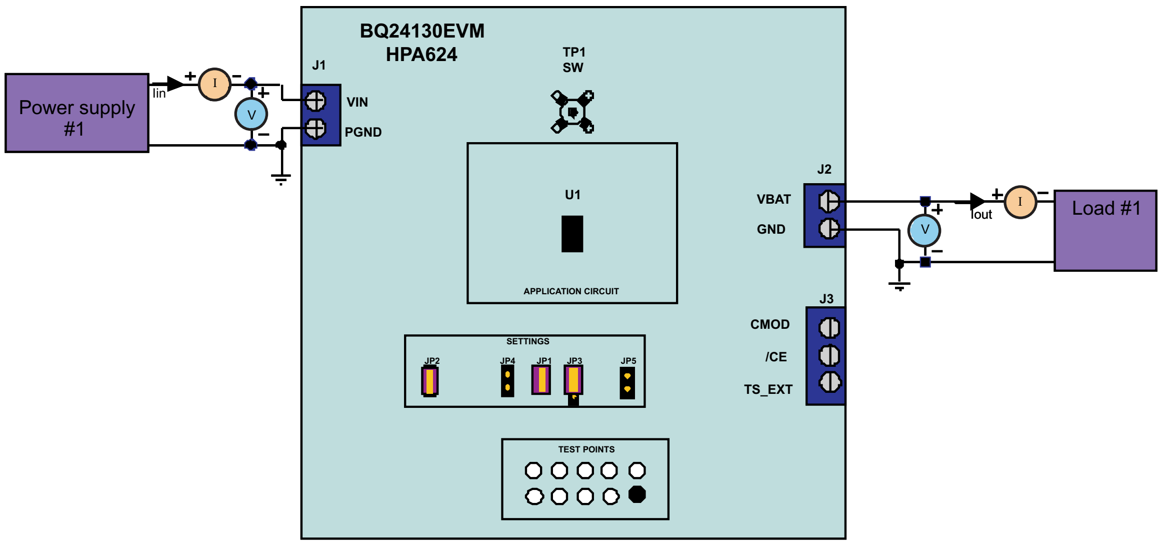

Figure 1. Original Test Setup for HPA624 (bq24130EVM)

2.7 Procedure

Make sure EQUIPMENT SETUP steps are followed.

1. Disconnect LOAD #1. Turn on PS#1

   Measure → V(J2(VBAT)) = 0.5V ± 500mV
   Measure → V(TP(VREF)) = 3.3V ± 200mV
   Measure → V(TP(REGN)) = 0.5V ± 500mV

2. Charger Enable

   Connect 2-3 of JP1 (Internal TS); Short JP4 (Charger Enable)
   Measure → V(TP(VREF)) = 3.3V ± 200mV
   Measure → V(TP(REGN)) = 6V ± 200mV
   Measure → V(J2(VBAT))=12.6V ± 200mV

3. Charge Voltage Setting

   Connect 2-3 of JP3

   Measure → V(J2(VBAT))=4.2V ± 200mV
   Disconnect JP3
   Measure → V(J2(VBAT))=8.4V ± 200mV

4. Charge Current Regulation and Battery Temperature Qualification

   Reconnect 1-2 of JP3
   Reconnect LOAD#1. Turn on. Use the constant voltage mode. Set the output voltage to be 10V.
   Measure → I(J2(VBAT)) = 0.2A ± 100mA

Observe → D1 (STAT) ON

Open JP4 (set fast charge)
Measure → I(J2(VBAT)) = 2A ± 200mA
Observe → D1 (STAT) ON

Open 2-3 of JP1 (external TS)
Measure → I(J2(VBAT)) = 0A ± 100mA
Observe → D1 (STAT) BLINK

Connect 2-3 of JP1 (Internal TS)
Measure → I(J2(VBAT)) = 2A ± 200mA
Observe → D1 (STAT) ON

5. Charge Voltage Regulation

   Observe → I(J2(VBAT)) decreases from 2A while V(J2(VBAT)) becomes constant.

6. Test Complete

   Turn off the power supply and remove all connections from the unit under test (UUT).

3 PCB Laout Guideline

1. It is critical that the exposed thermal pad on the backside of the BQ24130 package be soldered to the PCB ground. Make sure there are sufficient thermal vias right underneath the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the thermal pad.
3. Charge current sense resistor must be connected to SRP, SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. Decoupling capacitors for VREF, AVCC, REGN should make the interconnections to the IC as short as possible.
5. Decoupling capacitors for BAT must be placed close to the corresponding IC pins and make the interconnections to the IC as short as possible.
6. Decoupling capacitor(s) for the charger input must be placed very close to SW and PGND.
7. Take the EVM layout for design reference.

4 Bill of Materials, Board Layouts and Schematics

4.1 Bill of Materials

Table 4. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 µF	Capacitor, Ceramic, 25V, X7R, 10%	805	STD	STD
3	C11,C12, C17	0.1 µF	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
0	C13	NONE	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
2	C14, C16	1.0 µF	Capacitor, Ceramic, 16V, X7R, 10%	805	STD	STD
0	C15	NONE	Capacitor, Ceramic, 16V, X7R, 10%	805	STD	STD
2	C2, C3	4.7 µF	Capacitor, Ceramic, 25V, X7R, 10%	805	STD	STD
2	C4, C10	1.0 µF	Capacitor, Ceramic, 25V, X7R, 10%	805	STD	STD
0	C5	NONE	Capacitor, Ceramic, Low Inductance, 50V, X7R, 10%	603	STD	STD
1	C6	47 nF	Capacitor, Ceramic, 50V, X7R, 10%	603	STD	STD
2	C7, C8	10 µF	Capacitor, Ceramic, 25V, X7R, 10%	1206	STD	STD
1	C9	1 µF	Capacitor, Ceramic, 25V, X7R, 10%	805	STD	STD
1	D1	PDS1040	Diode, Schottky Barrier, 10A, 40V	Power DI 5	PDS1040-13	Diodes
1	D2	BAT54XV2T1G	Diode, Schottky, 10 mA, 30 V	SOD523	BAT54XV2T1G	On Semi
0	D3	B220A	Diode, Schottky, 20V, 2A	SMA	B220A-13-F	Diodes
1	D4	Green	Diode, LED, Green, 2.1V, 20mA, 6mcd	603	LTST-C190GKT	Lite On
0	D5	BAT54XV2T1G	Diode, Schottky, 10 mA, 30 V	SOD523	BAT54XV2T1G	On Semi
1	J1, J2	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
1	J3	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
3	JP2, JP4, JP5	PEC02SAAN	Header, 2 pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
2	JP1, JP3	PEC03SAAN	Header, 3 pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	6.8uH	Inductor, SMT, 8A, 21milliohm	0.400 x 0.453 inch	HLP4040DZER6R8M01	Vishay
1	Q1	2N7002-7-F	MOSFET, N-ch, 60V, 115mA, 1.2Ohms	SOT23	2N7002-7-F	Diodes Inc
2	R10, R14	0	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R11	100	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R12	30.1k	Resistor, Chip, 1/16W, 1%	603	STD	STD
2	R13, R5	10k	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R15	232k	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R16	154k	Resistor, Chip, 1/16W, 1%	603	STD	STD

Table 4. Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
2	R17, R18	100k	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R19	4.99k	Resistor, Chip, 1/16W, 1%	603	STD	STD
2	R2, R3	3.9	Resistor, Chip, 1/4W, 5%	1206	STD	STD
1	R20	32.4k	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R4	10	Resistor, Chip, 1/10W, 1%	805	STD	STD
0	R6	NONE	Resistor, Chip, 1/16W, 1%	805	STD	STD
1	R7	0.01	Resistor, Chip, 1/2 watt, 1.0%	1206	WSL1206R0100FEA	Vishay
1	R8	0	Resistor, Chip, 1/16W, 5%	603	STD	STD
1	R9	5.23k	Resistor, Chip, 1/16W, 1%	603	STD	STD
0	SH1	None	Short jumper			
1	TP	131-4244-00	Adaptor, 3.5-mm probe clip (or 131-5031-00)	0.200 inch	131-4244-00	Tektronix
1	TP1	VCC	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
0	TP2, TP4, TP5	NONE	Test Point, White, Thru Hole Color Keyed	0.02 x 0.02 inch	STD	STD
1	TP3	VREF	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP6	REGN	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP7	TS	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP8	GND	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	TP9	STAT	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP10	CELL	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP11	CMOD	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP12	ISET1	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	TP13	ISET2	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	U1	BQ24130RHL	IC, 1.6-MHz High Efficiency Synchronous Switch-Mode Li-Ion and Li-Polymer Battery Charger	VQFN	BQ24130RHL	TI
1	—		PCB, 2.500 In X 2.500 In x 0.0062 In	2.500 In X 2.500 In	HPA624	Any
4		929950-00	Shorting jumper, 2-pin, 100mil spacing		929950-00	3M/ESD

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.2 Board Layout

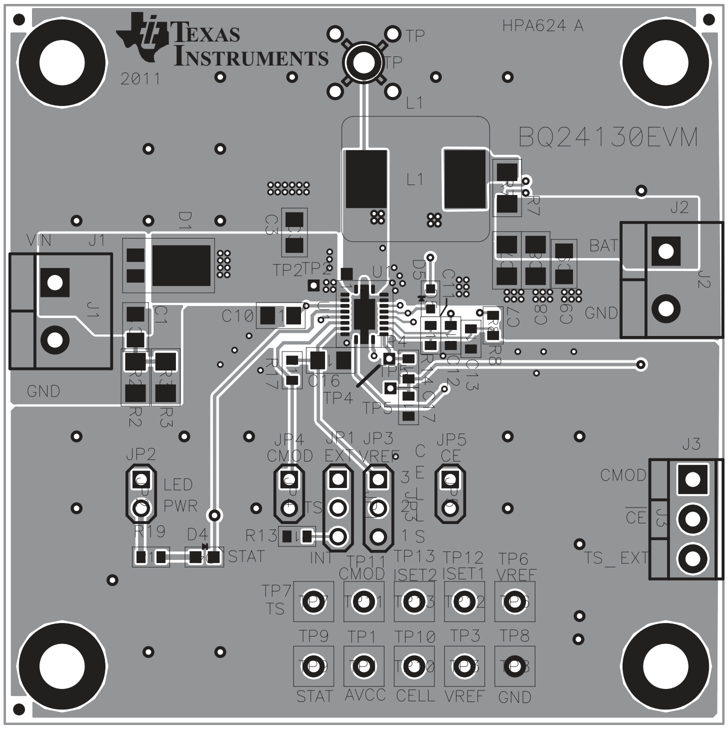

Figure 2. Top Assembly

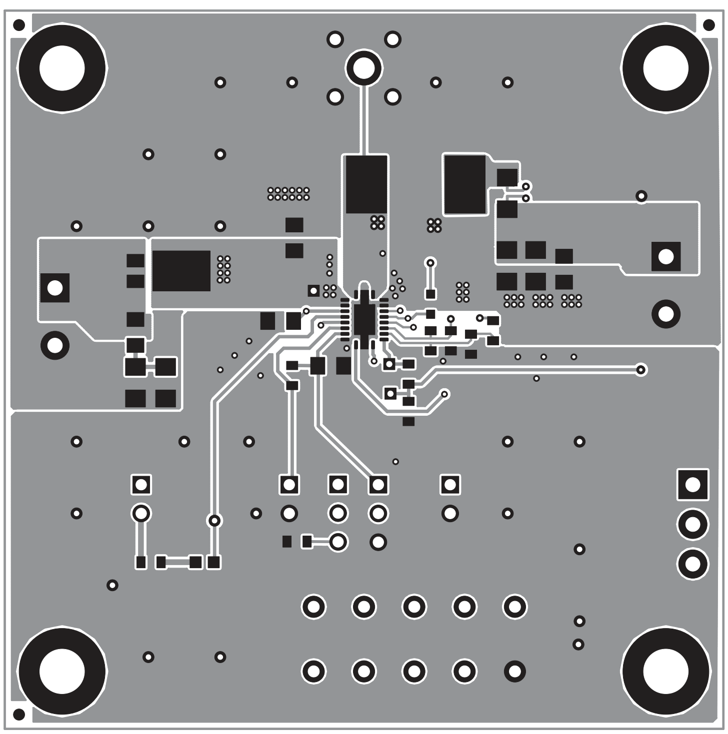

Figure 3. Top Layer

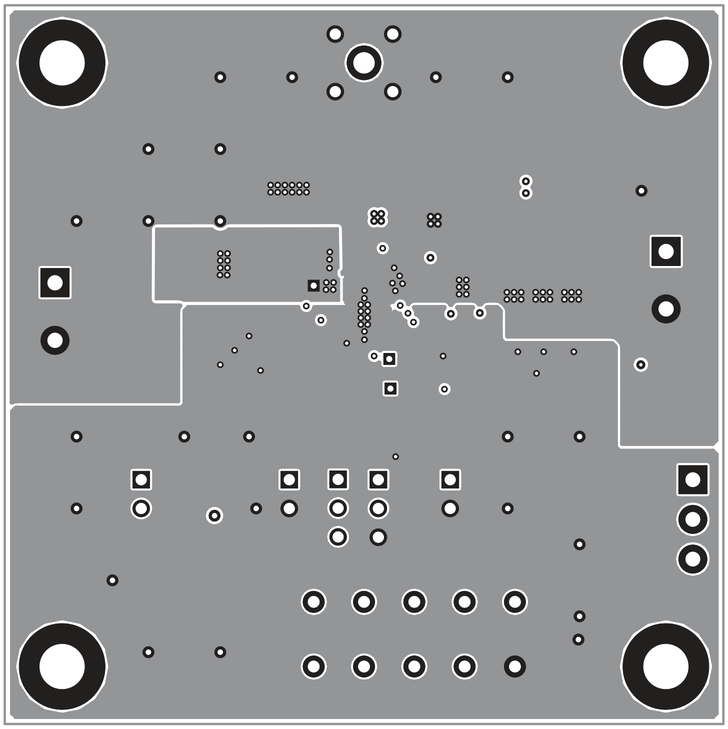

Figure 4. Second Layer

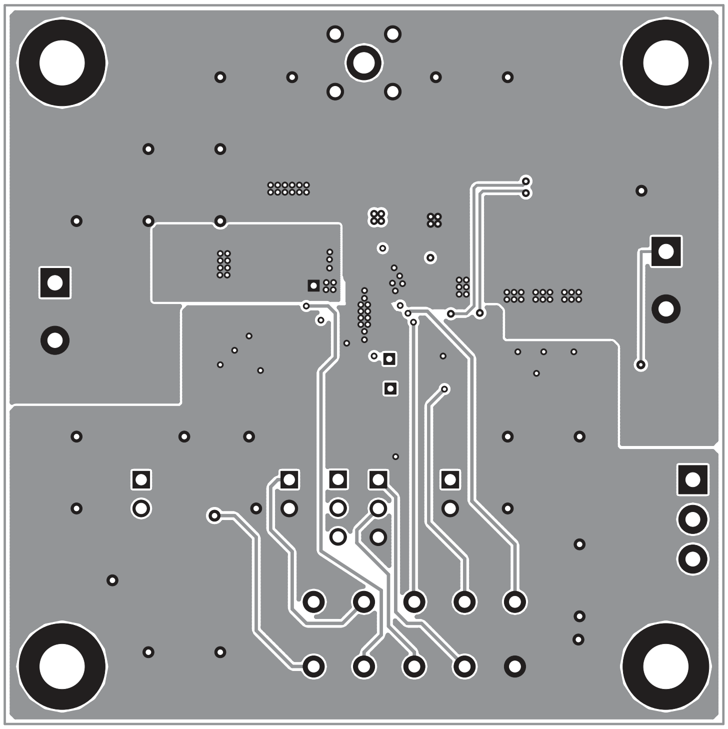

Figure 5. Third Layer

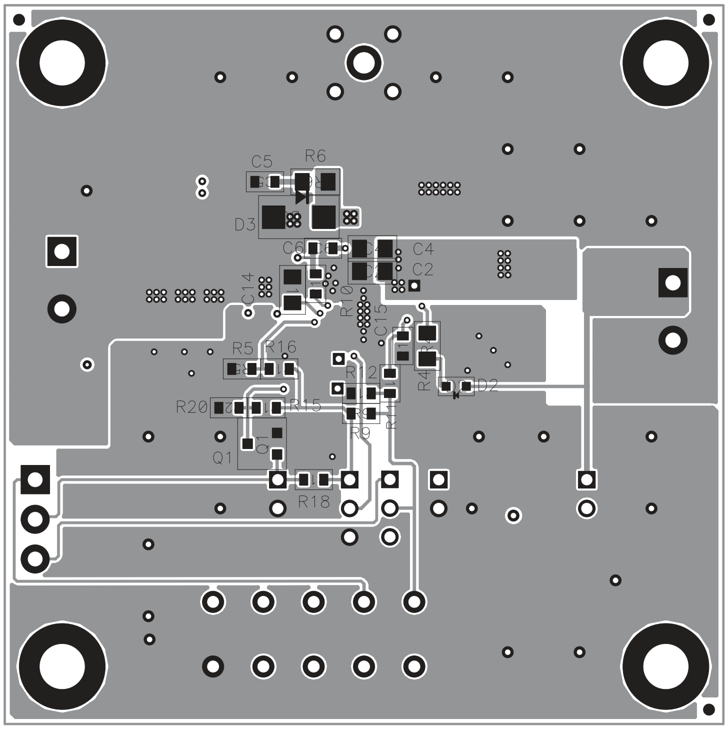

Figure 6. Bottom Assembly

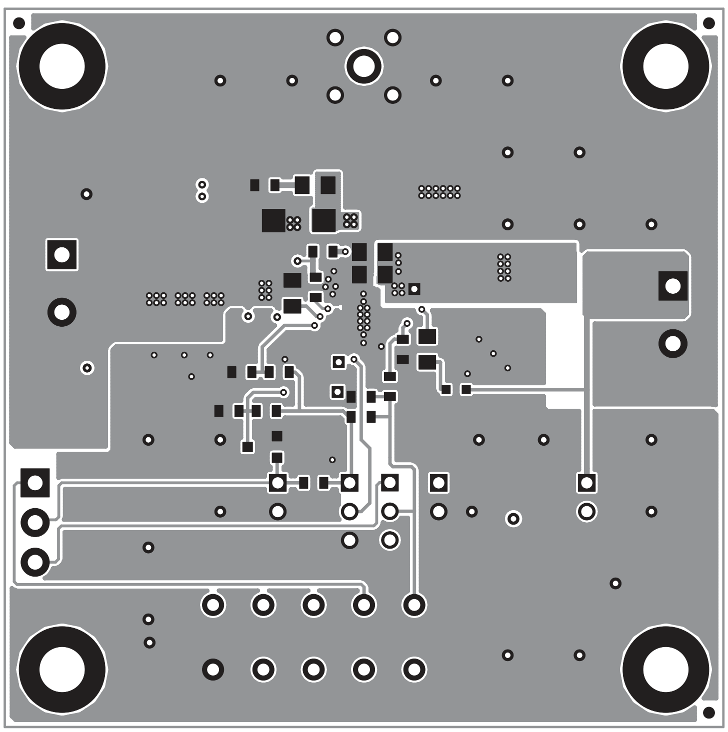

Figure 7. Bottom Layer

4.3 Schematic

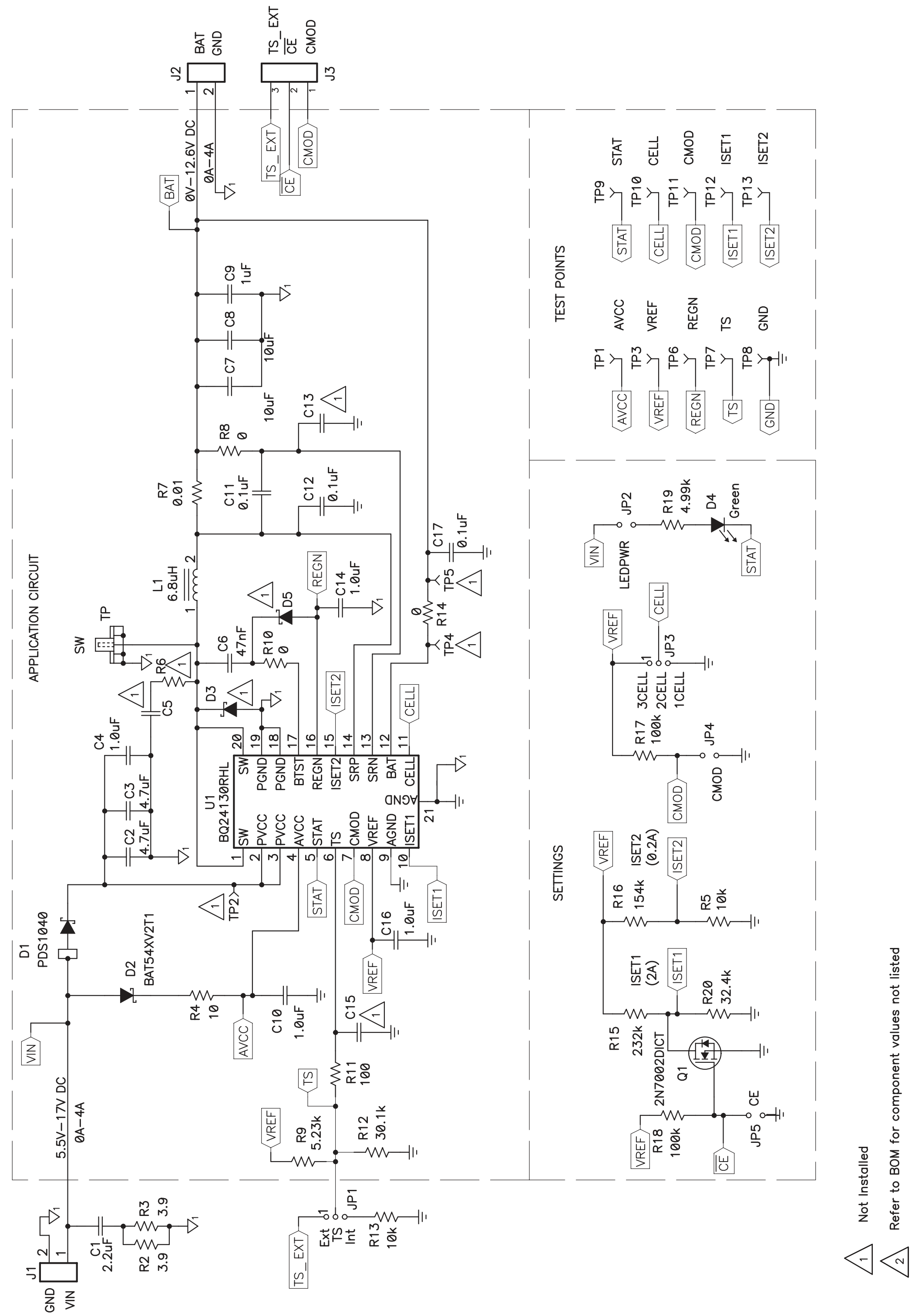

Figure 8. bq24130 EVM Schematic

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 18 V to 22 V and the output voltage range of 0 V to 18 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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RFID	www.ti-rfid.com		
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