NCP4688

Voltage Regulator - Low Noise, LDO Linear

150 mA

The NCP4688 is a CMOS 150 mA LDO linear voltage regulator with high output voltage accuracy which features a low noise output voltage and high ripple rejection. The low level of output noise 10 μVrms typically is kept at any output voltage. The very common SOT23−5 package and small μDFN 1x1 package are suitable for industrial applications, portable communication equipments and RF modules.

Features

- Operating Input Voltage Range: 2 V to 5.25 V
- Output Voltage Range: 1.2 to 4.8 V (available in 0.1 V steps)
- ±1% Output Voltage Accuracy
- Output Noise: 10 μVrms
- Line Regulation: 0.02%/V
- Current Limit Circuit
- High PSRR: 80 dB at 1 kHz, 75 dB at 10 kHz
- Available in SOT−23−5 and μDFN 1.0 x 1.0 mm Package
- These are Pb−Free Devices

Typical Applications

- Home Appliances, Industrial Equipment
- Cable Boxes, Satellite Receivers, Entertainment Systems
- Car Audio Equipment, Navigation Systems
- Notebook Adaptors, LCD TVs, Cordless Phones and Private LAN Systems
- RF Modules

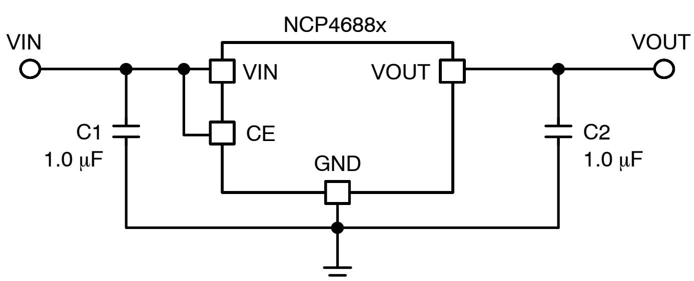
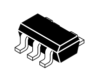


Figure 1. Typical Application Schematic

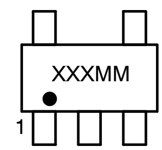
ON Semiconductor™

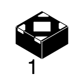
http://onsemi.com

MARKING DIAGRAMS

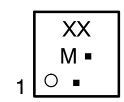


SOT−23−5
CASE 1212





UDFN−4
CASE 517BR



(Top Views)

XX, XXX = Specific Device Code
M, MM = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

October, 2019 − Rev. 1
Publication Order Number:
NCP4688/D

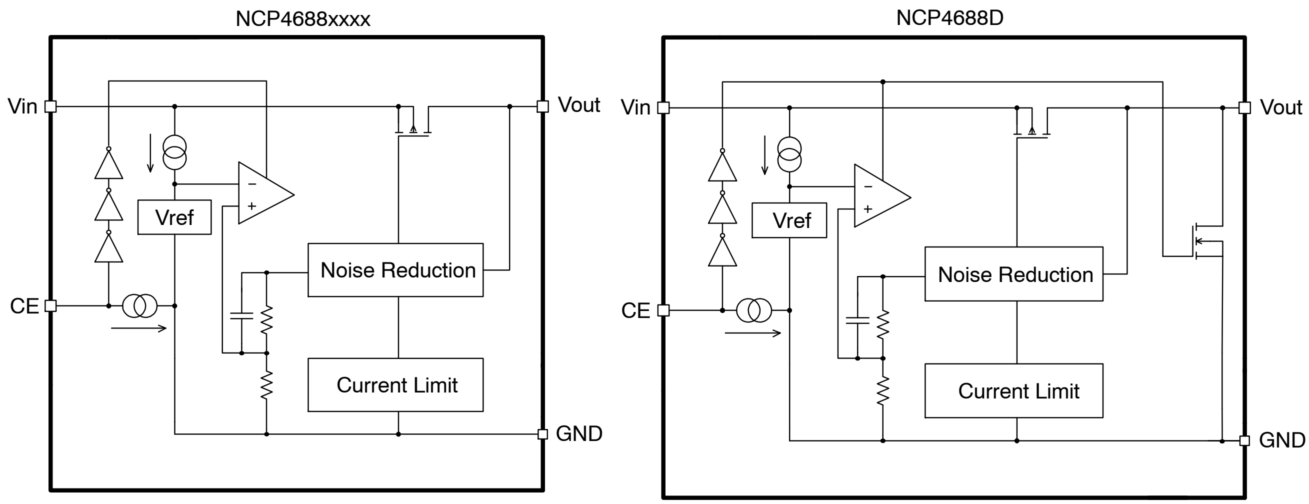


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. SOT−23−5	Pin No. DFN 1x1	Pin Name	Description
1	4	VIN	Input pin
2	2	GND	Ground pin
3	3	CE	Chip enable pin (“H” active)
4		NC	Non connected
5	1	VOUT	Output pin
	*EP	EP	Exposed Pad (leave floating or connect to GND)

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	0 – 6 V	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	0 – 6 V	V
Power Dissipation SOT−23−5	P_D	420	mW
Power Dissipation μDFN 1.0 x 1.0 mm		400	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, μDFN 1x1 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W

Table 4. ELECTRICAL CHARACTERISTICS
(−40°C ≤ T_A ≤ 85°C; C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage	1.2 V < Vout < 4.8 V		V_{IN}	2.0		5.25	V
Output Voltage	Ta = 25°C, Vout > 2.0 V		V_{OUT}	x0.99		x1.01	V
	−40°C < Ta < 85°C, Vout > 2.0 V			x0.985		x1.015	V
	Ta = 25°C, Vout ≤ 2.0 V			−20		+20	mV
	−40°C < Ta < 85°C, Vout ≤ 2.0 V			−30		+30	mV
Output Voltage Temp. Coefficient	−40°C < Ta < 85°C				±100		ppm/°C
Line Regulation	Set Vout + 0.3 < VIN < 5.25 V	Vout > 4.1 V	$Line_{Reg}$		0.02	0.10	%/V
	Set Vout + 0.5 < VIN < 5.0 V	1.7 V ≤ V_{OUT} < 4.1 V					
	2.2 < VIN < 5.0 V	Vout < 1.7 V					
Load Regulation	1 mA < I_{OUT} ≤ 150 mA		$Load_{Reg}$	−14	0	14	mV
Dropout Voltage	I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.3 V	V_{DO}		0.39	0.80	V
		1.3 V ≤ V_{OUT} < 1.4 V			0.37	0.70	
		1.4 V ≤ V_{OUT} ≤ 1.5 V			0.34	0.60	
		1.5 V ≤ V_{OUT} < 1.7 V			0.32	0.50	
		1.7 V ≤ V_{OUT} < 2.0 V			0.29	0.41	
		2.0 V ≤ V_{OUT} < 2.5 V			0.25	0.36	
		2.5 V ≤ V_{OUT} < 2.8 V			0.22	0.31	
		2.8 V ≤ V_{OUT} ≤ 4.8 V			0.20	0.28	
Output Current			I_{OUT}	150			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		40		mA
Quiescent Current	Iout = 0 mA	Vout > 4.1 V	I_Q		80	100	μA
		Vout ≤ 4.1 V			75		
Standby Current	V_{IN} = $V_{IN\ max}$, V_{CE} = 0 V		I_{STB}		0.1	1.0	μA
CE Pin Pull−Down Current			I_{PD}		0.3	0.6	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	1.0		V_{IN}	V
	CE Input Voltage “L”		V_{CEL}			0.4	
Power Supply Rejection Ratio	V_{OUT} > 4.1 V @ V_{IN} = 5.25 V, V_{OUT} ≤ 4.1 V @ V_{IN} = Set V_{OUT} + 1.0 V, ΔV_{IN_PK-PK} = 0.2 V, I_{OUT} = 30 mA	f = 1 kHz	PSRR		80		dB
		f = 10 kHz			75		
		f = 100 kHz			65		
Output Noise Voltage	I_{OUT} = 30 mA, f = 10 Hz to 100 kHz		V_{NOISE}		10		μV_{rms}
Autodischarge NMOS Resistance	V_{IN} = 4.0 V, V_{CE} = 0.0 V		R_{DSON}		60		ohm

TYPICAL CHARACTERISTICS

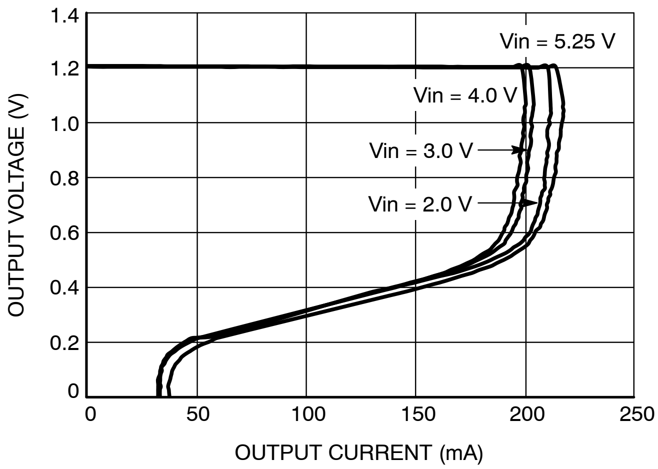


Figure 3. Output Voltage vs. Output Current NCP4688xx12

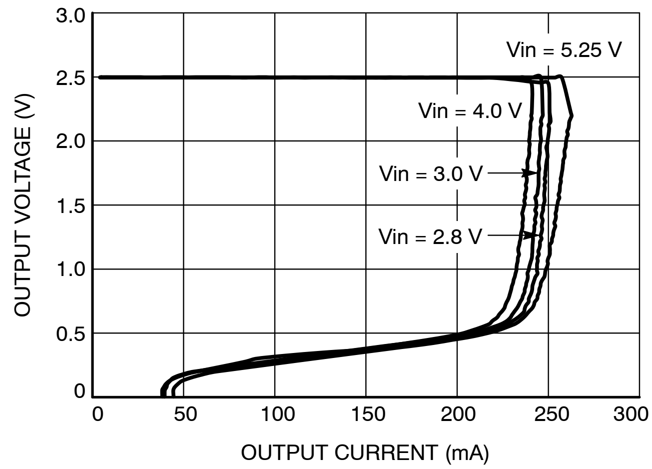


Figure 4. Output Voltage vs. Output Current NCP4688xx25

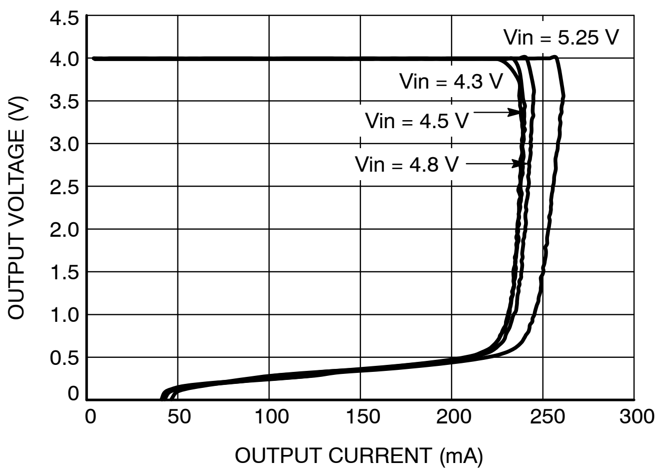


Figure 5. Output Voltage vs. Output Current NCP4688xx40

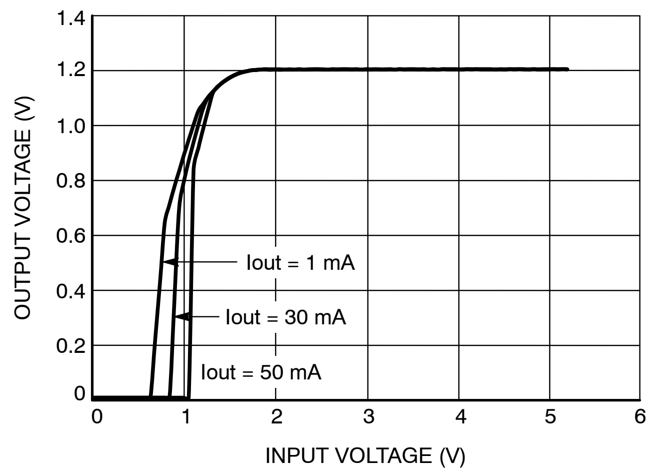


Figure 6. Output Voltage vs. Input Voltage NCP4688xx12

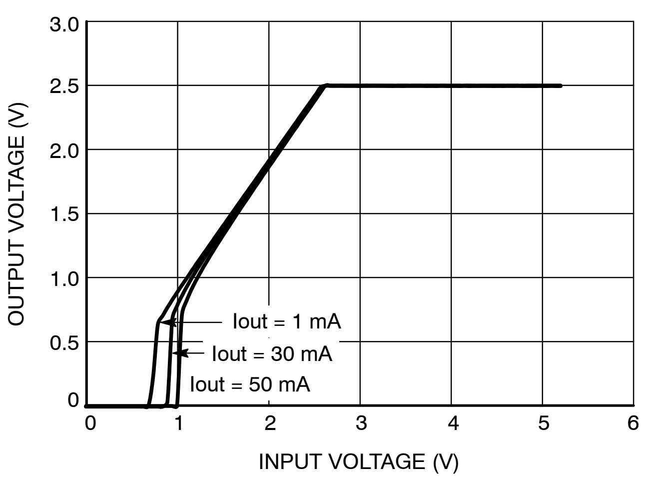


Figure 7. Output Voltage vs. Input Voltage NCP4688xx25

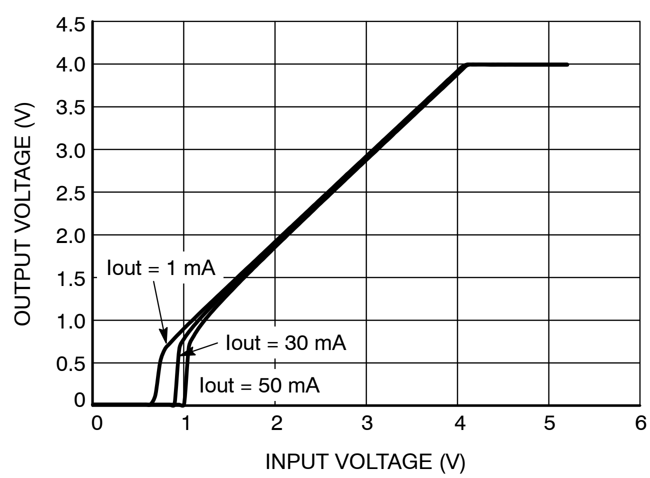


Figure 8. Output Voltage vs. Input Voltage NCP4688xx40

TYPICAL CHARACTERISTICS

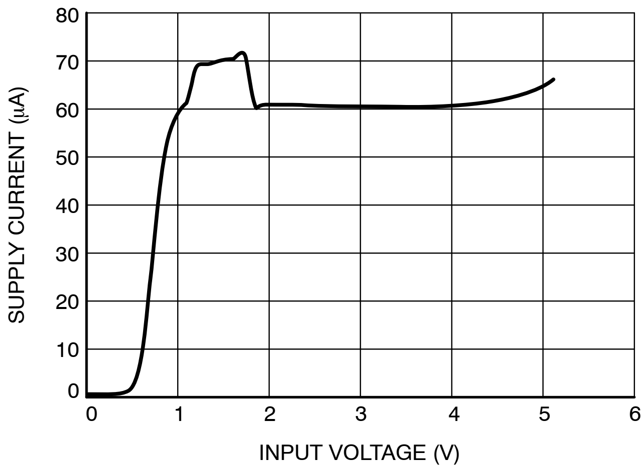


Figure 9. Supply Current vs. Input Voltage NCP4688xx12

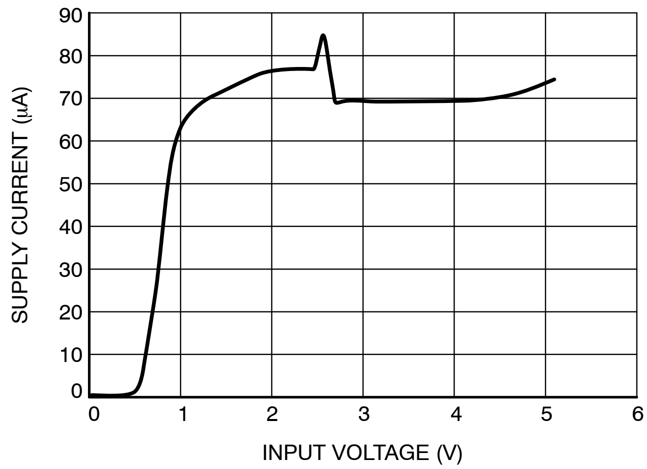


Figure 10. Supply Current vs. Input Voltage NCP4688xx25

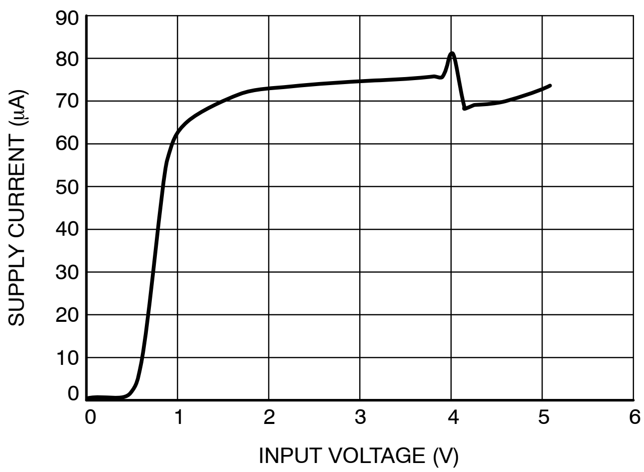


Figure 11. Supply Current vs. Input Voltage NCP4688xx40

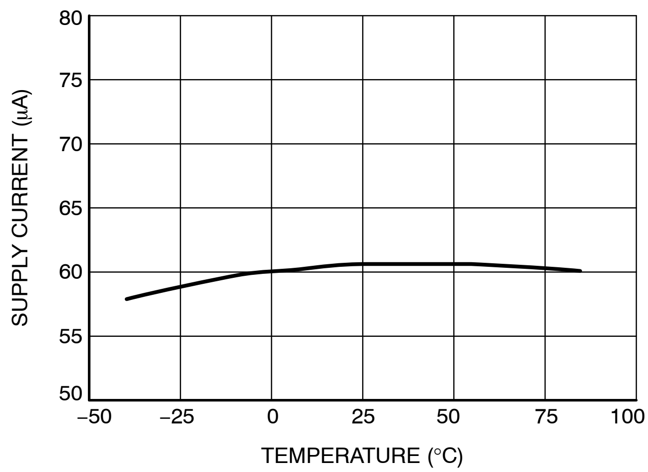


Figure 12. Supply Current vs. Temperature NCP4688xx12

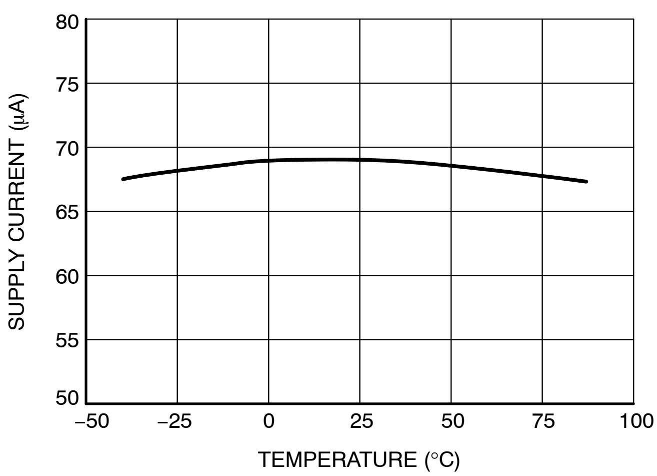


Figure 13. Supply Current vs. Temperature NCP4688xx25

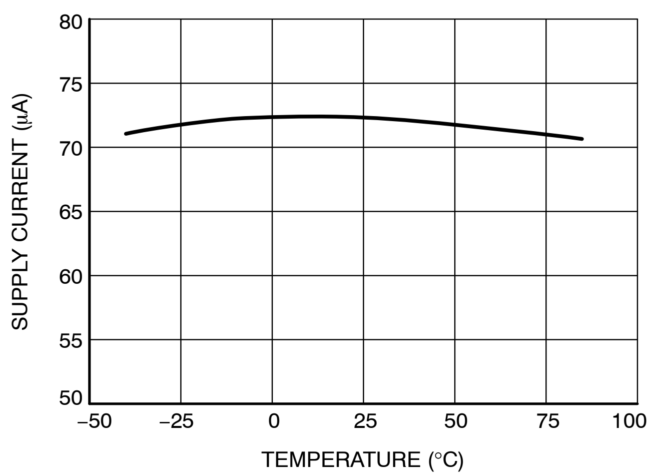


Figure 14. Supply Current vs. Temperature NCP4688xx40

TYPICAL CHARACTERISTICS

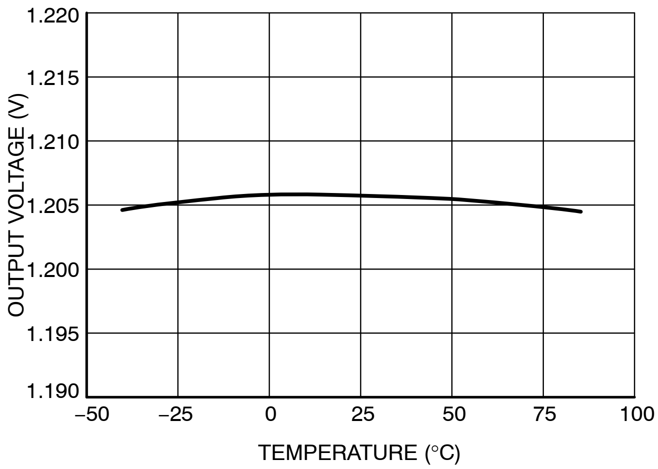


Figure 15. Output Voltage vs. Temperature NCP4688xx12

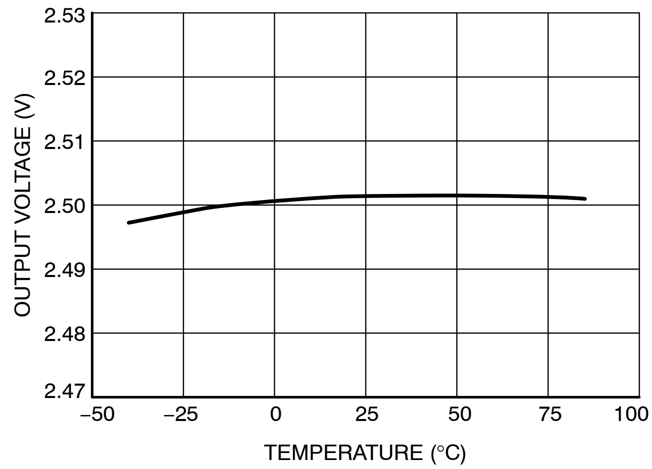


Figure 16. Output Voltage vs. Temperature NCP4688xx25

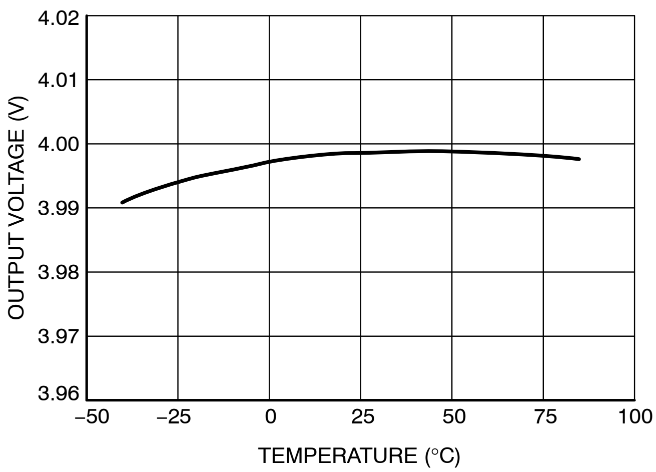


Figure 17. Output Voltage vs. Temperature NCP4688xx40

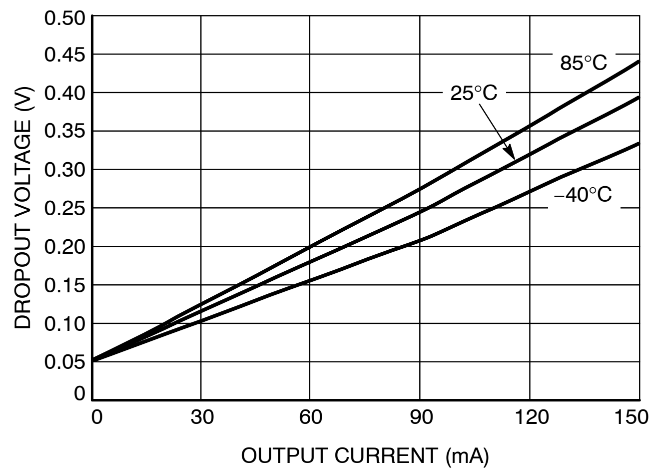


Figure 18. Dropout Voltage vs. Output Current NCP4688xx12

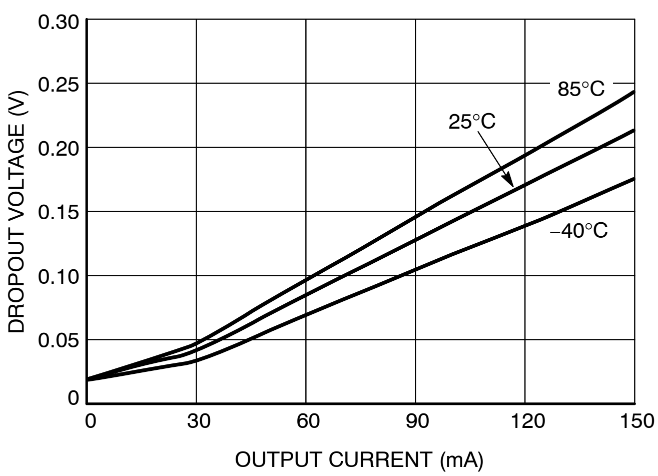


Figure 19. Dropout Voltage vs. Output Current NCP4688xx25

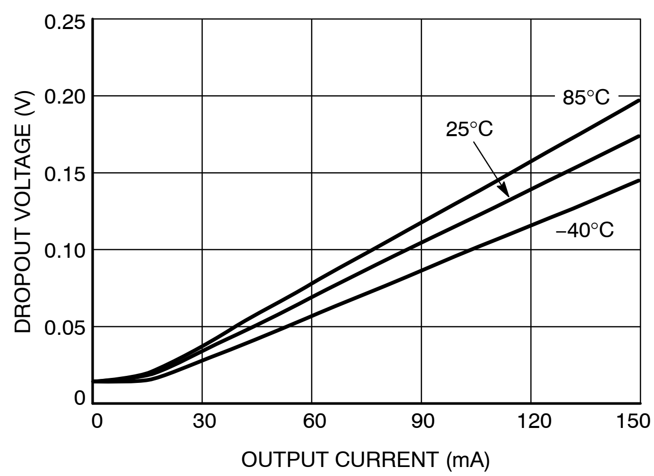


Figure 20. Dropout Voltage vs. Output Current NCP4688xx40

TYPICAL CHARACTERISTICS

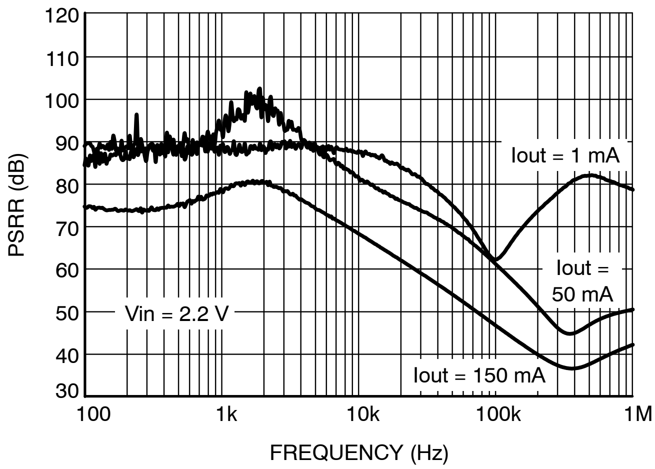


Figure 21. PSRR vs. Frequency NCP4688xx12

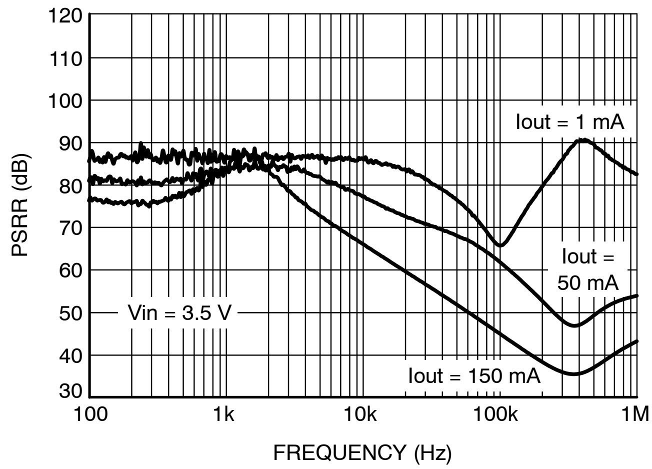


Figure 22. PSRR vs. Frequency NCP4688xx25

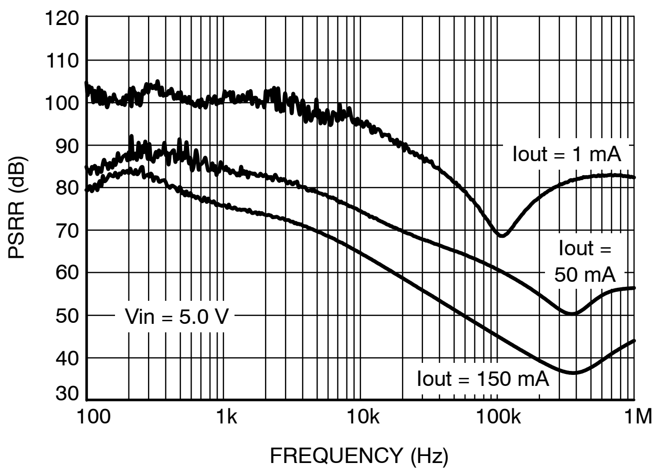


Figure 23. PSRR vs. Frequency NCP4688xx40

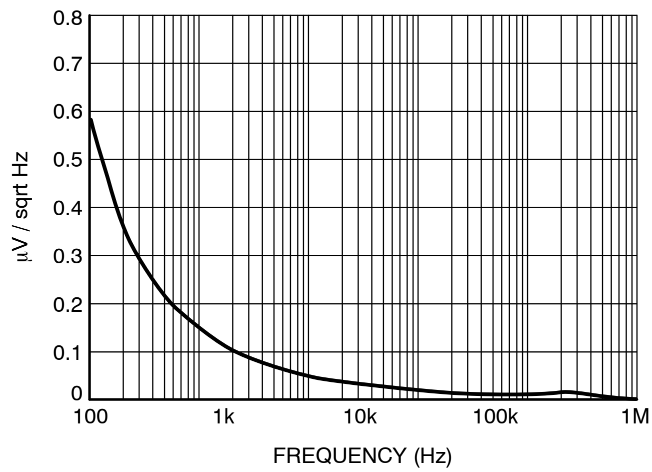


Figure 24. Output Noise Density vs. Frequency NCP4688xx12

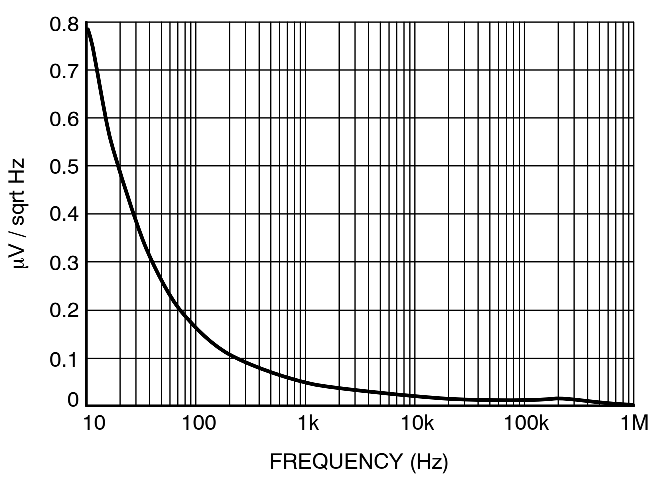


Figure 25. Output Noise Density vs. Frequency NCP4688xx25

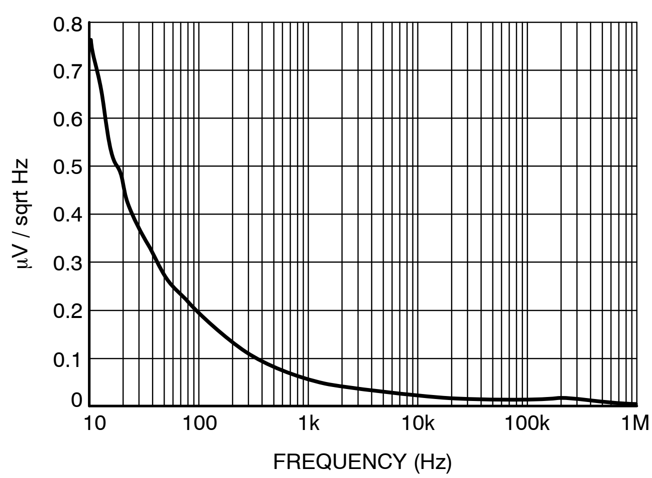


Figure 26. Output Noise Density vs. Frequency NCP4688xx40

TYPICAL CHARACTERISTICS

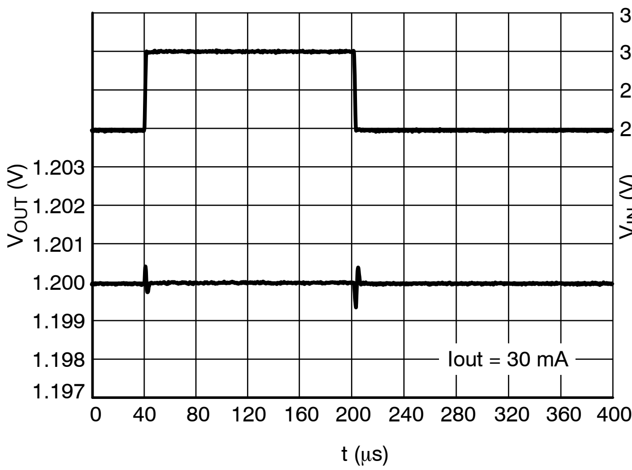


Figure 27. Line Transient Response NCP4688xx12

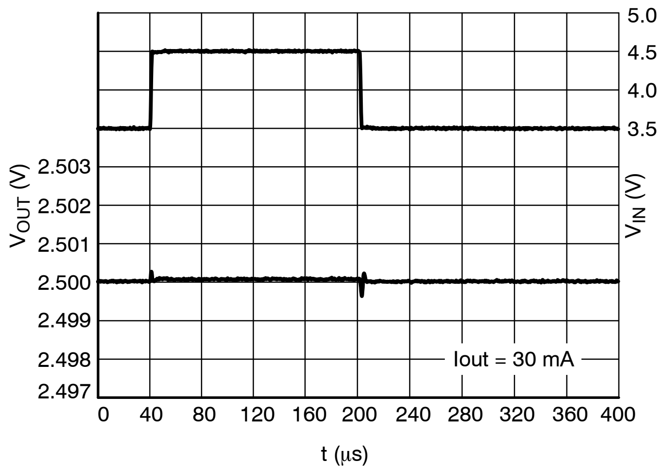


Figure 28. Line Transient Response NCP4688xx25

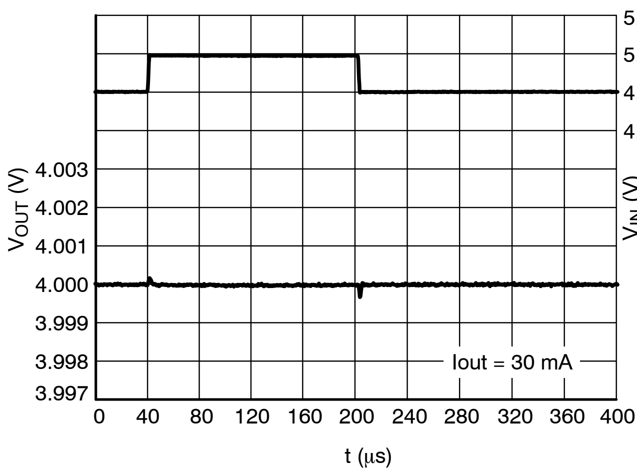


Figure 29. Line Transient Response NCP4688xx40

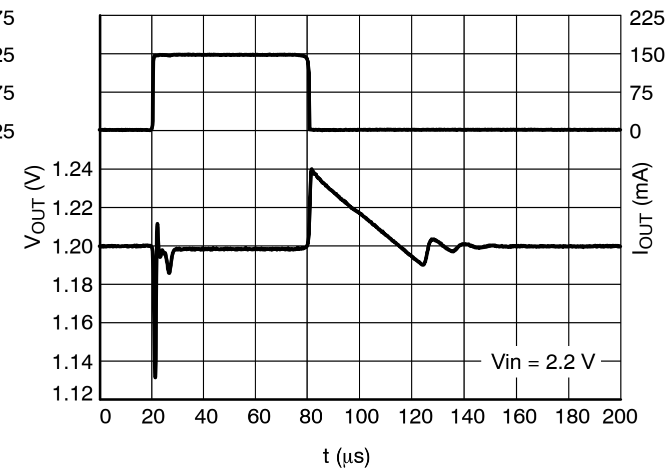


Figure 30. Load Transient Response Load Step 1 mA to 150 mA NCP4688xx12

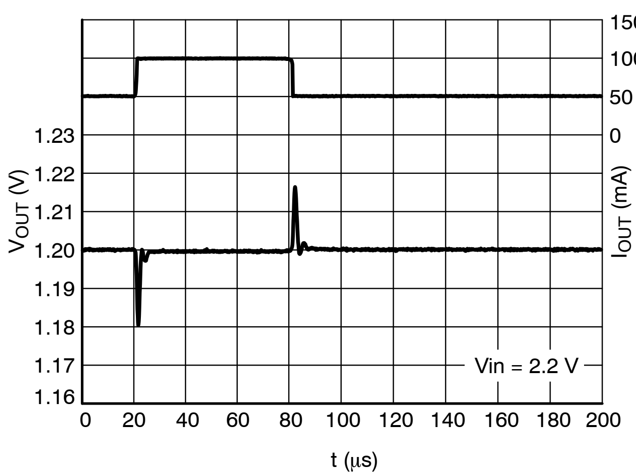


Figure 31. Load Transient Response Load Step 50 mA to 100 mA NCP4688xx12

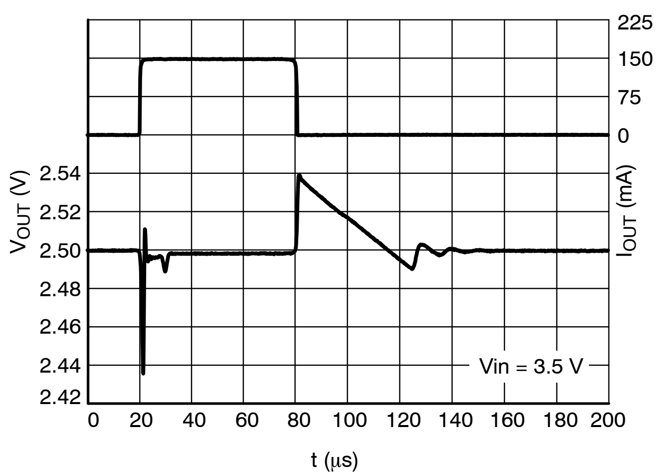


Figure 32. Load Transient Response Load Step 1 mA to 150 mA NCP4688xx25

TYPICAL CHARACTERISTICS

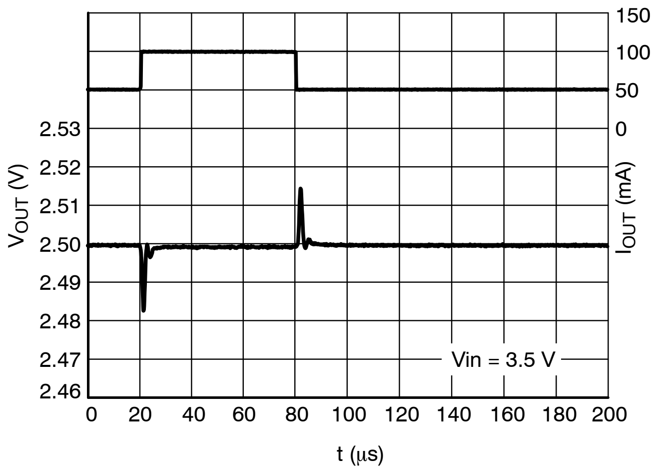


Figure 33. Load Transient Response Load Step 50 mA to 100 mA NCP4688xx25

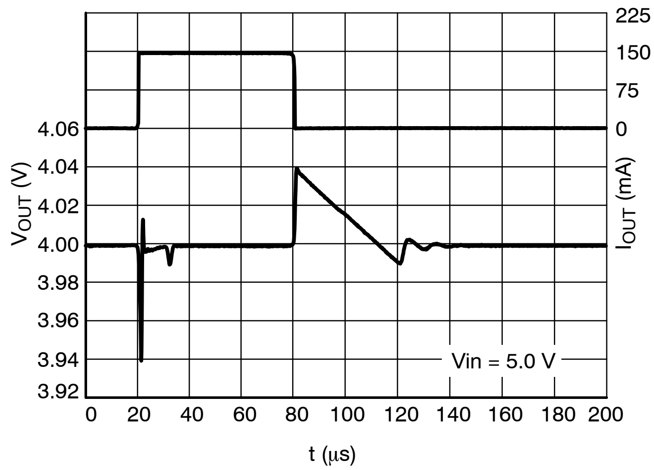


Figure 34. Load Transient Response Load Step 1 mA to 150 mA NCP4688xx40

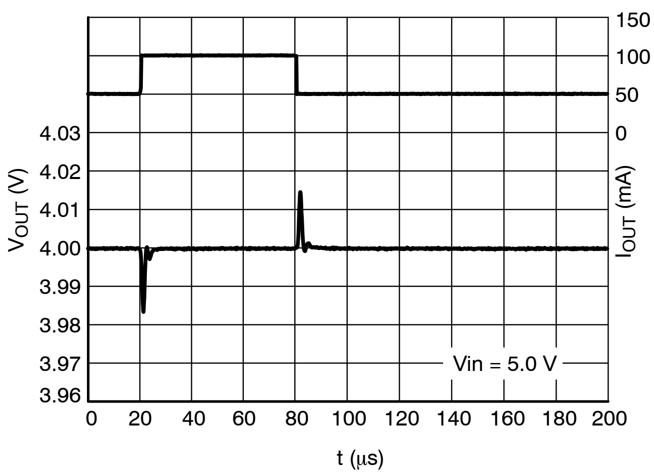


Figure 35. Load Transient Response Load Step 50 mA to 100 mA NCP4688xx40

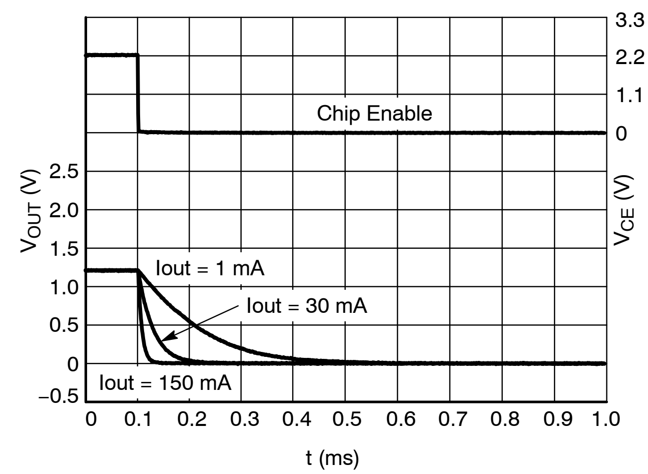


Figure 36. Turn Off with CE Behavior NCP4688Dx12

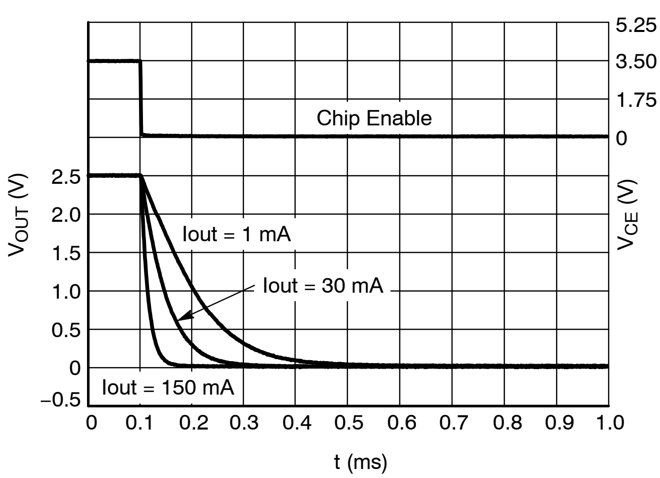


Figure 37. Turn Off with CE Behavior NCP4688Dx25

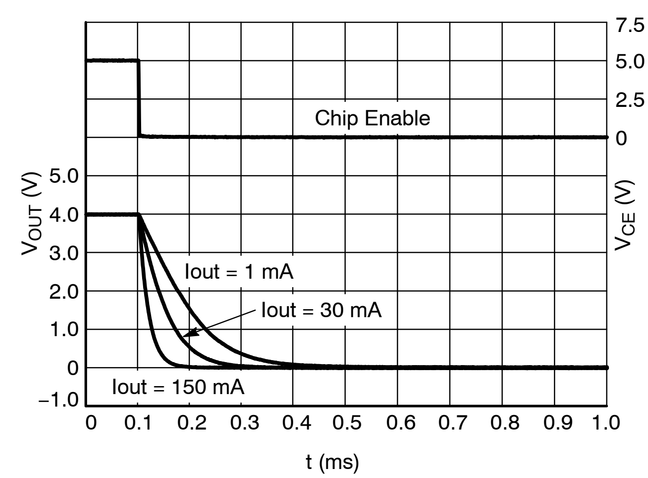


Figure 38. Turn Off with CE Behavior NCP4688Dx40

TYPICAL CHARACTERISTICS

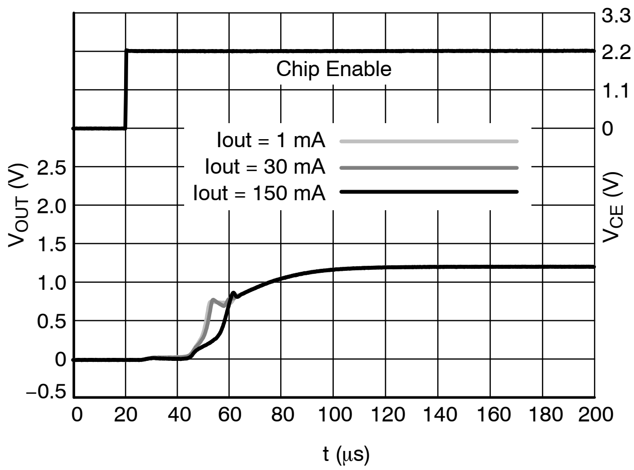


Figure 39. Turn ON with CE Behavior NCP4688xx12

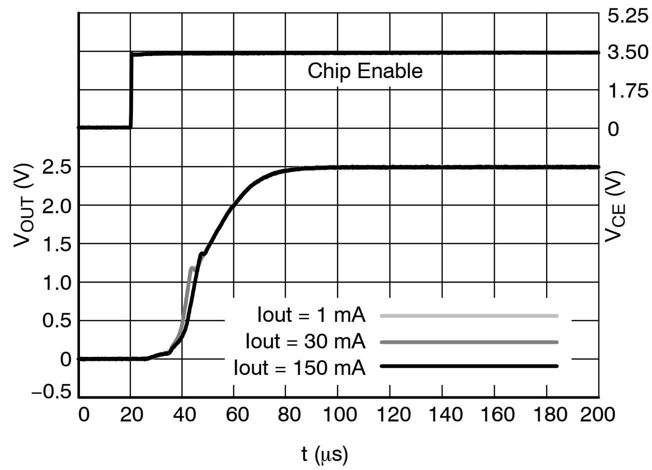


Figure 40. Turn ON with CE Behavior NCP4688xx25

APPLICATION INFORMATION

A typical application circuit for NCP4688 series is shown in the Figure 41.

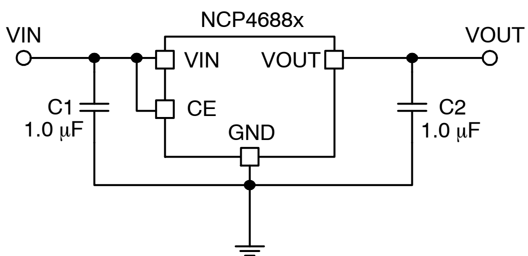


Figure 41. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1.0 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4688 device. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1.0 μF ceramic output decoupling capacitor is sufficient to achieve stable operation of the device. If tantalum capacitor is used, and its ESR is high, the loop oscillation may result. For information about ESR see Figures 42, 43 and 44. The capacitor should be connected as close as possible to the output and ground pin. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source which assure off state of LDO in case the CE pin will stay floating. If the enable function is not needed connect CE pin to V_{IN}.

The D version of the NCP4688 device includes a transistor between V_{OUT} and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal Consideration

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

ESR vs. Output Current

When using the NCP4688 devices, consider the following points:

The relation between Output Current Iout and ESR of the output capacitor are shown below in Figures 42, 43 and 44. The conditions when the device performs stable operation are marked as the hatched area in the charts.

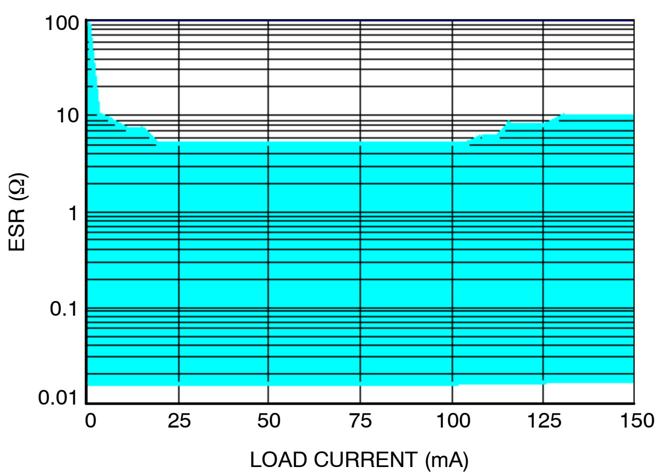


Figure 42. ESR vs. Load Current NCP4688xx12

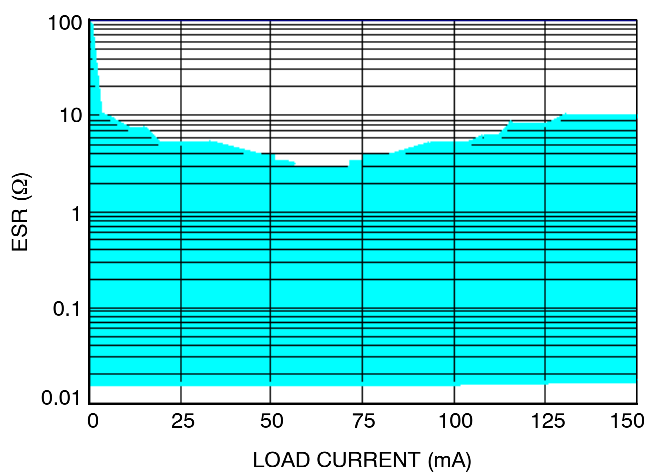


Figure 43. ESR vs. Load Current NCP4688xx25

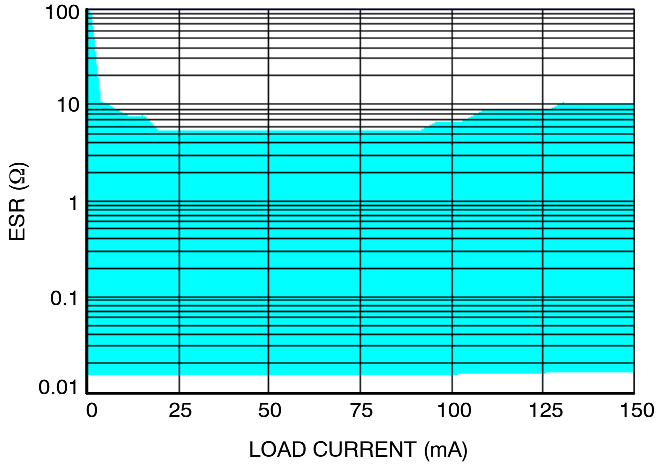
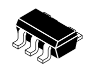


Figure 44. ESR vs. Load Current NCP4688xx40

ORDERING INFORMATION

Device	Marking	Nominal Output Voltage	Feature	Package	Shipping†
NCP4688DMU12TCG	3A	1.2 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU15TCG	3E	1.5 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU18TCG	3H	1.8 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU25TCG	3R	2.5 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU28TCG	3U	2.8 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU30TCG	3X	3.0 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DMU33TCG	4A	3.3 V	Auto discharge	DFN1010 (Pb−Free)	10000 / Tape & Reel
NCP4688DSN12T1G	L12	1.2 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4688DSN15T1G	L15	1.5 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4688DSN18T1G	L18	1.8 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4688DSN25T1G	L25	2.5 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4688DSN28T1G	L28	2.8 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel
NCP4688DSN33T1G	L33	3.3 V	Auto discharge	SOT−23 (Pb−Free)	3000 / Tape & Reel

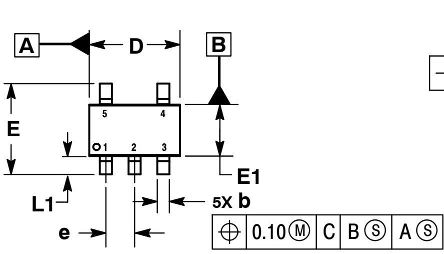
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

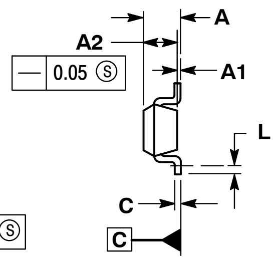


SCALE 2:1

SOT−23 5−LEAD
CASE 1212−01
ISSUE A

DATE 28 JAN 2011

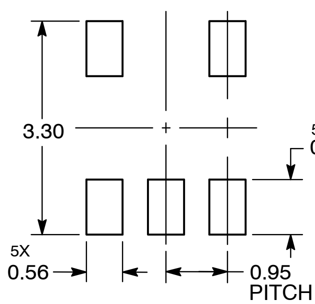




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

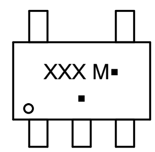
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	SOT−23 5−LEAD	PAGE 1 OF 1

MECHANICAL CASE OUTLINE

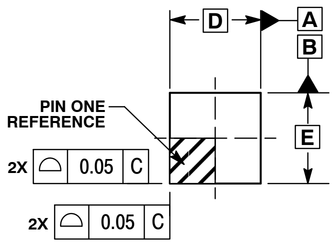
PACKAGE DIMENSIONS

ON Semiconductor®

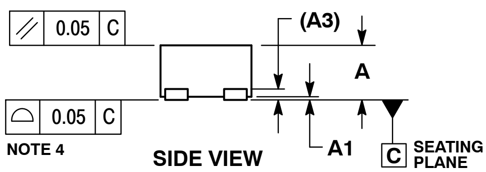
SCALE 4:1

UDFN4 1.0x1.0, 0.65P
CASE 517BR−01
ISSUE O

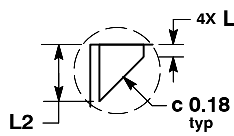
DATE 27 OCT 2010



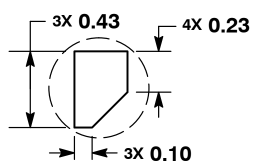
TOP VIEW



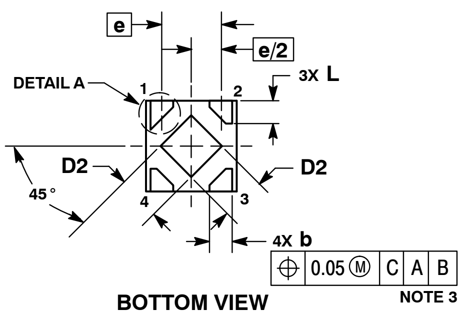
SIDE VIEW



DETAIL A



DETAIL B

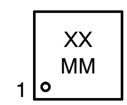


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.00	0.05
A3	0.10 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37
L3	0.02	0.12

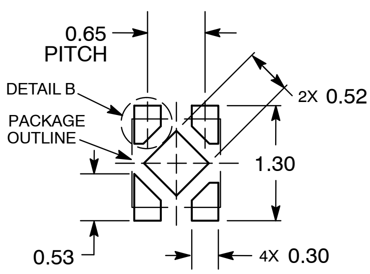
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
MM = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN4, 1.0X1.0, 0.65P	PAGE 1 OF 1

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