Low $V_{CE(sat)}$ NPN Transistors, 60 V, 1 A

NSS60101DMR6

ON Semiconductor's e[2]PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and LED lightning, power management…etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e[2]PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	60	Vdc
Collector−Base Voltage	V_{CBO}	80	Vdc
Emitter−Base Voltage	V_{EBO}	6	Vdc
Collector Current − Continuous	I_C	1	A
Collector Current − Peak	I_{CM}	2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Ambient (Notes 1 and 2)	$R_{\theta JA}$	234	°C/W
Total Power Dissipation per Package @ T_A = 25°C (Note 2)	P_D	0.53	W
Thermal Resistance Junction−to−Ambient (Note 3)	$R_{\theta JA}$	300	°C/W
Power Dissipation per Transistor @ T_A = 25°C (Note 3)	P_D	0.40	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Dual Operation).
2. P_D per Transistor when both are turned on is one half of Total P_D or 0.53 Watts.
3. Per JESD51−7 with 100 mm² pad area and 2 oz. Cu (Single−Operation).

ON Semiconductor®

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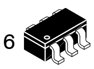
60 Volt, 1 Amp
NPN Low $V_{CE(sat)}$ Transistors

MARKING DIAGRAM



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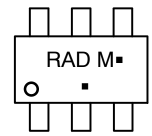
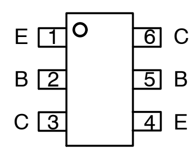
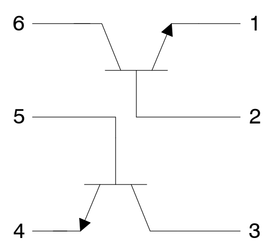
CASE 318F



RAD = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS





ORDERING INFORMATION

Device	Package	Shipping†
NSS60101DMR6T1G	SC−74 (Pb−Free)	3000/Tape & Reel
NSS60101DMR6T2G		
NSV60101DMR6T1G		
NSV60101DMR6T2G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	$V_{(BR)CEO}$	60			V
Collector−Base Breakdown Voltage (Ic = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	80			V
Emitter−Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	6			V
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)	I_{CBO}			100	nA
Emitter Cutoff Current (V_{BE} = 5.0 V)	I_{EBO}			100	nA
ON CHARACTERISTICS					
DC Current Gain (Note 4)	h_{FE}				
(I_C = 100 mA, V_{CE} = 2 V)		200	320		
(I_C = 500 mA, V_{CE} = 2 V)		150	290		
(I_C = 1 A, V_{CE} = 2 V)		70	110		
(I_C = 1 mA, V_{CE} = 5 V)		250	335		
(I_C = 100 mA, V_{CE} = 5 V)		250	335		
(I_C = 500 mA, V_{CE} = 5 V)		200	310		
(I_C = 1 A, V_{CE} = 5 V)		100	295		
Collector−Emitter Saturation Voltage (Note 4)	$V_{CE(sat)}$				V
(I_C = 100 mA, I_B = 1 mA)			0.080	0.200	
(I_C = 500 mA, I_B = 50 mA)			0.078	0.150	
(I_C = 1 A, I_B = 50 mA)			0.170	0.250	
(I_C = 1 A, I_B = 100 mA)			0.143	0.200	
Base − Emitter Saturation Voltage (Note 4)	$V_{BE(sat)}$				V
(I_C = 500 mA, I_B = 50 mA)			0.87	1.50	
(I_C = 1 A, I_B = 50 mA)			0.91	1.50	
(I_C = 1 A, I_B = 100 mA)			0.94	1.60	
Base−Emitter Turn−on Voltage (Note 4)	$V_{BE(on)}$				V
(I_C = 1 mA, V_{CE} = 1 V)		0.27	0.57		
(I_C = 500 mA, V_{CE} = 2 V)			0.76	0.90	
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{EB} = 1 V, f = 1.0 MHz)	C_{ibo}		100		pF
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	C_{obo}		8.0		pF
Cutoff Frequency (I_C = 50 mA, V_{CE} = 2.0 V, f = 100 MHz)	f_T		200		MHz
SWITCHING TIMES					
Delay Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_d		10		ns
ON Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_{on}		28		ns
Rise Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_r		18		ns
Storage Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_s		622		ns
OFF Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_{off}		709		ns
Fall Time (V_{CC} = 10 V, I_C = 0.5 A, I_{B1} = 25 mA, I_{B2} = −25 mA)	t_f		87		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

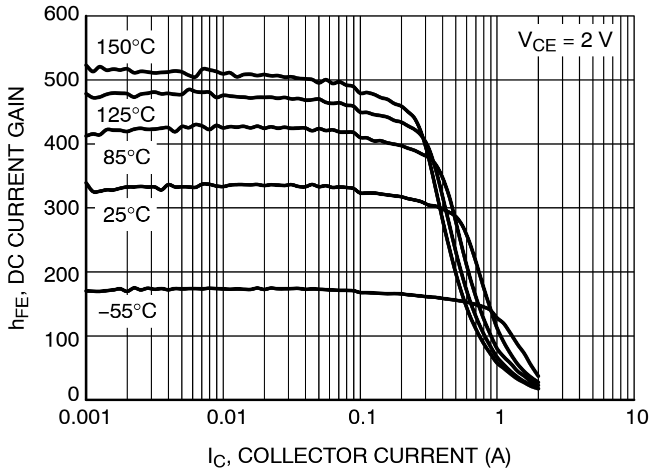


Figure 1. DC Current Gain

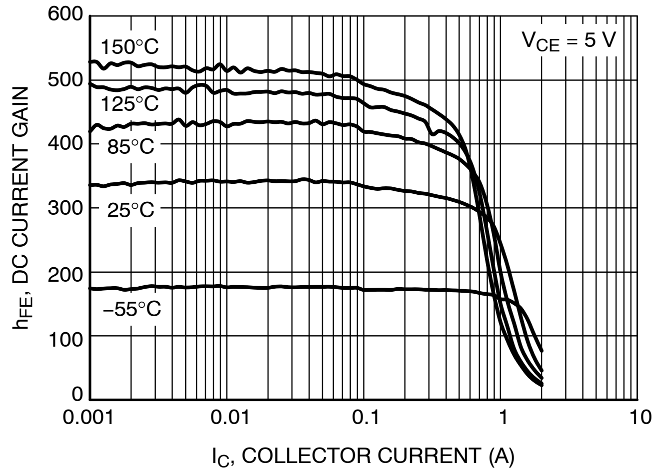


Figure 2. DC Current Gain

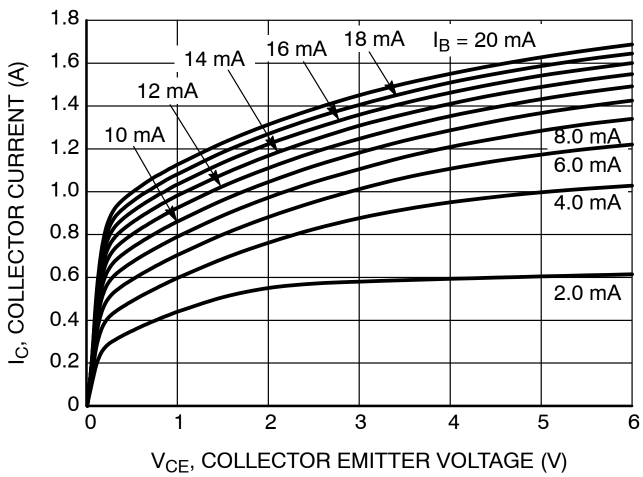


Figure 3. Collector Current as a Function of Collector Emitter Voltage

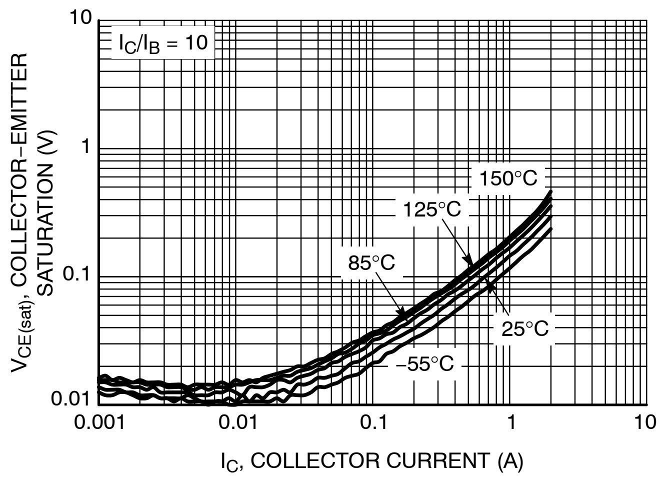


Figure 4. Collector−Emitter Saturation Voltage

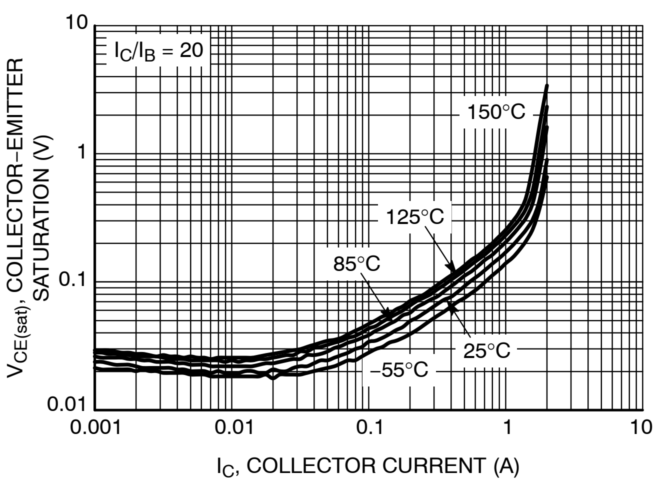


Figure 5. Collector−Emitter Saturation Voltage

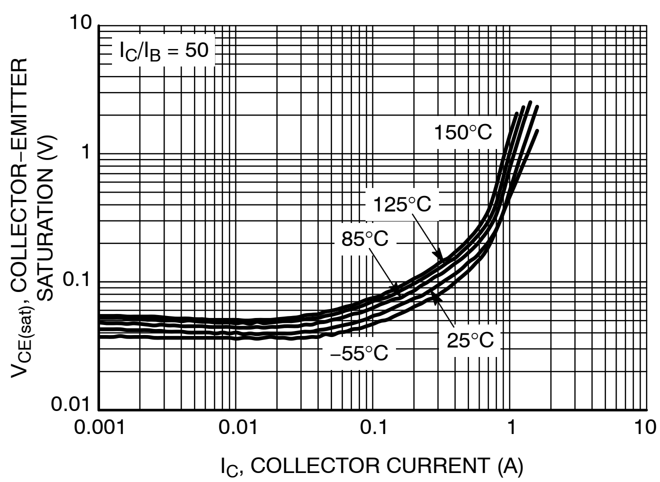


Figure 6. Collector−Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

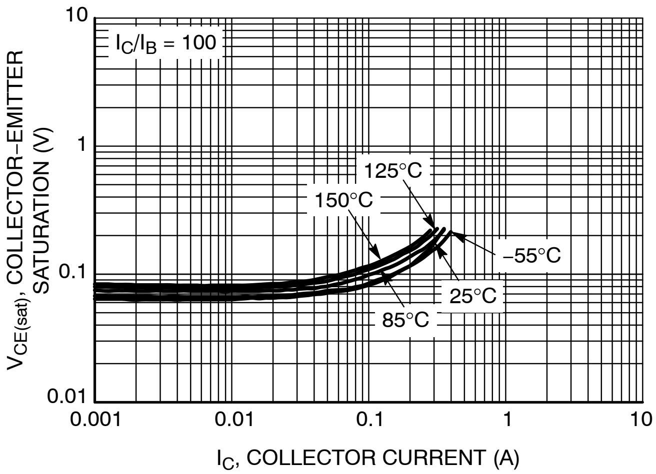


Figure 7. Collector−Emitter Saturation Voltage

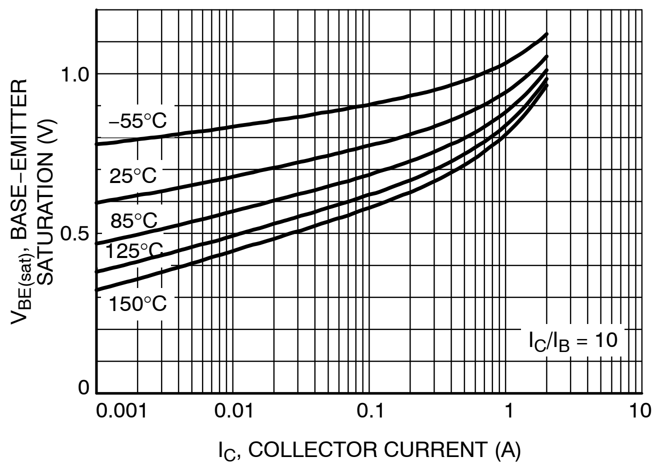


Figure 8. Base−Emitter Saturation Voltage

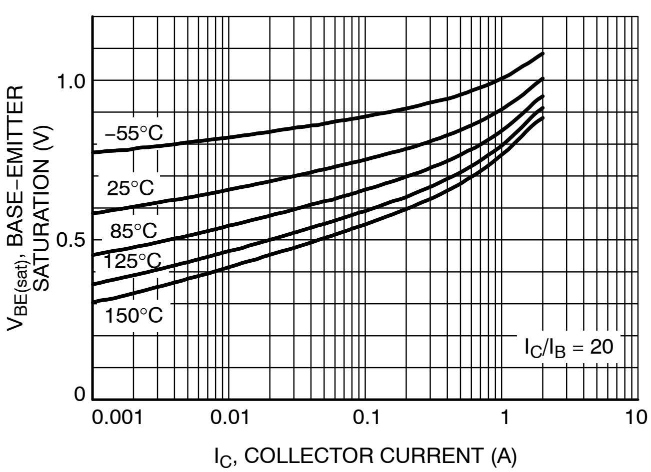


Figure 9. Base−Emitter Saturation Voltage

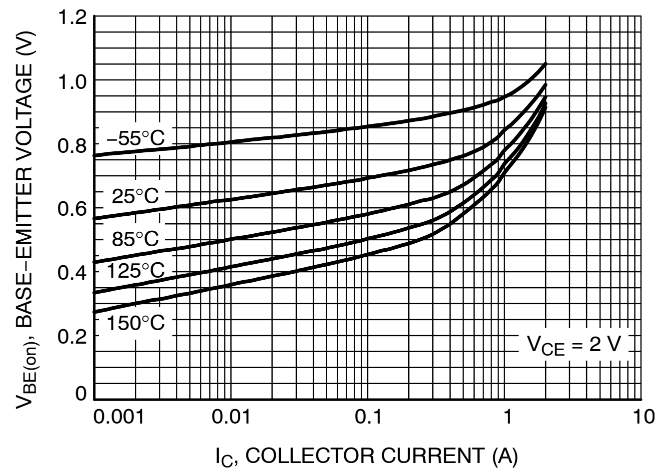


Figure 10. Base−Emitter "ON" Voltage

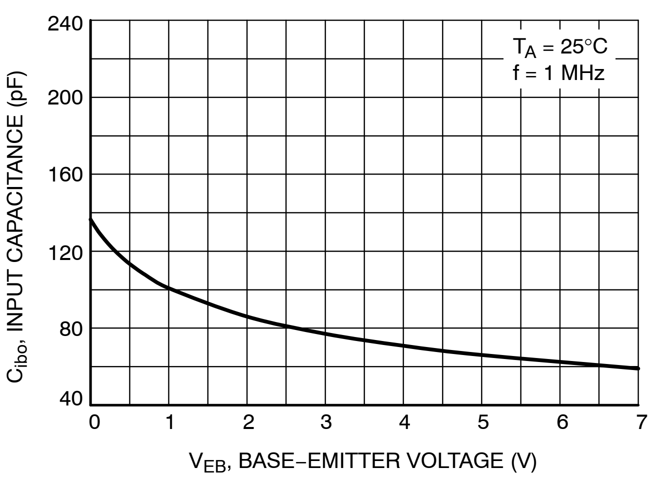


Figure 11. Input Capacitance

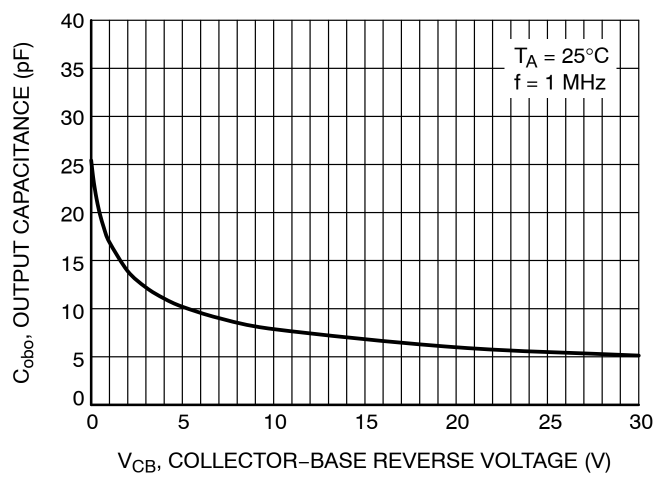


Figure 12. Output Capacitance

TYPICAL CHARACTERISTICS

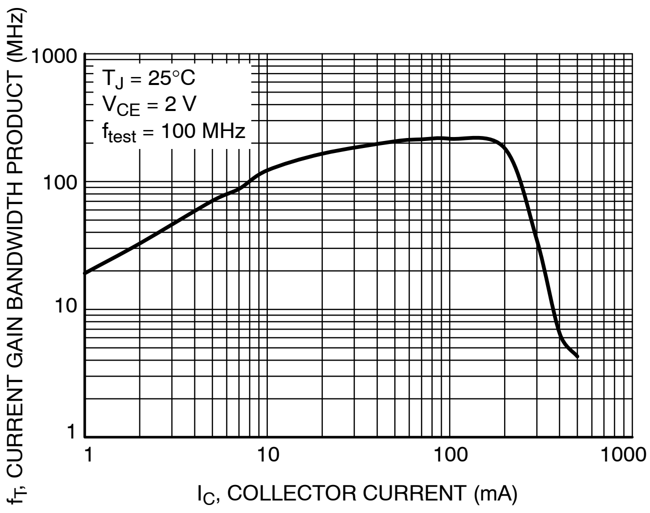


Figure 13. f_T, Current Gain Bandwidth Product

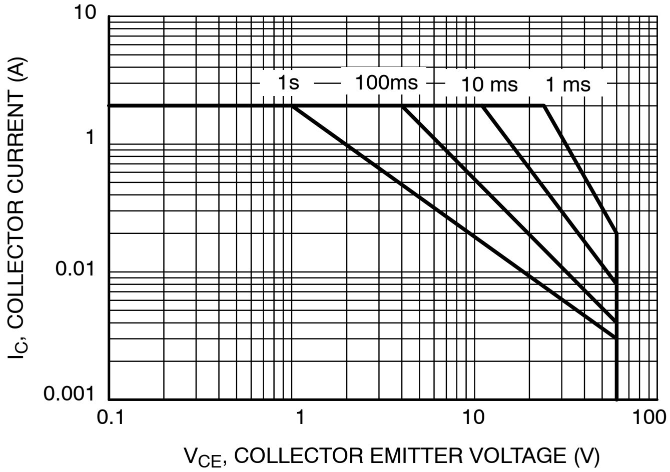


Figure 16. Safe Operating Area (T_A = 25°C)

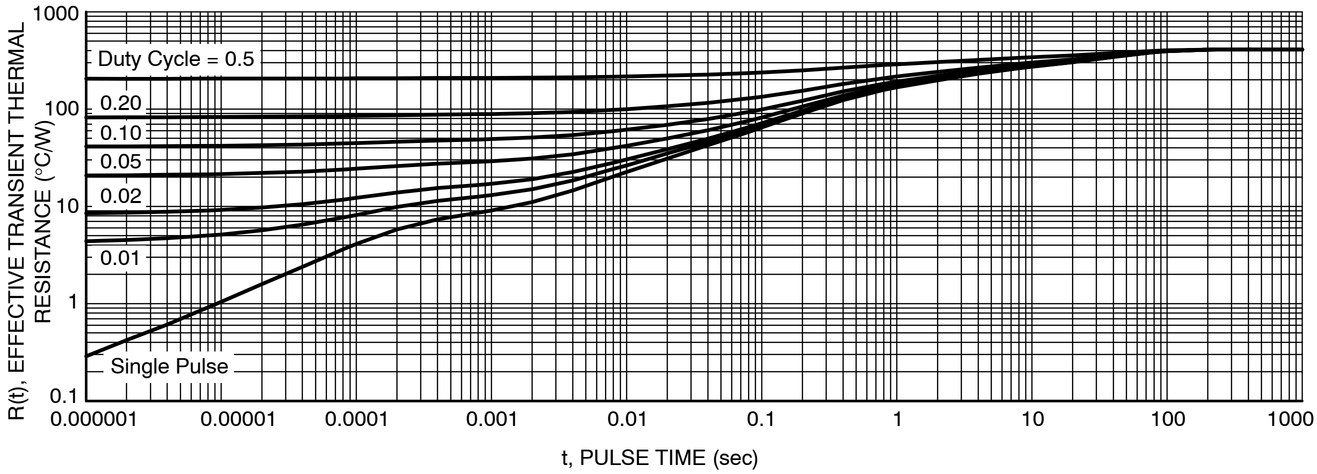


Figure 14. Thermal Resistance by Transistor

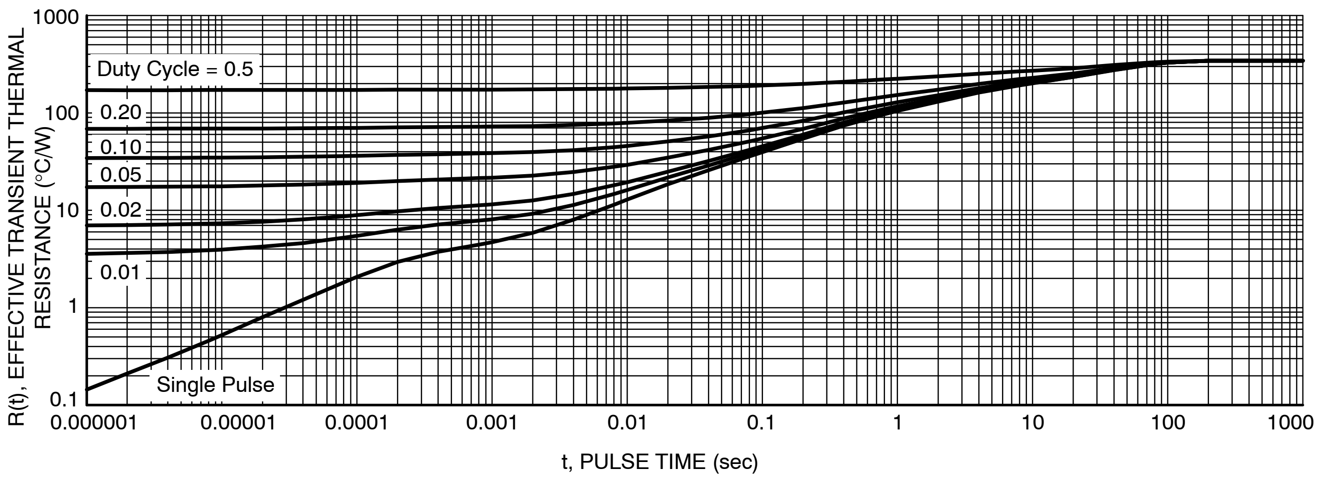
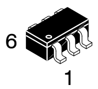


Figure 15. Thermal Resistance for Both Transistors



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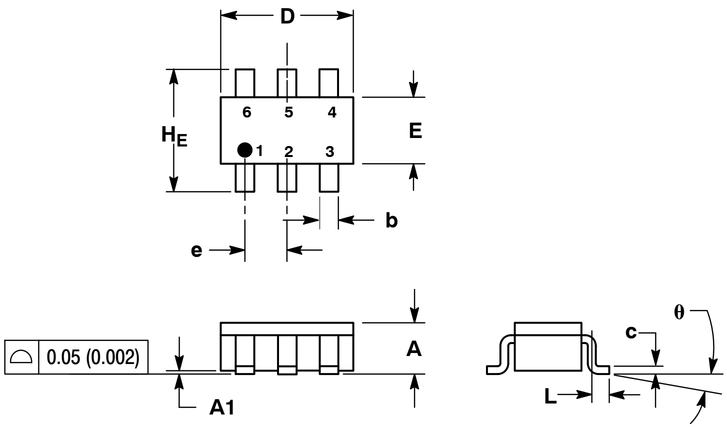
CASE 318F−05
ISSUE N

DATE 08 JUN 2012

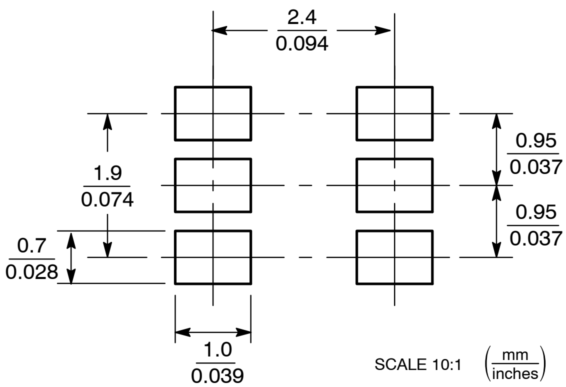
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

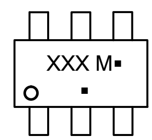
	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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