

TRX_024_046

24-GHz Highly Integrated IQ Transceiver

Data Sheet

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Version Control

Version	Changed section	Description of change	Reason for change
1.0	All	Document creation	
1.1	7 Measurement Results	Update, diagrams added	New measurements results available
1.2	4.4 Electrical Chars	Gain low gain mode: 'Max' value corrected and associated conditions enhanced (Note 3)	Necessary correction
1.3	4.4 Electrical Chars 7 Measurement Results	Divider output power: 'Max' value corrected Gain high gain mode: 'Max' value corrected Fig. 14, 15 "Linearity of receiver..." corrected Fig. 23, 24: Curves with measurement temperature > operational Ta.max removed	Necessary correction

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1 Features

- Radar transceiver for 24-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 300 mW in continuous operating mode
- Transmitter with power control in two steps
- Receiver with homodyne quadrature mixers
- Low-noise amplifier (LNA) with gain control
- Integrated low phase noise VCO
- Single ended TX output
- Single ended RX input
- QFN20 leadless plastic package 3 × 3 mm²
- Pb-free, RoHS compliant package
- Replaces the obsolete TRX_024_006



1.1 Overview

The IC is an integrated transceiver circuit for the 24-GHz ISM band and general ultra-wide band applications. It includes a low-noise amplifier (LNA) with gain control, quadrature mixers, a poly-phase filter, a voltage controlled oscillator with band switching and a divide-by-32 circuit. The transmitter can be powered down if TX_EN pin is supplied with 0V. The gain of the receiver can be digitally controlled by Vct pin: Vct = 3.3 V sets the receiver in high gain mode, Vct = 0V sets the receiver in low gain mode. The output power of the transmitter can be controlled by the pwr1 input. The IC is fabricated in SiGe BiCMOS technology.

1.2 Applications

The TRX_024_046 can be used in radar systems and in wireless communication systems for the 24-GHz ISM band (24.0 GHz to 24.25 GHz), for level probing radar application (24.05 GHz to 26.5 GHz), and for general ultra-wide band applications between 23 GHz and 26 GHz.

2 Block Diagram

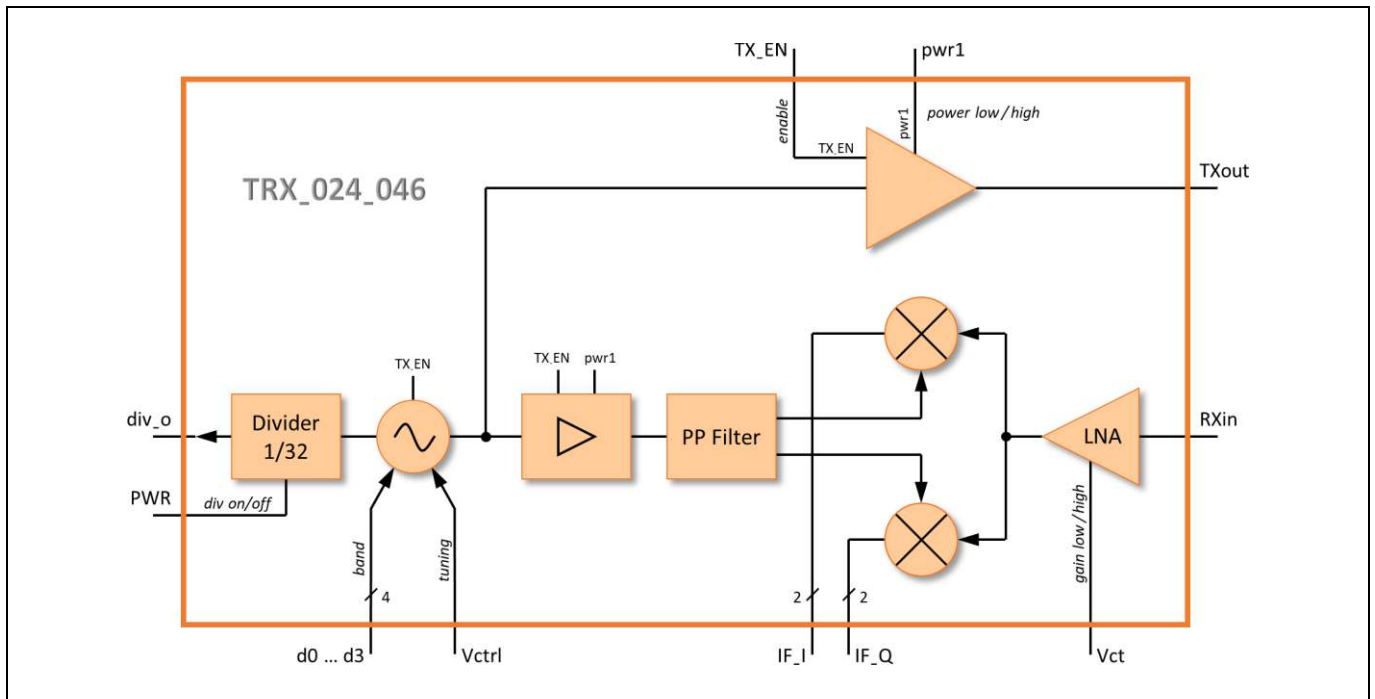


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

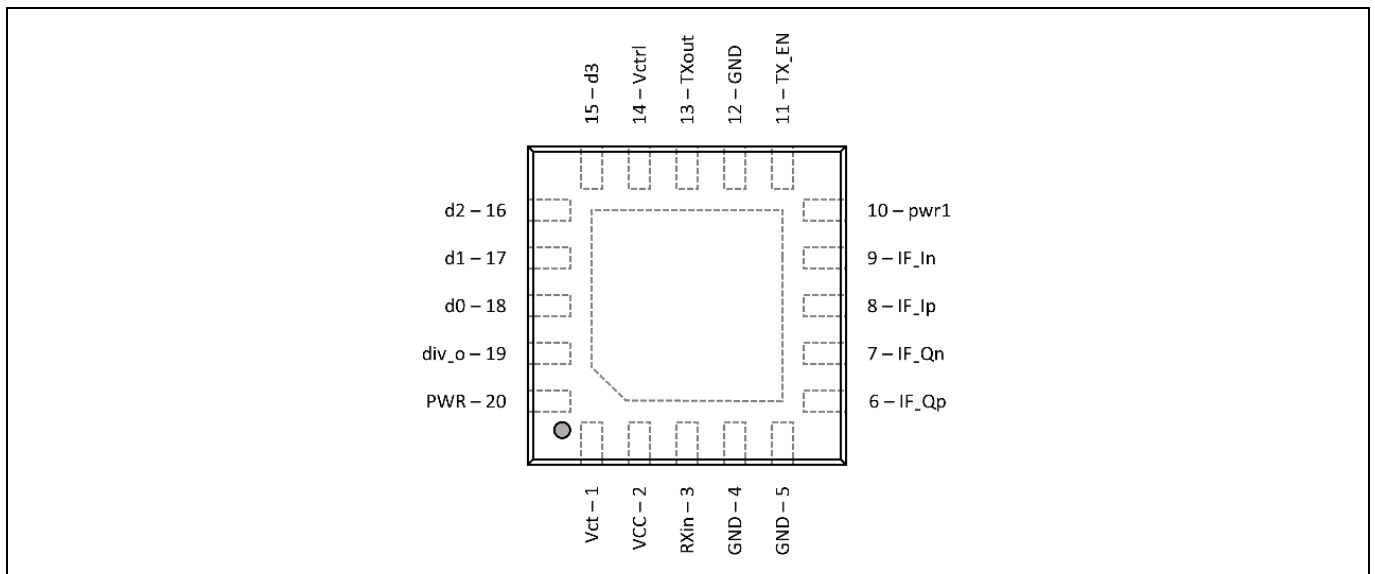


Figure 2 Pin Assignment (QFN20, Top View)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1	Vct	LNA gain control input: 3.3 V – high gain mode, 0 – low gain mode. CMOS Schmitt trigger input with 100-k Ω pull-up resistor, see also chapter ‘Input / Output Stages’.
2	VCC	Supply voltage
3	RXin	RF input, 50 Ω
4, 5	GND	Ground
6	IF_Qp	IF outputs, DC coupled, external AC coupling capacitors required
7	IF_Qn	
8	IF_Ip	
9	IF_In	
10	pwr1	Power-amplifier gain control input: 3.3 V – P _{OUT_MAX} , 0 – P _{OUT_MAX} - 4 dB. CMOS Schmitt trigger input with 100-k Ω pull-up resistor, see also chapter ‘Input / Output Stages’.
11	TX_EN	TX enable input, high active: 3.3 V – enable, 0 – off. CMOS Schmitt trigger input with 100-k Ω pull-up resistor, see also chapter ‘Input / Output Stages’.
12	GND	Ground
13	TXout	Transmitter output, 50 Ω
14	Vctrl	VCO tuning voltage input
15	d3	VCO band switching inputs, each input with internal 120-k Ω pull-down resistor, can be used as analog tuning inputs as well
16	d2	
17	d1	
18	d0	
19	div_o	Divider output, 50 Ω , DC coupled, external decoupling capacitor required (min. 100 pF)
20	PWR	Divider enable input: 3.3 V – enable, 0 – off. CMOS Schmitt trigger input with 100-k Ω pull-up resistor, see also chapter ‘Input / Output Stages’.
(21)	GND	Exposed die attach pad of the QFN package, must be soldered to ground

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the device may cause permanent damage to the device. Actual performance of the device is only given within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V _{CC}		3.6	V	to GND
DC voltage at RF pins	V _{DCRF}	0	2	mV	IC provides low ohmic circuit to GND for TXout and RXin
Junction temperature	T _J		150	°C	
Storage temperature range	T _{STG}	-65	150	°C	
DC voltage at control inputs	V _{CTL}	-0.3	V _{CC} + 0.3	V	d0, d1, d2, d3, Vctrl, Vct, pwr1, TX_EN, PWR
Input power into pin RFin	P _{IN}		0	dBm	
ESD robustness, HBM	V _{ESD1}		2000	V	Class 2, 2 kV to ≤ 4 kV; Note 1
ESD robustness, CDM	V _{ESD2}		500	V	Class 1, 0 to ≤ 500 V; Note 2

Note 1 According to JEDEC JESD22-A114C Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component (HBM), Component Level

Note 2 According to JEDEC JS-002-2018 Joint Standard for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T _A	-40	85	°C	
Supply voltage	V _{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at control inputs	V _{CTL}	0	V _{CC}	V	d0, d1, d2, d3, Vctrl, Vct, pwr1, TX_EN, PWR

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R _{thja}			75	K/W	Four-layer PCB according to JEDEC standard JESD-51

4.4 Electrical Characteristics

$T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise noted. Typical values measured at $T_A = 25\text{ }^{\circ}\text{C}$ and $V_{CC} = 3.3\text{ V}$.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current consumption	I_{CC}	80	89	100	mA	TX, divider enabled
Control input voltage, low level	V_{IN_L}	0		1.0	V	Inputs TX_EN, pwr1, PWR and Vct
Control input voltage, high level	V_{IN_H}	2.2		V_{CC}	V	
Transmitter Section TX						
Transmitter start frequency	f_{TX}	22.3	22.8	23.3	GHz	
Transmitter stop frequency		25.9	26.4	26.9	GHz	
Divider division ratio	D_{div_o}	32				Note 1
Divider output frequency	f_{div_o}	700		840	MHz	
Tuning voltage VCO	V_{ctrl}	0		3.3	V	
Tuning slope VCO (Vctrl)	$\Delta f_{TX}/\Delta V_{ctrl}$		220		MHz/V	Only Vctrl swept
Number of adjustable frequency bands		16				d0 - d3: VCO band switching, Note 1
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		135		MHz/V	$f_{TX} = 24.15\text{ GHz}$
Phase noise	P_N		-102		dBc/Hz	at 1 MHz offset
RF output impedance	Z_{TXout}		50		Ω	
Transmitter output power	P_{TX}	2.5	4	6	dBm	$f_{TX} = 24.15\text{ GHz}$
Adjustable range output power	P_{TX_ADJ}	0		4	dBm	pwr1 = 0 / 3.3 V
Divider output power	P_{div_o}	-9	-8.5	-6	dBm	Note 2
Spurious power	P_{Sp-}		-40		dBm	$f_{TX} - f_{div}$
	P_{Sp+}		-43		dBm	$f_{TX} + f_{div}$
Harmonics power	P_{Ha12}		-46		dBm	12 GHz
	P_{Ha48}		-40		dBm	48 GHz
Receiver Section RX						
Receiver frequency	f_{RX}	22.3		26.9	GHz	
Receiver RF input impedance	Z_{RXIN}		50		Ω	
Number of adjustable gain modes		2				Adjustable LNA gain control
Gain high gain mode		15	17	21	dB	$V_{ct} = 3.3\text{ V}$, Note 3
Gain low gain mode		9	10	12	dB	$V_{ct} = 0$, Note 3
IF frequency range	Δf_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		470		Ω	Differential
IQ amplitude imbalance		-1		1	dB	
IQ phase imbalance		-10		10	deg	
Noise figure, high gain mode			4		dB	Simulated (double side band at $f_{IF} = 1\text{ MHz}$)
Noise figure, low gain mode			6		dB	
Input compression point	1dB ICP	-20		-13	dBm	

Note 1 See also chapter 'Measurement Results', Figure 10 and 11.

Note 2 Divider output is loaded with $50\ \Omega$, DC coupled, external decoupling capacitor $\geq 100\text{ pF}$ required.

Note 3 $f_{TX} = 24.0\text{ GHz} - 24.25\text{ GHz}$, IF frequency f_{IF} set to 1.5 MHz using VCO tuning inputs (d0 - d3, Vctrl)

5 Packaging

5.1 Package Dimensions

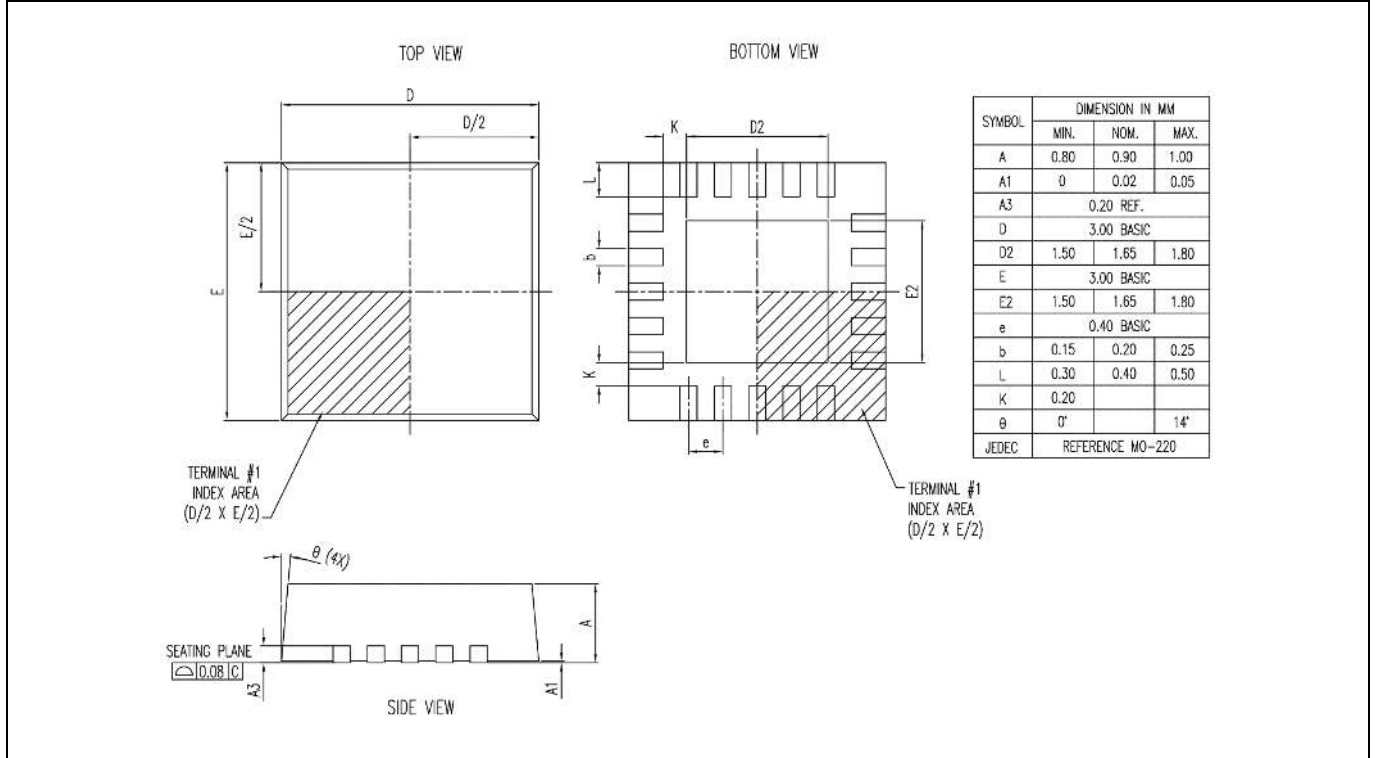


Figure 3 Outline Dimensions of QFN20, 3 × 3 mm², 0.4 mm Pitch

IC Weight: 0.235 g (typ.)

5.2 Package Footprint

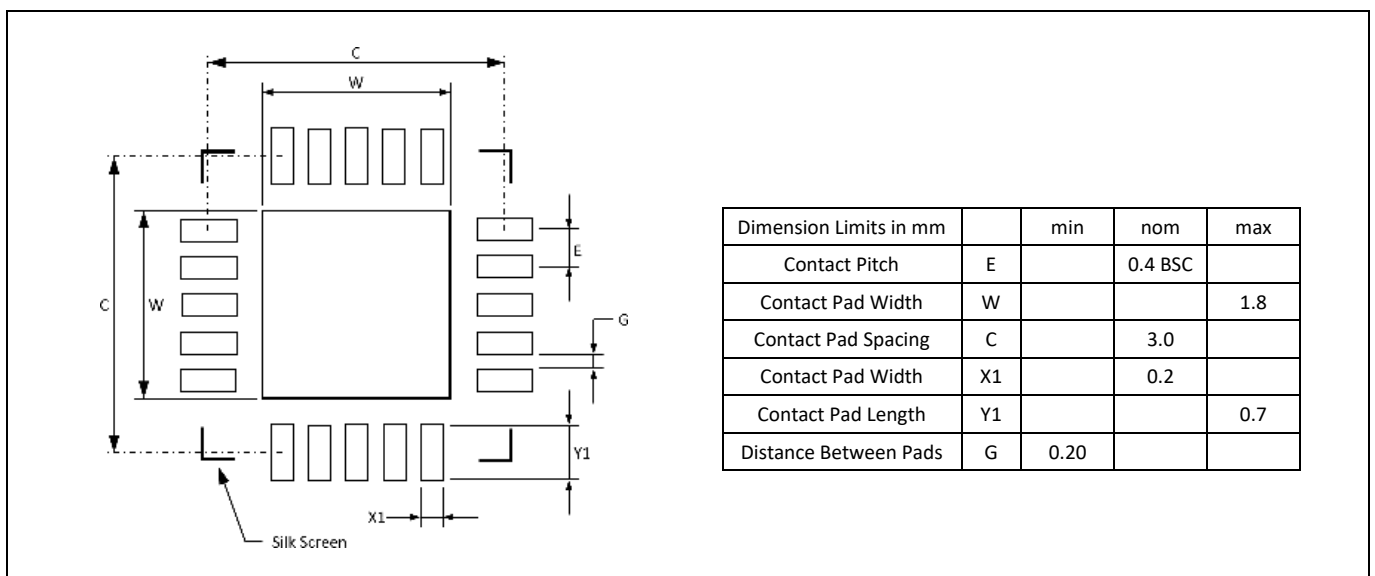


Figure 4 Recommended Land Pattern

5.3 Package Code

Top-Side Markings: TRX046
 YYWW

5.4 Qualification Test

Table 6 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass

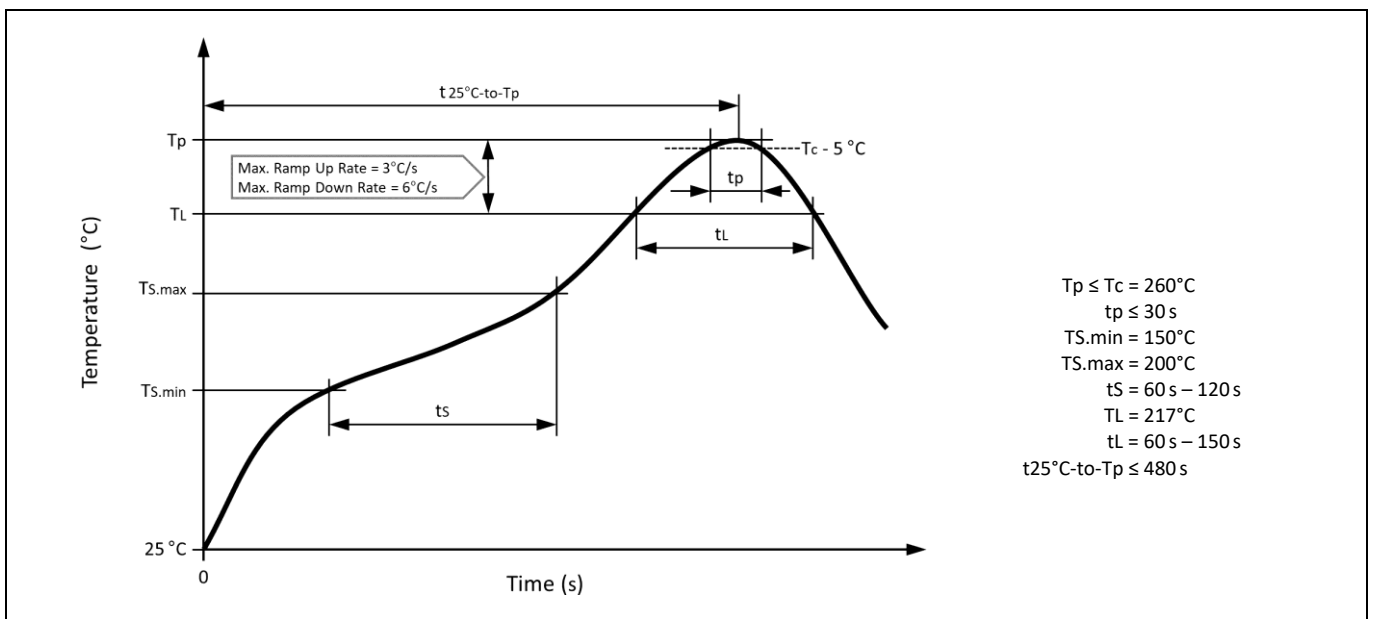


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

6 Application

6.1 Application Circuit Schematic

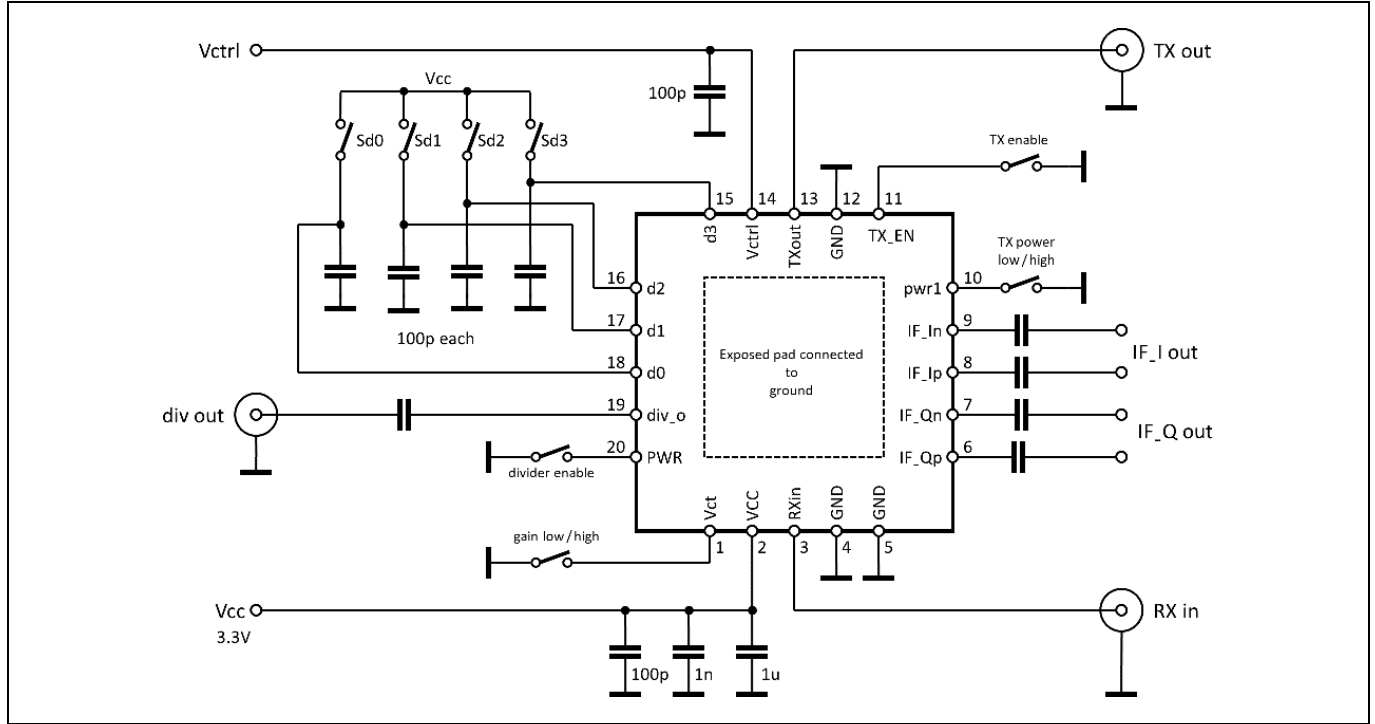


Figure 6 Application Circuit for Band Switching

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 μ s is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Board

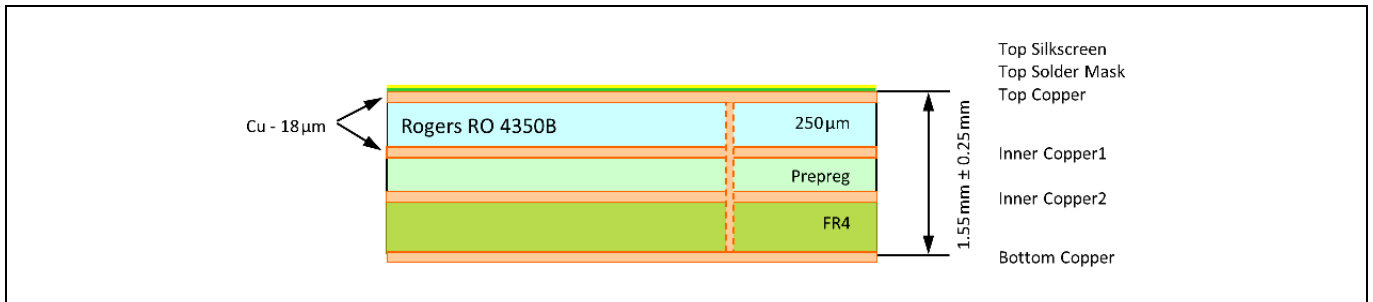


Figure 7 Evaluation Board Stack-up

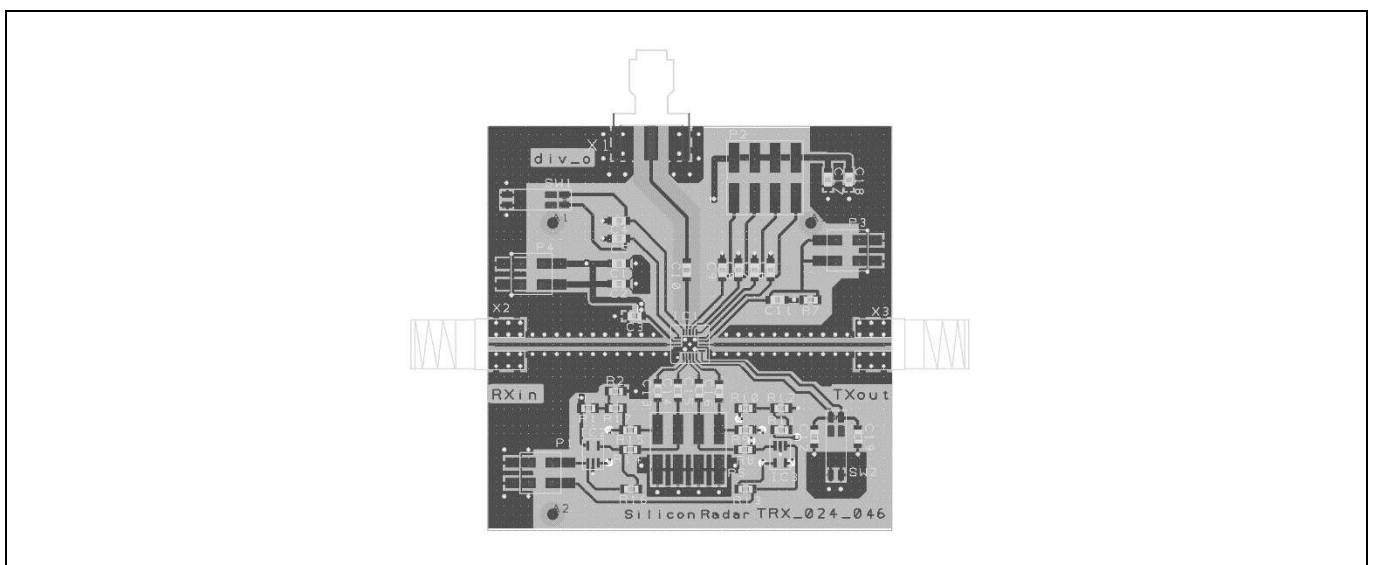


Figure 8 Evaluation Board Layout Including Via Holes (50 mm × 50 mm, Top View)

6.4 Evaluation Kit

For a quick and easy start into radar development Silicon Radar offers *SiRad Easy® r4*. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.

It features:

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- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

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6.5 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin. RXin and TXout are DC-grounded.

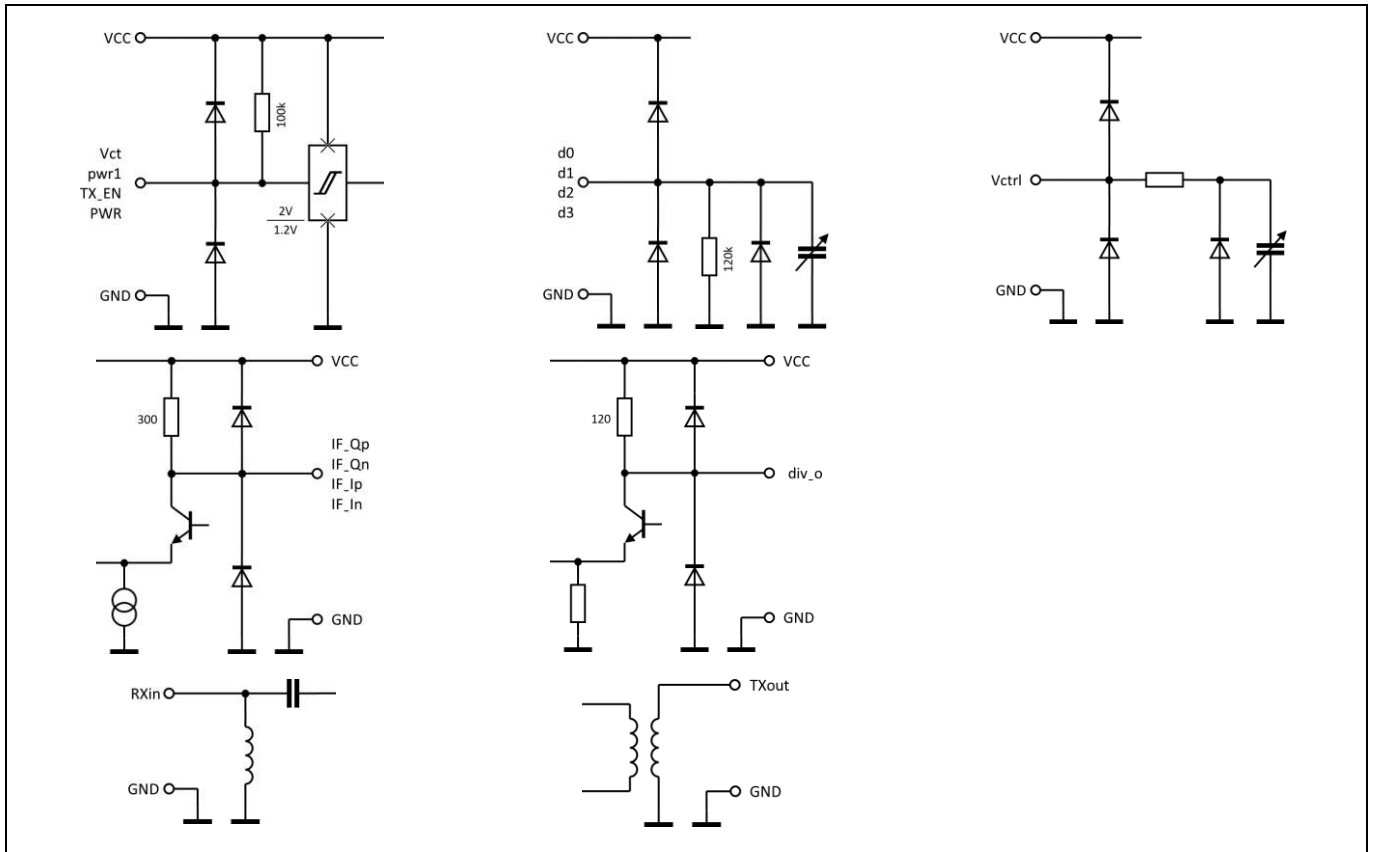


Figure 9 Equivalent I/O Circuits

7 Measurement Results

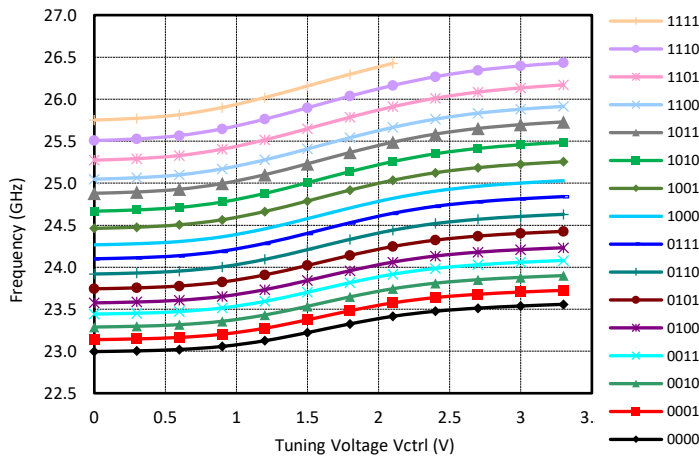


Figure 10 VCO tuning bandwidth switching (d3|d2|d1|d0)

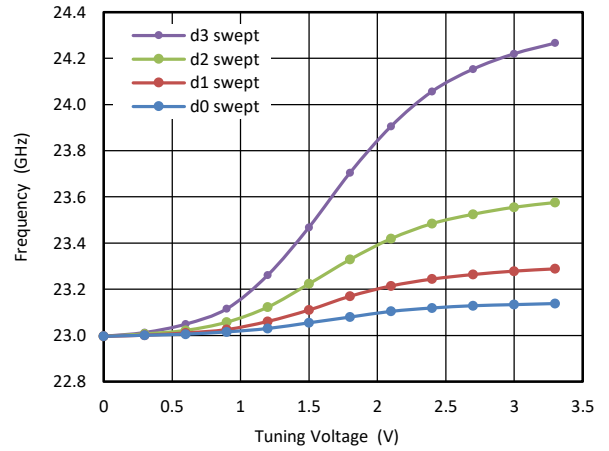


Figure 11 VCO tuning, d3 - d0 swept, Vctrl = 0 = constant

VCO band switching inputs d3 to d0 can be used to switch the output frequency band as in Figure 10. As an example, input combination '0101' with d3, d1 = 3.3 V and d2, d0 = 0 includes the 24-GHz ISM band. However, the designer should take into account that output frequency bands may shift from chip to chip, and same switch settings may not give the same output band.

Note, VCO band switching inputs d0 - d3 are analog inputs and can be used to control the output frequency analogously as well. The bandwidth of the switching inputs increases from d0 to d3. Any of these pins can be interconnected to each other and/or to pin Vctrl to use different bandwidth capabilities of the VCO.

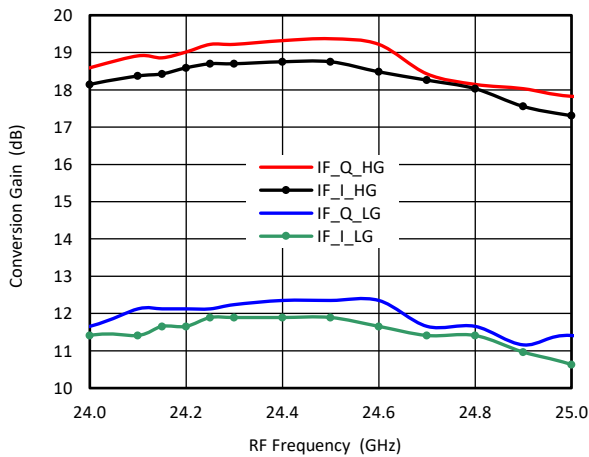


Figure 12 Conversion gain for high gain and low gain mode

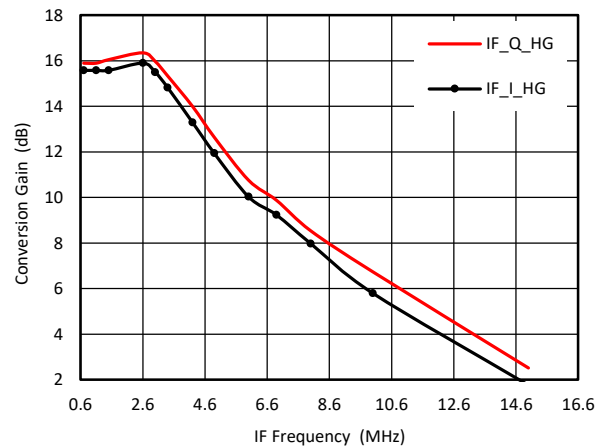


Figure 13 Conversion for high gain mode for different IF frequencies

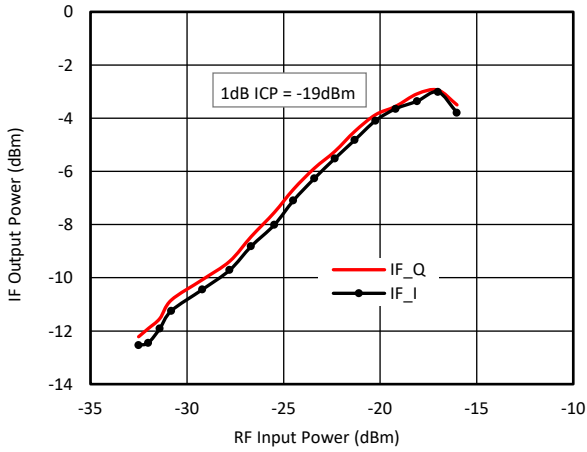


Figure 14 Linearity of receiver for high gain mode

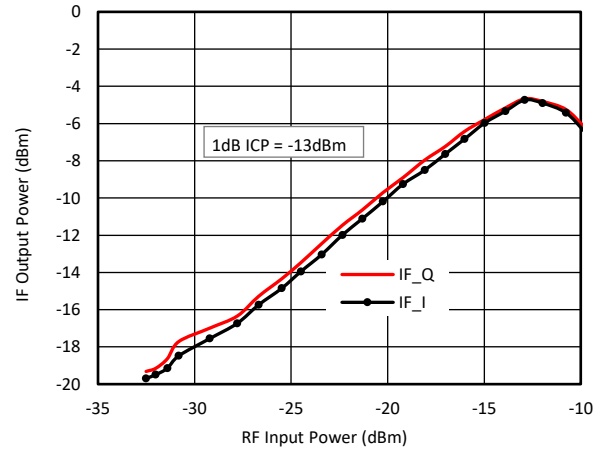


Figure 15 Linearity of receiver for low gain mode

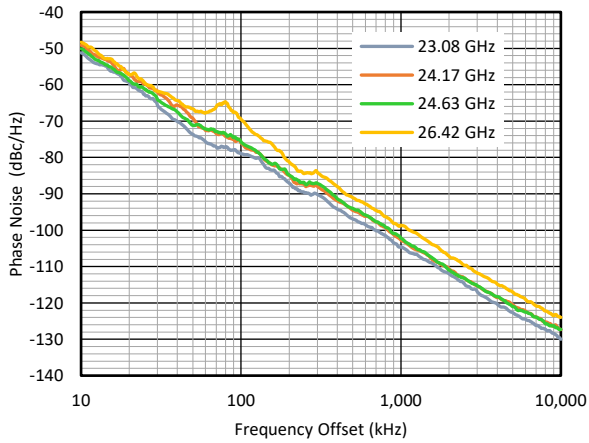


Figure 16 Phase noise

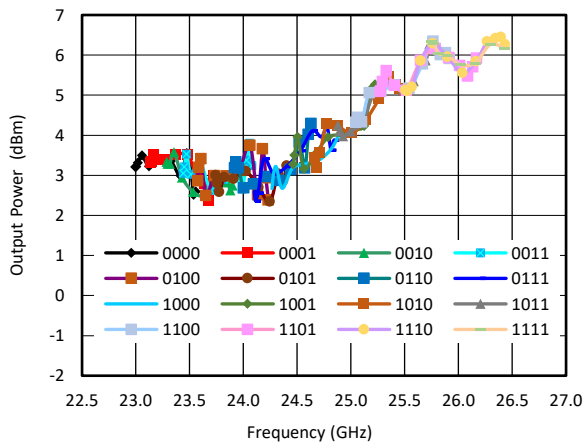


Figure 17 Transmitter output power versus frequency for all d3|d2|d1|d0 settings

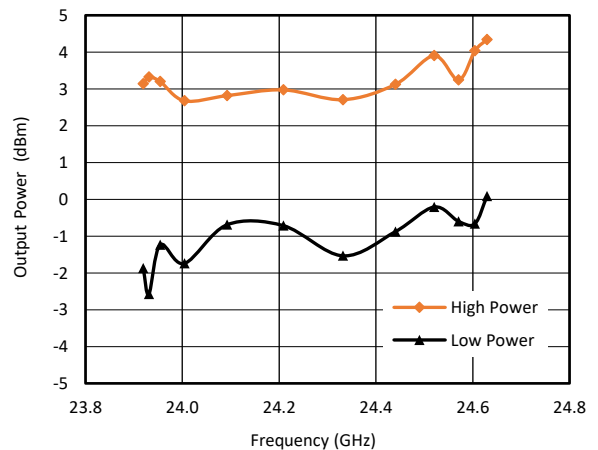


Figure 18 Transmitter output power in high and low power mode (d3|d2|d1|d0 = 0110)

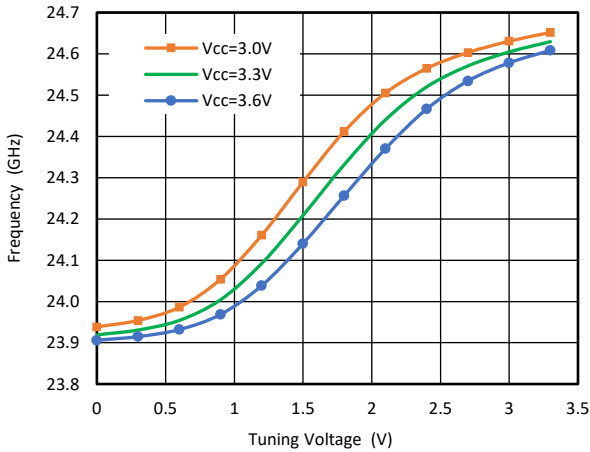


Figure 19 VCO tuning curves with 300 mV pushing (d3|d2|d1|d0 = 0110)

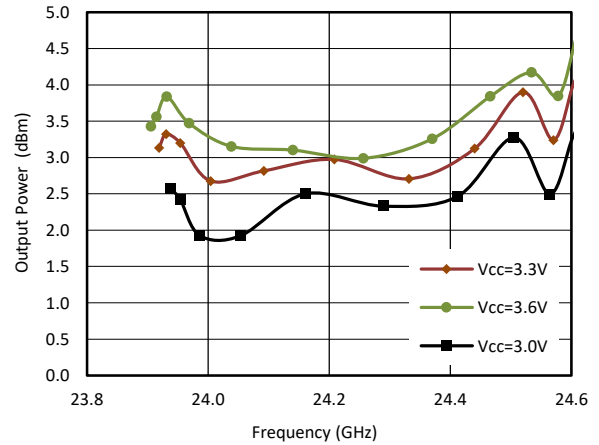


Figure 20 Transmitter output power with 300 mV VCO pushing (d3|d2|d1|d0 = 0110)

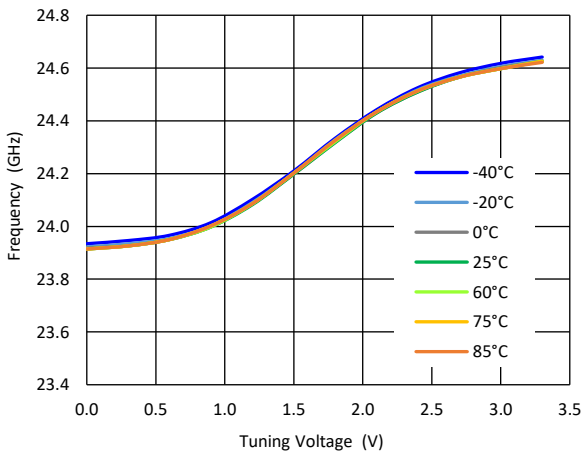


Figure 21 VCO tuning curves for different temperatures (d3|d2|d1|d0 = 0110)

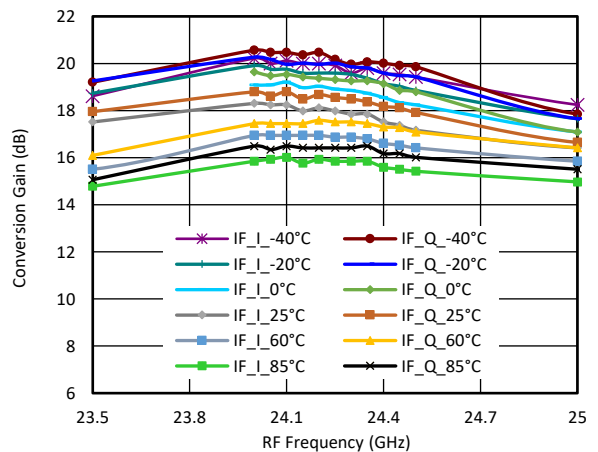


Figure 22 Conversion gain for different temperatures, high gain

Note to Figure 21: Frequency stability over full temperature range is better than 10 MHz.

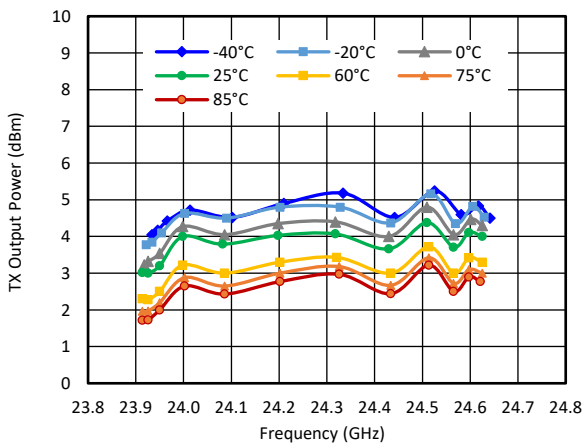


Figure 23 Transmitter output power for different temperatures

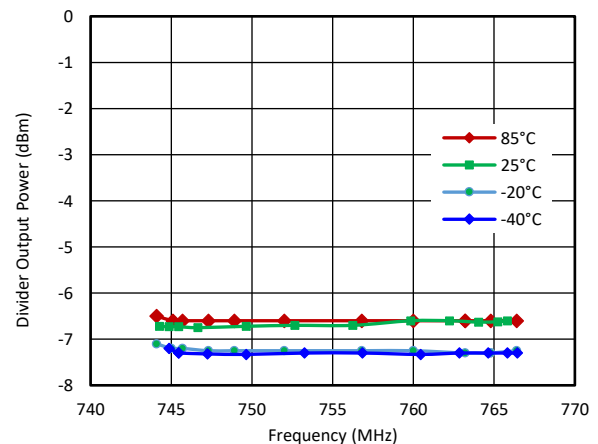


Figure 24 Divider output power for different temperatures (d3|d2|d1|d0 = 0110)

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