Features

- ESD Protect for 2 high-speed I/O lines and one VDD line
- Provide ESD protection for each line to
  IEC 61000-4-2, (ESD) ±15kV (contact/air)
  IEC 61000-4-4 (EFT), 60A (5/50ns)
  IEC 61000-4-5 (Lightning) 6A (8/20μs)
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V etc.
- Low capacitance : 2pF typical
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Back-drive protection for power-down mode
- **Green Part**

Applications

- **USB2.0 Power and Data lines protection**
- **Cellular Handsets and Accessories**
- **Notebook and PC Computers**
- **SIM card**
- **Portable Devices**
- **Digital Cameras**
- **Touch Panels**
- **Ethernet port: 10/100 Mb/s**
- **Peripherals**

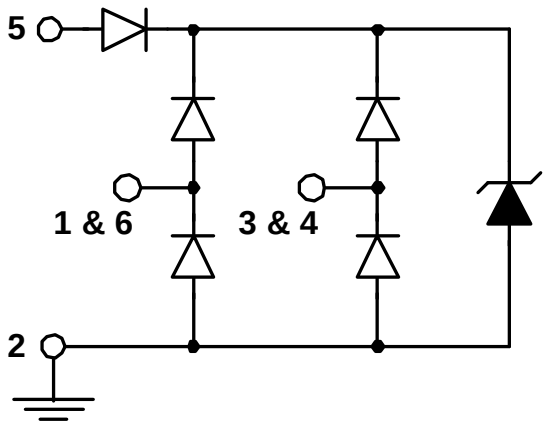
Description

AZC299-02R is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZC299-02R has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

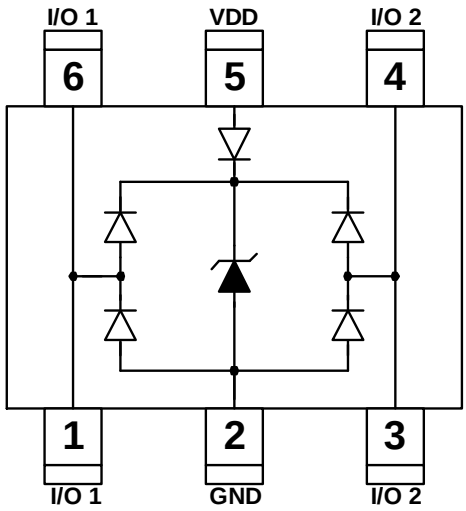
AZC299-02R is a unique design which includes ESD rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components. Besides, there is a back-drive protection design in AZC299-02R for power-down mode operation.

AZC299-02R may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



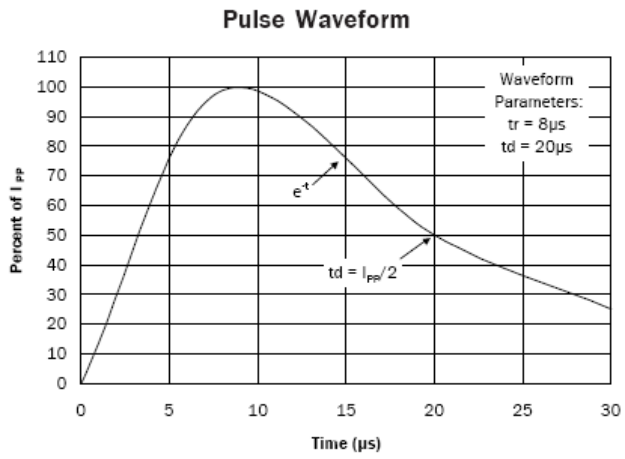
SOT563 (Top View)

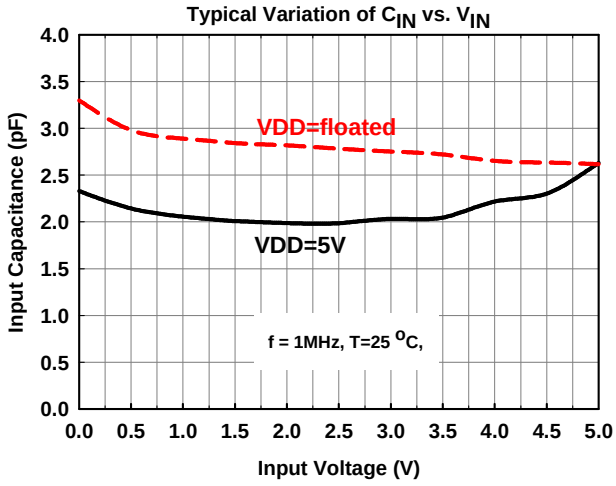
SPECIFICATIONS

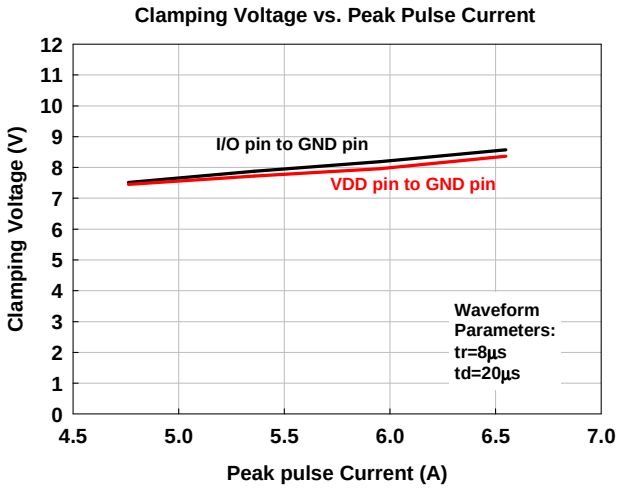
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**PARAMETER**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	6	**A**
Operating Supply Voltage (VDD-GND)	V_{DC}	6	**V**
ESD per IEC 61000-4-2 (Contact /Air) (I/O pins)	V_{ESD_IO}	±15	**kV**
ESD per IEC 61000-4-2 (Contact /Air) (VDD pin)	V_{ESD_PW}	±18	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-40 to +125	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	**V**

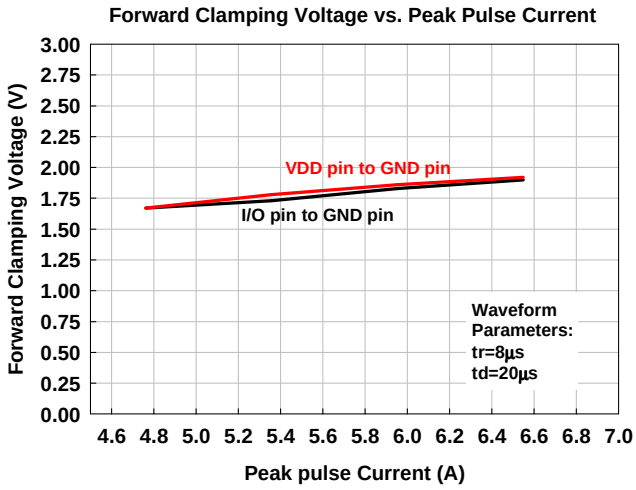
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	pin 5 to pin 2, T=25 °C			5	**V**
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 °C, pin 5 to pin 2			5	**μA**
Channel Leakage Current	$I_{CH-Leak}$	V_{pin5} = 5V, V_{pin2} = 0V, T=25 °C			1	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin 5 to Pin 2	6		9	**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin 2 to Pin 5		0.8	1	**V**
ESD Clamping Voltage –I/O	V_{clamp_io}	IEC 61000-4-2 +6kV, T=25 °C, contact mode, any channel pin to ground		9.5		**V**
ESD Clamping Voltage –VDD	V_{clamp_VDD}	IEC 61000-4-2 +6kV, T=25 °C, contact mode, VDD pin to ground		9		**V**
ESD Dynamic Turn on Resistance –I/O	$R_{dynamic\_io}$	IEC 61000-4-2 0~+6kV,T=25 °C, contact mode, any channel pin to ground		0.18		**Ω**
ESD Dynamic Turn on Resistance –VDD	$R_{dynamic\_VDD}$	IEC 61000-4-2 0~+6kV, T=25 °C, contact mode, VDD pin to ground		0.15		**Ω**
Lightning Clamping Voltage	$V_{lightning\_io}$	I_{PP}=5A, tp=8/20μs, T=25 °C, any channel pin to ground		7.8		**V**
Lightning Clamping Voltage	$V_{lightning\_VDD}$	I_{PP}=5A, tp=8/20μs, T=25 °C, VDD pin to ground		7.8		**V**
Channel Input Capacitance -1	C_{IN-1}	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C, any channel pin to ground		2	2.5	**pF**
Channel Input Capacitance - 2	C_{IN-2}	**V_{pin5}=floated**,V_{pin2}=0V,**V_{IN}=2.5V**,f=1MHz, T=25°C, any channel pin to ground		2.8	3.6	**pF**
Channel to Channel Input Capacitance -1	$C_{CROSS-1}$	**V_{pin5} =5V,** V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , between channel pins		0.4	0.5	**pF**
Channel to Channel Input Capacitance -2	$C_{CROSS-2}$	**V_{pin5} =floated**,V_{pin2} =0V,**V_{IN} =2.5V**,f =1MHz,T=25 °C, between channel pins		0.55	0.65	**pF**
Variation of Channel Input Capacitance -1	$\triangle C_{IN-1}$	**V_{pin5} =5V**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , (channel_x pin to ground) – (channel_y pin to ground)		0.05	0.1	**pF**
Variation of Channel Input Capacitance -2	$\triangle C_{IN-2}$	**V_{pin5} =floated**, V_{pin2} =0V, **V_{IN} =2.5V**, f =1MHz, T=25 °C , (channel_x pin to ground) – (channel_y pin to ground)		0.05	0.1	**pF**

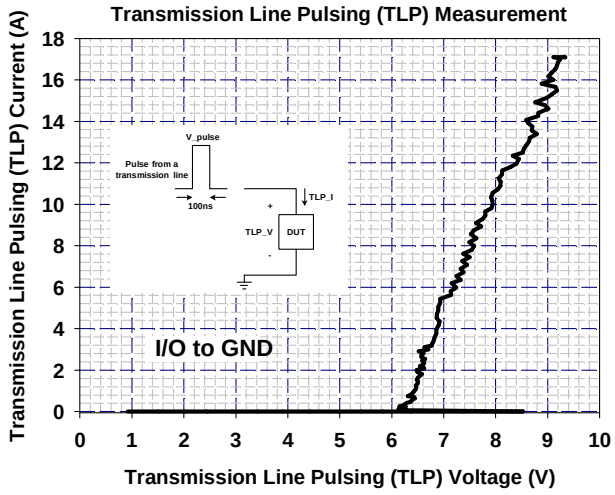
Typical Characteristics

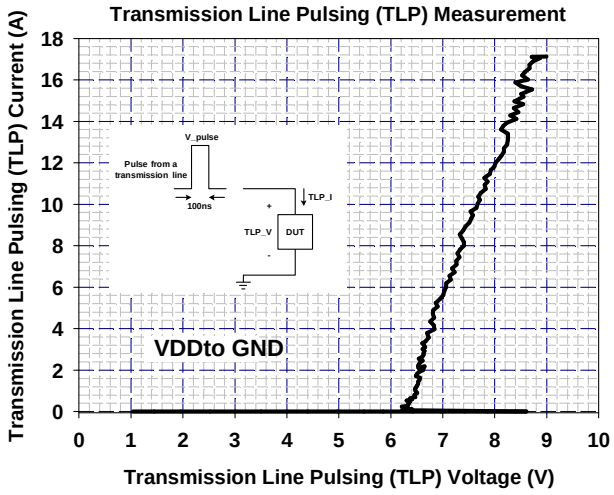












Applications Information

A. Design Considerations

The ESD protection scheme for system I/O connector is shown in the Fig. 1. In Fig. 1, the diodes D1 and D2 are general used to protect data line from ESD stress pulse. The diode D3 is a back-drive protection design, which blocks the DC back-drive current when the potential of I/O pin is greater than that of VDD pin. If the power-rail ESD clamping circuit is not placed between VDD and GND rails, the positive pulse ESD current (I_{ESD1}) will pass through the ESD current path1. Thus, the ESD clamping voltage V_{CL} of data line can be described as follow:

V_{CL} = Fwd voltage drop of D1 + Breakdown voltage drop of D3 + supply voltage of VDD rail + $L_1 \times d(I_{ESD1})/dt + L_2 \times d(I_{ESD1})/dt$

Where L_1 is the parasitic inductance of data line, and L_2 is the parasitic inductance of VDD rail.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30A in 1ns. Here $d(I_{ESD1})/dt$ can be approximated by $\Delta I_{ESD1}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of total parasitic inductance (L_1 and L_2 combined) will lead to over 300V increment in V_{CL}! Besides, the ESD pulse current which is directed into the VDD rail may potentially damage any components that are attached to that rail. Moreover, it is common for the forward voltage drop of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. Of course, the discrete diode is also possible to be destroyed due to its power dissipation capability is exceeded.

The AZC299-02R has an integrated power-rail ESD clamped circuit between VDD and GND rails. It can successfully overcome previous disadvantages. During an ESD event, the positive ESD pulse current (I_{ESD2}) will be directed through the integrated power-rail ESD clamped circuit to GND rail (ESD current path2). The clamping voltage V_{CL} on the data line is small and protected IC will not be damaged because power-rail ESD clamped circuit offer a low impedance path to discharge ESD pulse current.

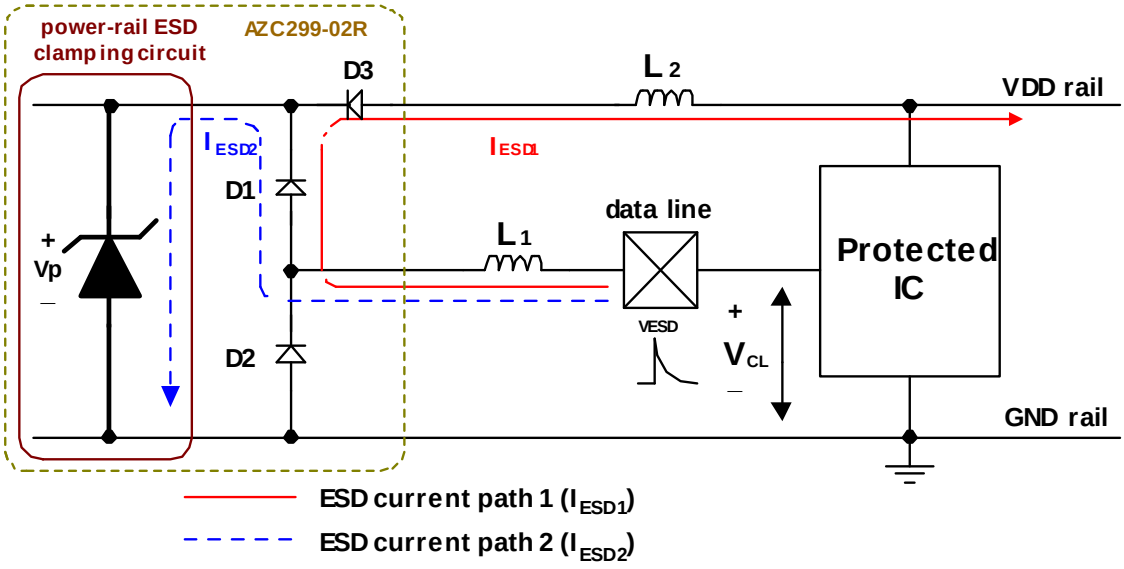


Fig. 1 Application of positive ESD pulse between data line and GND rail.

B. Device Connection

The AZC299-02R is designed to protect two data lines and one power rail from transient over-voltage (such as ESD stress pulse). The device connection of AZC299-02R is shown in the Fig. 2. In Fig. 2, the two protected data lines are connected to the ESD protection pins (pin1, pin6, pin3, and pin4) of AZC299-02R. The ground pin (pin2) of AZC299-02R is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin 5) of AZC299-02R is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZC299-02R.

AZC299-02R can provide protection for 2 I/O signal lines simultaneously. In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD Level, a 0.1μF chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZC299-02R.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin 5) of AZC299-02R can be left as floating. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 3 shows the detail connection.

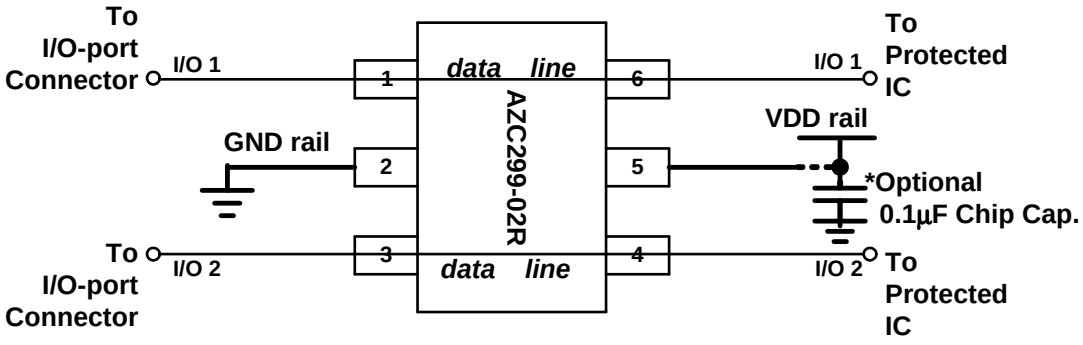


Fig. 2 Data lines and power rails connection of AZC299-02R.

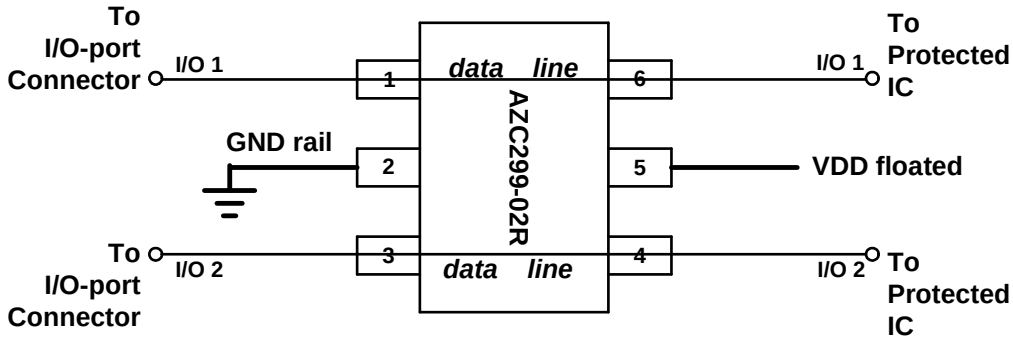


Fig. 3 Data lines and power rails connection of AZC299-02R. VDD pin is left as floating when no power rail presented on the PCB.

C. Application

AZC299-02R is designed for protecting high speed I/O ports from very high over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZC299-02R, especially, the USB port.

Universal Serial Bus (USB) ESD Protection

The AZC299-02R can be used to protect the USB port on the monitors, computers, peripherals or portable systems. The ESD protection scheme for USB port is shown in Fig. 4. In the Fig. 4, each AZC299-02R will protect one USB port. The voltage bus (V_{BUS}) of USB port is connected to the power pin (pin 5) of AZC299-02R. Each data line (D+/D-) of USB port is connected to the ESD protection pin of AZC299-02R.

When ESD voltage pulse appears on the data line, the ESD pulse current will be conducted by AZC299-02R away from the USB controller chip. In addition, the ESD pulse current also can be conducted by AZC299-02R away from the USB controller chip when the ESD voltage pulse appears on the voltage bus (V_{BUS}) of USB port. Therefore, the data lines (D+/D-) and voltage bus (V_{BUS}) of USB port are simultaneously protected with one AZC299-02R.

The AZC299-02R has been integrated with back-drive protection diode for preventing the back-drive current to occur. The back-drive current occurs as shown in Fig, 5. When the device stays at OFF state, its V_{BUS} might be tied to ground potential. At this moment, if without the integrated back-drive current protection diode, the HUB stays at ON state, and a DC bias might be presented on the D+ or D- data line, a current may flow through the steering diode to the grounded V_{BUS}, as shown in Fig. 5. This back drive current may lead system to an abnormal state. Therefore, it should be eliminated, and the integrated back-drive protection diode can eliminate this current.

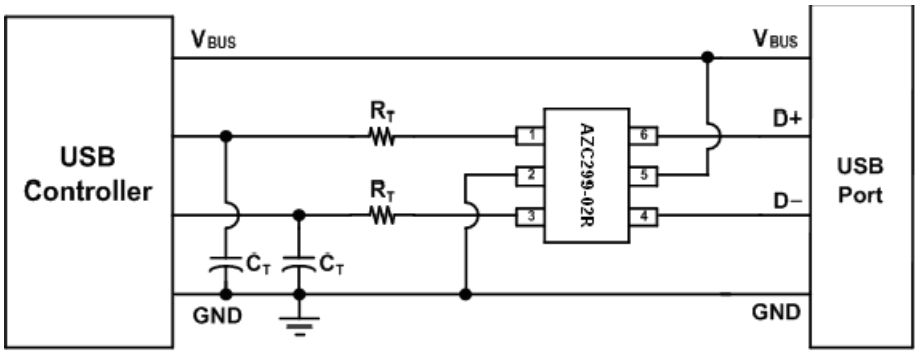


Fig. 4 ESD Protection scheme for USB port by using AZC299-02R.

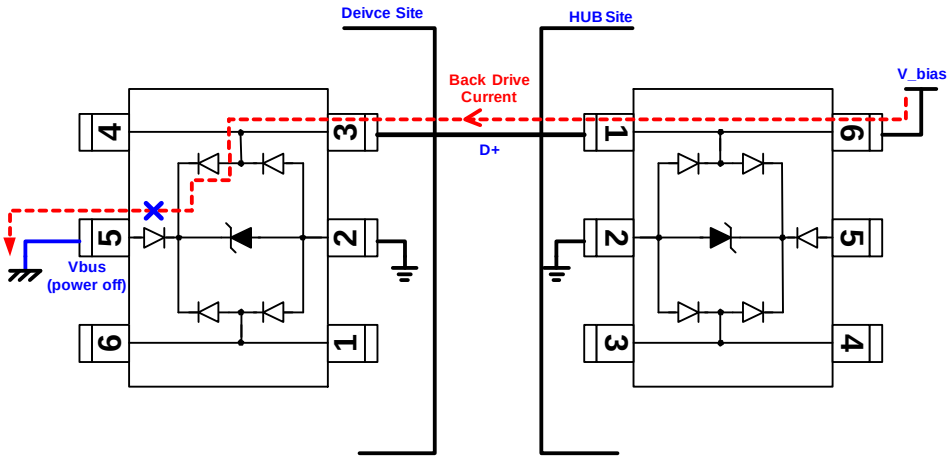


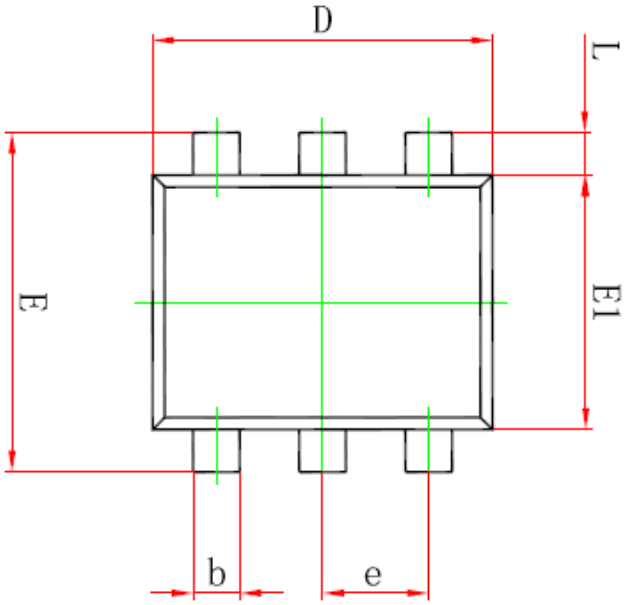
Fig. 5 The possible occurred back drive current when the device is at OFF state and the HUB is at ON state. The AZC299-02R can avoid this back drive current to occur.

Mechanical Details

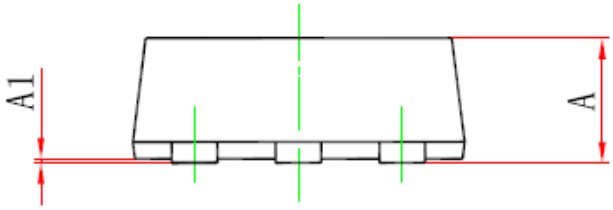
SOT563

PACKAGE DIAGRAMS

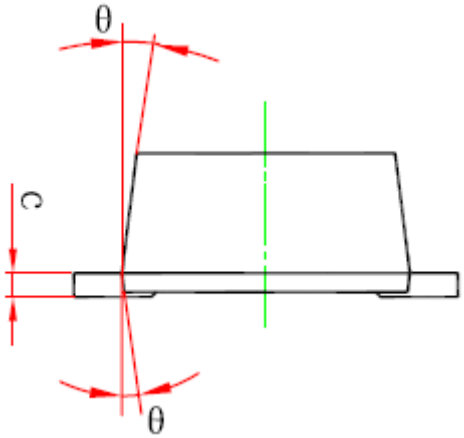
TOP VIEW



SIDE VIEW



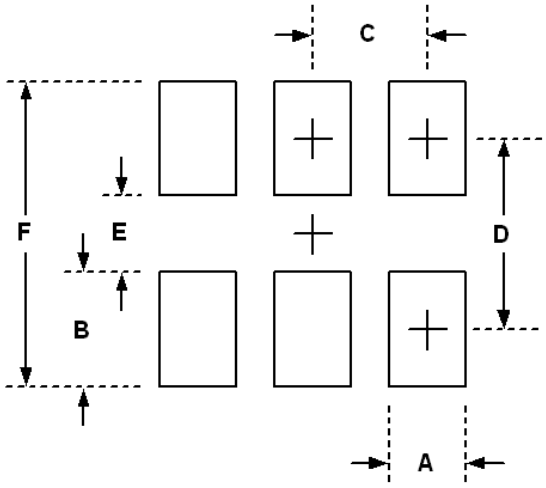
END VIEW



PACKAGE DIMENSIONS

SYMBOL	Millimeters		
	MIN.	NOMINAL	MAX.
A	0.525	-	0.60
A1	0	-	0.05
e	0.45	-	0.55
c	0.09	-	0.16
D	1.50	-	1.70
b	0.17	-	0.27
E1	1.10	-	1.30
E	1.50	-	1.70
L	0.10	-	0.30
θ	7^{o} REF		

LAND LAYOUT

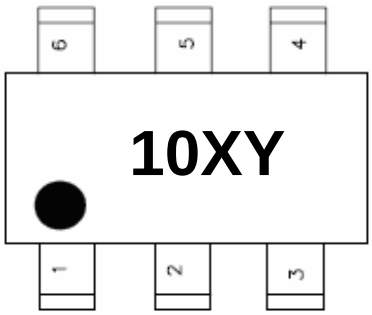


Dimensions	
Index	**Millimeter**
A	0.30
B	0.50
C	0.50
D	1.40
E	0.90
F	1.90

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZC299-02R (Green Part)	10XY

10=Device Code

X=Date Code

Y=Control Code

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZC299-02R.R7G	Green	T/R	7 inch	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2008/11/28	Initial Release.
Revision 2009/04/22	Correct the parameters of LAND LAYOUT
Revision 2011/02/16	Redraw the Fig. 2 and Fig. 3 in Section B.
Revision 2011/07/30	1. Update the Company Logo. 2. Add the Ordering Information.