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New Japan Radio Co.,Ltd.

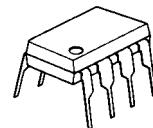
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SYSTEM RESET IC

■ GENERAL DESCRIPTION

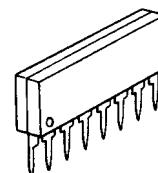
NJM2103 is supply voltage supervisory IC to detect the abnormal conditions, such as shut down of all supply voltages at once, or sudden voltage down and then generate the reset signal. It supervises both 5V supply voltage and the voltage optionally set up.

■ PACKAGE OUTLINE



NJM2103D

NJM2103M

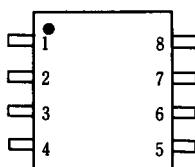
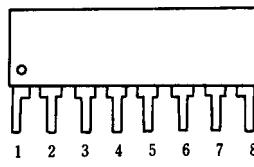


NJM2103L

■ FEATURES

- Precise Detection of Supply Voltage Down ($V_{SA}=4.2V\pm2.5\%$)
- Possible Detection of Optional Voltage Down ($V_{SB}=1.22V\pm1.5\%$)
- Possible Detection of Optional Over-loading
- Low Operating Current ($I_{CC}\leq560\mu A@V_{SB}=5V$)
- Reference Voltage can be taken out.
- Low Reset Validated Voltage ($V^+=0.8V$ Typ.)
- Voltage Detection with Hysteresis Feature
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

■ PIN CONFIGURATION

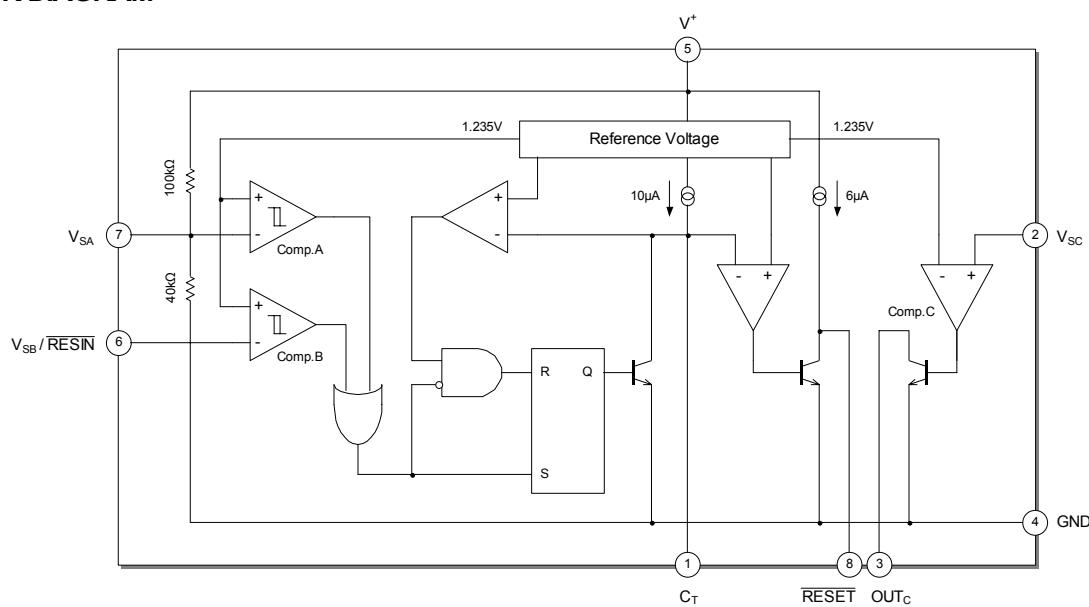
NJM2103D
NJM2103M

NJM2103L

PIN FUNCTION

1. C_T
2. V_{SC}
3. OUT_C
4. GND
5. V^+
6. $V_{SB}/RESIN$
7. V_{SA}
8. RESET

■ BLOCK DIAGRAM



NJM2103

■ ABSOLUTE MAXIMUM RATINGS

($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	20	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SIP8) 800	mW
Input Voltage A	V_{SA}	$V^+ + 0.3 (< 20)$	V
Input Voltage B	V_{SB}	20	V
Input Voltage C	V_{SC}	20	V
Operating Temperature Range	T_{opr}	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to +125	$^\circ\text{C}$

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS

($V^+=5.0\text{V}$, $V_{SB}=0\text{V}$, $V_{SC}=0\text{V}$, $T_a=25^\circ\text{C}$)

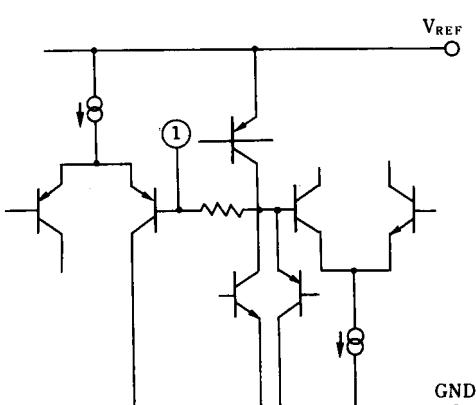
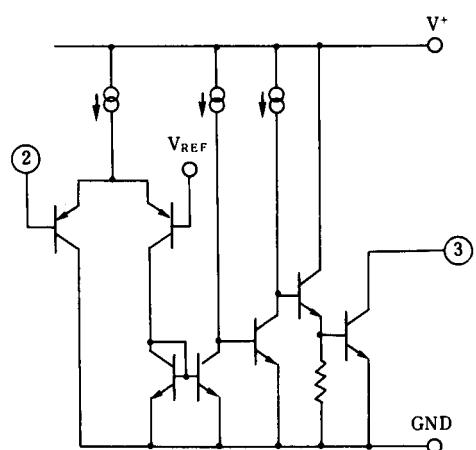
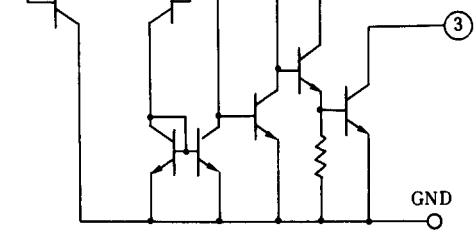
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC1}	$V_{SB}=5\text{V}$	-	380	560	μA
Operating Current (2)	I_{CC2}		-	460	700	μA
V_{SA} Detecting Voltage (1)	V_{SAL}	V^+ fall time $V_{SB}=V^+$	4.10	4.20	4.30	V
V_{SA} Detecting Voltage (2)	V_{SAH}	V^+ rise time $V_{SB}=V^+$	4.20	4.30	4.40	V
V_{SA} Hysteresis Width	V_{HRSA}		50	100	150	mV
V_{SB} Detecting Voltage	V_{SBL}	V_{SB} fall time	1.202	1.220	1.238	V
V_{SB} Ddetecting Supply Voltage Fluctuation	ΔV_{SBL}	$V^+=3.5$ to 18V	-	3	10	mV
V_{SB} Hysteresis Width	V_{HRSB}		14	28	42	mV
V_{SB} Input Current (1)	I_{IHB}	$V_{SB}=5\text{V}$	-	0	250	nA
V_{SB} Input Current (2)	I_{ILB}		-	20	250	nA
High Level $\overline{\text{RESET}}$ Output Voltage	V_{OHR}	$I_{\overline{\text{RESET}}}=5\mu\text{A}$, $V_{SB}=5\text{V}$	4.5	4.9	-	μV
$\overline{\text{RESET}}$ Output Saturating Voltage (1)	V_{OLR1}	$I_{\overline{\text{RESET}}}=2\text{mA}$	-	0.20	0.40	V
$\overline{\text{RESET}}$ Output Saturating Voltage (2)	V_{OLR2}	$I_{\overline{\text{RESET}}}=10\text{mA}$	-	0.30	0.50	V
$\overline{\text{RESET}}$ Output Sink Current	$I_{\overline{\text{RESET}}}$	$V_{OLR}=1.0\text{V}$	20	80	-	mA
C_T Charge Current	I_{CT}	$V_{SB}=5\text{V}$, $V_{CT}=0.5\text{V}$	6.0	9.5	13.0	μA
V_{SC} Input Current (1)	I_{IHC}	$V_{SC}=5\text{V}$	-	0	500	nA
V_{SC} Input Current (2)	I_{ILC}		-	50	500	nA
V_{SC} Detecting Voltage	V_{SC}		1.215	1.235	1.255	V
V_{SC} Detecting Supply Voltage Fluctuation	ΔV_{SC}	$V^+=3.5$ to 13.5V	-	3	10	mV
OUT _C Output Leak Current	I_{OHC}	$V_{OHC}=13.5\text{V}$	-	0	1	μA
OUT _C Output Saturation Voltage	V_{OLC}	$I_{\text{OUT}}=4\text{mA}$, $V_{SC}=5\text{V}$	-	0.10	0.40	V
OUT _C Output Sink Current	I_{OUTC}	$V_{OLC}=1.0\text{V}$, $V_{SC}=5\text{V}$	6	20	-	mA
$\overline{\text{RESET}}$ Guarantee Minimum Supply Voltage	V_L^+	$V_{OLR}=0.4\text{V}$, $I_{\overline{\text{RESET}}}=200\mu\text{A}$	-	0.8	1.2	V

• AC CHARACTERISTICS

($V^+=5.0\text{V}$, $V_{SB}=5.0\text{V}$, $V_{SC}=0\text{V}$, $C_T=0.01\mu\text{F}$, $T_a=25^\circ\text{C}$)

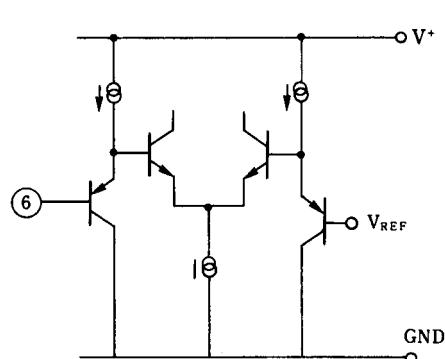
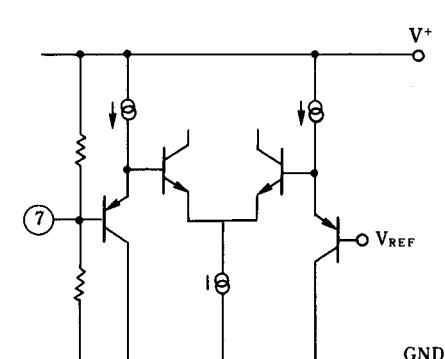
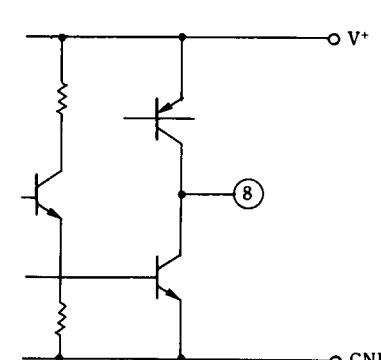
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SA} Input Pulse Width	t_{PIA}		-	3.0	-	μs
V_{SB} Input Pulse Width	t_{PIB}		-	1.5	-	μs
$\overline{\text{RESET}}$ Output Pulse Width	t_{PO}	$V_{SB}=V^+$	-	1.5	-	ms
$\overline{\text{RESET}}$ Rise Time	t_r	$V_{SB}=V^+$, $R_L=2.2\text{k}\Omega$, $C_L=100\text{pF}$	-	1.0	-	μs
$\overline{\text{RESET}}$ Fall Time	t_f	$V_{SB}=V^+$, $R_L=2.2\text{k}\Omega$, $C_L=100\text{pF}$	-	0.1	-	μs
Output Delay Time	t_{PD}	V_{SB} fall time	-	2	-	μs
Output Delay Time	t_{PHL}	V_{SC} rise time, $R_L=2.2\text{k}\Omega$, $C_L=100\text{pF}$	-	0.5	-	μs
Output Delay Time	t_{PLH}	V_{SC} fall time, $R_L=2.2\text{k}\Omega$, $C_L=100\text{pF}$	-	1.0	-	μs

■ TERMINAL FUNCTION

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	C_T	Pin Connection to Capacitor, Set the reset holding time.	
2	V_{SC}	Comparator Input	
3	OUT_C	Open Collector Output of Comparator C.	

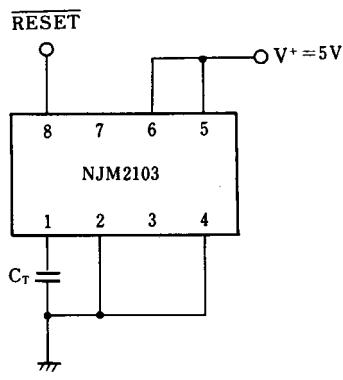
NJM2103

■ TERMINAL FUNCTION

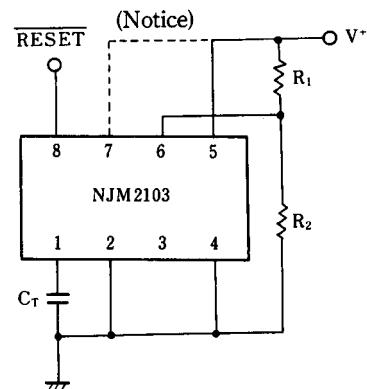
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
4	GND	Ground	
5	V ⁺	Operating Voltage	
6	V _{SB} /RESIN	Comparator B Input	 <p>The circuit diagram for Pin 6 shows a differential input stage. It consists of two NPN transistors connected in an anti-series configuration. The base of the top transistor is connected to the input terminal (Pin 6) through a resistor. The collector of the top transistor is connected to the collector of the bottom transistor. The base of the bottom transistor is connected to ground through a resistor. The collector of the bottom transistor is connected to the output terminal (Pin 8). A reference voltage source labeled V_{REF} is connected between the collector of the bottom transistor and ground. The output terminal (Pin 8) is also connected to ground.</p>
7	V _{SA}	Comparator A Input	 <p>The circuit diagram for Pin 7 shows a differential input stage. It consists of two NPN transistors connected in an anti-series configuration. The base of the top transistor is connected to the input terminal (Pin 7) through a resistor. The collector of the top transistor is connected to the collector of the bottom transistor. The base of the bottom transistor is connected to ground through a resistor. The collector of the bottom transistor is connected to the output terminal (Pin 8). A reference voltage source labeled V_{REF} is connected between the collector of the bottom transistor and ground. The output terminal (Pin 8) is also connected to ground.</p>
8	RESET	Reset Output Internalizing pull up resistor	 <p>The circuit diagram for Pin 8 shows a simple inverter stage. It consists of a single NPN transistor. The base of the transistor is connected to the input terminal (Pin 8) through a resistor. The collector of the transistor is connected to the output terminal (Pin 8). The emitter of the transistor is connected to ground through a resistor. The output terminal (Pin 8) is also connected to ground.</p>

■ APPLICATION CIRCUIT

1) 5V Supply Voltage Monitor



2) Monitoring of Optional Supply Voltage ($V^+ \leq 13.5V$)

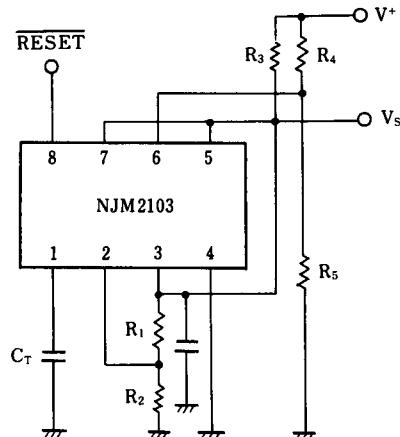


$$\text{Detecting Voltage} = \left(1 + \frac{R_1}{R_2}\right) \times V_{SB}$$

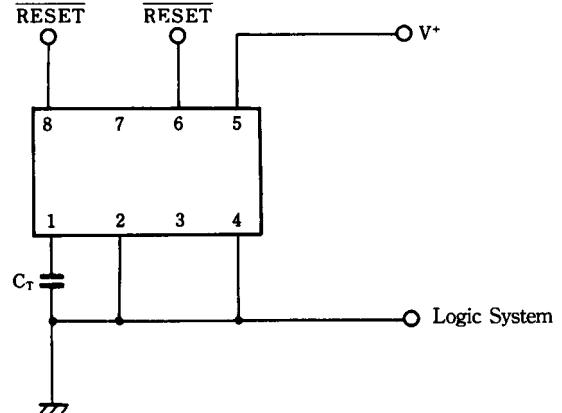
(Notice)

If it were that V^+ indicates under 4.50V, Connect 7 pin to V^+

3) Monitoring of Optional Supply Voltage ($V^+ > 13.5V$)



4) Compulsory Reset



$$\text{Detecting Voltage} = \left(1 + \frac{R_4}{R_5}\right) \times V_{SB}$$

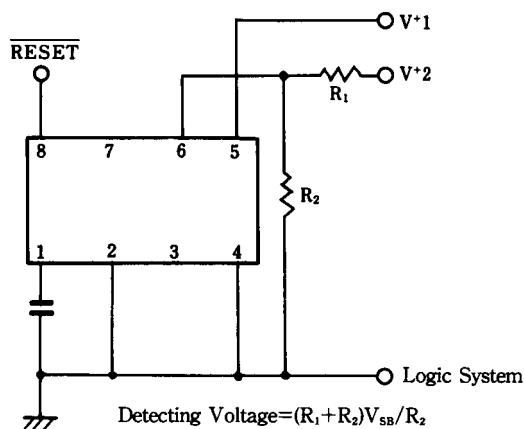
$$\text{Constant Voltage Output } V_S = \left(1 + \frac{R_1}{R_2}\right) \times V_{SC}$$

$$\overline{\text{RESET}} \text{ Output} = \begin{cases} V_S & (\text{High Level}) \\ OV & (\text{Low Level}) \end{cases}$$

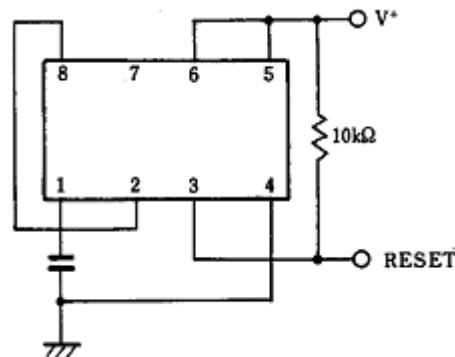
Input Reset signal TTL level to V_{SB} - terminal

NJM2103

5) 5V, $V_{CC} < 12V$ Supply Voltage Monitor

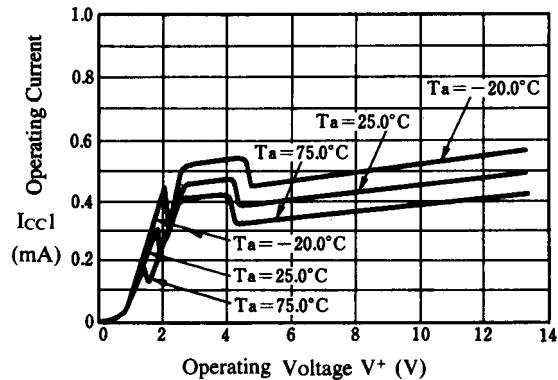


6) Non-Inverting Reset

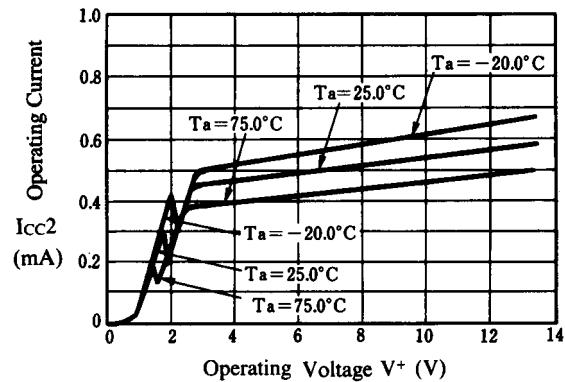


■ TYPICAL CHARACTERISTICS

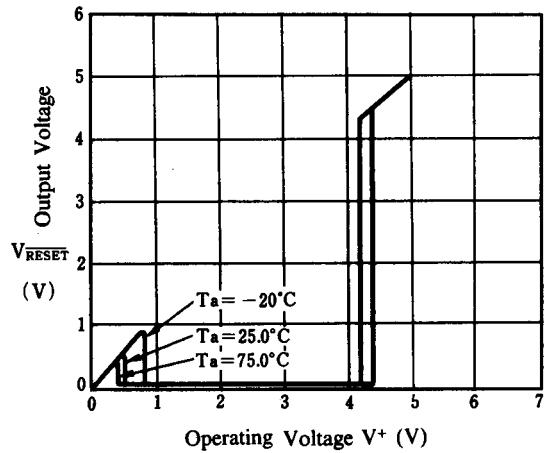
Operating Current 1 vs. Operating Voltage



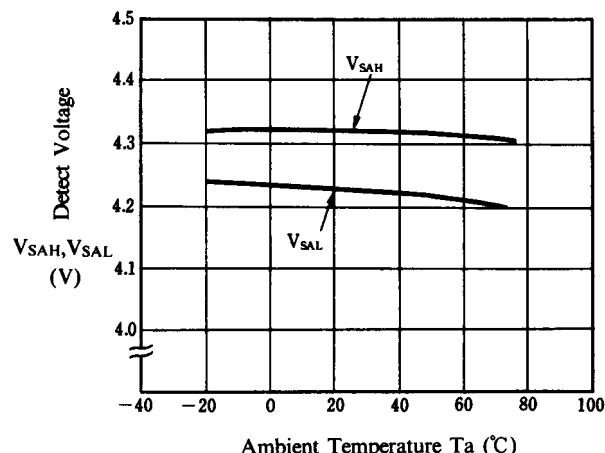
Operating Current 2 vs. Operating Voltage



Output Voltage vs. Operating Voltage

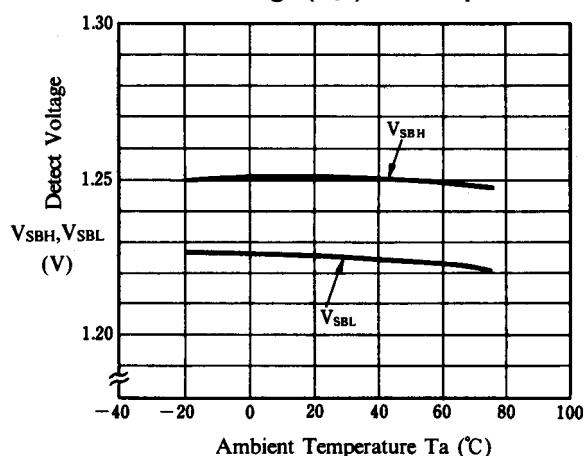


Detect Voltage (V_{SA}) vs. Temperature

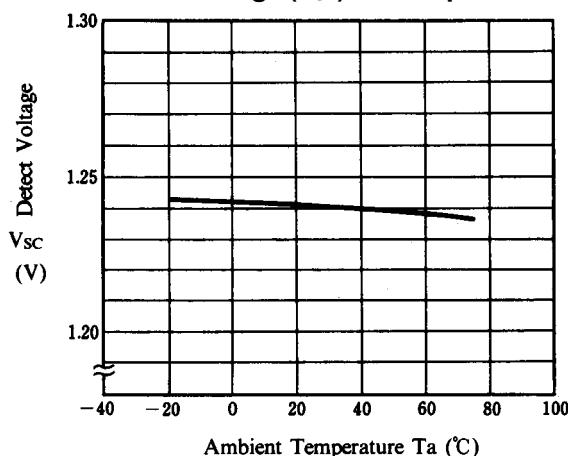


■ TYPICAL CHARACTERISTICS

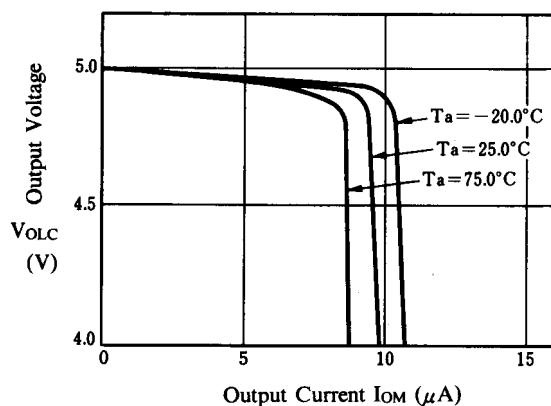
Detect Voltage (V_{SA}) vs. Temperature



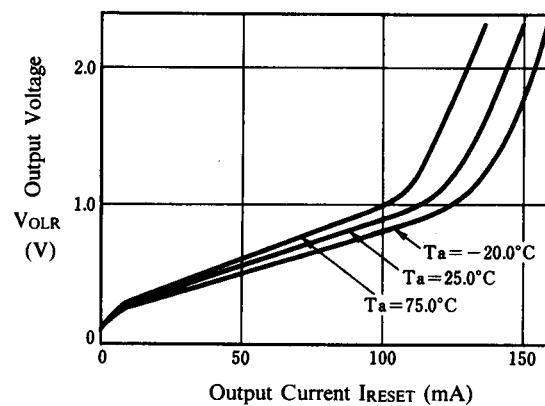
Detect Voltage (V_{SC}) vs. Temperature



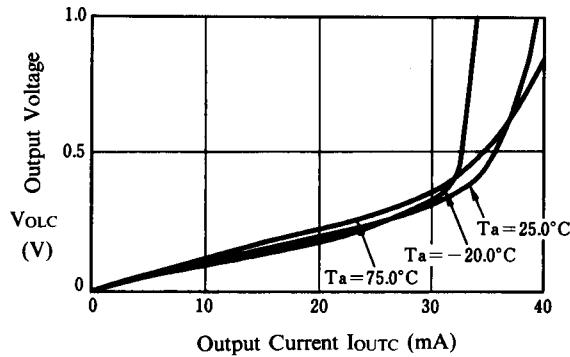
Output Voltage vs. Output Current



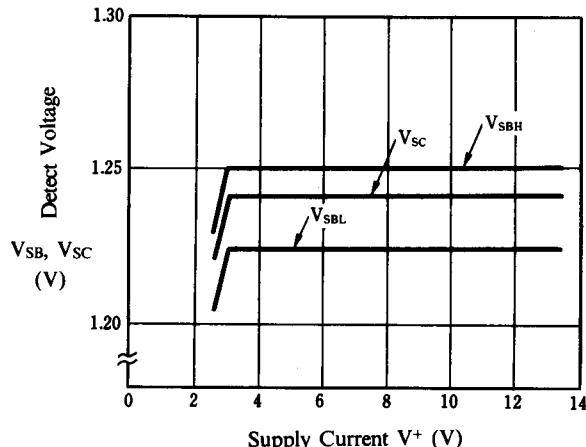
Output Voltage vs. Output Current



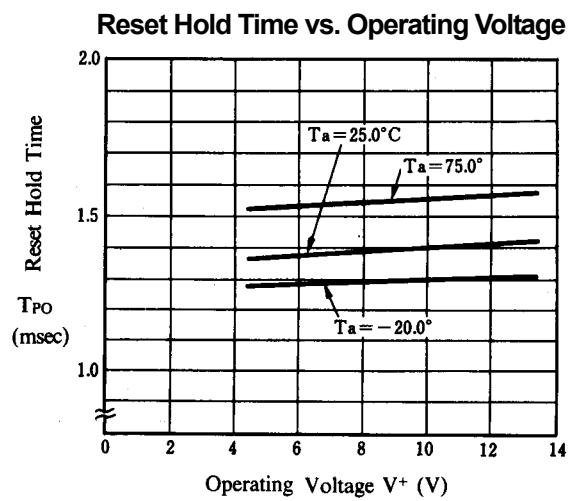
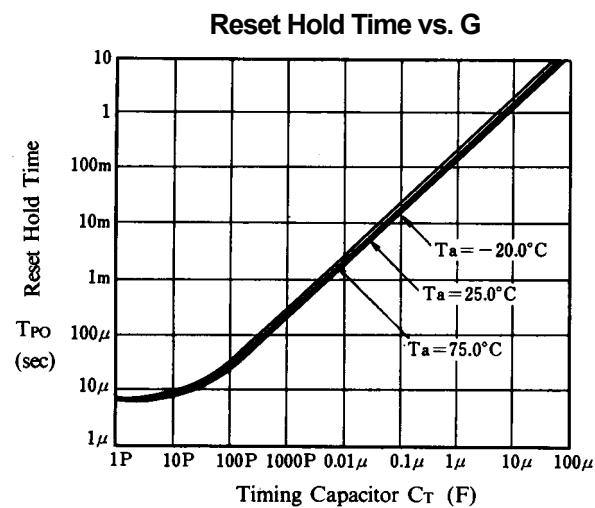
Output Voltage (OUT_C) vs. Output Current (I_{OUTC})



Detect Voltage (V_{SB}, V_{SC}) vs. Supply Voltage



■ TYPICAL CHARACTERISTICS



[CAUTION]
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