

## High-Speed Quad-MOSFET Driver

### Features

- 6 ns Rise and Fall Time
- 2A Peak Output Source and Sink Currents
- 1.8V to 5V Input CMOS Compatible
- Smart Logic Threshold
- Low-jitter Design
- Four Matched Channels
- Drives Two N-channel and Two P-channel MOSFETs
- Outputs can Swing below Ground
- Built-in Level Translator for Negative Gate Bias
- Non-inverting Gate Driver OUTD for Easy Logic
- Low-inductance Quad Flat No-lead Package
- Thermally Enhanced Package

### Applications

- Ultrasound PN Code Transmitter
- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-destructive Testing
- High-speed Level Translator
- High-voltage Bipolar Pulser

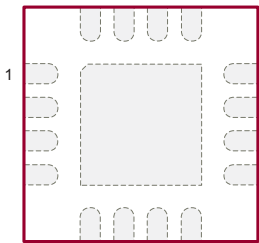
### General Description

The MD1813 is a high-speed quad-MOSFET driver. It is designed to drive two N-channel and two P-channel, high-voltage, DMOS FETs for medical ultrasound applications and may be used in any application requiring a high output current for a capacitive load. The input stage of the MD1813 is a high-speed level translator that is able to operate from logic input signals of 1.8V to 5V amplitude. An adaptive threshold circuit is used to set the level translator threshold to the average of the input logic 0 and logic 1 levels. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1813 has separate power connections, enabling the output signal L and H levels to be chosen independently from the driver supply voltages. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and -5V and the output L and H levels may be varied anywhere over the range of -5V to +5V. The output stage is capable of peak currents of up to  $\pm 2$  amps, depending on the supply voltages used and load capacitance. The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Second, when OE is low, the outputs are disabled, with the A output high and the B output low. This assists in properly pre-charging the coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS. A built-in level shifter is for PMOS gate negative bias driving. It enables the user-defined damping control to generate return-to-zero bipolar output pulses. The MD1813 has a non-inverting driver OUTD for easy logic.

### Package Type

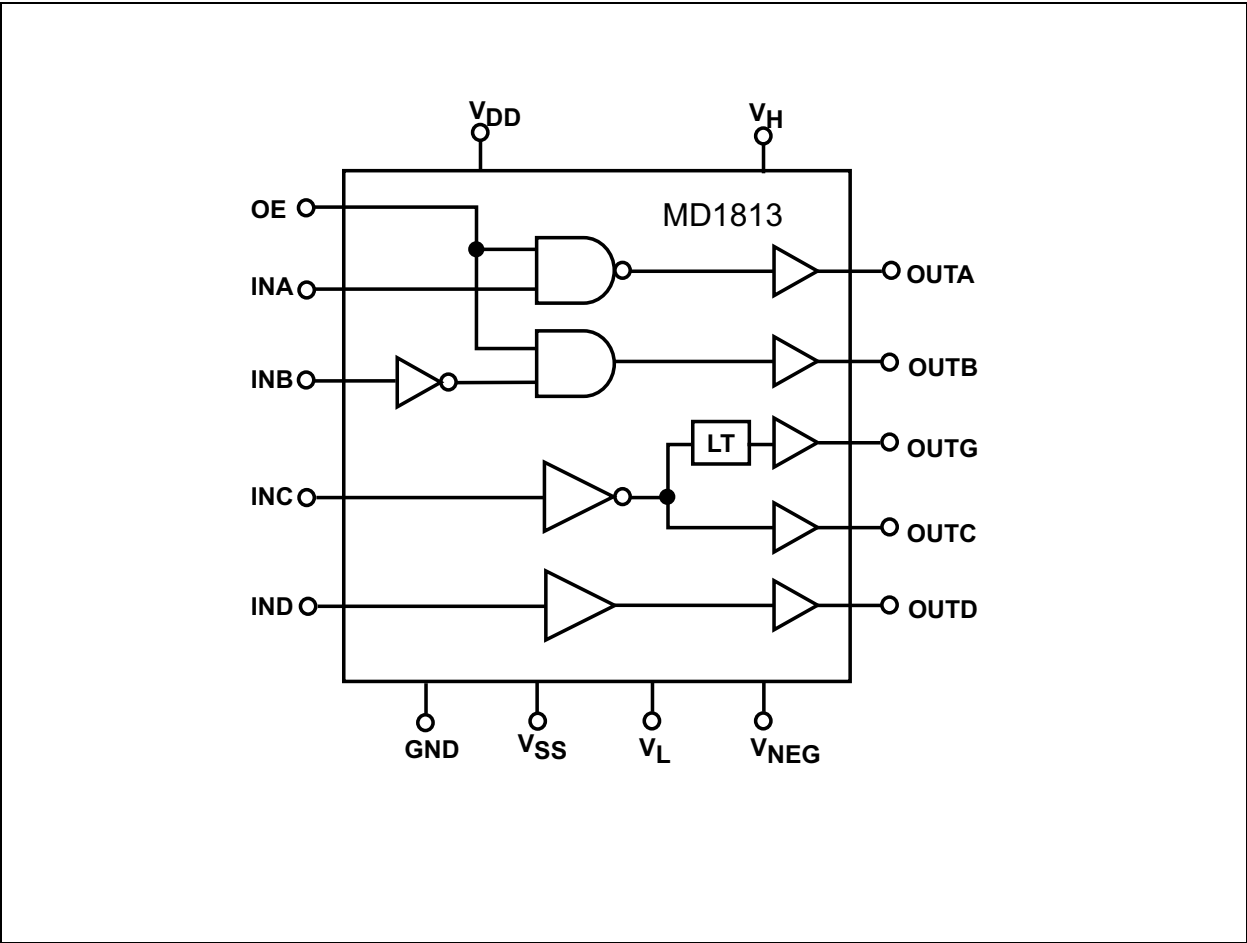
**16-lead QFN**  
(Top view)



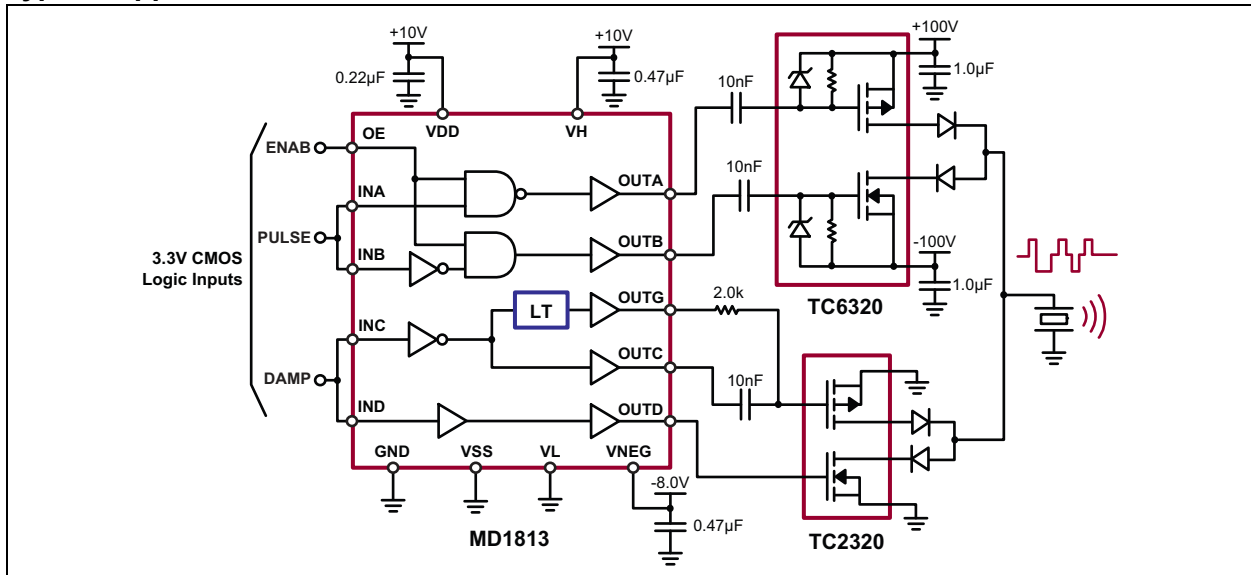
See [Table 2-1](#) for pin information.

# MD1813

## Functional Block Diagram



## Typical Application Circuit



# MD1813

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Supply Voltage, $V_{DD}-V_{SS}$	-0.5V to +13.5V
Output High Supply Voltage, $V_H$	$V_L-0.5V$ to $V_{DD}+0.5V$
Output Low Supply Voltage, $V_L$	$V_{SS}-0.5V$ to $V_H+0.5V$
Low-side Supply Voltage, $V_{SS}$	-7V to +0.5V
Supply Voltage, $V_{DD}-V_{NEG}$	-0.5V to +20V
Negative Supply Voltage, $V_{NEG}-V_{SS}$	$V_{SS}-10V$ to $V_{SS}+0.5V$
Logic Input Levels	$V_{SS}-0.5V$ to GND +7V
Maximum Junction Temperature, $T_J$	+125°C
Operating Ambient Temperature, $T_A$	-20°C to +85°C
Storage Temperature, $T_S$	-65°C to +150°C
Power Dissipation	2.2W
ESD Rating ( <b>Note 1</b> )	ESD Sensitive

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Device is ESD sensitive. Handling precautions are recommended.

### DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD} = 12V$ , $V_L = V_{SS} = GND = 0V$ , $V_{NEG} = -6V$ , $V_{OE} = 3.3V$ and $T_A = 25^\circ C$							
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
Supply Voltage	$V_{DD}-V_{SS}$	4.5	—	13	V	$2.5V \leq V_{DD} \leq 13V$	
Supply Voltage	$V_{DD}-V_{NEG}$	—	—	18	V		
Low-side Supply Voltage	$V_{SS}$	-5.5	—	0	V		
Output High Supply Voltage	$V_H$	$V_{SS}+2$	—	$V_{DD}$	V		
Output Low Supply Voltage	$V_L$	$V_{SS}$	—	$V_{DD}-2$	V		
Negative Supply Voltage	$V_{NEG}$	-9	—	$V_{SS}-2$	V	May be connected to $V_{SS}$ if OUTG is not used.	
$V_{DD}$ Quiescent Current	$I_{DDQ}$	—	1.5	—	mA	No input transitions, OE = 1	
$V_H$ Quiescent Current	$I_{HQ}$	—	—	10	$\mu A$		
$V_{NEG}$ Quiescent Current	$I_{NEGQ}$	—	150	—	$\mu A$		
$V_{DD}$ Average Current	$I_{DD}$	—	7	—	mA	One channel on at 5 MHz, no load	
$V_H$ Average Current	$I_H$	—	22	—	mA		
$V_{NEG}$ Average Current	$I_{NEG}$	—	1.5	—	mA		
Input Logic Voltage High	$V_{IH}$	$V_{OE}-0.3$	—	5	V	For logic inputs INA, INB, INC and IND	
Input Logic Voltage Low	$V_{IL}$	0	—	0.3	V		
Input Logic Current High	$I_{IH}$	—	—	1	$\mu A$		
Input Logic Current Low	$I_{IL}$	—	—	1	$\mu A$		
OE Input Logic Voltage High	$V_{IH}$	1.7	—	5	V	For logic input OE	
OE Input Logic Voltage Low	$V_{IL}$	0	—	0.3	V		
OE Input Resistance	$R_{IN}$	10	20	30	k $\Omega$		
Logic Input Capacitance	$C_{IN}$	—	5	10	pF		
Output Sink Resistance	OUTA-D	$R_{SINK}$	—	—	12.5	$\Omega$	$I_{SINK} = 50\text{ mA}$
	OUTG		—	—	200	$\Omega$	$I_{SINK} = 5\text{ mA}$
Output Source Resistance	OUTA-D	$R_{SOURCE}$	—	—	12.5	$\Omega$	$I_{SOURCE} = 50\text{ mA}$
	OUTG		—	—	200	$\Omega$	$I_{SOURCE} = 5\text{ mA}$

## DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $V_H = V_{DD} = 12V$ , $V_L = V_{SS} = GND = 0V$ , $V_{NEG} = -6V$ , $V_{OE} = 3.3V$ and $T_A = 25^\circ C$						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Output Sink Current	$I_{SINK}$	—	2	—	A	
Peak Output Source Current	$I_{SOURCE}$	—	2	—	A	

## AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD} = 12V$ , $V_L = V_{SS} = GND = 0V$ , $V_{NEG} = -6V$ , $V_{OE} = 3.3V$ and $T_A = 25^\circ C$						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input or OE Rise and Fall Time	$t_{irf}$	—	—	10	ns	Logic input edge speed requirement
Propagation Delay INC to OUTG	$t_{PCG}$	—	40	—	ns	10 M $\Omega$ load to GND
Propagation Delay when Output is from Low to High for OUTA-D	$t_{PLH}$	—	7	—	ns	$C_{LOAD} = 1000$ pF, input signal rise/fall time of 2 ns (See <a href="#">Timing Diagram</a> .)
Propagation Delay when Output is from High to Low for OUTA-D	$t_{PHL}$	—	7	—	ns	
Output Rise Time	$t_r$	—	6	—	ns	
Output Fall Time	$t_f$	—	6	—	ns	
Rise and Fall Time Matching	$ t_r - t_f $	—	1	—	ns	
Propagation Low-to-high and High-to-low Matching	$ t_{PLH} - t_{PHL} $	—	1	—	ns	For each channel
Propagation Delay Matching	$\Delta t_{dm}$	—	$\pm 2$	—	ns	Device-to-device delay match
Output Enable Time	$t_{POE}$	—	9	—	ns	

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Maximum Junction Temperature	$T_J$	—	—	+125	$^\circ C$	
Operating Ambient Temperature	$T_A$	-20	—	+85	$^\circ C$	
Storage Temperature	$T_S$	-65	—	+150	$^\circ C$	
<b>PACKAGE THERMAL RESISTANCE</b>						
16-lead QFN	$\theta_{JA}$	—	25	—	$^\circ C/W$	<a href="#">Note 1</a>

**Note 1:** 1 oz. 4-layer 3" x 4" PCB

# MD1813

## Timing Diagram

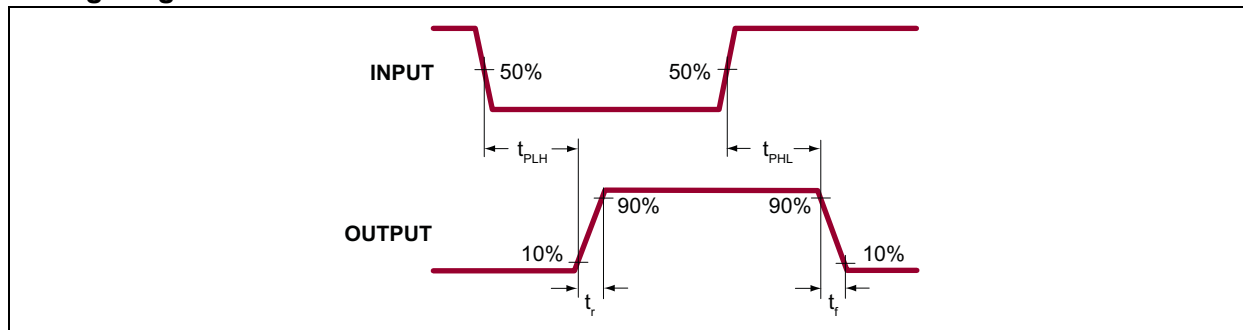


TABLE 1-1: TRUTH FUNCTION TABLE

Logic Inputs			Outputs		
OE	INA	INB	OUTA		OUTB
H	L	L	$V_H$		$V_H$
H	L	H	$V_H$		$V_L$
H	H	L	$V_L$		$V_H$
H	H	H	$V_L$		$V_L$
L	X	X	$V_H$		$V_L$
OE <sup>(1)</sup>	INC	IND	OUTC	OUTG	OUTD <sup>(2)</sup>
—	L	L	$V_H$	$V_{SS}$	$V_L$
—	L	H	$V_H$	$V_{SS}$	$V_H$
—	H	L	$V_L$	$V_{NEG}$	$V_L$
—	H	H	$V_L$	$V_{NEG}$	$V_H$

**Note 1:** No control to OUTG, OUTC or OUTD

**2:** OUTD is non-inverting output.

## 2.0 PIN DESCRIPTION

The details on the pins of MD1813 are listed on [Table 2-1](#). See [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	INB	Logic input. Controls OUTB when OE is high.
2	VL	Supply voltage for N-channel output stage
3	GND	Device ground
4	VNEG	Supply voltage for the auxiliary gate drive. ( <a href="#">Note 1</a> )
5	INC	Logic input. Controls OUTC. Not controlled by OE.
6	IND	Logic input. Controls OUTD. Not controlled by OE.
7	VSS	Supply voltage for low-side analog, level shifter and gate drive circuit
8	OUTD	Output driver
9	OUTC	Output driver
10	OUTG	Not controlled by OE
11	VH	Supply voltage for P-channel output stage
12	OUTB	Output driver
13	OUTA	Output driver
14	VDD	Supply voltage for high-side analog, level shifter and gate drive circuit
15	INA	Logic input. Controls OUTA when OE is high.
16	OE	Output enable logic input (See <a href="#">Figure 3-1</a> .)

**Note 1:** Thermal pad and pin 4, VNEG must be connected externally.

## 3.0 APPLICATION INFORMATION

For proper operation of the MD1813, low-inductance bypass capacitors should be used in the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND and OE pins should be connected to a logic source with a swing of GND to  $V_{CC}$ , where  $V_{CC}$  is 1.8V to 5V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1813 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents due to the capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the  $V_{SS}$  and  $V_L$  pins should have low-inductance feed-through connections directly to a ground plane. If these voltages are not zero, they need bypass capacitors in a manner similar to the positive power supplies. The power connections  $V_{DD}$  should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

Output drivers, OUTA and OUTC drive the gate of an external P-channel MOSFET, while output drivers OUTB and OUTD drive the gate of an external N-channel MOSFET, and they all swing from  $V_H$  to  $V_L$ . The auxiliary output drive, OUTG, swings from  $V_{SS}$  to  $V_{NEG}$ , and drives the external P-channel MOSFET as negative bias via a 2 k $\Omega$  series resistor.

The voltages of  $V_H$  and  $V_L$  decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1  $\mu$ F may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead going to the capacitor. Pay particular attention to minimizing trace lengths, current loop area, and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistor in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

The OE pin sets the threshold level of logic for inputs  $(V_{OE} + V_{GND})/2$ . When OE is low, OUTA is at  $V_H$ . OUTB is at  $V_L$ , regardless of the inputs INA and INB. This pin will not control OUTC, OUTD or OUTG.

Ensure that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. The use of a

solid ground plane and good power and signal layout practices will prevent this problem. Make sure that a circulating ground return current from a capacitive load will not react with common inductance to cause noise voltages in the input logic circuitry. Best timing performance is obtained for OUTC when the voltage of  $V_{SS} - V_{NEG} = V_H - V_L$ . When input logic is high, output will swing to  $V_L$ , and when input logic is low, output will swing to  $V_H$ . All inputs must be kept low until the device is powered up.

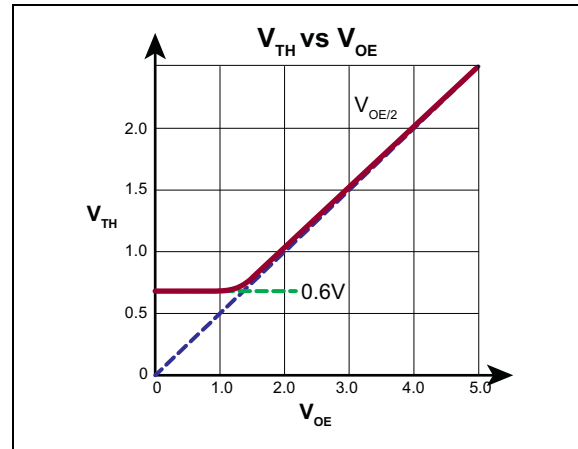


FIGURE 3-1:  $V_{TH}/V_{OE}$  Curve.



## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

16-lead QFN

XXXXXX
XXXXXX
Ⓔ <sup>3</sup> YYWW
NNN

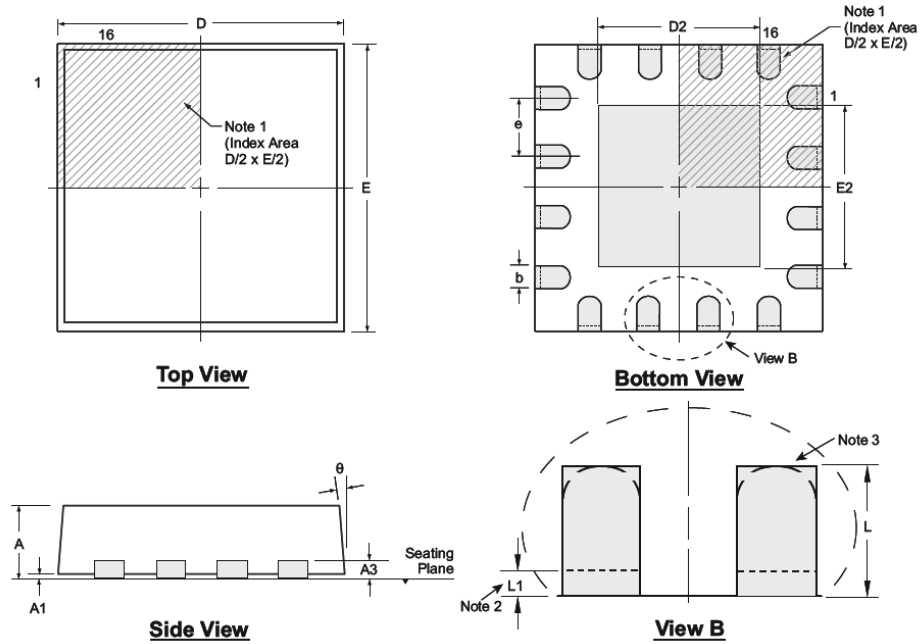
Example

MD
1813K6
Ⓔ <sup>3</sup> 1714
895

<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	Ⓔ <sup>3</sup>	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (Ⓔ <sup>3</sup> ) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

# MD1813

## 16-Lead QFN Package Outline (K6) 4.00x4.00mm body, 1.00mm height (max), 0.65mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	$\theta$	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	2.50	3.85*	2.50	0.65 BSC	0.30 <sup>†</sup>	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40 <sup>†</sup>	-	-
	MAX	1.00	0.05		0.35	4.15*	2.80	4.15*	2.80		0.50 <sup>†</sup>	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

## APPENDIX A: REVISION HISTORY

### Revision A (May 2017)

- Converted Supertex Doc# DSFP-MD1813 to Microchip DS20005747A
- Changed the package marking format
- Changed the quantity of the 16-lead QFN K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

# MD1813

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>				
Device	XX Package Options	-	X Environmental	- X Media Type
Device:	MD1813	=	High-Speed Quad-MOSFET Driver	
Package:	K6	=	16-lead QFN	
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package	
Media Type:	(blank)	=	3300/Reel for a K6 Package	

**Example:**

a) MD1813K6-G: High-Speed Quad-MOSFET Driver, 16-lead QFN, 3300/Reel

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