# ISO224 Reinforced Isolated Amplifier
## With Single-Ended Input of ±12 V and Differential Output of ±4 V

## 1 Features

- Offered in High-Grade (ISO224B) and Low-Grade (ISO224A) Versions
- ±12-V Input Voltage Range Optimized for Isolated Voltage Measurement in Industrial Applications
- Overvoltage Input Clamp With 9-kV ESD
- ±4-V Differential Output Voltage Range With Common-Mode at VDD2 / 2
- Low DC-Error Operation (ISO224B):
  - Input Offset: ±5 mV at 25°C, ±15 µV/°C max
  - Gain Error: ±0.3% at 25°C, ±35 ppm/°C max
  - Nonlinearity: ±0.01% max, ±0.1 ppm/°C typ
- 4.5-V to 18-V Single-Supply on High-Side
- 4.5-V to 5.5-V Operation on Low-Side
- Safety-Related Certifications:
  - 7071-$V_{PEAK}$ Reinforced Isolation per DIN VDE V 0884-11: 2017-01
  - 5000-$V_{RMS}$ Isolation for 1 Minute per UL1577
- High CMTI (ISO224B): 80 kV/µs (typ)

## 2 Applications

- Isolated Analog Signal Acquisition in:
  - Grid Automation
  - Protection Relays
  - Factory Automation and Control
  - Rail Transport
  - Motor Drives
  - Power Analyzers

## 3 Description

The ISO224 is a precision isolated amplifier with an output separated from the input circuitry by an isolation barrier with high immunity to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV$_{RMS}$ with an exceptionally long lifetime and low power dissipation. When used with isolated power supplies, this device separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage devices from damage.

The input of the ISO224 is optimized for accurate sensing of ±10-V signals that are widely used in industrial applications. The device operates of a single supply on the high-side. This unique feature simplifies the design of the isolated power supply and reduces the system cost. The integrated high-side supply voltage detection feature simplifies system level diagnostics. The ±4-V output of the ISO224 allows lower-cost analog-to-digital converters (ADCs) to be used. The differential structure of the output supports high immunity to noise.

The ISO224 is fully specified over the extended industrial temperature range of –55°C to +125°C and is available in a wide-body 8-pin SOIC (DWV) package.

### Device Information[1]

| DEVICE NAME | PACKAGE | BODY SIZE |
|---|---|---|
| ISO224 | SOIC (8) | 5.85 mm × 7.5 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.
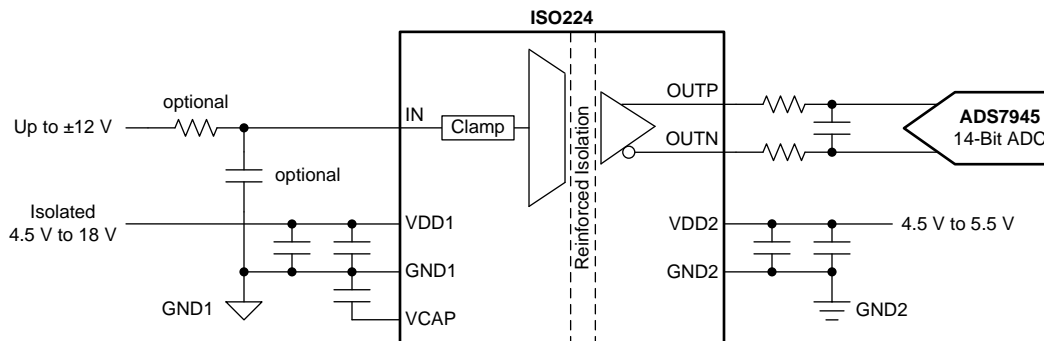
**Simplified Schematic**

## Table of Contents

## 4 Revision History

**Changes from Original (June 2018) to Revision A**           **Page**

# 5 Device Comparison Table

| PARAMETER | ISO224B | ISO224A |
|---|---|---|
| Input offset voltage, $V_{OS}$ | ±5 mV (max) | ±50 mV (max) |
| Input offset drift, $TCV_{OS}$ | ±15 µV/°C (max) | ±60 µV/°C (max) |
| Input-referred noise | 3 µV/$\sqrt{Hz}$ (typ) | 4 µV/$\sqrt{Hz}$ (typ) |
| Gain error, $E_G$ | ±0.3% (max) | ±1% (max) |
| Gain error drift, $TCE_G$ | ±35 ppm/°C (max) | ±60 ppm/°C (max) |
| Nonlinearity | ±0.01% (max) | ±0.02% (max) |
| Output bandwidth, BW | 275 kHz (typ) | 185 kHz (typ) |
| Common-mode transient immunity, CMTI | 80 kV/µs (typ) | 30 kV/µs (typ) |
| IN to OUTP, OUTN signal delay (50% – 50%) | 2.2 µs (typ) | 2.8 µs (typ) |

# 6 Pin Configuration and Functions

**DWV Package**
**8-Pin SOIC**
**Top View**

| | | | |
|---|---|---|---|
| VCAP | 1 | 8 | VDD2 |
| IN | 2 | 7 | OUTP |
| VDD1 | 3 | 6 | OUTN |
| GND1 | 4 | 5 | GND2 |

Not to scale

**Pin Functions**

| PIN NO. | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | VCAP | — | Supply decoupling capacitor.<br>Connect a 0.22-µF capacitor between this pin and the high-side analog ground. |
| 2 | IN | I | Analog input |
| 3 | VDD1 | — | High-side power supply, 4.5 V to 18 V.<br>See the *Power Supply Recommendations* section for decoupling recommendations. |
| 4 | GND1 | — | High-side analog ground |
| 5 | GND2 | — | Low-side analog ground |
| 6 | OUTN | O | Inverting analog output |
| 7 | OUTP | O | Noninverting analog output |
| 8 | VDD2 | — | Low-side power supply, 4.5 V to 5.5 V.<br>See the *Power Supply Recommendations* section for decoupling recommendations. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

see [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power-supply voltage | VDD1 to GND1 | −0.3 | 26 | V |
|  | VDD2 to GND2 | −0.3 | 6.5 |  |
| Input voltage | IN to GND1[2] | −15 | 15 | V |
| Input current | Continuous, at IN pin[3] | −10 | 10 | mA |
| Output voltage | OUTP, OUTN | GND2 − 0.3 | VDD2 + 0.3 | V |
| Temperature | Junction, $T_J$ |  | 150 | °C |
|  | Storage, $T_{stg}$ | −65 | 150 |  |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Exposure to absolute-maximum-rated condition for extended periods may increase input leakage current.
(3) Limit the input current at IN pin to prevent permanent damage to the device. The IN pin is internally protected by a voltage clamp. See Figure 42 for a typical current versus voltage characteristic curve of the input clamp.

## 7.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] — IN pin only | ±9000 | V |
|  |  | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] — All pins except IN | ±3000 |  |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|  |  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
|  | High-side power supply | VDD1 to GND1 | 4.5 | 5 | 18 | V |
|  | Low-side power supply | VDD2 to GND2 | 4.5 | 5 | 5.5 | V |
| **ANALOG INPUT** | | | | | | |
| $V_{Clipping}$ | Input voltage before clipping output[1] | IN to GND1 |  | ±13.8 |  | V |
| $V_{FSR}$ | Specified linear input full-scale voltage[1] | IN to GND1 | −12 |  | 12 | V |
| **TEMPERATURE RANGE** | | | | | | |
| $T_A$ | Specified ambient temperature |  | −55 | 25 | 125 | °C |

(1) See the *Analog Input* section for more details.

Product Folder Links: *ISO224*

## 7.4 Thermal Information

| THERMAL METRIC [1] | | ISO224x | UNIT |
| --- | --- | --- | --- |
| | | DWV (SOIC) | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 96.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 60.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 16.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 58.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Power Ratings[1]

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
| --- | --- | --- | --- | --- |
| $P_D$ | Maximum power dissipation (both sides) | VDD1 = 18 V, VDD2 = 5.5 V | 194.9 | mW |
| | | VDD1 = VDD2 = 5.5 V | 97.4 | |
| $P_{D1}$ | Maximum power dissipation (high-side supply) | VDD1 = 18 V | 140.4 | mW |
| | | VDD1 = 5.5 V | 42.9 | |
| $P_{D2}$ | Maximum power dissipation (low-side supply) | VDD2 = 5.5 V | 54.5 | mW |

(1) See the *Electrical Characteristics* table for maximum supply current specifications.

## 7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance[1] | Shortest pin-to-pin distance through air | ≥ 8.5 | mm |
| CPG | External creepage[1] | Shortest pin-to-pin distance across the package surface | ≥ 8.5 | mm |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the double insulation | ≥ 0.021 | mm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | ≥ 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN VDE V 0884-11 (VDE V 0884-11): 2017-01[2]** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | At AC voltage (bipolar or unipolar) | 2121 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum-rated isolation working voltage | At AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test; see Figure 4 | 1500 | $V_{RMS}$ |
| | | At DC voltage | 2121 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification test) | 7071 | $V_{PK}$ |
| | | $V_{TEST} = 1.2 × V_{IOTM}$, t = 1 s (100% production test) | 8485 | |
| $V_{IOSM}$ | Maximum surge isolation voltage[3] | Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 × V_{IOSM} = 12800\ V_{PK}$ (qualification) | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge[4] | Method A, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 × V_{IORM} = 2545\ V_{PK}$, $t_m = 10$ s | ≤ 5 | pC |
| | | Method A, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.6 × V_{IORM} = 3394\ V_{PK}$, $t_m = 10$ s | ≤ 5 | |
| | | Method B1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s, $V_{pd(m)} = 1.875 × V_{IORM} = 3977\ V_{PK}$, $t_m = 1$ s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output[5] | $V_{IO} = 0.5\ V_{PP}$ at 1 MHz | ~1 | pF |
| $R_{IO}$ | Insulation resistance, input to output[5] | $V_{IO} = 500$ V at $T_A = 25°C$ | > $10^{12}$ | Ω |
| | | $V_{IO} = 500$ V at 100°C ≤ $T_A$ ≤ 125°C | > $10^{11}$ | |
| | | $V_{IO} = 500$ V at $T_S = 150°C$ | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 55/125/21 | |
| **UL1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7071 $V_{DC}$, t = 60 s (qualification), $V_{TEST} = 1.2 × V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test) | 5000 | $V_{RMS}$ |

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

## 7.7  Safety-Related Certifications

| VDE | UL |
|---|---|
| Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11 | Recognized under 1577 component recognition and CSA component acceptance NO 5 programs |
| Reinforced insulation | Single protection |
| File number: 40040142 | File number: E181974 |

## 7.8  Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | $R_{\theta JA}$ = 96.3°C/W, $T_J$ = 150°C, $T_A$ = 25°C, VDD1 = 18 V, VDD2 = 5.5 V, see Figure 2 | | | 55 | mA |
| | | $R_{\theta JA}$ = 96.3°C/W, $T_J$ = 150°C, $T_A$ = 25°C, VDD1 = VDD2 = 5.5 V, see Figure 2 | | | 236 | |
| $P_S$ | Safety input, output, or total power | $R_{\theta JA}$ = 96.3°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 1298[1] | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1)  The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of $I_S$ and $P_S$. These limits vary with the ambient temperature, $T_A$.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side supply voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

## 7.9  Electrical Characteristics

minimum and maximum specifications apply from $T_A$ = –55°C to +125°C, VDD1 = 4.5 V to 18 V, VDD2 = 4.5 V to 5.5 V, $V_{IN}$ = –12 V to 12 V, and $R_{LOAD}$ = 10 kΩ; typical specifications are at $T_A$ = 25°C, and VDD1 = VDD2 = 5 V (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| $V_{OS}$ | Input offset voltage[1] | Initial, at $T_A$ = 25°C, IN = GND1, ISO224B | –5 | ±1 | 5 | mV |
| | | Initial, at $T_A$ = 25°C, IN = GND1, ISO224A | –50 | ±1 | 50 | |
| $TCV_{OS}$ | Input offset voltage drift[1] | ISO224B | –15 | ±3 | 15 | µV/°C |
| | | ISO224A | –60 | ±12 | 60 | |
| $C_{IN}$ | Input capacitance | IN to GND1 | | 2 | | pF |
| $R_{IN}$ | Input resistance | IN to GND1 | 1 | 1.25 | | MΩ |
| $I_{IB}$ | Input bias current | IN = GND1 | | ±15 | | nA |
| $TCI_{IB}$ | Input bias current drift | IN = GND1 | | ±30 | | pA/°C |
| $e_n$ | Input-referred noise density | ISO224B | | 3 | | µV/√Hz |
| | | ISO224A | | 4 | | |

(1)  The typical value includes one sigma statistical variation.

## Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A$ = –55°C to +125°C, VDD1 = 4.5 V to 18 V, VDD2 = 4.5 V to 5.5 V, $V_{IN}$ = –12 V to 12 V, and $R_{LOAD}$ = 10 kΩ; typical specifications are at $T_A$ = 25°C, and VDD1 = VDD2 = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG OUTPUTS** | | | | | | |
| | Nominal gain | $(V_{OUTP} - V_{OUTN}) / V_{IN}$ | | 1/3 | | V/V |
| $E_G$ | Gain error[1] | Initial, at $T_A$ = 25°C, ISO224B | –0.3% | ±0.05% | 0.3% | |
| | | Initial, at $T_A$ = 25°C, ISO224A | –1% | 0.4% | 1% | |
| $TCE_G$ | Gain error drift[1] | ISO224B | –35 | ±10 | 35 | ppm/°C |
| | | ISO224A | –60 | ±20 | 60 | |
| | Nonlinearity | ISO224B | –0.01% | ±0.003% | 0.01% | |
| | | ISO224A | –0.02% | ±0.003% | 0.02% | |
| | Nonlinearity drift | | | ±0.1 | | ppm/°C |
| THD | Total harmonic distortion | $f_{IN}$ = 10 kHz | | –84 | | dB |
| | Output noise | IN = GND1, $f_{IN}$ = 0 Hz, BW = 10 kHz | | 300 | | $\mu V_{RMS}$ |
| | | IN = GND1, $f_{IN}$ = 0 Hz, BW = 100 kHz | | 360 | | |
| PSRR | Power-supply rejection ratio[2] | vs VDD1, at DC | | –107 | | dB |
| | | vs VDD1, 100-mV and 10-kHz ripple | | –101 | | |
| | | vs VDD2, at DC | | –71 | | |
| | | vs VDD2, 100-mV and 10-kHz ripple | | –56 | | |
| $V_{OUT}$ | Output voltage | OUTP or OUTN to GND2 | GND2 + 0.2 | | VDD2 – 0.2 | V |
| $V_{CMout}$ | Common-mode output voltage | $(V_{OUTP} + V_{OUTN}) / 2$ | 0.48 × VDD2 | VDD2 / 2 | 0.52 × VDD2 | V |
| $V_{FAILSAFE}$ | Failsafe output voltage | VDD1 missing, OUTP and OUTN forced to GND2 | | | GND2 + 0.1 | V |
| $I_{SC}$ | Output short-circuit current | On OUTP or OUTN to GND2 | | ±18 | | mA |
| | Overload recovery time | | | 5 | | µs |
| $R_{OUT}$ | Output resistance | On OUTP or OUTN to GND2 | | < 0.5 | | Ω |
| $C_{LOAD}$ | Capacitive load drive[3] | On OUTP or OUTN to GND2 | | | 100 | pF |
| | | OUTP to OUTN | | | 50 | |
| $R_{LOAD}$ | Resistive load | On OUTP or OUTN | | 10 | | kΩ |
| BW | Small signal output bandwidth | ISO224B | 220 | 275 | | kHz |
| | | ISO224A | 150 | 185 | | |
| CMTI | Common-mode transient immunity | |GND1 – GND2| = 1 kV, ISO224B | 55 | 80 | | kV/µs |
| | | |GND1 – GND2| = 1 kV, ISO224A | 15 | 30 | | |
| **POWER SUPPLY** | | | | | | |
| $I_{DD1}$ | High-side supply current | | | 6.1 | 7.8 | mA |
| $I_{DD2}$ | Low-side supply current | | | 7.8 | 9.9 | mA |

(2) This parameter is output referred.
(3) Use series resistor to decouple higher capacilive load.

## 7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Rise time, fall time | ISO224B on OUTP, OUTN | | 1.5 | | µs |
| | | ISO224A on OUTP, OUTN | | 2 | | µs |
| | IN to OUTP, OUTN signal delay (50% – 10%) | ISO224B, unfiltered output, see Figure 1 | | 1.5 | 2 | µs |
| | | ISO224A, unfiltered output, see Figure 1 | | 1.9 | 2.9 | |
| | IN to OUTP, OUTN signal delay (50% – 50%) | ISO224B, unfiltered output, see Figure 1 | | 2.2 | 2.7 | µs |
| | | ISO224A, unfiltered output, see Figure 1 | | 2.8 | 3.8 | |
| | IN to OUTP, OUTN signal delay (50% – 90%) | ISO224B, unfiltered output, see Figure 1 | | 3 | 3.5 | µs |
| | | ISO224A, unfiltered output, see Figure 1 | | 3.8 | 4.8 | |
| $t_{AS}$ | Analog startup time | VDD1 step to 4.5 V with VDD2 ≥ 4.5 V, to OUTP, OUTN valid, 0.1% settling | | 250 | | µs |
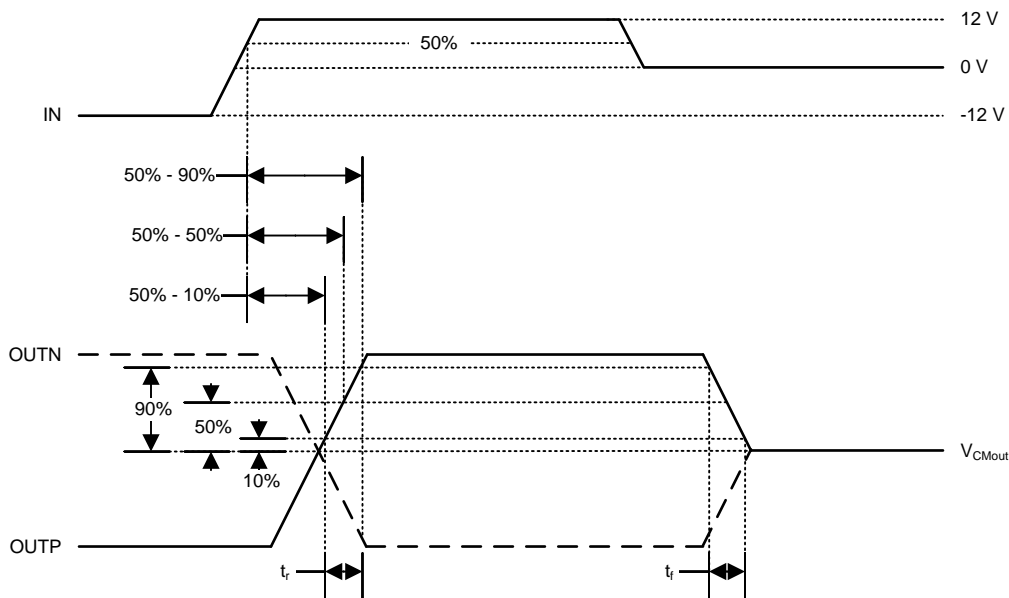


**Figure 1. Delay Time Test Waveforms**

Product Folder Links: ISO224

## 7.11   Insulation Characteristics Curves



**Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE**



**Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE**



$T_A$ up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 $V_{RMS}$, operating lifetime = 135 years

**Figure 4. Reinforced Isolation Capacitor Lifetime Projection**
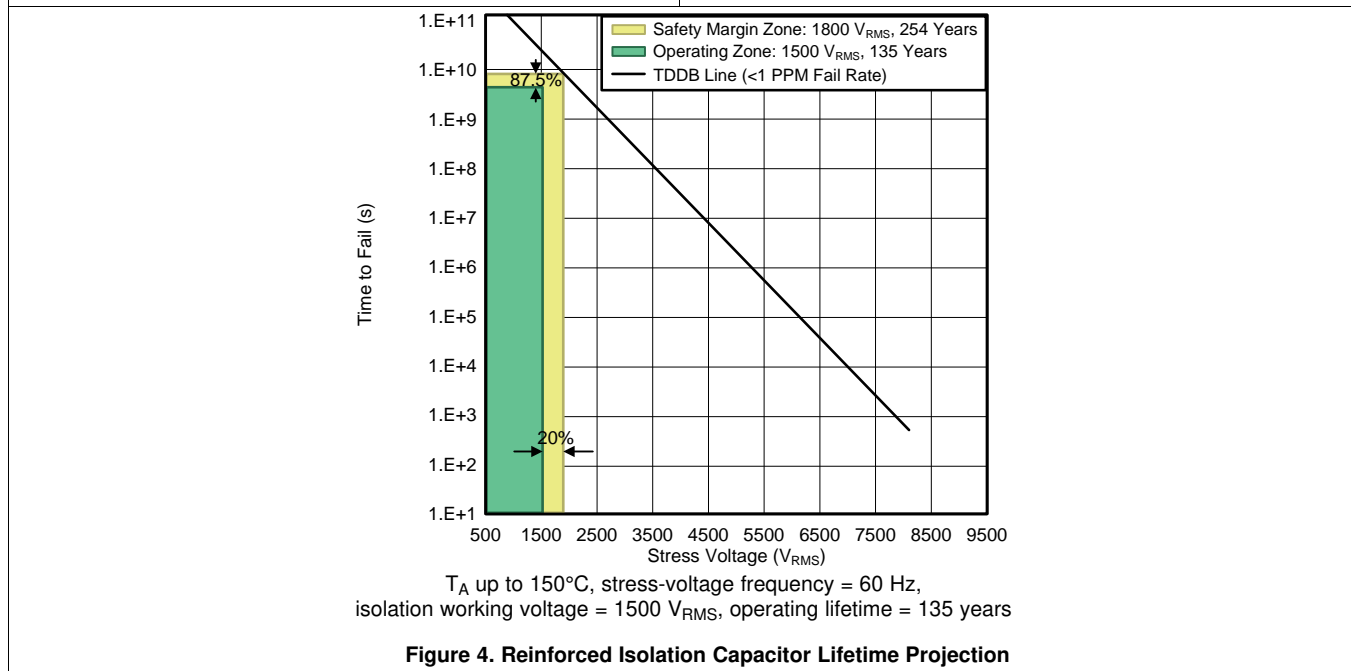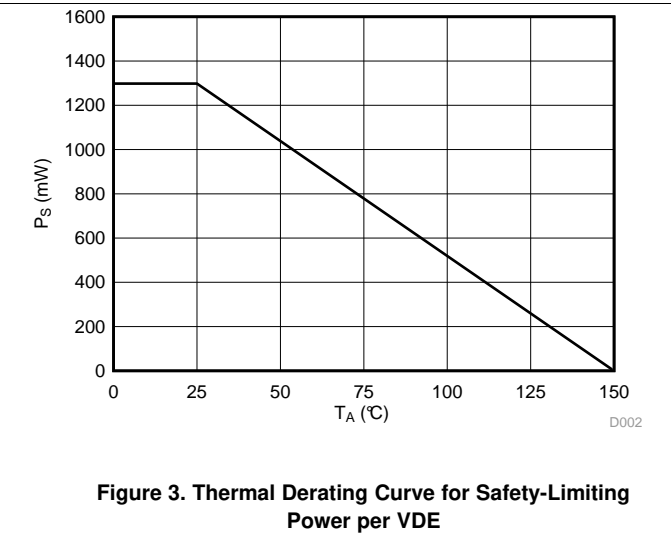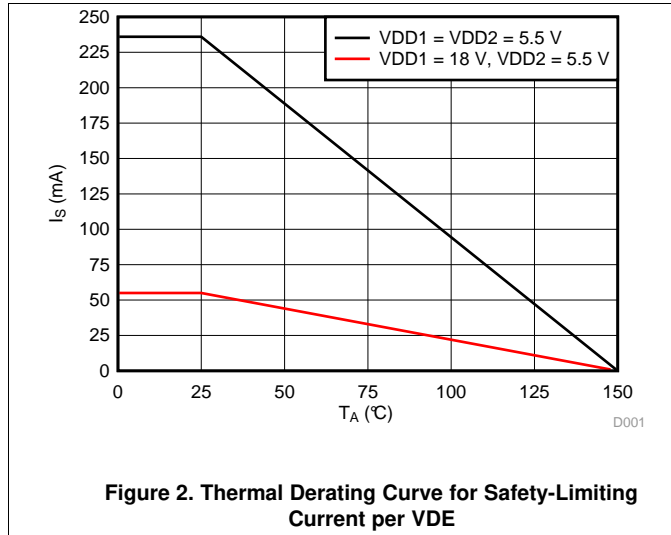
## 7.12 Typical Characteristics

at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.



**Figure 5. Input Offset Voltage Histogram**



**Figure 6. Input Offset Voltage vs High-Side Supply Voltage**



**Figure 7. Input Offset Voltage vs Low-Side Supply Voltage**



**Figure 8. Input Offset Voltage vs Temperature**



**Figure 9. Input Offset Drift Histogram**



**Figure 10. Input Bias Current vs High-Side Supply Voltage**

## Typical Characteristics (continued)

at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = −12 V to 12 V, unless otherwise noted.



**Figure 11. Input Bias Current vs Temperature**



ISO224B

**Figure 12. Input-Referred Noise Density vs Frequency**



ISO224B

**Figure 13. Gain Error Histogram**



ISO224A

**Figure 14. Gain Error Histogram**



**Figure 15. Gain Error vs High-Side Supply Voltage**



**Figure 16. Gain Error vs Low-Side Supply Voltage**

Product Folder Links: *ISO224*

## Typical Characteristics (continued)

at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.
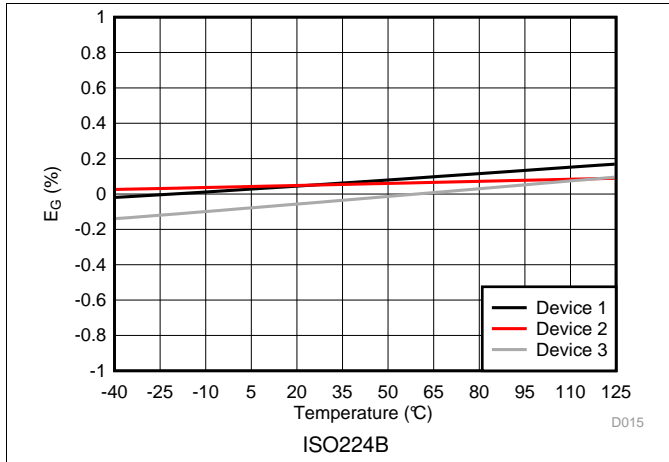


Figure 17. Gain Error vs Temperature
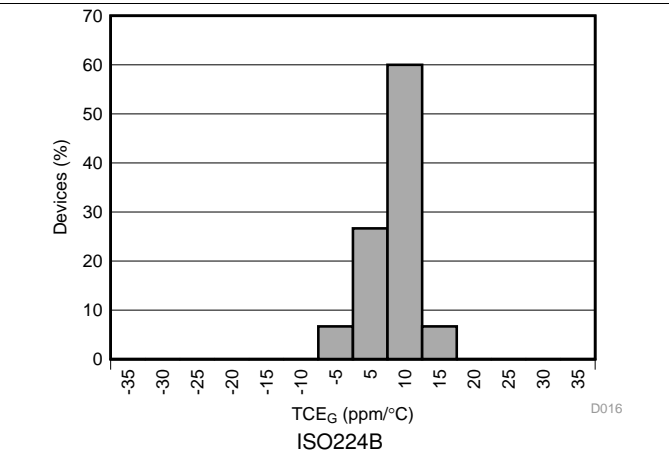


Figure 18. Gain Error Drift Histogram
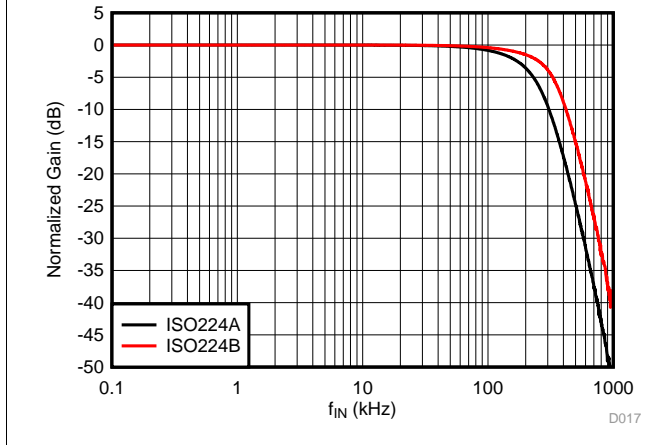


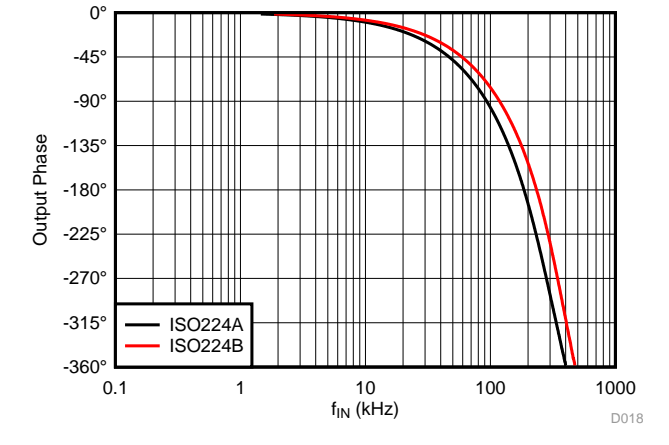Figure 19. Normalized Gain vs Input Frequency
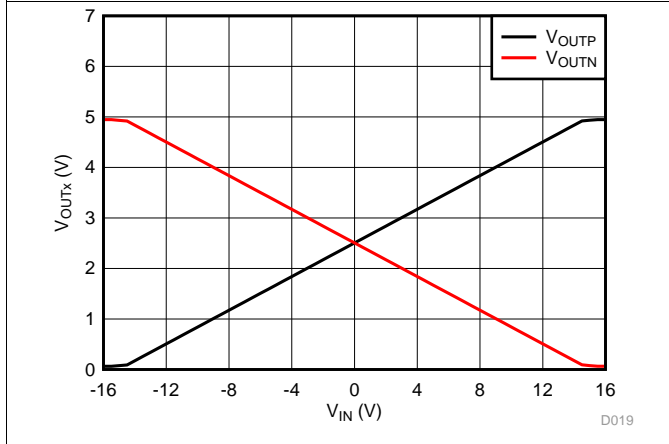


Figure 20. Output Phase vs Input Frequency
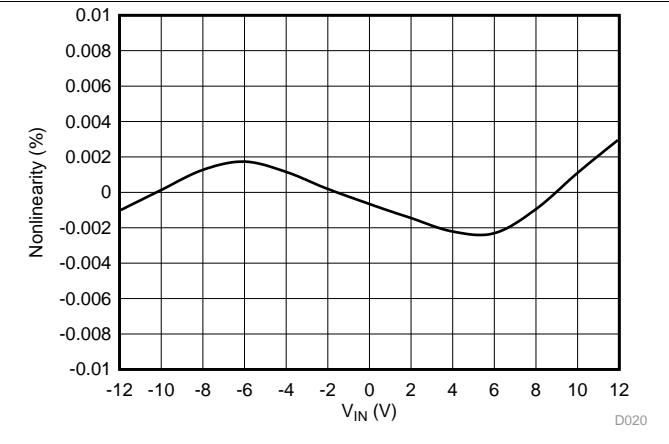


Figure 21. Output Voltage vs Input Voltage



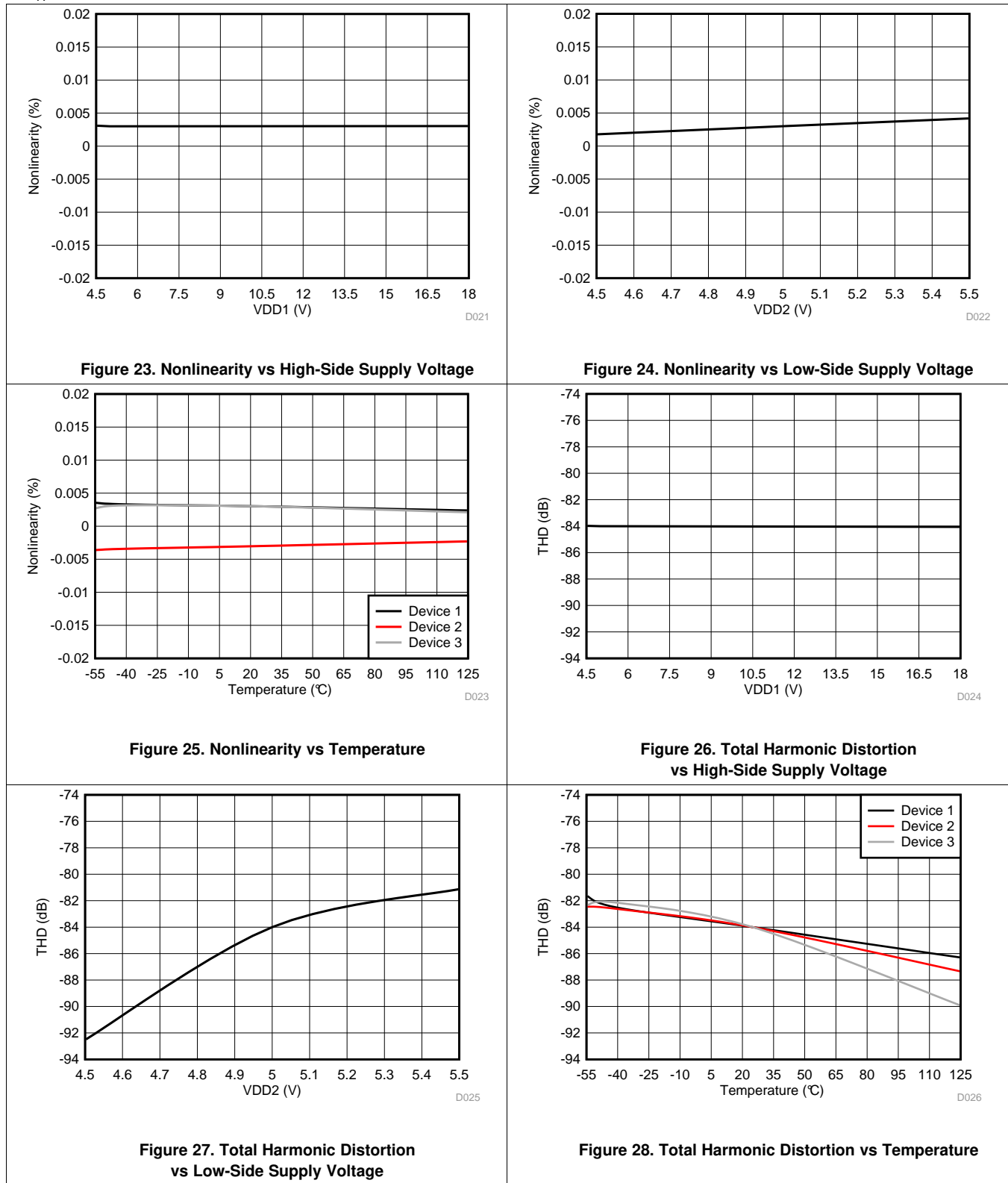Figure 22. Nonlinearity vs Input Voltage

## Typical Characteristics (continued)

at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = −12 V to 12 V, unless otherwise noted.

**Figure 23. Nonlinearity vs High-Side Supply Voltage**

**Figure 24. Nonlinearity vs Low-Side Supply Voltage**

**Figure 25. Nonlinearity vs Temperature**

**Figure 26. Total Harmonic Distortion
vs High-Side Supply Voltage**

**Figure 27. Total Harmonic Distortion
vs Low-Side Supply Voltage**

**Figure 28. Total Harmonic Distortion vs Temperature**

Product Folder Links: *ISO224*

## Typical Characteristics (continued)

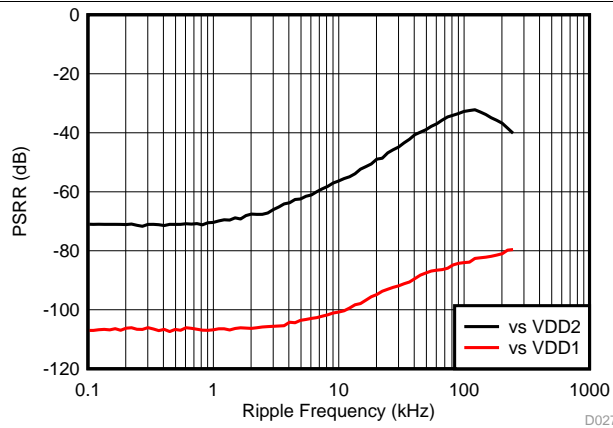at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = −12 V to 12 V, unless otherwise noted.



**Figure 29. Power-Supply Rejection Ratio
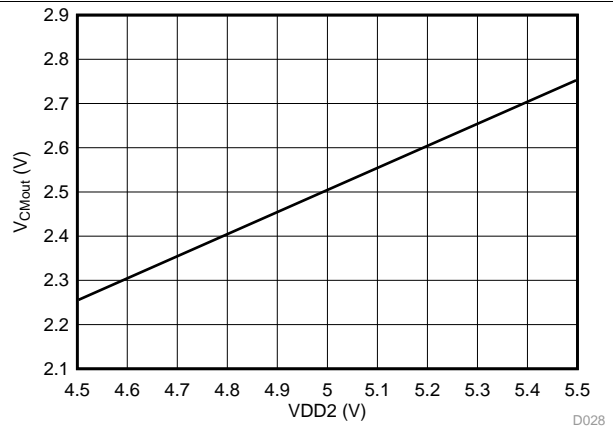vs Ripple Frequency**



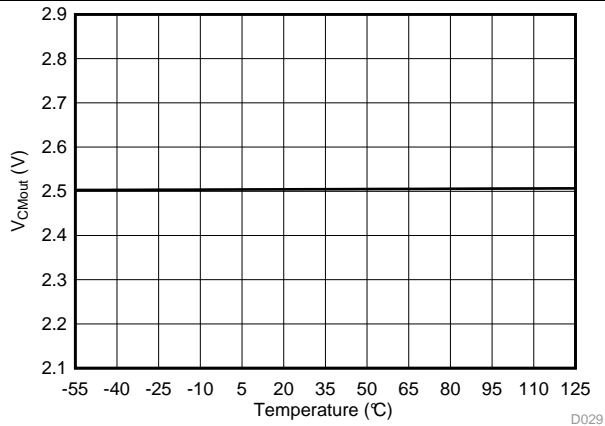**Figure 30. Output Common-Mode Voltage
vs Low-Side Supply Voltage**



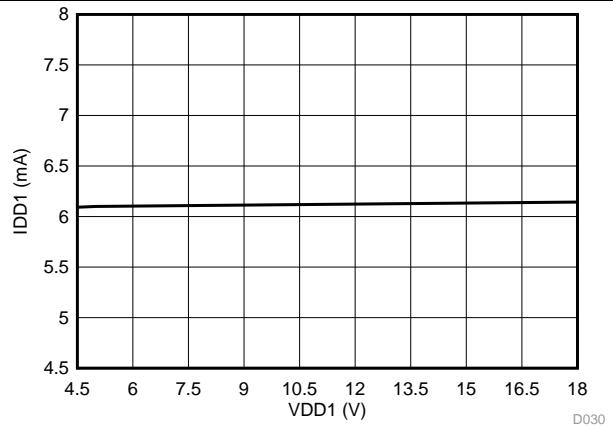**Figure 31. Output Common-Mode Voltage vs Temperature**


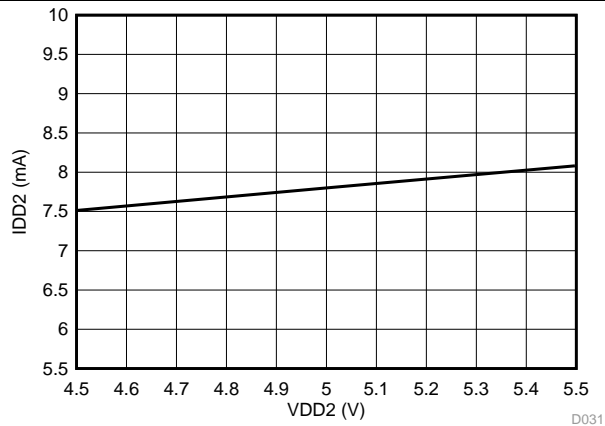
**Figure 32. High-Side Supply Current
vs High-Side Supply Voltage**



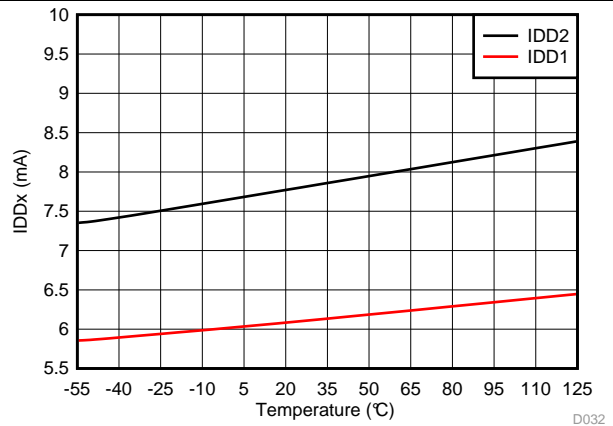**Figure 33. Low-Side Supply Current
vs Low-Side Supply Voltage**



**Figure 34. Supply Current vs Temperature**

Product Folder Links: *ISO224*

## Typical Characteristics (continued)

at $T_A$ = 25°C, VDD1 = VDD2 = 5 V, and VINP = −12 V to 12 V, unless otherwise noted.



**Figure 35. Output Rise and Fall Time
vs Low-Side Supply Voltage**



**Figure 36. Output Rise and Fall Time vs Temperature**



**Figure 37. V$_{IN}$ to V$_{OUT}$ Signal Delay
vs Low-Side Supply Voltage**



**Figure 38. V$_{IN}$ to V$_{OUT}$ Signal Delay
vs Low-Side Supply Voltage**



**Figure 39. V$_{IN}$ to V$_{OUT}$ Signal Delay vs Temperature**



**Figure 40. V$_{IN}$ to V$_{OUT}$ Signal Delay vs Temperature**

Product Folder Links: *ISO224*
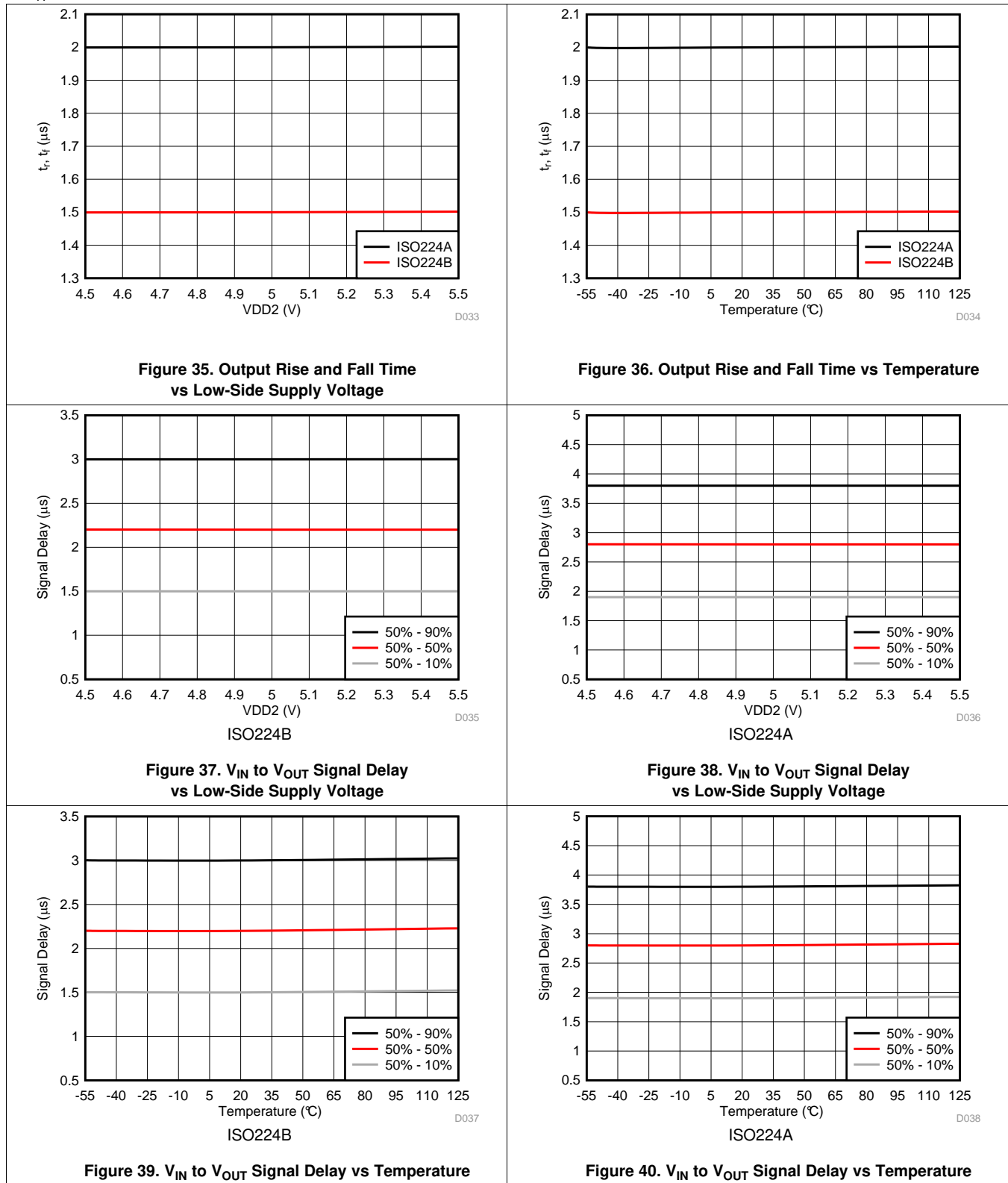
# 8 Detailed Description

## 8.1 Overview

The ISO224 is a precision, isolated amplifier with a high input impedance and wide input voltage range suitable for wide range of industrial applications. The input stage of the device drives a delta-sigma ($\Delta\Sigma$) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram* section) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a digital-to-analog conversion stage on the low-side and presented as a differential analog output.

The SiO$_2$-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the ISO224 and the isolation barrier characteristics result in high reliability and high common-mode transient immunity.

## 8.2 Functional Block Diagram
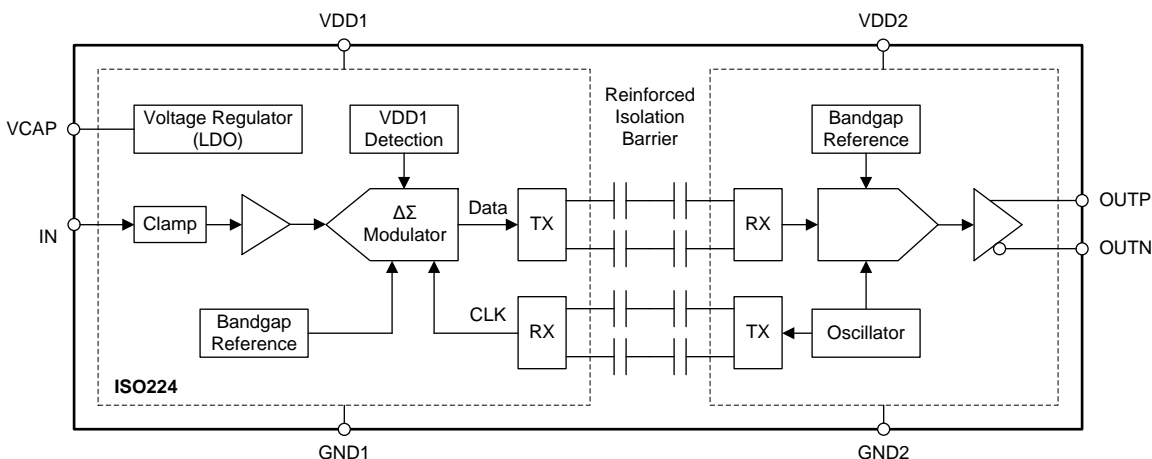
## 8.3 Feature Description

### 8.3.1 Analog Input

The input stage of the ISO224 feeds a switched capacitor, feed-forward $\Delta\Sigma$ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance and low bias-current input of the ISO224 makes the device suitable for isolated voltage sensing applications.

Figure 41 visualizes the difference in the transfer function of the ISO224 depending on the input signal $V_{IN}$, as specified in the *Recommended Operating Conditions* table. With the input voltage within the specified full-scale range $V_{FSR}$, the output of the device changes in a linear way with small error as specified by the nonlinearity parameter in the *Electrical Characteristics* table. If the input signal exceeds the $V_{FSR}$ range, the nonlinearity of the output signals increases and the amplitude clips at $V_{IN} = V_{CLIPPING}$.
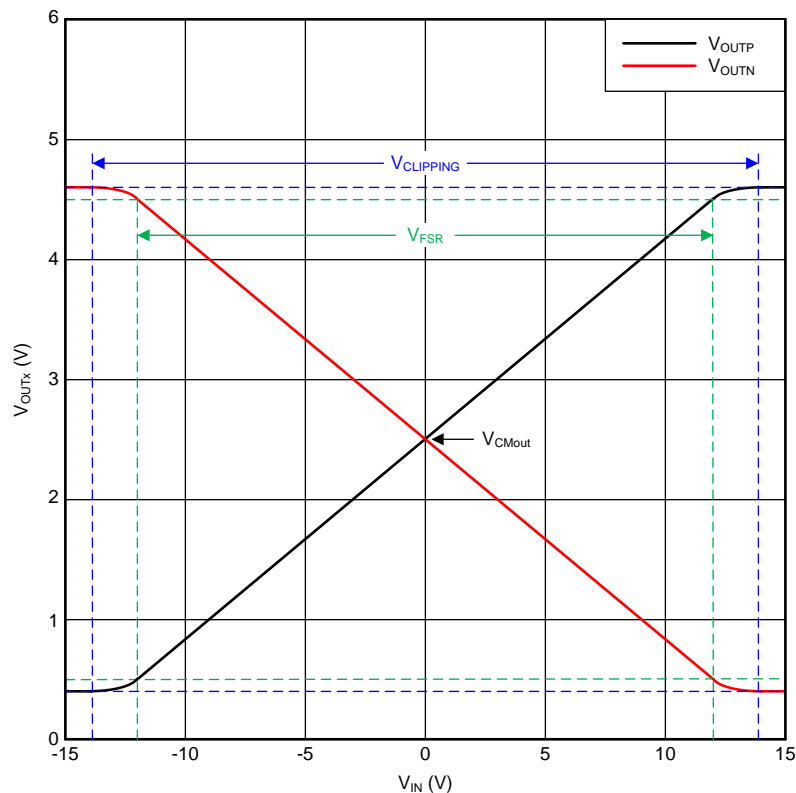


**Figure 41. Transfer Function of the ISO224**

There are two restrictions on the analog input signal at the IN pin. First, if the input voltage $V_{IN}$ exceeds the range of –15 V to 15 V, the current must be limited to 10 mA to prevent damage to the input clamp, see the *Input Clamp Protection Circuit* section for further information. In addition, the linearity and noise performance of the ISO224 are ensured only when the analog input voltage remains within the specified linear full-scale range ($V_{FSR}$).

Product Folder Links: *ISO224*

# Feature Description (continued)

## 8.3.2 Input Clamp Protection Circuit

As illustrated in the *Functional Block Diagram*, the ISO224 features an internal clamp protection circuit on the analog input IN. Using external protection circuits is recommended as a secondary protection scheme to protect the device against surges, ESD events, and electrical fast transient (EFT) conditions.

Figure 42 shows a typical current versus voltage characteristic curve for the input clamp. Limit either the voltage $V_{IN}$ at the input pin IN to the voltage range as defined in the *Recommended Operating Conditions* table or the input current to the limits as defined in the *Absolute Maximum Ratings* table.
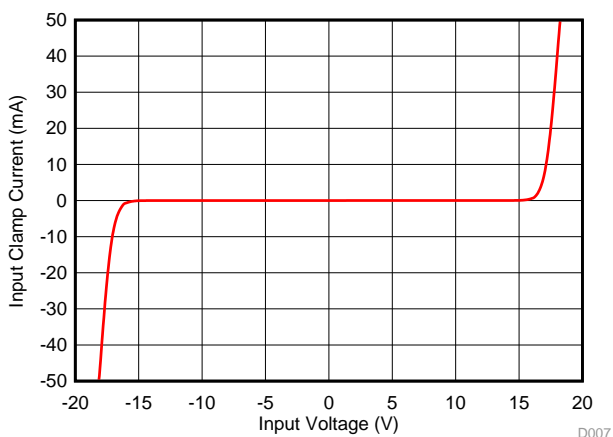


**Figure 42. I-V Curve of the Input Clamp Protection Circuit**

Figure 43 shows a simple method to limit the input current with an external series resistor that is also used as part of the input low-pass filter.



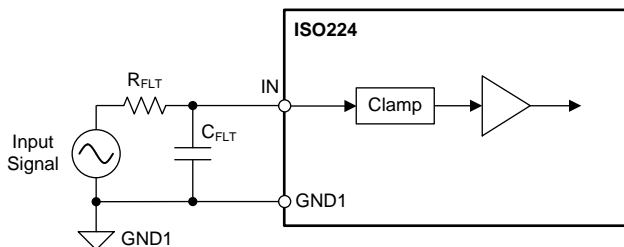**Figure 43. Series Resistor-Based Input Current Limitation on the Analog Inputs of ISO224**

The input overvoltage protection clamp on the ISO224 is intended to control transient excursions on the input pins. Leaving the device in a state such that the clamp circuit is activated for extended periods of time in normal or power-down mode is not recommended because this fault condition can degrade device performance and reliability.

# Feature Description (continued)

### 8.3.3 Isolation Channel Signal Transmission

The ISO224 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the $SiO_2$-based isolation barrier. As shown in Figure 44, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the ISO224 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The ISO224 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.
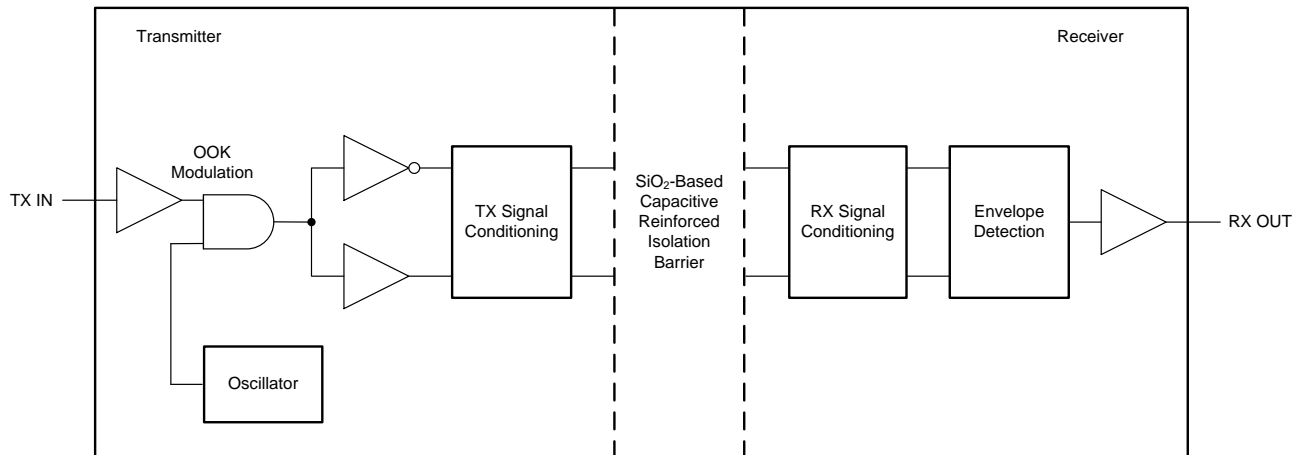


**Figure 44. Block Diagram of an Isolation Channel**
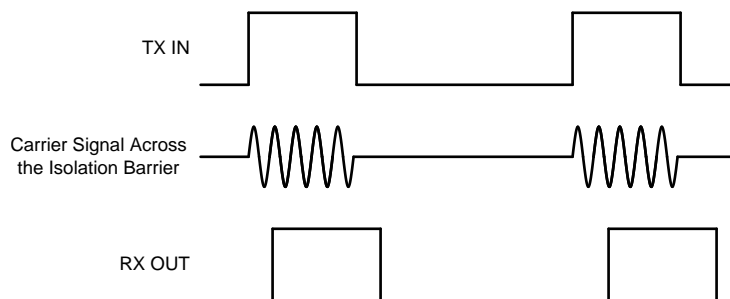
Figure 45 shows the concept of the OOK scheme.



**Figure 45. OOK-Based Modulation Scheme**

**Feature Description (continued)**

### 8.3.4 Fail-Safe Output

The ISO224 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active when the high-side power supply VDD1 of the device is missing, independent of the input signal at the IN pin. Figure 46 shows that in that case both outputs, OUTP and OUTN, of the device are actively driven close to GND2 (see the $V_{FAILSAFE}$ specification in the *Electrical Characteristics* table for details). For easy visualization, an example with the input signal $V_{IN} = 0$ V is shown for the valid VDD1 range of 4.5 V to 5.5 V.
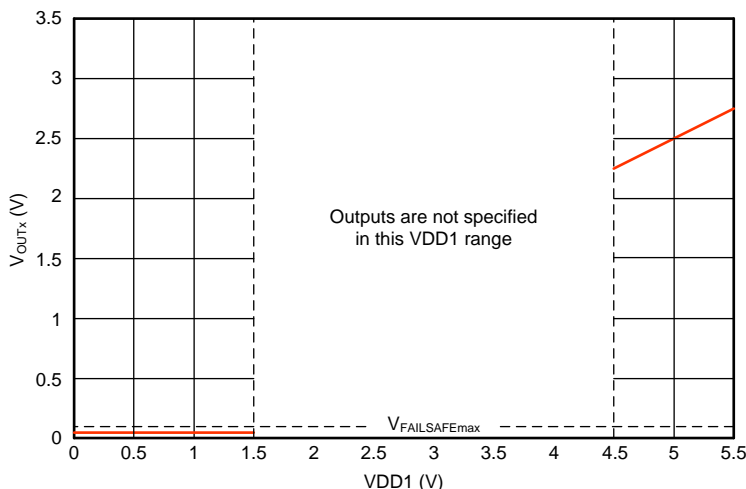


**Figure 46. ISO224 Failsafe Output Behavior With $V_{IN}$ = 0 V**

The *ISO224 Fail-Safe Output Feature* application report describes an example of a comparator-based circuit that detects the missing high-side supply in a system.

## 8.4 Device Functional Modes

The ISO224 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

*Submit Documentation Feedback*          21

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ISO224 enables high-precision measurement of ±10-V signals that are used in a harsh environment in a wide range of industrial applications. The high input resistance of the device simplifies the connection of its input to different sensors or other signal sources. The very low nonlinearity, AC and DC errors, and temperature drift make the ISO224 a robust, high-performance, isolated amplifier for applications where high voltage isolation is required. The differential output with a full-scale voltage of 4 V offers high immunity to noise and allows connection to a wide range of analog-to-digital converters (ADCs) powered on a 5-V nominal supply.

## 9.2 Typical Application

Isolated amplifiers are often used for data acquisition in industrial applications to safely separate the low-voltage portion of the system from the high common-mode voltage input of the system. The input structure of the ISO224 is optimized for isolated voltage sensing in this kind of application.

Figure 47 shows a typical operation of the device for voltage sensing as used in power line monitoring systems. The phase voltage amplitude is reduced with a resistive divider to match the input voltage range of the ISO224. The high input voltage range and the high common-mode transient immunity of the device ensure reliable and accurate operation even in high-noise environments.
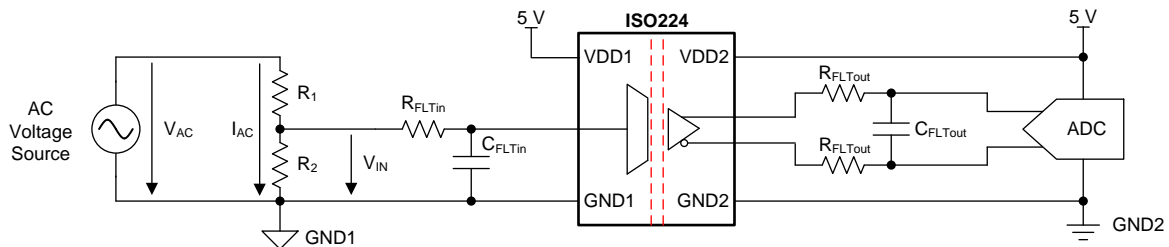


**Figure 47. Using the ISO224 for AC Voltage Sensing**

### 9.2.1 Design Requirements

Table 1 summarizes the typical design requirements for an AC power line voltage sensing application.

**Table 1. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| AC voltage range, $V_{AC}$ | 50 V to 750 V |
| Bandwidth | 600 Hz (minimum) |
| Current through the resistive divider, $I_{AC}$ | 1 mA (maximum) |

Product Folder Links: *ISO224*

### 9.2.2  Detailed Design Procedure

The high-side power supply (VDD1) for the device is generated with a suitable isolated power source. An example of such a circuit is provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the device (VINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current $I_{AC}$ to the desired value: $R_1 + R_2 = V_{AC} / I_{AC}$. The input voltage at the ISO224 results from the resistance ratio of $R_1$ and $R_2$ and the actual AC voltage: $V_{IN} = V_{AC} \times R_2 / (R_1 + R_2)$.

Consider the following two restrictions to choose the proper value of the $R_1$ and $R_2$ resistors:
*   The voltage drop on $R_2$ caused by the nominal AC voltage range of the system must not exceed the recommended input voltage range $V_{IN}$ of the ISO224
*   The voltage drop on $R_2$ caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{IN} \leq V_{Clipping}$

Table 2 lists examples of nominal E96-series (1% accuracy) resistor values for AC systems using 120 V, 240 V, and 400 V as nominal voltages.

**Table 2. Resistor Value Examples**

| PARAMETER | 120-$V_{AC}$ SYSTEM | 240-$V_{AC}$ SYSTEM | 400-$V_{AC}$ SYSTEM |
|---|---|---|---|
| Resistive divider resistor $R_1$ | 115 kΩ | 237 kΩ | 392 kΩ |
| Resistive divider resistor $R_2$ | 12.7 kΩ | 12.4 kΩ | 12.1 kΩ |
| Resulting current through resistive divider $I_{AC}$ | 0.93 mA | 0.93 mA | 0.98 mA |
| Resulting input voltage $V_{IN}$ | ±11.934 V | ±11.933 V | ±11.977 V |

For systems using single-ended input ADCs with a 5-V supply, Figure 48 shows an example of a TLV6001-based signal conversion and filter circuit. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.
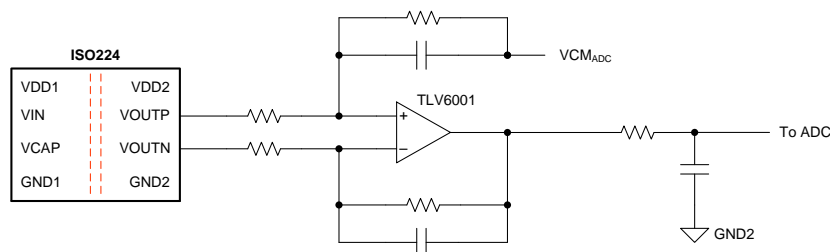


**Figure 48.  Connecting the ISO224 Output to a Single-Ended Input 5-V ADC**

For systems using single-ended, ±10-V input ADCs, the ISO224EVM offers a signal path based on an OPA277 that converts the differential output of the ISO224 and limits the signal bandwidth to 50 kHz.

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, consult the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* TI Precision Designs, available for download at www.ti.com.

### 9.2.3 Application Curves

In some applications the system must be protected in case of an overvoltage condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. Figure 49 shows the typical full-scale step response of the device. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

**Figure 49. Step Response of the ISO224**

Figure 50 shows the typical AC response of the device with a full-scale sine wave with a frequency of 20 kHz applied at the input.

**Figure 50. AC Response of the ISO224 at $f_{IN}$ = 20 kHz**
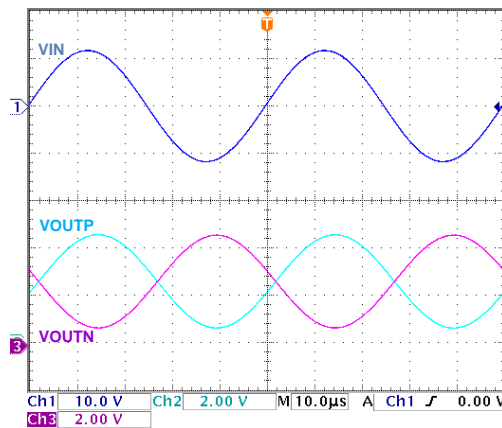
## 9.3 What to Do and What Not to Do

Do not leave the input of the ISO224 unconnected (floating) when the device is powered up. If the device input is left floating, both outputs are at the common-mode output voltage level $V_{CMout}$ as specified in the *Switching Characteristics* table. See the *ISO224 Fail-Safe Output Feature* application report for more details.

# 10 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the ISO224 is generated from the low-side supply (VDD2) of the device by an isolated DC/DC converter circuit. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings. TI recommends using a low-ESR decoupling capacitor of 0.1 µF and an additional capacitor of a minimum 1 µF for both supplies of the ISO224. Figure 51 shows the recommended placement of these decoupling capacitors as close as possible to the ISO224 power-supply pins to minimize supply current loops and electromagnetic emissions.

To decouple the output of the integrated LDO, use a 0.22-µF capacitor placed as close to the VCAP pin of the ISO224 as possible.

The ISO224 does not require any specific power up sequencing. Consider the analog settling time $t_{AS}$ as specified in the *Switching Characteristics* table after ramp up of the VDD1 high-side supply.
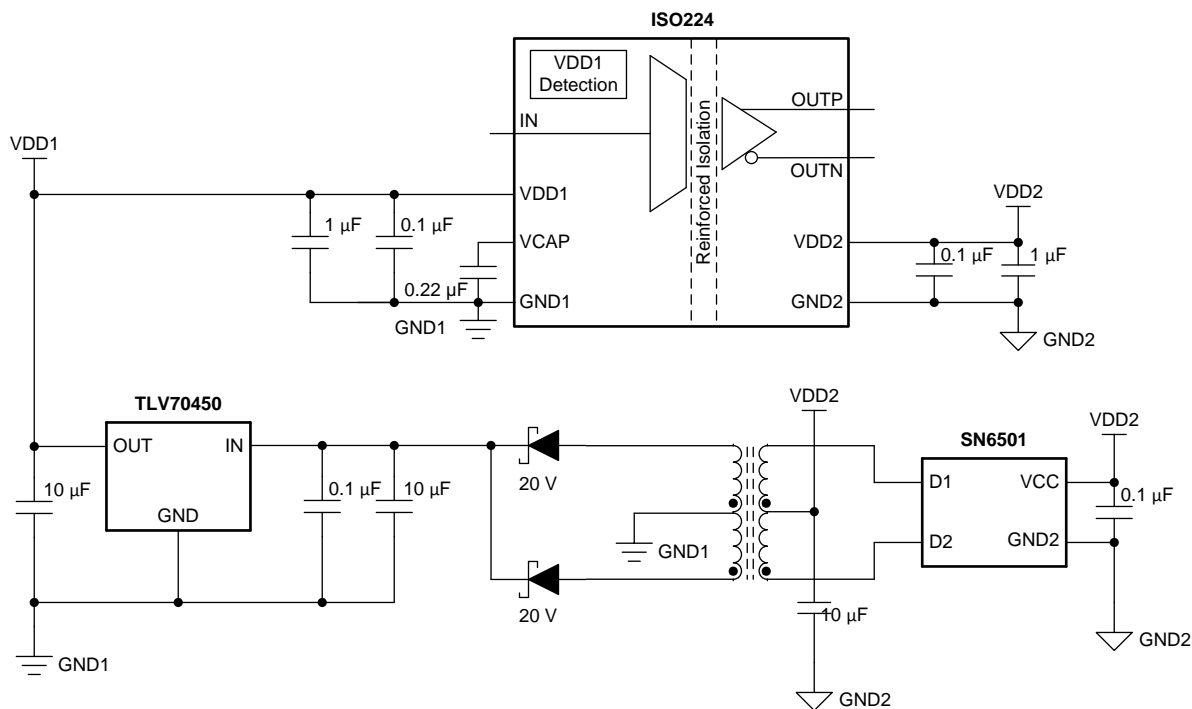


**Figure 51. SN6501-Based, High-Side Power Supply**

# 11 Layout

## 11.1 Layout Guidelines

For best performance, place the 0.22-µF capacitor (C7, as shown in Figure 52) required for decoupling of the internal LDO output as close as possible to the ISO224 VCAP pin. The 0.1-µF ceramic decoupling capacitors for both power supplies (C8 and C9) are located as close as possible to the corresponding VDDx pins followed by the additional 1-µF ceramic capacitors for lower-frequency decoupling (C3 and C12). The resistor and capacitor used for the analog input (R1 and C2) are placed next to the decoupling capacitors. For best performance, use 0603-size or 1206-size, SMD-type, ceramic capacitors with low ESR. Connect the supply voltage sources in a way that allows the supply current to flow through the pads of the decoupling capacitors before powering the device.

Figure 52 shows this approach as implemented on the ISO224EVM. Capacitors C3 and C8 decouple the high-side supply VDD1 and capacitors C9 and C12 are used to support the low-side supply VDD2 of the ISO224.

## 11.2 Layout Example
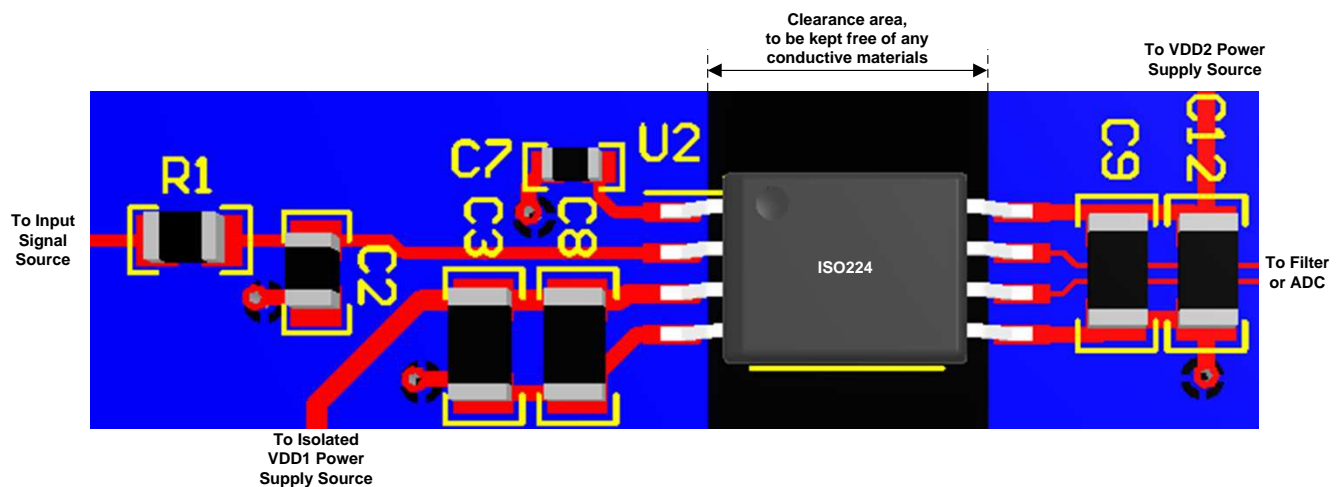


**Figure 52. Recommended Layout of the ISO224**

Product Folder Links: *ISO224*

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:
• Texas Instruments, *Isolation Glossary* application report
• Texas Instruments, *ADS794x 14-Bit, 2 MSPS, Dual-Channel, Differential/Single-Ended, Ultralow-Power Analog-to-Digital Converters* data sheet
• Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
• Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
• Texas Instruments, *ISO224 Fail-Safe Output Feature* application report
• Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
• Texas Instruments, *OPAx277 High Precision Operational Amplifiers* data sheet
• Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* TI design
• Texas Instruments, *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* TI design
• Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
• Texas Instruments, *TLV704 24-V Input Voltage, 150-mA, Ultralow $I_Q$ Low-Dropout Regulators* data sheet
• Texas Instruments, *ISO224EVM Evaluation Module* users guide

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO224ADWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO224A | Samples |
| ISO224ADWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO224A | Samples |
| ISO224BDWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO224B | Samples |
| ISO224BDWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -55 to 125 | ISO224B | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
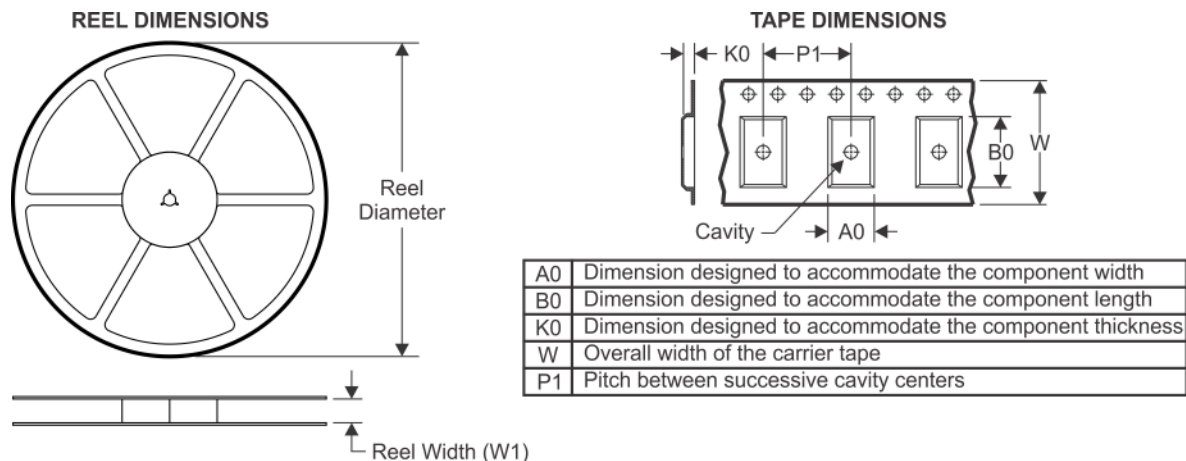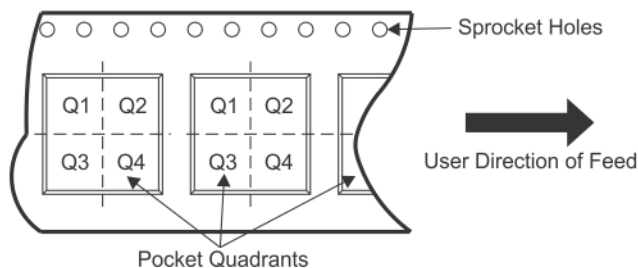
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO224ADWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO224BDWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO224ADWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO224BDWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |

# PACKAGE MATERIALS INFORMATION

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| ISO224ADWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| ISO224BDWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |

PIN 1 ID
AREA

11.5± 0.25
TYP

C

SEATING PLANE

0.1  C

6X  1.27

1

8

5.95
5.75
NOTE 3

2X
3.81

4

5

A

7.6
7.4
NOTE 4

B

8X  0.51
0.31

⊕  0.25 Ⓜ  C  AⓈ  BⓈ

2.8 MAX

0.33
0.13  TYP

SEE DETAIL A

0.25
GAGE PLANE

(2.286)

0°-8°

1.0
0.5

(2)

0.46
0.36

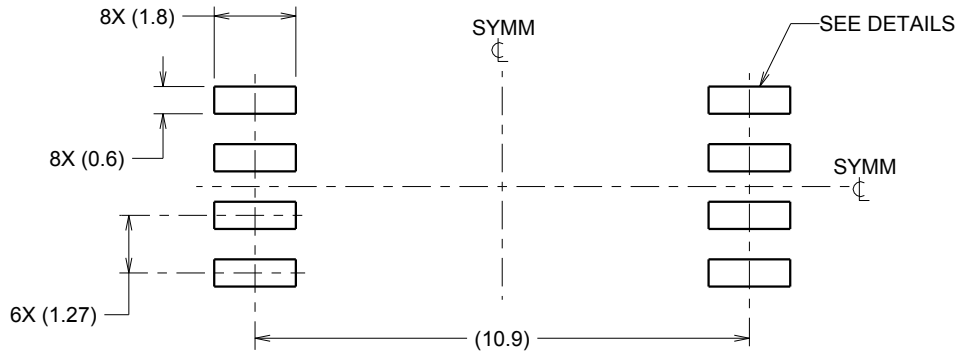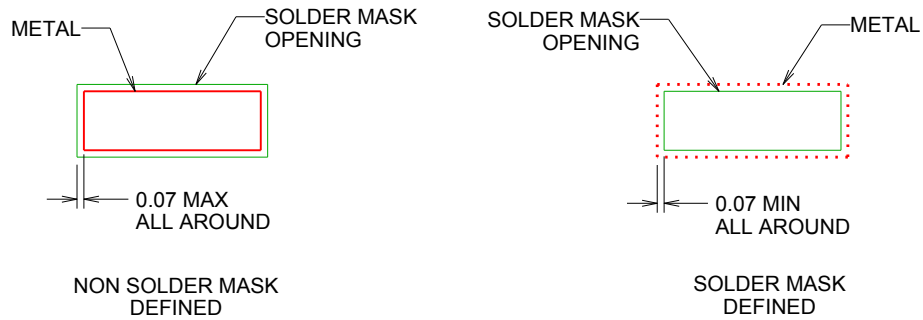DETAIL A
TYPICAL

4218796/A  09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

8X (1.8)

SYMM

SEE DETAILS

8X (0.6)

SYMM

6X (1.27)

(10.9)

**LAND PATTERN EXAMPLE**
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
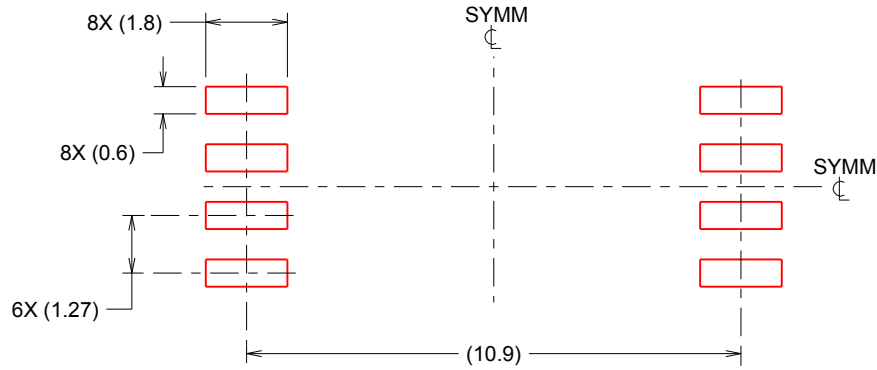ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4218796/A   09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## DWV0008A

SOIC - 2.8 mm max height

SOIC

8X (1.8)

SYMM

8X (0.6)

SYMM

6X (1.27)

(10.9)

### SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A   09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated