

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

MOS INTEGRATED CIRCUIT

μ PD78P054, 78P058

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78P054 and 78P058 are the members of the μ PD78054 Subseries of 78K/0 Series products, in which the on-chip mask ROM of the μ PD78054 and 78058 is replaced with one-time PROM or EPROM.

Because these devices can be programmed by users, they are ideally suited to applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

Caution The reliability of the μ PD78P054KK-T and 78P058KK-T is not guaranteed when used in mass-production applications. Please use these devices only experimentally or for evaluation during trial manufacture.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD78054, 78054Y Subseries User's Manual: U11747E

78K/0 Series User's Manual Instructions: U12326E

FEATURES

- Pin compatible with mask ROM versions (except the V_{PP} pin)
- Internal high-capacity PROM and RAM

Parameter Part Number	Program Memory (PROM)	Internal Data Memory		
		High-Speed RAM	Buffer RAM	Expansion RAM
μ PD78P054	32 Kbytes ^{Note 1}	1024 bytes ^{Note 1}	32 bytes	None
μ PD78P058	60 Kbytes ^{Note 1}			1024 bytes ^{Note 2}

- μ PD78P05xKK-T: Reprogrammable (ideal for system evaluation)
- μ PD78P05xGC, 78P05xGK: Programmable once only (ideal for small-scale production)
- Operable in the same supply voltage range as mask ROM versions ($V_{DD} = 2.0$ to 6.0 V)
- Corresponding to QTOP™ microcontrollers

- Notes**
1. The internal PROM and internal high-speed RAM capacity can be changed using the internal memory size switching register (IMS).
 2. The internal expansion RAM capacity can be changed using the internal expansion RAM size switching register (IXS).

- Remarks**
1. QTOP microcontroller is the general name of the microcontrollers with one-time PROM that are totally supported by the NEC writing service (from writing to marking, screening, and testing).
 2. For the differences between PROM versions and mask ROM versions, refer to **1. DIFFERENCES BETWEEN μ PD78P054, 78P058 AND MASK ROM VERSIONS.**

In this document, "PROM" is used in sections common to the one-time PROM and EPROM versions.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

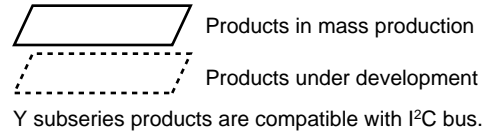
ORDERING INFORMATION

	Part Number	Package	Internal ROM	Quality Grade
★	μ PD78P054GC-8BT	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	One-time PROM	Standard
	μ PD78P054GK-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	One-time PROM	Standard
	μ PD78P054KK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM	Not applicable
	μ PD78P058GC-8BT	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	One-time PROM	Standard
	μ PD78P058KK-T	80-pin ceramic WQFN (14 × 14 mm)	EPROM	Not applicable

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



78K/0 Series

Pin Count	Subseries Name	Description
Control		
100-pin	μPD78075B	EMI-noise reduced version of the μPD78078
100-pin	μPD78078	μPD78054 with timer added and enhanced external interface
100-pin	μPD78078Y	
100-pin	μPD78070A	ROM-less version of the μPD78078
100-pin	μPD78070AY	
100-pin	μPD780018AY	μPD78078Y with enhanced serial I/O and limited functions
80-pin	μPD780058	μPD78054 with enhanced serial I/O
80-pin	μPD780058Y	
80-pin	μPD78058F	EMI-noise reduced version of the μPD78054
80-pin	μPD78058FY	
80-pin	μPD78054	μPD78018F with added UART and D/A converter and enhanced I/O
80-pin	μPD78054Y	
80-pin	μPD780065	μPD780024 with increased RAM capacity
64-pin	μPD780078	A timer added to the μPD780034A and serial I/O enhanced
64-pin	μPD780078Y	
64-pin	μPD780034A	μPD780024 with enhanced A/D converter
64-pin	μPD780034AY	
64-pin	μPD780024A	μPD78018F with enhanced serial I/O
64-pin	μPD780024AY	
64-pin	μPD78014H	EMI-noise reduced version of the μPD78018F
64-pin	μPD78018F	Basic subseries for control
64-pin	μPD78018FY	
42/44-pin	μPD78083	On-chip UART, capable of operating at low voltage (1.8 V)
Inverter control		
64-pin	μPD780988	On-chip inverter control circuit and UART. EMI-noise reduced.
FIP™ drive		
100-pin	μPD780208	μPD78044F with enhanced I/O and FIP C/D. Display output total: 53
100-pin	μPD780228	μPD78044H with enhanced I/O and FIP C/D. Display output total: 48
80-pin	μPD780232	For panel control. On-chip FIP C/D. Display output total: 53
80-pin	μPD78044H	μPD78044F with added N-ch open drain I/O. Display output total: 34
80-pin	μPD78044F	Basic subseries for driving FIP. Display output total: 34
LCD drive		
100-pin	μPD780308	μPD78064 with enhanced SIO, and increased ROM, RAM capacity.
100-pin	μPD780308Y	
100-pin	μPD78064B	EMI-noise reduced version of the μPD78064
100-pin	μPD78064Y	Basic subseries for driving LCDs, on-chip UART
Call ID supported		
80-pin	μPD780841	On-chip Call ID function, simple DTMF. EMI-noise reduced.
Bus interface supported		
100-pin	μPD780948	On-chip D-CAN controller
80-pin	μPD78098B	μPD78054 with IEBus™ controller added. EMI-noise reduced.
80-pin	μPD780701Y	On-chip D-CAN/IEBus controller
80-pin	μPD780833Y	On-chip controller compliant with J1850 (Class 2)
Meter control		
100-pin	μPD780958	For industrial meter control
80-pin	μPD780955	Ultra low-power consumption. On-chip UART.
80-pin	μPD780973	On-chip automobile meter controller/driver

The major functional differences among the subseries are listed below.

Function Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion						
			8-bit	16-bit	Watch	WDT													
Control	μPD78075B	32K to 40K	4c h	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√						
	μPD78078	48K to 60K									61	2.7 V							
	μPD78070A	—																	
	μPD780058	24K to 60K	2 ch	—	—	—	—	4 ch (UART: 1 ch)	68	1.8 V									
	μPD78058F	48K to 60K							69	2.7 V									
	μPD78054	16K to 60K									2.0 V								
	μPD780065	40K to 48K							—	8 ch		—		3 ch (UART: 2 ch)	52	1.8 V			
	μPD780078	48K to 60K									2 ch				—	—	3 ch (UART: 1 ch)	51	—
	μPD780034A	8K to 32K																1 ch	
	μPD780024A	—	—	—	—	—	—												
	μPD78014H							8K to 60K	—	—	—	—		—					
	μPD78018F	8K to 60K	—	—	—	—	—								—				
μPD78083	8K to 16K	—						—	—	—	—	1 ch (UART: 1 ch)	33	—					
Inverter control	μPD780988	16K to 60K	3 ch	Note	—	1 ch	—	8 ch	—	3 ch (UART: 2 ch)	47	4.0 V	√						
FIP drive	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—						
	μPD780228	48K to 60K	3 ch	—	—	—	4 ch	—	—	1 ch	72	4.5 V							
	μPD780232	16K to 24K	2 ch	1 ch	1 ch					8 ch	—	—		2 ch	40	2.7 V			
	μPD78044H	32K to 48K				1 ch	68												
	μPD78044F	16K to 40K				2 ch	—												
LCD drive	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (time division UART: 1 ch)	57	2.0 V	—						
	μPD78064B	32K								2 ch (UART: 1 ch)									
	μPD78064	16K to 32K																	
Call ID supported	μPD780841	24K to 32K	2 ch	—	1 ch	1 ch	2 ch	—	—	2 ch (UART: 1 ch)	61	2.7 V	—						
Bus interface supported	μPD780948	60K	2 ch	2 ch	1 ch	1 ch	8 ch	—	—	3 ch (UART: 1 ch)	79	4.0 V	√						
	μPD78098B	40K to 60K		1 ch							2 ch	69	2.7 V	—					
Meter control	μPD780958	48K to 60K	4 ch	2 ch	—	1 ch	—	—	—	2 ch (UART: 1 ch)	69	2.2 V	—						
	μPD780955	40K	6 ch	1 ch			1 ch			2 ch (UART: 2 ch)	50	2.2 V							
	μPD780973	24K to 32K	3 ch	—			1 ch			5 ch	2 ch (UART: 1 ch)	56		4.5 V					

Note 16-bit timer: 2 channels

10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Part Number		μPD78P054	μPD78P058
Internal memory	PROM	32 Kbytes ^{Note 1}	60 Kbytes ^{Note 1}
	High-speed RAM	1024 bytes ^{Note 1}	
	Buffer RAM	32 bytes	
	Expansion RAM	None	1024 bytes ^{Note 2}
Memory space		64 Kbytes	
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		Minimum instruction execution time is variable.	
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0-MHz operation)	
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)	
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc. 	
I/O ports		Total: 69 <ul style="list-style-type: none"> • CMOS input: 2 • CMOS input/output: 63 • N-ch open-drain input/output: 4 	
A/D converter		8-bit resolution × 8 ch	
D/A converter		8-bit resolution × 2 ch	
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O, SBI, or 2-wire serial I/O mode selectable: 1 ch • 3-wire serial I/O mode (with on-chip max. 32-byte automatic transmit/receive function): 1 ch • 3-wire serial I/O or UART mode selectable: 1 ch 	
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter: 1 ch • 8-bit timer/event counter: 2 ch • Watch timer: 1 ch • Watchdog timer: 1 ch 	
Timer outputs		3 (14-bit PWM output capable: 1)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (@ 5.0-MHz operation with main system clock)	
Vectored interrupt sources	Maskable	Internal: 13, external: 7	
	Non-maskable	Internal: 1	
	Software	1	
Test inputs		Internal: 1, external: 1	
Supply voltage		V _{DD} = 2.0 to 6.0 V	
Operating ambient temperature		T _A = -40 to +85°C	
Package		<ul style="list-style-type: none"> • 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) : μPD78P054 only • 80-pin ceramic WQFN (14 × 14 mm) 	

★

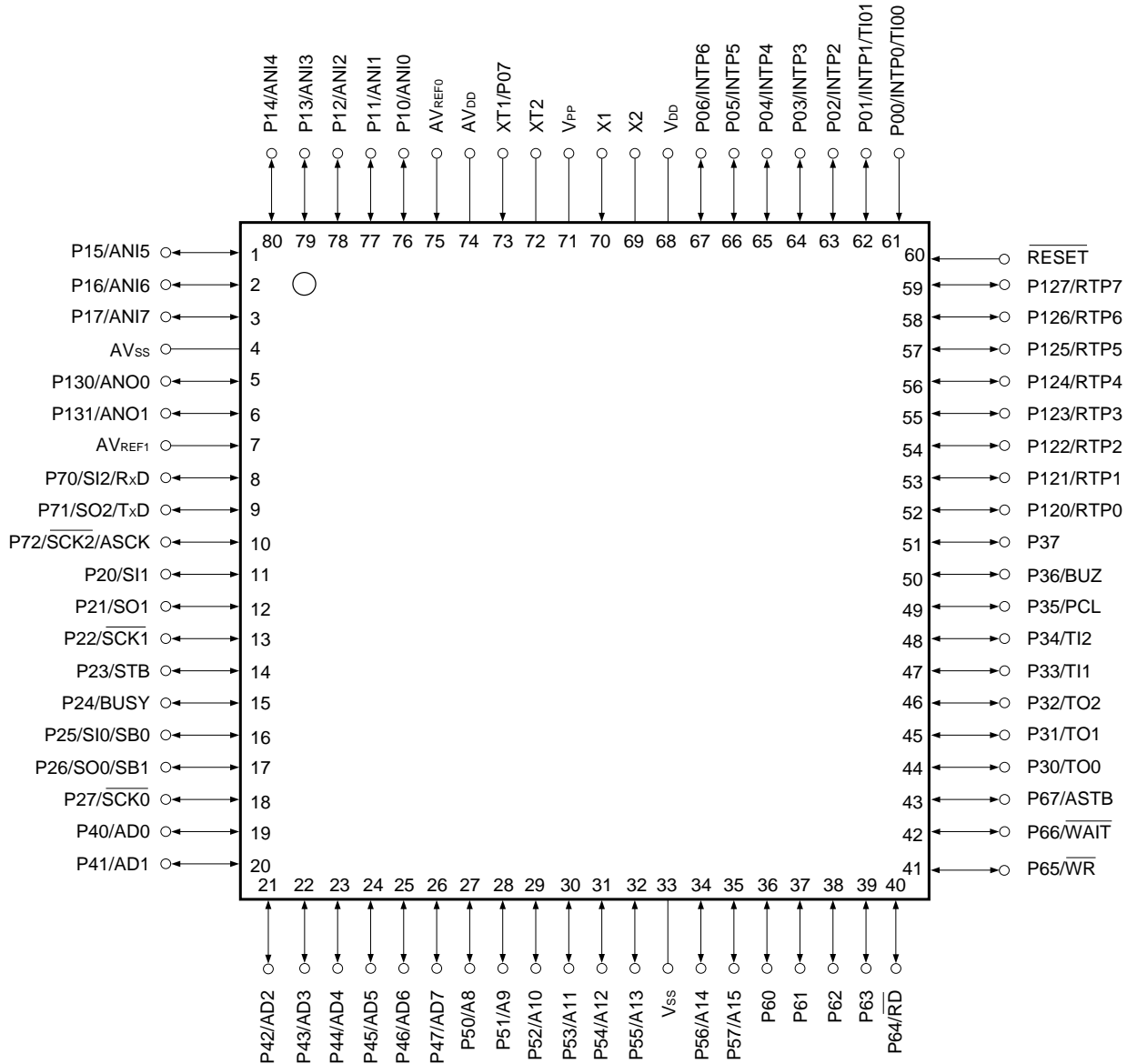
Notes 1. The internal PROM/internal high-speed RAM capacity can be changed using the internal memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed using the internal expansion RAM size switching register (IXS).

PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

- ★ • 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
μPD78P054GC-8BT, 78P058GC-8BT
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78P054GK-BE9
- 80-pin ceramic WQFN (14 × 14 mm)
μPD78P054KK-T, 78P058KK-T

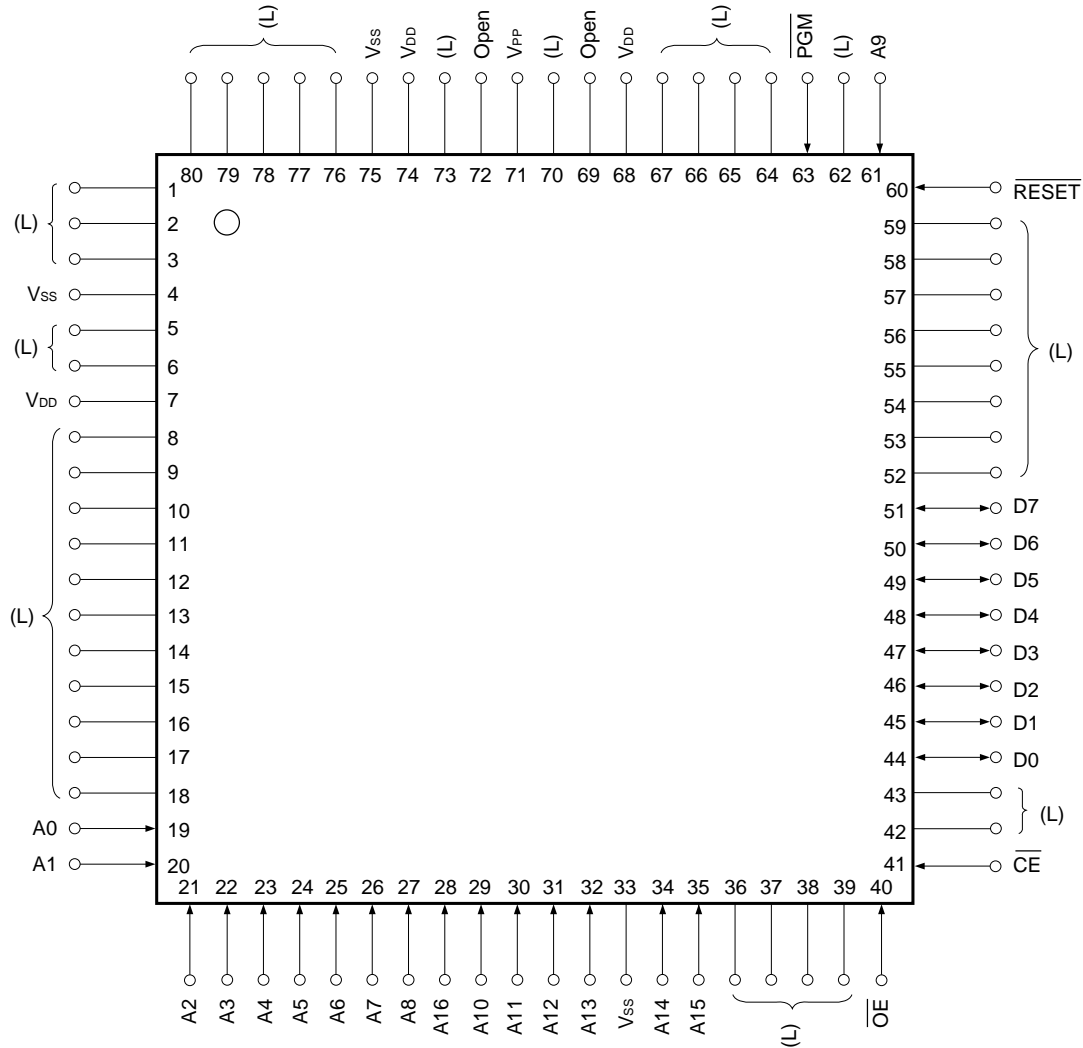


- Cautions**
1. Connect the V_{PP} pin directly to V_{SS}.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to V_{SS}.

A8 to A15:	Address Bus	\overline{RD} :	Read Strobe
AD0 to AD7:	Address/Data Bus	\overline{RESET} :	Reset
ANI0 to ANI7:	Analog Input	RTP0 to RTP7:	Real-Time Output Port
ANO0, ANO1:	Analog Output	RxD:	Receive Data
ASCK:	Asynchronous Serial Clock	SB0, SB1:	Serial Bus
ASTB:	Address Strobe	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
AV _{DD} :	Analog Power Supply	SI0 to SI2:	Serial Input
AV _{REF0} , AV _{REF1} :	Analog Reference Voltage	SO0 to SO2:	Serial Output
AV _{SS} :	Analog Ground	STB:	Strobe
BUSY:	Busy	TI00, TI01:	Timer Input
BUZ:	Buzzer Clock	TI1, TI2:	Timer Input
INTP0 to INTP6:	External Interrupt Input	TO0 to TO2:	Timer Output
P00 to P07:	Port 0	TxD:	Transmit Data
P10 to P17:	Port 1	V _{DD} :	Power Supply
P20 to P27:	Port 2	V _{PP} :	Programming Power Supply
P30 to P37:	Port 3	V _{SS} :	Ground
P40 to P47 :	Port 4	\overline{WAIT} :	Wait
P50 to P57 :	Port 5	\overline{WR} :	Write Strobe
P60 to P67:	Port 6	X1, X2:	Crystal (Main System Clock)
P70 to P72:	Port 7	XT1, XT2:	Crystal (Subsystem Clock)
P120 to P127:	Port 12		
P130, P131:	Port 13		
PCL:	Programmable Clock		

(2) PROM programming mode

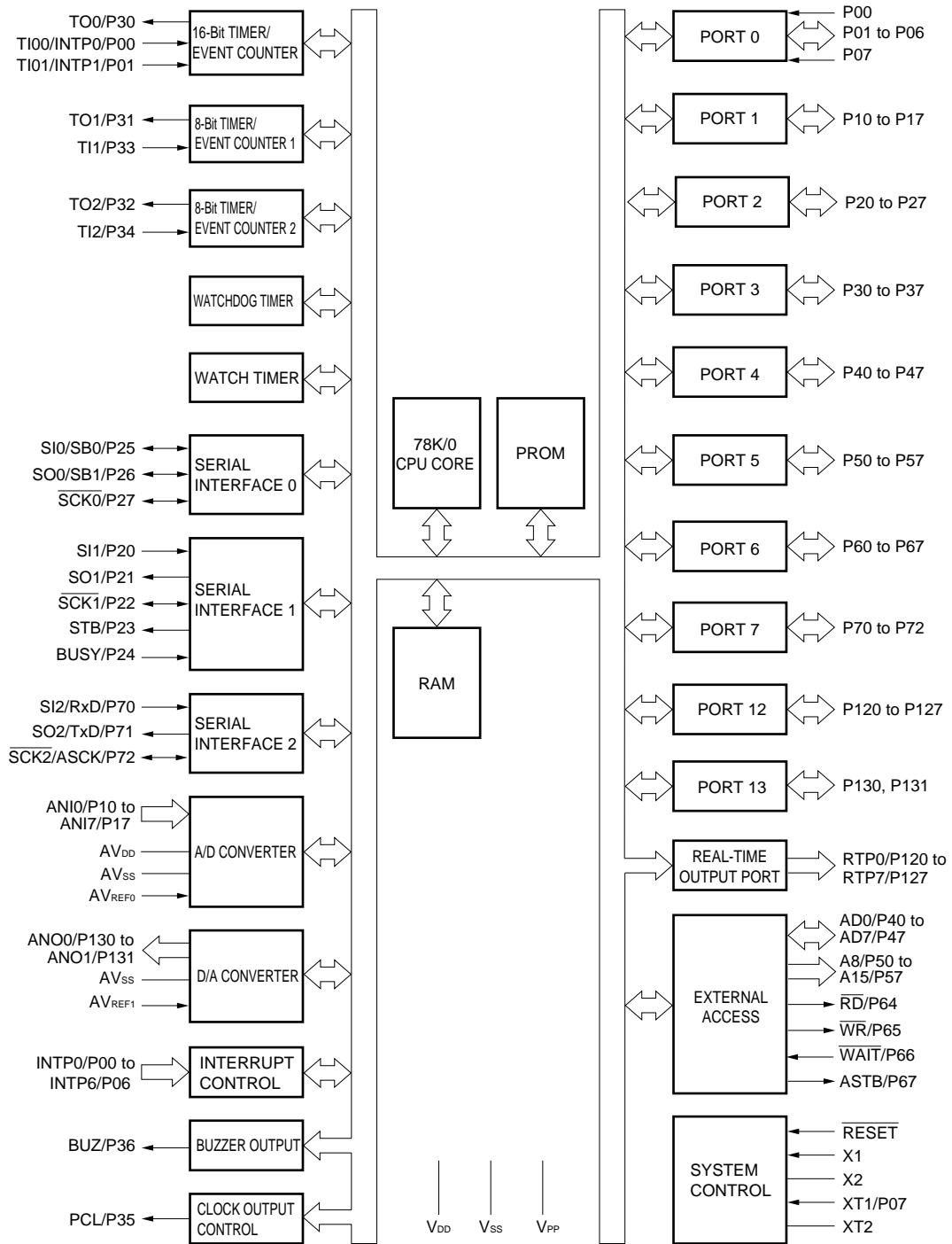
- 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
μPD78P054GC-8BT, 78P058GC-8BT
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78P054GK-BE9
- 80-pin ceramic WQFN (14 × 14 mm)
μPD78P054KK-T, 78P058KK-T



- Cautions**
1. (L): Individually connect to V_{SS} via a pull-down resistor.
 2. V_{SS}: Connect to GND.
 3. $\overline{\text{RESET}}$: Set to low level.
 4. Open: No connection

A0 to A16:	Address Bus	$\overline{\text{RESET}}$:	Reset
$\overline{\text{CE}}$:	Chip Enable	V _{DD} :	Power Supply
D0 to D7:	Data Bus	V _{PP} :	Programming Power Supply
$\overline{\text{OE}}$:	Output Enable	V _{SS} :	Ground
PGM:	Program		

BLOCK DIAGRAM



Remark The internal PROM and internal RAM capacities differ depending on the product.

CONTENTS

1. DIFFERENCES BETWEEN μPD78P054, 78P058 AND MASK ROM VERSIONS 11

2. PIN FUNCTIONS 12

 2.1 Pins in Normal Operating Mode 12

 2.2 Pins in PROM Programming Mode 15

 2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins 16

3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS) 20

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS) (μPD78P058 ONLY) 22

5. PROM PROGRAMMING 23

 5.1 Operating Modes 23

 5.2 PROM Write Procedure 25

 5.3 PROM Read Procedure 29

6. ERASURE METHOD (μPD78P054KK-T, 78P058KK-T ONLY) 30

7. ERASURE WINDOW OPAQUE FILM (μPD78P054KK-T, 78P058KK-T ONLY) 30

8. SCREENING OF ONE-TIME PROM VERSIONS 30

9. ELECTRICAL SPECIFICATIONS 31

10. CHARACTERISTICS CURVES (FOR REFERENCE ONLY) 66

11. PACKAGE DRAWINGS 70

12. RECOMMENDED SOLDERING CONDITIONS 73

APPENDIX A. DEVELOPMENT TOOLS 75

APPENDIX B. RELATED DOCUMENTS 81

1. DIFFERENCES BETWEEN μPD78P054, 78P058 AND MASK ROM VERSIONS

The μPD78P054 and 78P058 are single-chip microcontrollers with on-chip one-time writable PROM or with on-chip EPROM which has program write, erasure, and rewrite capability.

It is possible to make all the functions, except for the PROM specification and mask option of P60 to P63 pins, the same as those of mask ROM versions by setting the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Differences between the PROM versions (μPD78P054 and 78P058) and mask ROM versions (μPD78052, 78053, 78054, 78055, 78056, and 78058) are shown in Table 1-1.

Table 1-1. Differences between μPD78P054, 78P058 and Mask ROM Versions

Item	μPD78P054, 78P058	Mask ROM Versions
Internal ROM structure	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	μPD78P054: 32 Kbytes μPD78P058: 60 Kbytes	μPD78052: 16 Kbytes μPD78053: 24 Kbytes μPD78054: 32 Kbytes μPD78055: 40 Kbytes μPD78056: 48 Kbytes μPD78058: 60 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD78052: 512 bytes Other than μPD78052: 1024 bytes
Internal expansion RAM capacity	μPD78P054: None μPD78P058: 1024 bytes	μPD78058: 1024 bytes Other than μPD78058: None
Change of internal ROM and internal high-speed RAM capacity by internal memory size switching register (IMS)	Can be changed ^{Note 1}	Cannot be changed
Change of internal expansion RAM capacity by internal expansion RAM size switching register (IXS)	Can be changed ^{Note 2}	Cannot be changed
IC pin	None	Provided
V _{PP} pin	Provided	None
Pull-up resistor on-chip mask option of P60 to P63 pins	None	Provided
Electrical specifications, recommended soldering conditions	Refer to the data sheet for each product.	

- Notes**
- The internal PROM capacity and internal high-speed RAM capacity become as follows by RESET input.
Internal PROM capacity: 32 Kbytes (μPD78P054), 60 Kbytes (μPD78P058)
Internal high-speed RAM capacity: 1024 bytes
 - The internal expansion RAM capacity becomes 1024 bytes by RESET input (μPD78P058 only).

Caution The PROM version and mask ROM version differ in noise tolerance and noise emission. When replacing a PROM version with a mask ROM version when switching from experimental production to mass production, make a thorough evaluation with a CS (commercial sample) version (not ES (engineering sample) version) of the mask ROM version.

- Remarks**
- The μPD78P054 is a PROM version of the μPD78052, 78053, and 78054.
The μPD78P058 is a PROM version of the μPD78055, 78056, and 78058.
 - The internal expansion RAM size switching register (IXS) is included only in the μPD78058 and 78P058.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 ^{Note 1}	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. ^{Note 2}		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI1
P21					SO1
P22					SCK1
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					SCK0
P30	Input/output	Port 3 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When using the P07/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1 (be sure not to use the feedback resistor of the subsystem clock oscillation circuit).

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, set port 1 to the input mode. At this time, the pull-up resistors are automatically disconnected.

(1) Port pins (2/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. Set the test input flag (KRIF) to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	Input/output	Port 5 8-bit input/output port LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port Input/output can be specified in 1-bit units.	N-ch open-drain input/output port. LEDs can be driven directly.	Input	—
P61					
P62					
P63					
P64		When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	\overline{RD}	
P65				\overline{WR}	
P66				\overline{WAIT}	
P67				ASTB	
P70	Input/output	Port 7 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{SI2/RxD}$	
P71				$\overline{SO2/TxD}$	
P72				$\overline{SCK2/ASCK}$	
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	ANO0, ANO1

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, and both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	Input/output	Serial interface serial data input/output	Input	P25/SI0
SB1				P26/SO0
$\overline{\text{SCK0}}$	Input/output	Serial interface serial clock input/output	Input	P27
$\overline{\text{SCK1}}$				P22
$\overline{\text{SCK2}}$				P72/ASCK
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
RxD	Input	Serial data input for asynchronous serial interface	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/ $\overline{\text{SCK2}}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port which outputs data in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	Input/output	Lower address/data bus for expanding memory externally	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{\text{WR}}$		Strobe signal output for writing to external memory	Input	P65

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
$\overline{\text{WAIT}}$	Input	Wait insertion when accessing external memory	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
ANI0 to ANI7	Input	Analog input of A/D converter	Input	P10 to P17
ANO0, ANO1	Output	Analog output of D/A converter	Input	P130, P131
AV _{REF0}	Input	Reference voltage input of A/D converter	—	—
AV _{REF1}	Input	Reference voltage input of D/A converter	—	—
AV _{DD}	—	Analog power supply of A/D converter. Connect to V _{DD} .	—	—
AV _{SS}	—	Ground potential of A/D converter and D/A converter. Connect to V _{SS} .	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	Input	P07
XT2	—		—	—
V _{DD}	—	Positive power supply	—	—
V _{PP}	—	High-voltage applied during program write/verify. Connect directly to V _{SS} in normal operating mode.	—	—
V _{SS}	—	Ground potential	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V _{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode.
V _{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$	Input	Read strobe input to PROM
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programming mode
V _{DD}	—	Positive power supply
V _{SS}	—	Ground potential

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

For the input/output circuit configuration of each type, see Figure 2-1.

Table 2-1. Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins	
P00/INTP0/TI00	2	Input	Connect to V _{SS} .	
P01/INTP1/TI01	8-A	I/O	Independently connect to V _{SS} via a resistor.	
P02/INTP2				
P03/INTP3				
P04/INTP4				
P05/INTP5				
P06/INTP6				
P07/XT1	16	Input	Connect to V _{DD} or V _{SS} .	
P10/ANI0 to P17/ANI7	11	I/O	Independently connect to V _{DD} or V _{SS} via a resistor.	
P20/SI1	8-A			
P21/SO1	5-A			
P22/SCK1	8-A			
P23/STB	5-A			
P24/BUSY	8-A			
P25/SI0/SB0	10-A			
P26/SO0/SB1				
P27/SCK0				
P30/TO0	5-A			
P31/TO1				
P32/TO2				
P33/TI1	8-A			
P34/TI2				
P35/PCL	5-A			
P36/BUZ				
P37				
P40/AD0 to P47/AD7	5-E			Independently connect to V _{DD} via a resistor.
P50/A8 to P57/A15	5-A			Independently connect to V _{DD} or V _{SS} via a resistor.
P60 to P63	13-D			Independently connect to V _{DD} via a resistor.
P64/RD	5-A			Independently connect to V _{DD} or V _{SS} via a resistor.
P65/WR				
P66/WAIT				
P67/ASTB				
P70/SI2/RxD	8-A			
P71/SO2/TxD	5-A			
P72/SCK2/ASCK	8-A			
P120/RTP0 to P127/RTP7	5-A			
P130/ANO0, P131/ANO1	12-A	Independently connect to V _{SS} via a resistor.		

Table 2-1. Pin Input/Output Circuit Type (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
RESET	2	Input	—
XT2	16	—	Leave open.
AVREF0	—		Connect to V _{SS} .
AVREF1			Connect to V _{DD} .
AVDD			
AVSS			Connect to V _{SS} .
VPP			Connect directly to V _{SS} .

Figure 2-1. Pin Input/Output Circuits (1/2)

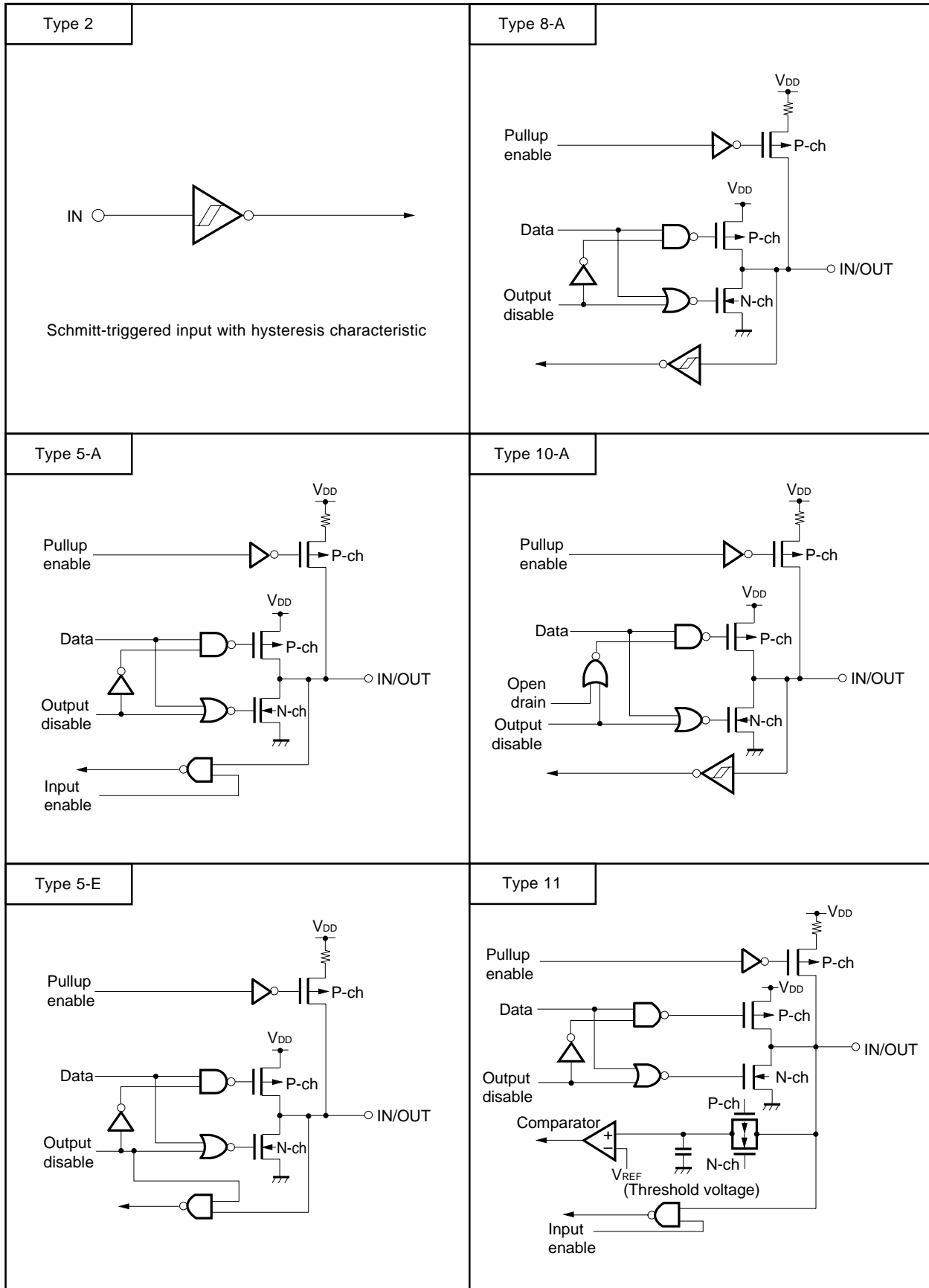
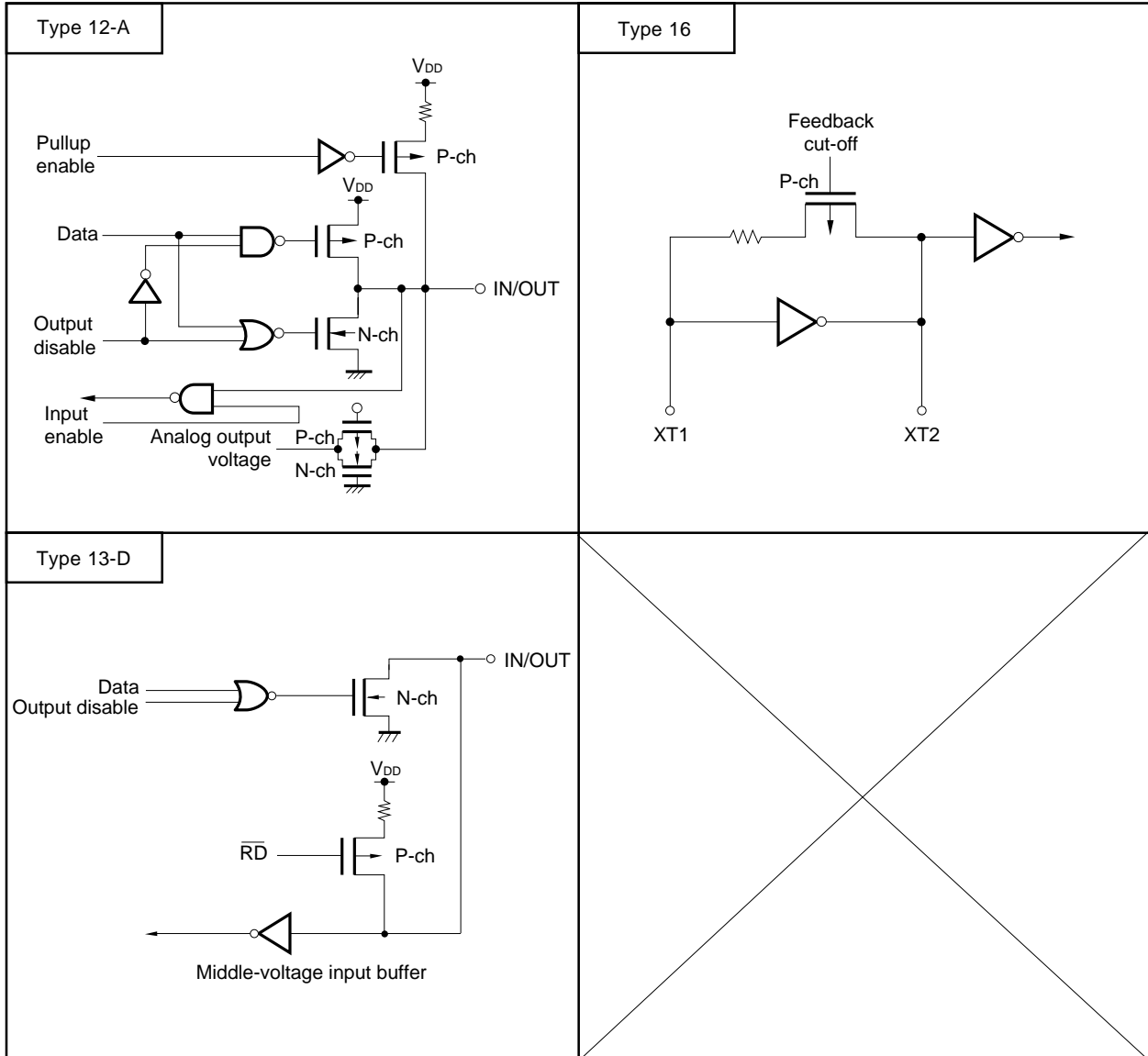


Figure 2-1. Pin Input/Output Circuits (2/2)



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting IMS, the internal memory (ROM, RAM) of the μPD78P054, 78P058 can be mapped identically to that of a mask ROM version.

IMS is set with an 8-bit memory manipulation instruction.

RESET input sets IMS to C8H (μPD78P054)/CFH (μPD78P058).

Figure 3-1. Format of Internal Memory Size Switching Register (μPD78P054)

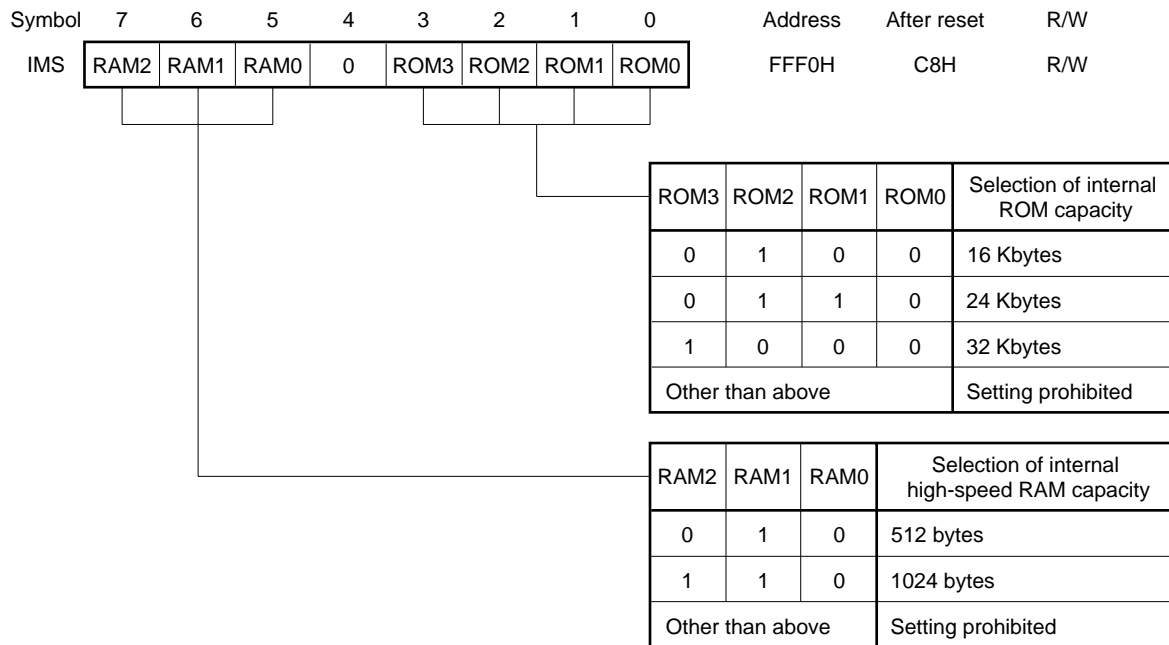
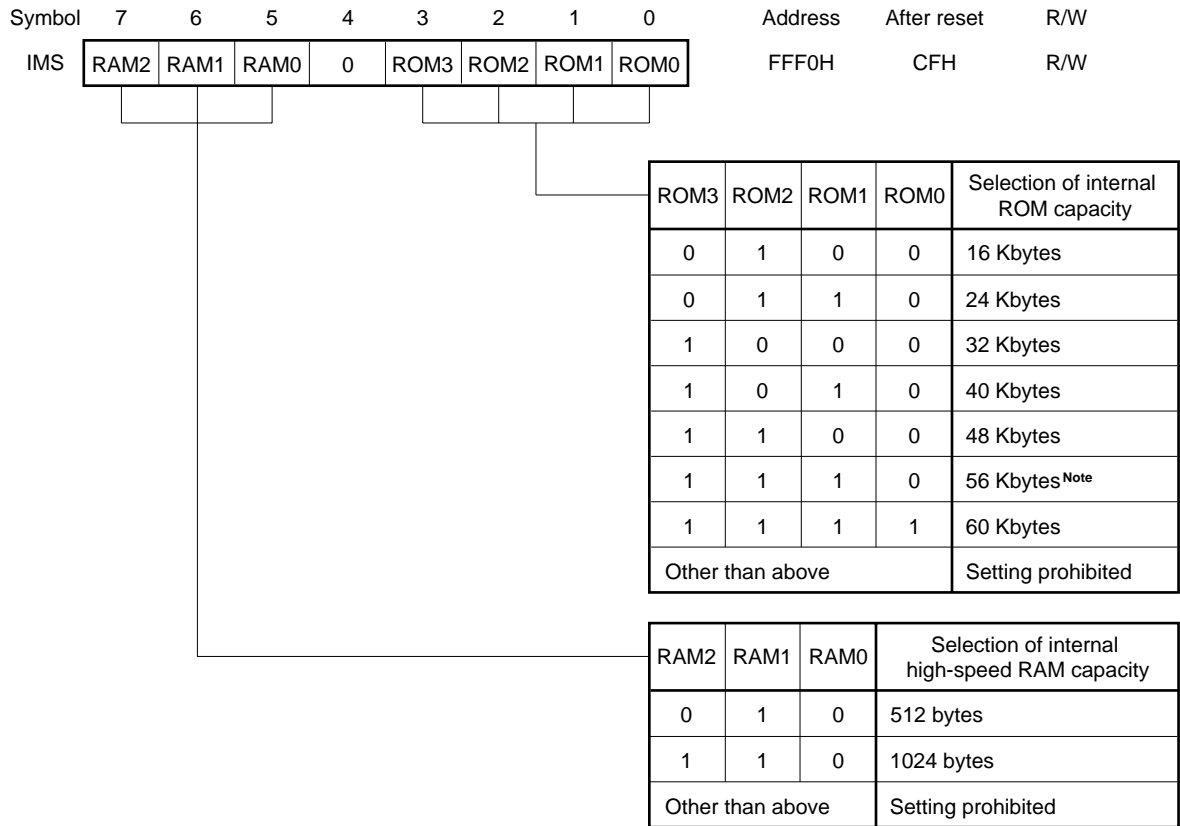


Table 3-1 shows the setting values of IMS which make the memory map the same as that of the various mask ROM versions.

Table 3-1. Internal Memory Size Switching Register Setting Values (μPD78P054)

Target Mask ROM Version	IMS Setting Value
μPD78052	44H
μPD78053	C6H
μPD78054	C8H

Figure 3-2. Format of Internal Memory Size Switching Register (μPD78P058)



Note Set the internal ROM capacity to 56 Kbytes or less when the external device expansion function is used.

Table 3-2 shows the setting values of IMS which make the memory map the same as that of the various mask ROM versions.

Table 3-2. Internal Memory Size Switching Register Setting Values (μPD78P058)

Target Mask ROM Version	IMS Setting Value
μPD78052	44H
μPD78053	C6H
μPD78054	C8H
μPD78055	CAH
μPD78056	CCH
μPD78058	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS) (μPD78P058 ONLY)

IXS is a register that is set by software and is used to set the internal expansion RAM capacity. By setting IXS, it is possible to get the same memory map as that of a mask ROM version having a different internal expansion RAM capacity.

IXS is set with an 8-bit memory manipulation instruction.

RESET input sets IXS to 0AH.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

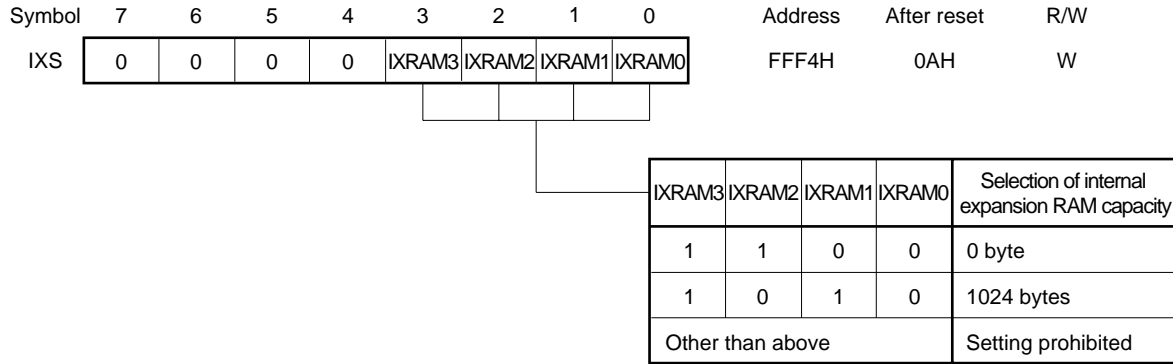


Table 4-1 shows the setting values of IXS which make the memory map the same as that of the various mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Version	IXS Setting Value
μPD78052	0CH
μPD78053	
μPD78054	
μPD78055	
μPD78056	
μPD78058	0AH

Remark Even if a μPD78P058 program that includes "MOV IXS, #0CH" is implemented in the μPD78052, 78053, 78054, 78055, or 78056, operation will not be affected.

5. PROM PROGRAMMING

The μPD78P054 and 78P058 have 32 Kbytes and 60 Kbytes respectively of on-chip PROM as program memory. For programming, set the PROM programming mode with the V_{PP} and \overline{RESET} pins. For the connector of unused pins, refer to **PIN CONFIGURATIONS (Top View) (2) PROM programming mode**.

Caution The program of the μPD78P054 should be written in the address range 0000H to 7FFFH (the last address, 7FFFH, should be specified). The program of the μPD78P058 should be written in the address range 0000H to EFFFH (the last address, EFFFH, should be specified). Writing cannot be performed with a PROM programmer that cannot specify the write addresses.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the \overline{RESET} pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the \overline{CE} , \overline{OE} and \overline{PGM} pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Operating Mode \ Pin	\overline{RESET}	V_{PP}	V_{DD}	\overline{CE}	\overline{OE}	\overline{PGM}	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	High-impedance
Read	L	+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

Remark ×: L or H

(1) Read mode

Read mode is set if $\overline{CE} = L$, $\overline{OE} = L$ is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE} = H$ is set.

Therefore, data can be read from any device by controlling the \overline{OE} pin, if multiple μ PD78P054s or 78P058s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE} = H$ is set.

In this mode, data output becomes high-impedance irrespective of the \overline{OE} status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE} = H$, $\overline{PGM} = H$, $\overline{OE} = L$ is set when page write mode is entered.

In this mode, 1-page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the \overline{PGM} pin with $\overline{CE} = H$, $\overline{OE} = H$. Program verification can then be performed when $\overline{CE} = L$, $\overline{OE} = L$ is set.

If programming is not performed by a one-time program pulse, X ($X \leq 10$) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the \overline{PGM} pin with $\overline{CE} = L$, $\overline{OE} = H$. Program verification can then be performed when $\overline{OE} = L$ is set.

If programming is not performed by a one-time program pulse, X ($X \leq 10$) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE} = L$, $\overline{PGM} = H$, $\overline{OE} = L$ is set.

In this mode, after writing, check if the write operation was performed correctly.

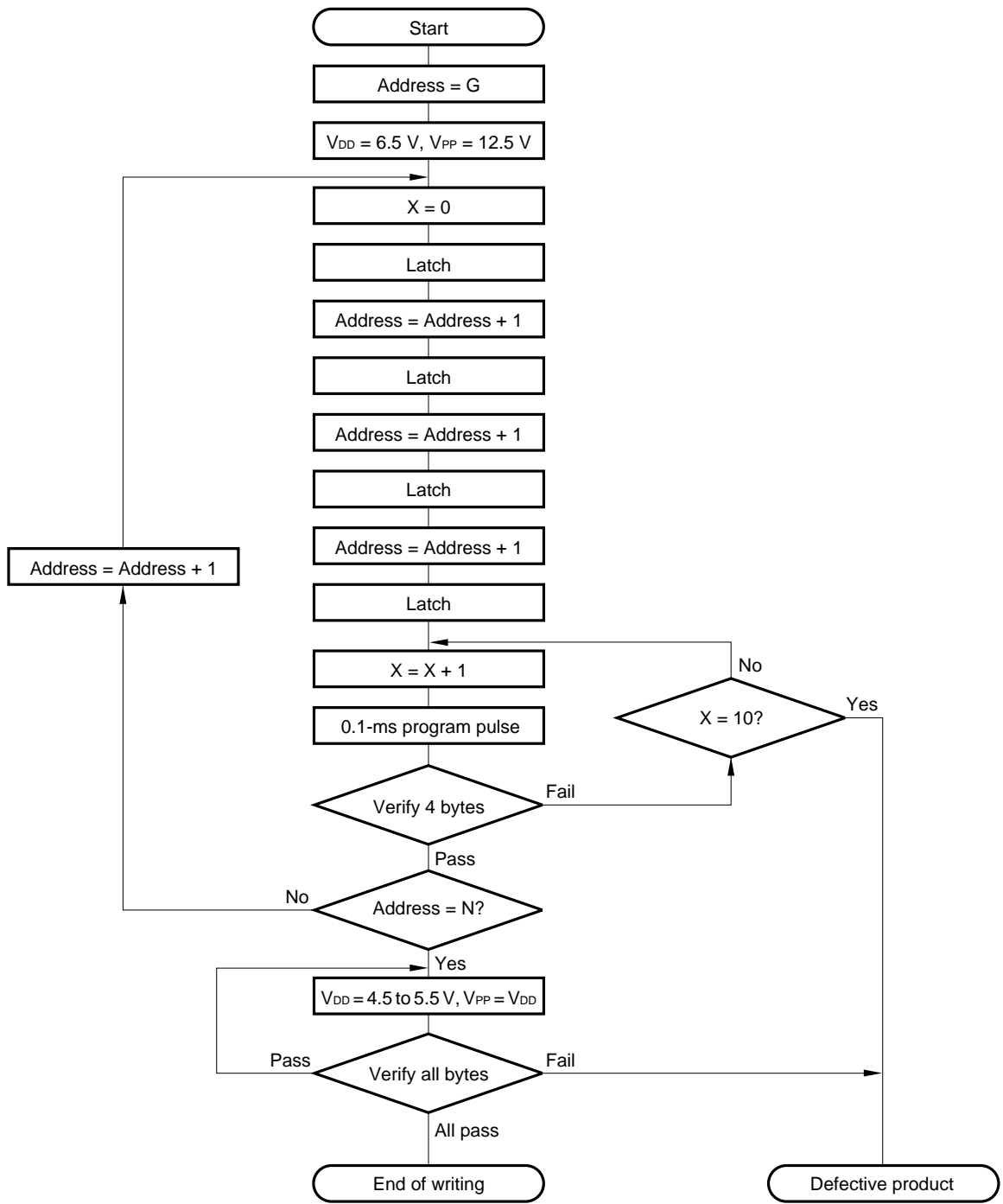
(8) Program inhibit mode

Program inhibit mode is used when the \overline{OE} pin, V_{PP} pin, and D0 to D7 pins of multiple μ PD78P054s or 78P058s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the \overline{PGM} pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flowchart



Remark G = Start address
 N = Program last address

Figure 5-2. Page Program Mode Timing

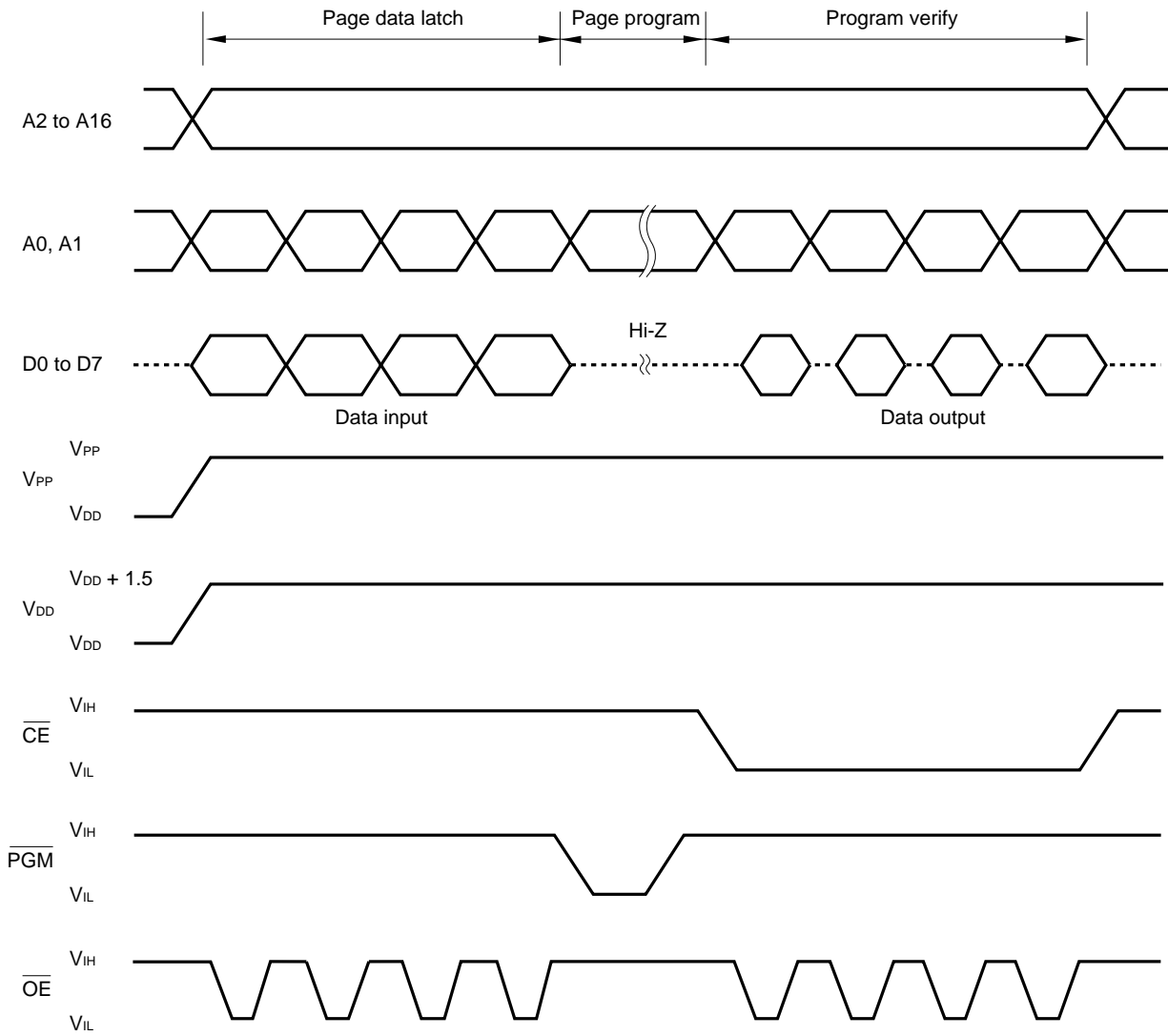
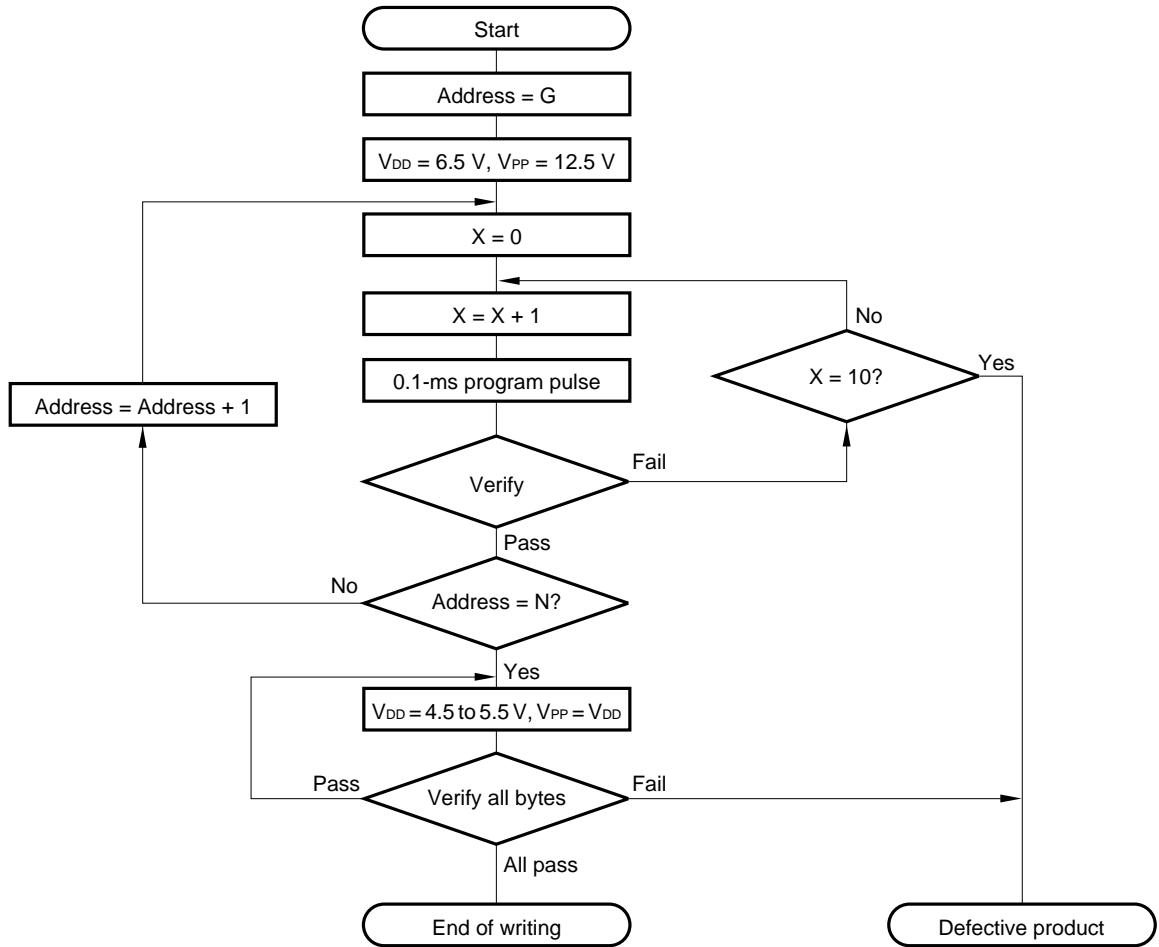
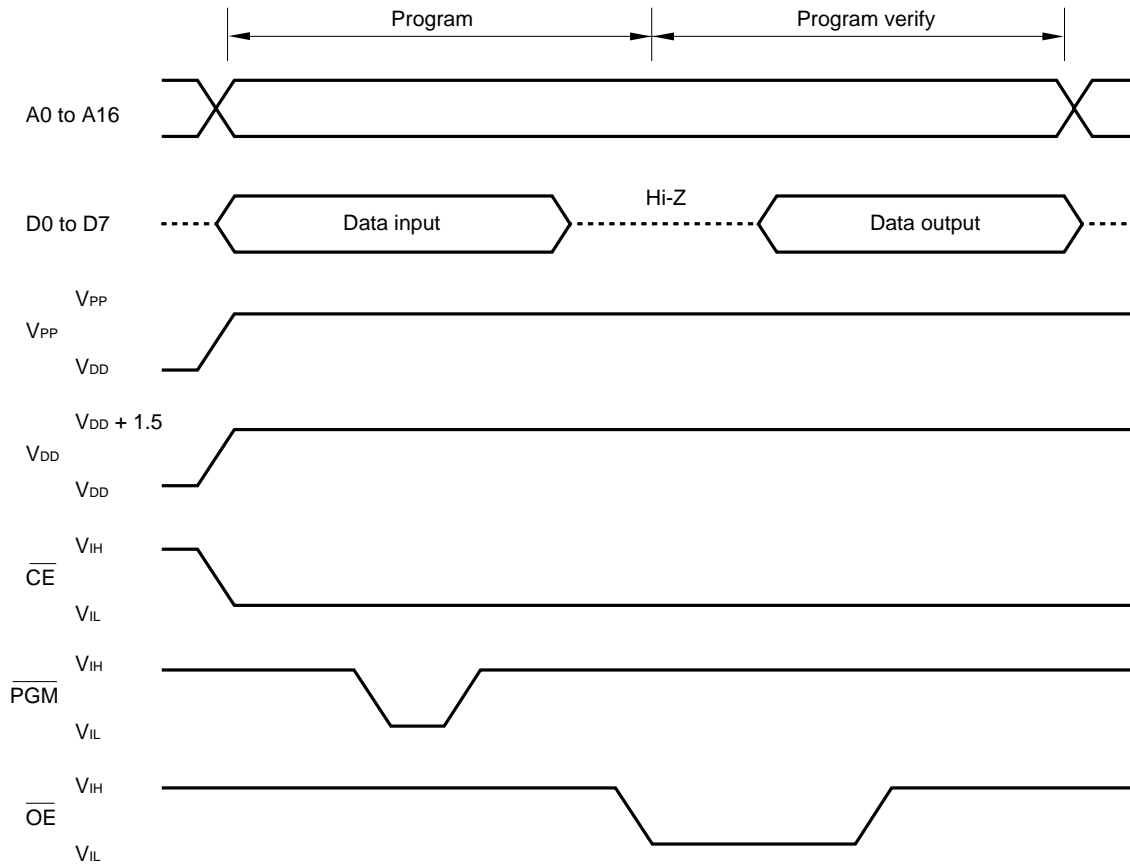


Figure 5-3. Byte Program Mode Flowchart



Remark G = Start address
 N = Program last address

Figure 5-4. Byte Program Mode Timing



- Cautions**
1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.
 2. V_{PP} must not exceed +13.5 V including overshoot.
 3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

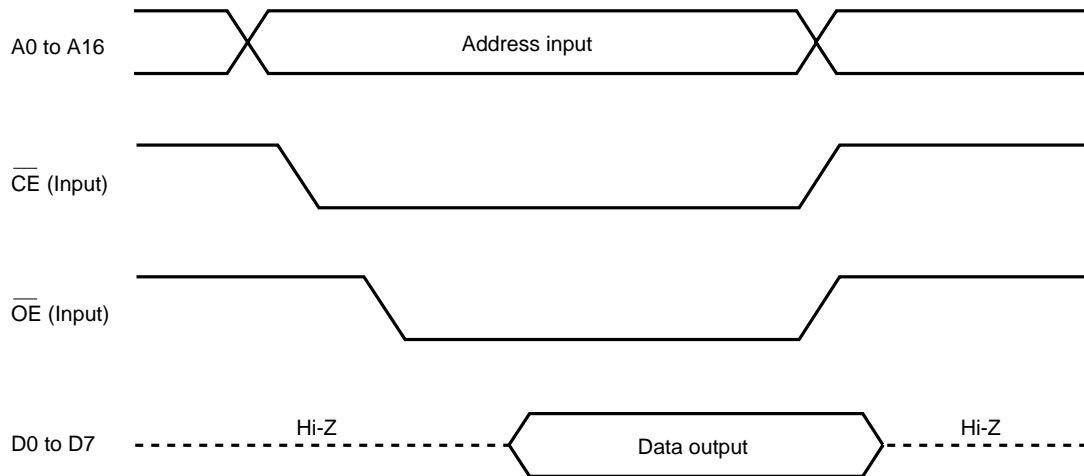
5.3 PROM Read Procedure

The contents of PROM can be read out to the external data bus (D0 to D7) using the read procedure shown below.

- (1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **PIN CONFIGURATIONS (Top View) (2) PROM programming mode.**
- (2) Supply +5 V to the V_{DD} and V_{PP} pins.
- (3) Input the address of data to be read to the A0 to A16 pins.
- (4) Read mode
- (5) Output data to D0 to D7 pins.

The timing of the above steps (2) to (5) is shown in Figure 5-5.

Figure 5-5. PROM Read Timing



6. ERASURE METHOD (μPD78P054KK-T, 78P058KK-T ONLY)

The μPD78P054KK-T and 78P058KK-T are capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the data, irradiate light having a wavelength of less than about 400 nm to the window on the top of the package. Normally, ultraviolet rays of 254-nm wavelength should be used. The volume of irradiation required to completely erase the data is as follows:

- UV intensity × erasing time: 30 W•s/cm² or more
- Erasing time: 40 minutes or more (When a UV lamp of 12 mW/cm² is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided on the UV lamp, remove the filter during the erasure process.

7. ERASURE WINDOW OPAQUE FILM (μPD78P054KK-T, 78P058KK-T ONLY)

To protect from unintentional erasure by other than EPROM erasure lamp light, or to protect internal circuits other than EPROM from malfunction due to light coming in through the window, mask the window with the attached opaque film when EPROM erasure is not being performed.

8. SCREENING OF ONE-TIME PROM VERSIONS

The one-time PROM versions (μPD78P054GC-8BT, 78P054GK-BE9, and 78P058GC-8BT) cannot be tested completely by NEC before being shipped, because of their structure. It is recommended to perform screening to verify PROM after writing the necessary data and following high-temperature storage under the conditions below.

Storage Temperature	Storage Time
125°C	24 hours

At present, a fee is charged by NEC for the one-time PROM writing, marking, screening, and verifying service for QTOP microcontrollers. For details, contact your sales representative.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	V _{PP}			-0.3 to +13.5	V
	AV _{DD}			-0.3 to V _{DD} + 0.3	V
	AV _{REF0}			-0.3 to V _{DD} + 0.3	V
	AV _{REF1}			-0.3 to V _{DD} + 0.3	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, RESET		-0.3 to V _{DD} + 0.3	V
	V _{I2}	P60 to P63	N-ch open-drain	-0.3 to +16	V
	V _{I3}	A9	PROM programming mode	-0.3 to +13.5	V
Output voltage	V _O			-0.3 to V _{DD} + 0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pins	AV _{SS} - 0.3 to AV _{REF0} + 0.3	V
Output current, high	I _{OH}	Per pin		-10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		-15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		-15	mA
Output current, low	I _{OL} ^{Note}	Per pin	peak value	30	mA
			r.m.s. value	15	mA
		Total for P50 to P55	peak value	100	mA
			r.m.s. value	70	mA
		Total for P56, P57, P60 to P63	peak value	100	mA
			r.m.s. value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	peak value	50	mA
			r.m.s. value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note r.m.s. values should be calculated as follows: [r.m.s. value] = [peak value] × √Duty

Caution Product quality may suffer if the absolute maximum rating is exceeded momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} /t _{xL})		85		500	ns

- Notes**
1. Indicates only the oscillator characteristics. See the **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after a reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _{XT}) ^{Note 1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 6.0 V		1.2	2	s
External clock		XT1 input frequency (f _{XT}) ^{Note 1}		32		100	kHz
		XT1 input high-/low-level width (t _{XTH} /t _{XTL})		5		15	μs

- Notes**
1. Indicates only the oscillator characteristics. See the **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

(1) μPD78P054

Main system clock: Ceramic resonator (T_A = -40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.0MC3	4.0	On-chip	On-chip	2.0	6.0
	CCR5.0MC3	5.0	On-chip	On-chip	2.0	6.0

Subsystem clock: Crystal resonator (T_A = -40 to +85°C)

Manufacturer	Product Name	Frequency (kHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku Corp.	DT-38 (1TA252E00, load capacitance 12.5 pF)	32.768	22	22	330	2.0	6.0

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

(2) μPD78P058

Main system clock: Ceramic resonator (T_A = -20 to +80°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kyocera Corp.	KBR-4.19MKS	4.19	On-chip	On-chip	2.0	6.0

Main system clock: Ceramic resonator (T_A = -40 to +85°C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CST5.00MGW	5.0	On-chip	On-chip	2.7	6.0
	CSA5.00MG	5.0	30	30	2.7	6.0

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz, Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C _{IO}	f = 1 MHz Unmeasured pins returned to 0 V			15	pF
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131 P60 to P63			20	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V _{DD} = 2.7 to 6.0 V	0.7V _{DD}		V _{DD}	V
				0.8V _{DD}		V _{DD}	V
	V _{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 6.0 V	0.8V _{DD}		V _{DD}	V
				0.85V _{DD}		V _{DD}	V
	V _{IH3}	P60 to P63 (N-ch open-drain)	V _{DD} = 2.7 to 6.0 V	0.7V _{DD}		15	V
				0.8V _{DD}		15	V
	V _{IH4}	X1, X2	V _{DD} = 2.7 to 6.0 V	V _{DD} - 0.5		V _{DD}	V
				V _{DD} - 0.2		V _{DD}	V
	V _{IH5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 6.0 V	0.8V _{DD}		V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0.9V _{DD}		V _{DD}	V
2.0 V ≤ V _{DD} < 2.7 V ^{Note}			0.9V _{DD}		V _{DD}	V	
Input voltage, low	V _{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131	V _{DD} = 2.7 to 6.0 V	0		0.3V _{DD}	V
				0		0.2V _{DD}	V
	V _{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V _{DD} = 2.7 to 6.0 V	0		0.2V _{DD}	V
				0		0.15V _{DD}	V
	V _{IL3}	P60 to P63	4.5 V ≤ V _{DD} ≤ 6.0 V	0		0.3V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.2V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL4}	X1, X2	V _{DD} = 2.7 to 6.0 V	0		0.4	V
				0		0.2	V
	V _{IL5}	XT1/P07, XT2	4.5 V ≤ V _{DD} ≤ 6.0 V	0		0.2V _{DD}	V
			2.7 V ≤ V _{DD} < 4.5 V	0		0.1V _{DD}	V
			2.0 V ≤ V _{DD} < 2.7 V ^{Note}	0		0.1V _{DD}	V
Output voltage, high	V _{OH1}	V _{DD} = 4.5 to 6.0 V, I _{OH} = -1 mA	V _{DD} - 1.0			V	
		I _{OH} = -100 μA	V _{DD} - 0.5			V	
Output voltage, low	V _{OL1}	P50 to P57, P60 to P63	V _{DD} = 4.5 to 6.0 V, I _{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V _{DD} = 4.5 to 6.0 V, I _{OL} = 1.6 mA			0.4	V
	V _{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V _{DD} = 4.5 to 6.0 V, N-ch open-drain, with pull-up resistor (R = 1 kΩ)			0.2V _{DD}	V
	V _{OL3}	I _{OL} = 400 μA				0.5	V

Note When the XT1/P07 pin is used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LH1}	V _{IN} = V _{DD}	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I _{LH2}		X1, X2, XT1/P07, XT2			20	μA
	I _{LH3}	V _{IN} = 15 V	P60 to P63			80	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			-3	μA
	I _{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
	I _{LIL3}		P60 to P63			-3 ^{Note 1}	μA
Output leakage current, high	I _{LOH1}	V _{OUT} = V _{DD}				3	μA
Output leakage current, low	I _{LOL1}	V _{OUT} = 0 V				-3	μA
Software pull-up resistor ^{Note 2}	R ₂	V _{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 V ≤ V _{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V _{DD} < 4.5 V	20		500	kΩ

Notes 1. For P60 to P63, a low-level input leakage current of -200 μA (MAX.) flows only for 1.5 clocks (without wait) after the read instruction has been executed to port 6 (P6) or port mode register 6 (PM6). At times other than this 1.5-clock interval a -3 μA (MAX.) current flows.

2. A software pull-up resistor can only be used in the range of V_{DD} = 2.7 to 6.0 V.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current ^{Note 5}	I _{DD1}	5.0-MHz crystal oscillation operating mode (f _{xx} = 2.5 MHz) ^{Note 3}	V _{DD} = 5.0 V ±10% ^{Note 1}	5	15	mA
			V _{DD} = 3.0 V ±10% ^{Note 2}	0.7	2.1	mA
			V _{DD} = 2.2 V ±10% ^{Note 2}	0.4	1.2	mA
		5.0-MHz crystal oscillation operating mode (f _{xx} = 5.0 MHz) ^{Note 4}	V _{DD} = 5.0 V ±10% ^{Note 1}	9.0	27.0	mA
			V _{DD} = 3.0 V ±10% ^{Note 2}	1.0	3.0	mA
	I _{DD2}	5.0-MHz crystal oscillation HALT mode (f _{xx} = 2.5 MHz) ^{Note 3}	V _{DD} = 5.0 V ±10%	1.4	4.2	mA
			V _{DD} = 3.0 V ±10%	0.5	1.5	mA
			V _{DD} = 2.2 V ±10%	280	840	μA
		5.0-MHz crystal oscillation HALT mode (f _{xx} = 5.0 MHz) ^{Note 4}	V _{DD} = 5.0 V ±10%	1.6	4.8	mA
			V _{DD} = 3.0 V ±10%	0.65	1.95	mA
	I _{DD3}	32.768-kHz crystal oscillation operating mode ^{Note 6}	V _{DD} = 5.0 V ±10%	135	270	μA
			V _{DD} = 3.0 V ±10%	95	190	μA
			V _{DD} = 2.2 V ±10%	70	140	μA
I _{DD4}	32.768-kHz crystal oscillation HALT mode ^{Note 6}	V _{DD} = 5.0 V ±10%	25	55	μA	
		V _{DD} = 3.0 V ±10%	5	15	μA	
		V _{DD} = 2.2 V ±10%	2.5	12.5	μA	
I _{DD5}	XT1 = V _{DD} STOP mode Feedback resistor used	V _{DD} = 5.0 V ±10%	1	30	μA	
		V _{DD} = 3.0 V ±10%	0.5	10	μA	
		V _{DD} = 2.2 V ±10%	0.3	10	μA	
I _{DD6}	XT1 = V _{DD} STOP mode Feedback resistor not used	V _{DD} = 5.0 V ±10%	0.1	30	μA	
		V _{DD} = 3.0 V ±10%	0.05	10	μA	
		V _{DD} = 2.2 V ±10%	0.05	10	μA	

- Notes**
1. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)
 2. Low-speed mode operation (when PCC is set to 04H)
 3. Operation with main system clock f_{xx} = f_x/2 (when the oscillation mode selection register (OSMS) is set to 00H)
 4. Operation with main system clock f_{xx} = f_x (when OSMS is set to 01H)
 5. Refers to the current flowing through the V_{DD} and AV_{DD} pins. The current flowing to the A/D converter, D/A converter, and on-chip pull-up resistors is not included.
 6. When the main system clock operation is stopped.

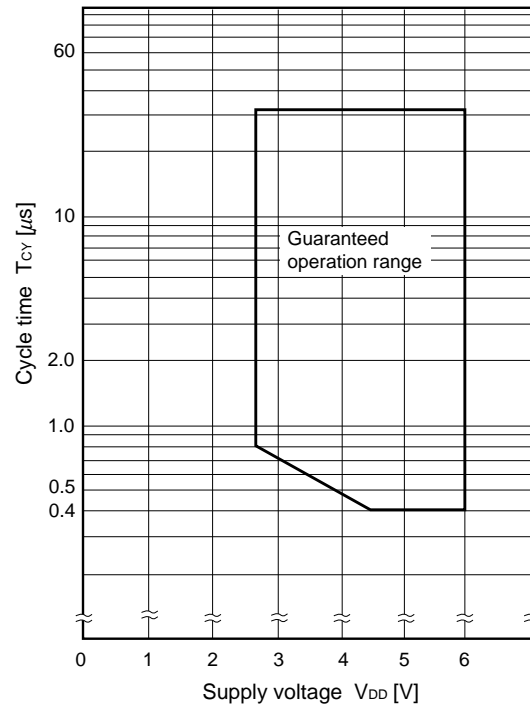
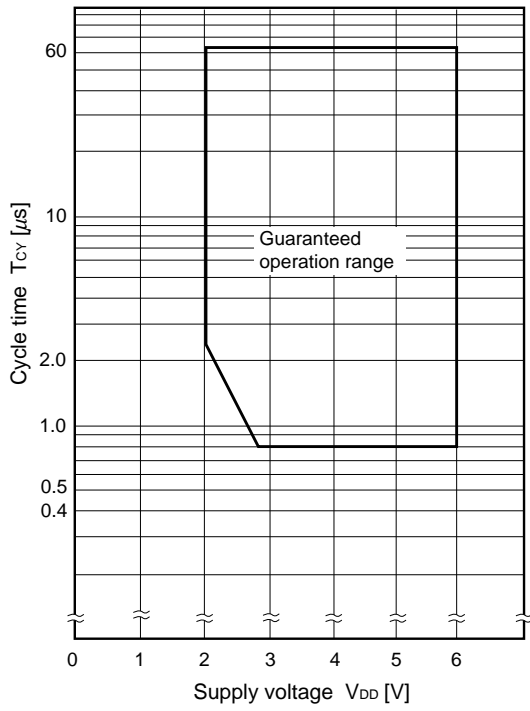
AC Characteristics

(1) Basic operation (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (minimum instruction execution time)	T _{CY}	Operating with main system clock (f _{XX} = 2.5 MHz) ^{Note 1}	V _{DD} = 2.7 to 6.0 V	0.8		64	μs
				2.2		64	μs
		Operating with main system clock (f _{XX} = 5.0 MHz) ^{Note 2}	4.5 V ≤ V _{DD} ≤ 6.0 V	0.4		32	μs
			2.7 V ≤ V _{DD} < 4.5 V	0.8		32	μs
		Operating with subsystem clock	40 ^{Note 3}	122	125	μs	
TI01, TI1, TI2 input frequency	f _{TI}	V _{DD} = 4.5 to 6.0 V		0		4	MHz
				0		275	kHz
TI00 input high-/low- level width	t _{TIH} , t _{TIL}		8/f _{sam} ^{Note 4}			μs	
TI01, TI1, TI2, input high-/low-level width	t _{TIH} , t _{TIL}	V _{DD} = 4.5 to 6.0 V		100			ns
				1.8			μs
Interrupt request input high-/low-level width	t _{INTH} , t _{INTL}	INTP0	8/f _{sam} ^{Note 4}			μs	
		INTP1 to INTP6, KR0 to KR7	V _{DD} = 2.7 to 6.0 V	10			μs
				20			μs
RESET low-level width	tr _{SL}	V _{DD} = 2.7 to 6.0 V		10			μs
				20			μs

- Notes**
1. Operation with main system clock f_{XX} = f_X/2 (when the oscillation mode selection register (OSMS) is set to 00H)
 2. Operation with main system clock f_{XX} = f_X (when OSMS is set to 01H)
 3. Value when an external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).
 4. Selection of f_{sam} = f_{XX}/2^N, f_{XX}/32, f_{XX}/64, f_{XX}/128 is possible using bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (SCS) (when N = 0 to 4).

T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation) T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) Read/write operations

(a) When MCS = 1, PCC2 to PCC0 = 000B ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 4.5$ to 6.0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}		$0.85t_{CY} - 50$		ns
Address setup time	t _{ADS}		$0.85t_{CY} - 50$		ns
Address hold time	t _{ADH}		50		ns
Data input time from address	t _{ADD1}			$(2.85 + 2n)t_{CY} - 80$	ns
	t _{ADD2}			$(4 + 2n)t_{CY} - 100$	ns
Data input time from $\overline{RD}\downarrow$	t _{RDD1}			$(2 + 2n)t_{CY} - 100$	ns
	t _{RDD2}			$(2.85 + 2n)t_{CY} - 100$	ns
Read data hold time	t _{RDH}		0		ns
\overline{RD} low-level width	t _{RDL1}		$(2 + 2n)t_{CY} - 60$		ns
	t _{RDL2}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t _{RDWT1}			$0.85t_{CY} - 50$	ns
	t _{RDWT2}			$2t_{CY} - 60$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t _{WRWT}			$2t_{CY} - 60$	ns
\overline{WAIT} low-level width	t _{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t _{WDS}		$(2.85 + 2n)t_{CY} - 100$		ns
Write data hold time	t _{WDH}		20		ns
\overline{WR} low-level width	t _{WRL1}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t _{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t _{ASTWR}		$0.85t_{CY} + 20$		ns
ASTB \uparrow delay time from $\overline{RD}\uparrow$ in external fetch	t _{RDASt}		$0.85t_{CY} - 10$	$1.15t_{CY} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t _{RDADH}		$0.85t_{CY} - 50$	$1.15t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t _{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t _{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t _{WRADH}		$0.85t_{CY}$	$1.15t_{CY} + 40$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t _{WTRD}		$1.15t_{CY} + 40$	$3.15t_{CY} + 40$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t _{WTWR}		$1.15t_{CY} + 30$	$3.15t_{CY} + 30$	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)**2.** PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)**3.** $t_{CY} = T_{CY}/4$ **4.** n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t _{ASTH}	V _{DD} = 2.7 to 6.0 V	t _{cy} - 80		ns
			t _{cy} - 150		ns
Address setup time	t _{ADS}	V _{DD} = 2.7 to 6.0 V	t _{cy} - 80		ns
			t _{cy} - 150		ns
Address hold time	t _{ADH}	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 10		ns
			0.37t _{cy} - 40		ns
Data input time from address	t _{ADD1}	V _{DD} = 2.7 to 6.0 V		(3 + 2n)t _{cy} - 160	ns
				(3 + 2n)t _{cy} - 320	ns
	t _{ADD2}	V _{DD} = 2.7 to 6.0 V		(4 + 2n)t _{cy} - 200	ns
				(4 + 2n)t _{cy} - 300	ns
Data input time from $\overline{RD}\downarrow$	t _{RDD1}	V _{DD} = 2.7 to 6.0 V		(1.4 + 2n)t _{cy} - 70	ns
				(1.37 + 2n)t _{cy} - 120	ns
	t _{RDD2}	V _{DD} = 2.7 to 6.0 V		(2.4 + 2n)t _{cy} - 70	ns
				(2.37 + 2n)t _{cy} - 120	ns
Read data hold time	t _{RDH}		0		ns
\overline{RD} low-level width	t _{RDL1}	V _{DD} = 2.7 to 6.0 V	(1.4 + 2n)t _{cy} - 20		ns
			(1.37 + 2n)t _{cy} - 20		ns
	t _{RDL2}	V _{DD} = 2.7 to 6.0 V	(2.4 + 2n)t _{cy} - 20		ns
			(2.37 + 2n)t _{cy} - 20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t _{RDWT1}	V _{DD} = 2.7 to 6.0 V		t _{cy} - 100	ns
				t _{cy} - 200	ns
	t _{RDWT2}	V _{DD} = 2.7 to 6.0 V		2t _{cy} - 100	ns
				2t _{cy} - 200	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t _{WRWT}	V _{DD} = 2.7 to 6.0 V		2t _{cy} - 100	ns
				2t _{cy} - 200	ns
\overline{WAIT} low-level width	t _{WTL}		(1 + 2n)t _{cy}	(2 + 2n)t _{cy}	ns
Write data setup time	t _{WDS}	V _{DD} = 2.7 to 6.0 V	(2.4 + 2n)t _{cy} - 60		ns
			(2.37 + 2n)t _{cy} - 100		ns
Write data hold time	t _{WDH}		20		ns
\overline{WR} low-level width	t _{WRL1}	V _{DD} = 2.7 to 6.0 V	(2.4 + 2n)t _{cy} - 20		ns
			(2.37 + 2n)t _{cy} - 20		ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RD↓ delay time from ASTB↓	t _{ASTRD}	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 30		ns
			0.37t _{cy} - 50		ns
WR↓ delay time from ASTB↓	t _{ASTWR}	V _{DD} = 2.7 to 6.0 V	1.4t _{cy} - 30		ns
			1.37t _{cy} - 50		ns
ASTB↑ delay time from RD↑ in external fetch	t _{RDAST}		t _{cy} - 10	t _{cy} + 20	ns
Address hold time from RD↑ in external fetch	t _{RDADH}		t _{cy} - 50	t _{cy} + 50	ns
Write data output time from RD↑	t _{RDWD}	V _{DD} = 2.7 to 6.0 V	0.4t _{cy} - 20		ns
			0.37t _{cy} - 40		ns
Write data output time from WR↓	t _{WRWD}	V _{DD} = 2.7 to 6.0 V	0	60	ns
			0	120	ns
Address hold time from WR↑	t _{WRADH}	V _{DD} = 2.7 to 6.0 V	t _{cy}	t _{cy} + 60	ns
			t _{cy}	t _{cy} + 120	ns
RD↑ delay time from WAIT↑	t _{WTRD}	V _{DD} = 2.7 to 6.0 V	0.6t _{cy} + 180	2.6t _{cy} + 180	ns
			0.63t _{cy} + 350	2.63t _{cy} + 350	ns
WR↑ delay time from WAIT↑	t _{WTWR}	V _{DD} = 2.7 to 6.0 V	0.6t _{cy} + 120	2.6t _{cy} + 120	ns
			0.63t _{cy} + 240	2.63t _{cy} + 240	ns

- Remarks**
1. MCS: Bit 0 of the oscillation mode selection register (OSMS)
 2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(3) Serial interface (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY1}	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH1} ,	V _{DD} = 4.5 to 6.0 V	t _{KCY1} /2 - 50			ns
	t _{KL1}		t _{KCY1} /2 - 100			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$)	t _{SIK1}	4.5 V ≤ V _{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
			300			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$)	t _{KSI1}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t _{KSO1}	C = 100pF ^{Note}			300	ns

Note C is the load capacitance of the SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t _{KCY2}	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH2} ,	4.5 V ≤ V _{DD} ≤ 6.0 V	400			ns
	t _{KL2}	2.7 V ≤ V _{DD} < 4.5 V	800			ns
			1600			ns
SIO setup time (to $\overline{\text{SCK0}}\uparrow$)	t _{SIK2}		100			ns
SIO hold time (from $\overline{\text{SCK0}}\uparrow$)	t _{KSI2}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t _{KSO2}	C = 100 pF ^{Note}			300	ns
$\overline{\text{SCK0}}$ rise, fall time	t _{R2} ,	When using external device expansion function			160	ns
	t _{F2}	When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{CY3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t_{KH3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{CY3}}/2 - 50$			ns
	t_{KL3}		$t_{\text{CY3}}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KS3}		$t_{\text{CY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{SO3}	R = 1 kΩ, C = 100 pF ^{Note}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0	250	ns
				0	1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}\uparrow$	t_{KB}		t_{CY3}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1↓	t_{BK}		t_{CY3}			ns
SB0, SB1 high-level width	t_{BH}		t_{CY3}			ns
SB0, SB1 low-level width	t_{BL}		t_{CY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output lines.

(iv) SBI mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{CY4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	800			ns
			3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	t_{KH4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	400			ns
	t_{KL4}		1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KS4}		$t_{\text{CY4}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{SO4}	R = 1 kΩ, C = 100 pF ^{Note}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0	300	ns
				0	1000	ns
SB0, SB1↓ from $\overline{\text{SCK0}}\uparrow$	t_{KB}		t_{CY4}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1↓	t_{BK}		t_{CY4}			ns
SB0, SB1 high-level width	t_{BH}		t_{CY4}			ns
SB0, SB1 low-level width	t_{BL}		t_{CY4}			ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R4} , t_{F4}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 2.7 to 6.0 V	1600		ns
				3200		ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		V _{DD} = 2.7 to 6.0 V	$t_{\text{KCY5}}/2 - 160$		ns
				$t_{\text{KCY5}}/2 - 190$		ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		V _{DD} = 4.5 to 6.0 V	$t_{\text{KCY5}}/2 - 50$		ns
				$t_{\text{KCY5}}/2 - 100$		ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK5}		4.5 V ≤ V _{DD} ≤ 6.0 V	300		ns
			2.7 V ≤ V _{DD} < 4.5 V	350		ns
				400		ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI5}		600		ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO5}		0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}	V _{DD} = 2.7 to 6.0 V	1600			ns	
			3200			ns	
$\overline{\text{SCK0}}$ high-level width	t_{KH6}	V _{DD} = 2.7 to 6.0 V	650			ns	
			1300			ns	
$\overline{\text{SCK0}}$ low-level width	t_{KL6}	V _{DD} = 2.7 to 6.0 V	800			ns	
			1600			ns	
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK6}		100			ns	
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI6}		$t_{\text{KCY6}}/2$			ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO6}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R6}},$ t_{F6}	When using external device expansion function			160	ns	
		When not using external device expansion function			1000	ns	

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH7}},$ t_{KL7}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY7}}/2 - 50$			ns
			$t_{\text{KCY7}}/2 - 100$			ns
S11 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			300			ns
S11 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KS17}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO7}	$C = 100 \text{ pF}$ ^{Note}			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK1}}$ high-/low-level width	$t_{\text{KH8}},$ t_{KL8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
			1600			ns
S11 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK8}		100			ns
S11 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KS18}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO8}	$C = 100 \text{ pF}$ ^{Note}			300	ns
$\overline{\text{SCK1}}$ rise, fall time	$t_{\text{R8}},$ t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) Automatic transmit/receive function 3-wire serial I/O mode ($\overline{\text{SCK1}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH9}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	t_{KL9}		$t_{\text{KCY9}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK9}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			300			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KS9}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO9}	$C = 100 \text{ pF}$ ^{Note}			300	ns
STB \uparrow from $\overline{\text{SCK1}}\uparrow$	t_{SBD}		$t_{\text{KCY9}}/2 - 100$		$t_{\text{KCY9}}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	$V_{\text{DD}} = 2.7 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY9}} - 30$		$t_{\text{KCY9}} + 30$	ns
			$t_{\text{KCY9}} - 60$		$t_{\text{KCY9}} + 60$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			200			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactive	t_{SPS}				$2t_{\text{KCY9}}$	ns

Note C is the load capacitance of the SO1 output line.

(iv) Automatic transmit/receive function 3-wire serial I/O mode ($\overline{\text{SCK1}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH10}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	400			ns
	t_{KL10}	$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
			1600			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KS10}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO10}	$C = 100 \text{ pF}$ ^{Note}			300	ns
$\overline{\text{SCK1}}$ rise, fall time	t_{R10} , t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY11}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH11}},$	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY11}}/2 - 50$			ns
	t_{KL11}					$t_{\text{KCY11}}/2 - 100$
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK11}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			300			ns
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{KS11}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO11}	$C = 100 \text{ pF}$ ^{Note}			300	ns

Note C is the load capacitance of the SO2 output line.

★

(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit			
$\overline{\text{SCK2}}$ cycle time	t_{KCY12}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns			
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns			
			3200			ns			
$\overline{\text{SCK2}}$ high-/low-level width	$t_{\text{KH12}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	400			ns			
	t_{KL12}					$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800		ns
							1600		ns
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK12}		100			ns			
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{KS12}		400			ns			
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO12}	$C = 100 \text{ pF}$ ^{Note}			300	ns			
$\overline{\text{SCK2}}$ rise, fall time	$t_{\text{R12}},$ t_{F12}	When using external device expansion function			160	ns			
		When not using external device expansion function			1000	ns			

Note C is the load capacitance of the SO2 output line.

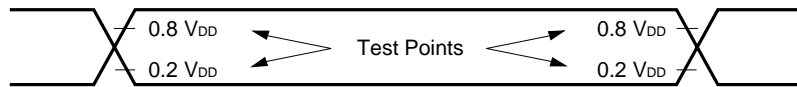
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$			78125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39063	bps
					19531	bps

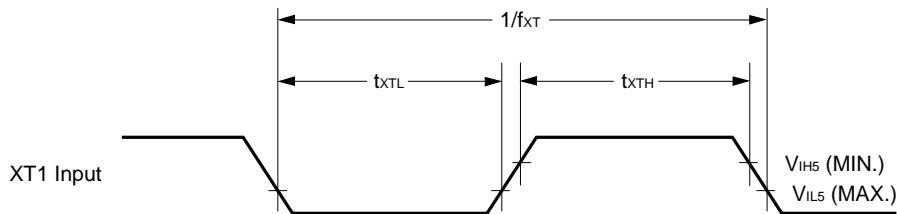
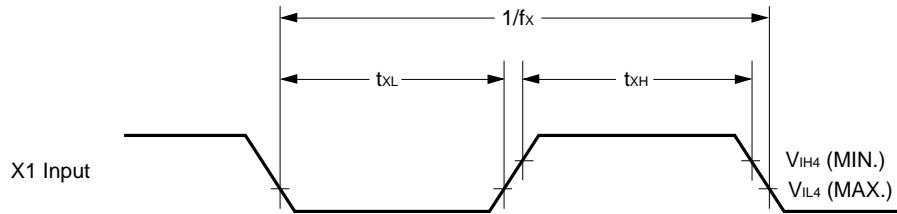
(iv) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t _{KCY13}	$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
			3200			ns
ASCK high-/low-level width	t _{KH13} ,	$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$	400			ns
	t _{KL13}	$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
			1600			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19531	bps
					9766	bps
ASCK rise, fall time	t _{R13} ,	V _{DD} = 4.5 to 6.0 V, when not using external device expansion function			1000	ns
	t _{F13}				160	ns

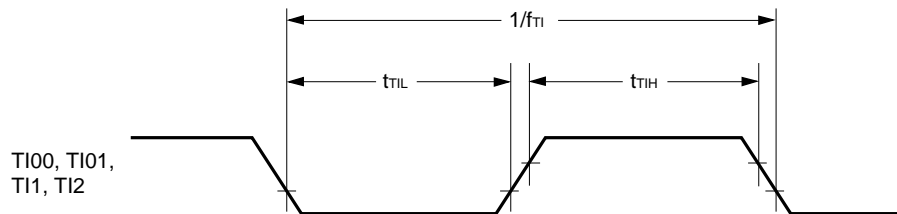
AC Timing Test Points (Excluding X1, XT1 inputs)



Clock Timing

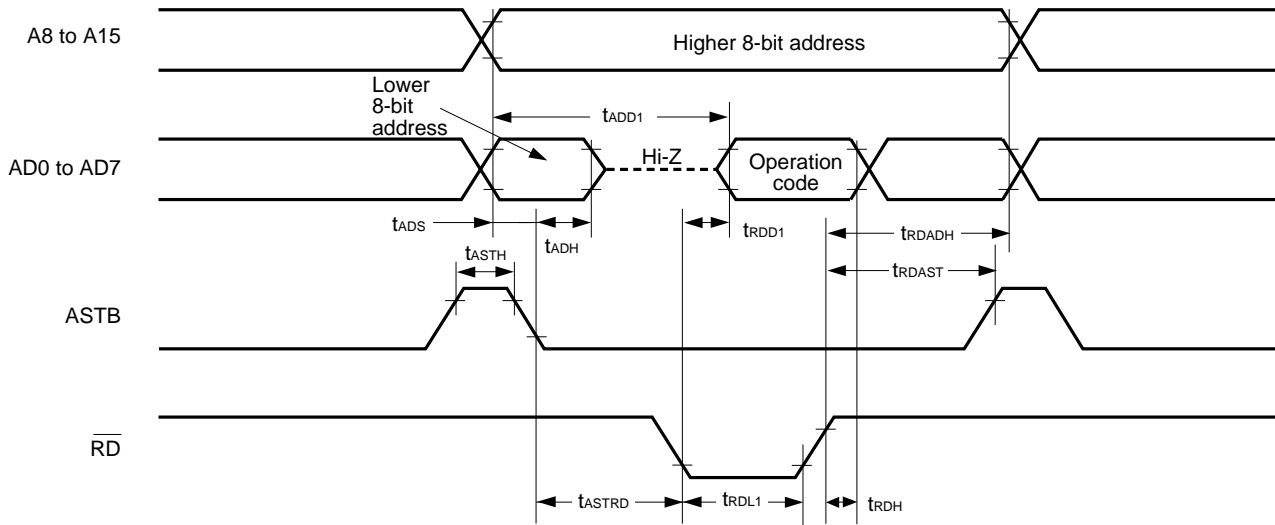


TI Timing

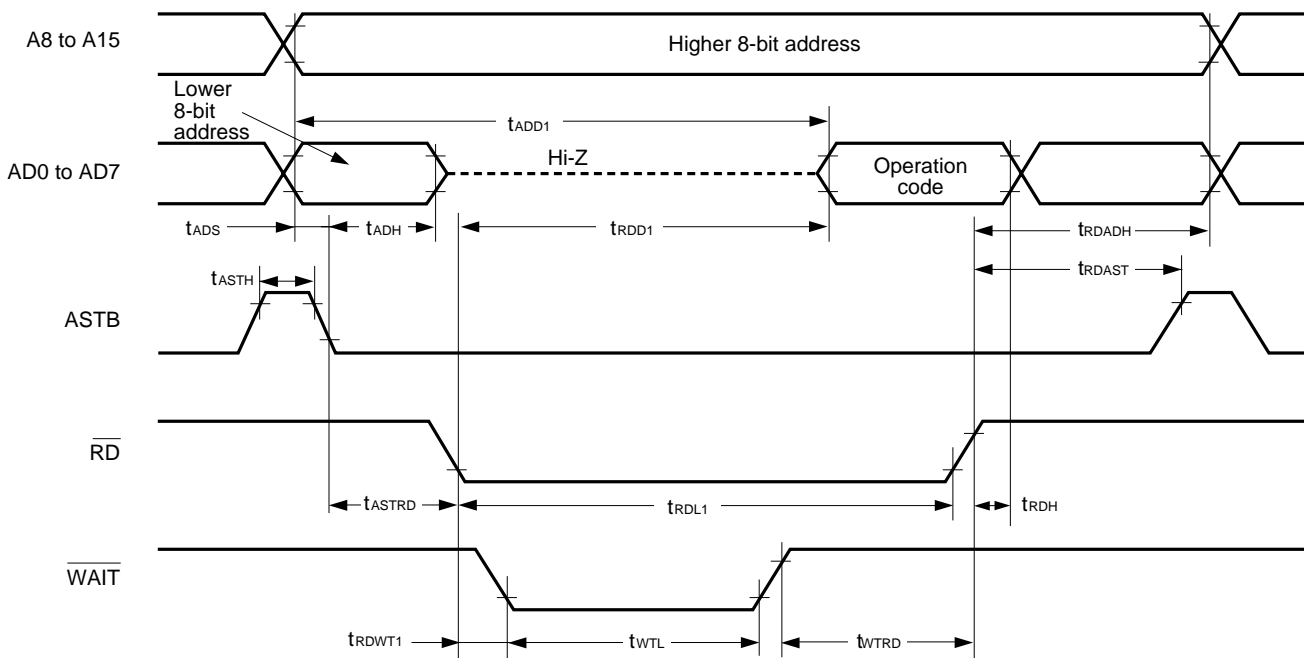


Read/Write Operations

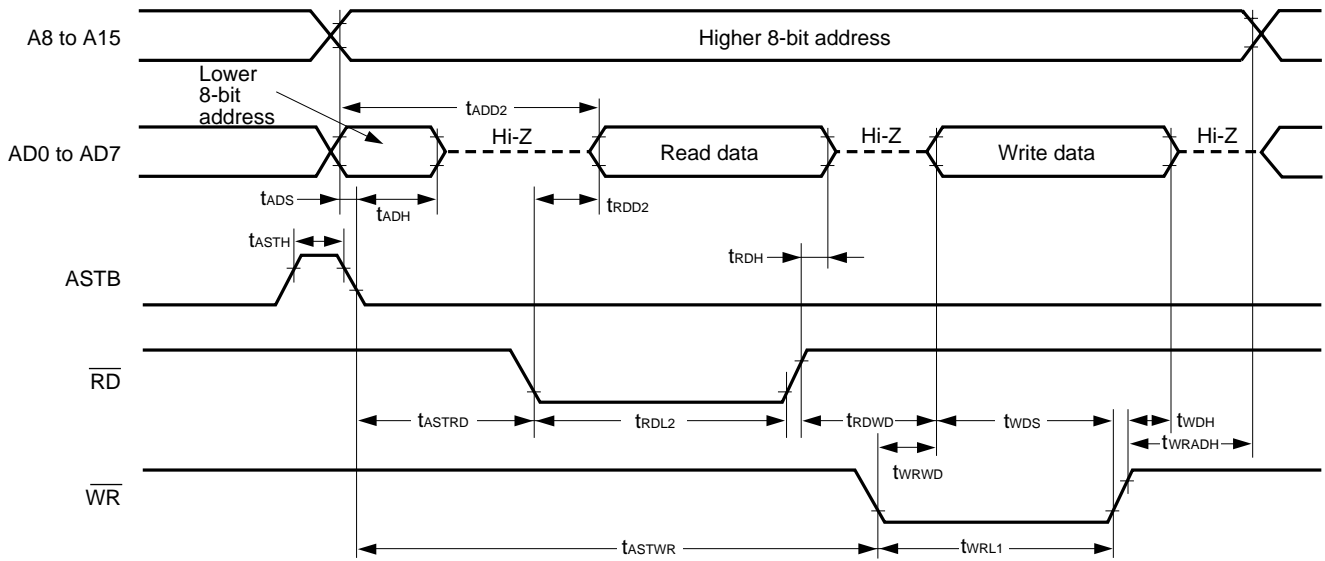
External fetch (no wait):



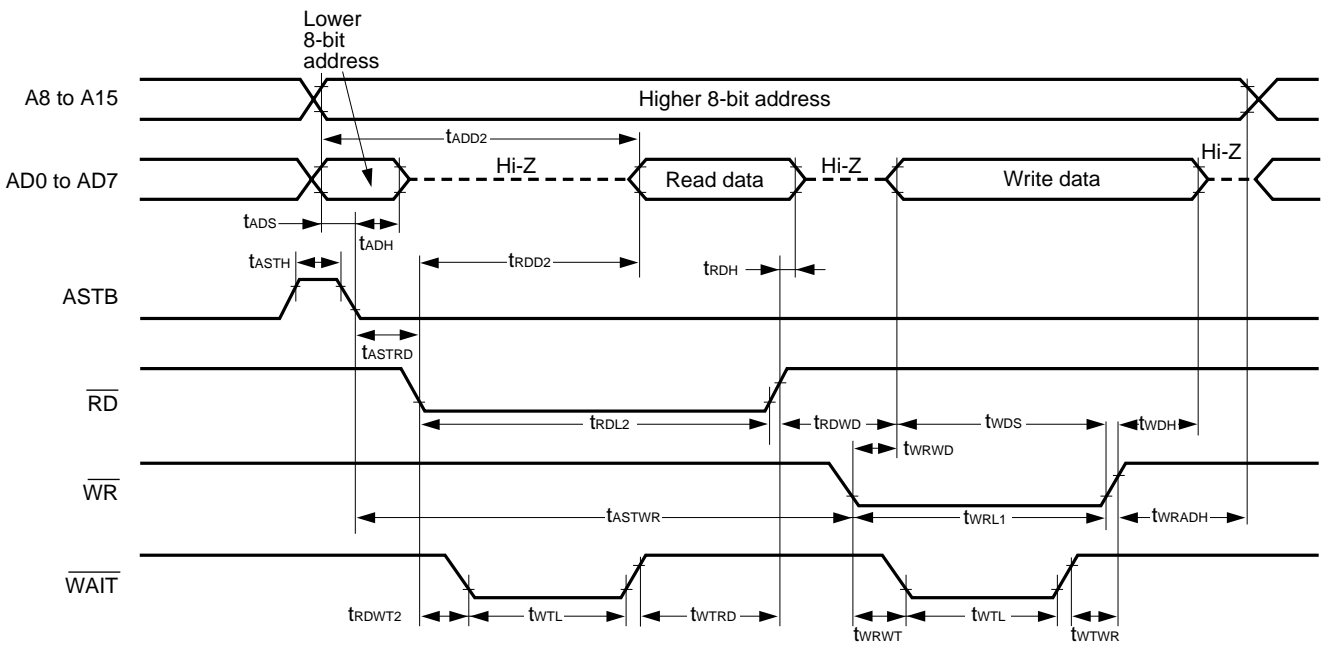
External fetch (wait insertion):



External data access (no wait):

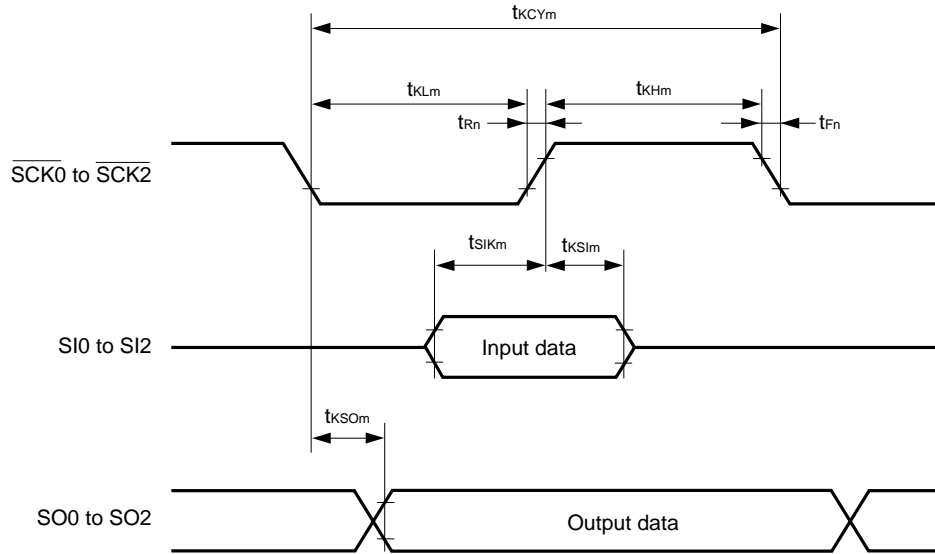


External data access (wait insertion):



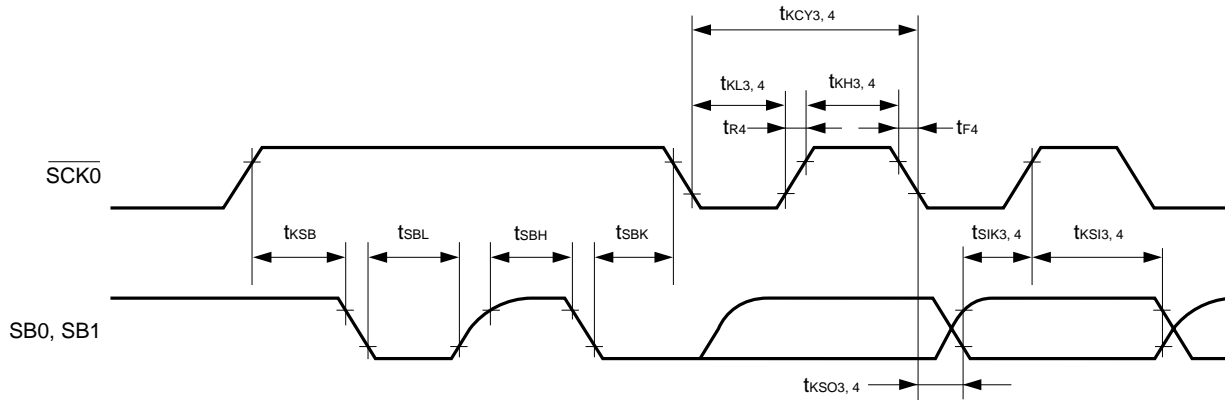
Serial Transfer Timing

3-wire serial I/O mode:

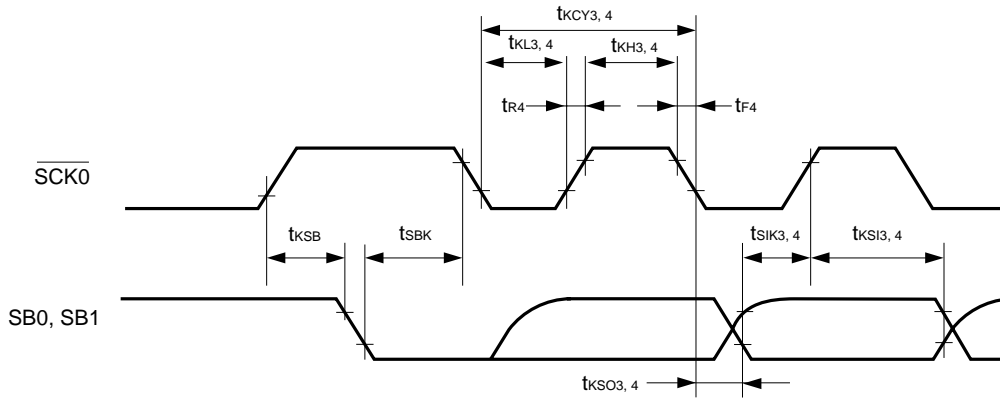


Remark $m = 1, 2, 7, 8, 11, 12$
 $n = 2, 8, 12$

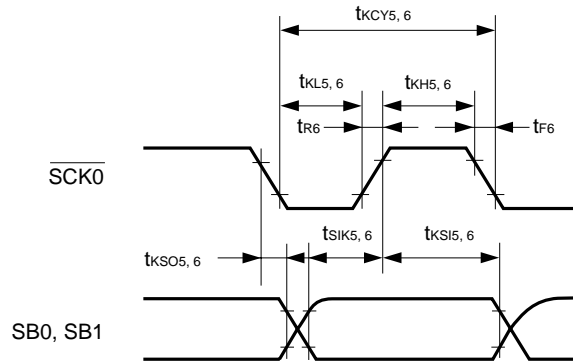
SBI mode (bus release signal transfer):



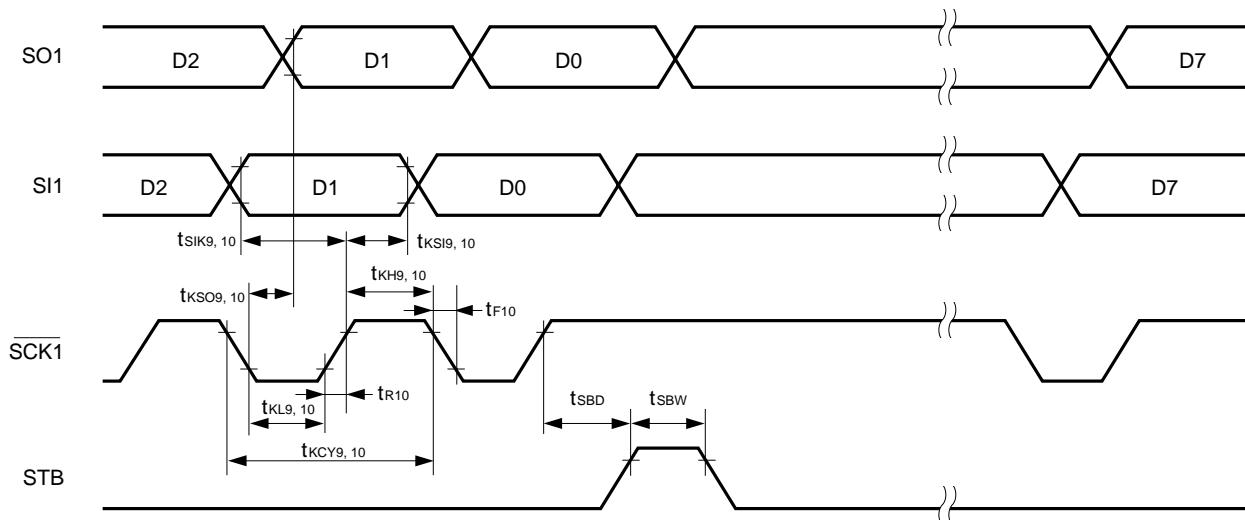
SBI mode (command signal transfer):



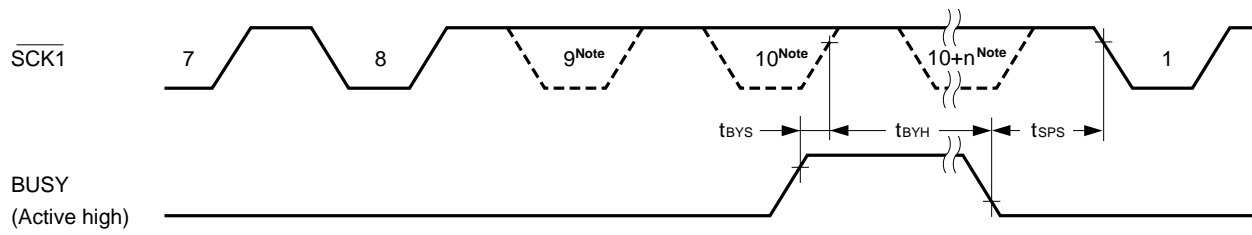
2-wire serial I/O mode:



Automatic transmit/receive function 3-wire serial I/O mode:

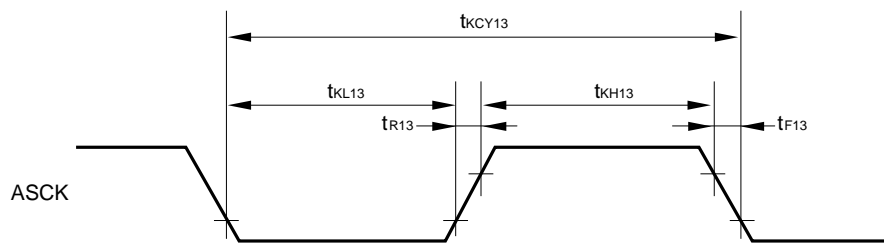


Automatic transmit/receive function 3-wire serial I/O mode (busy processing):



Note The signal is not actually driven low here; It is shown as such to indicate the timing.

UART mode (external clock input):



A/D Converter Characteristics (T_A = -40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error ^{Note}		2.7 V ≤ AV _{REF0} ≤ AV _{DD}	μPD78P054		1.0	%
			μPD78P058		1.4	%
Conversion time	t _{CONV}		19.1		200	μs
Sampling time	t _{SAMP}		12/f _{XX}			μs
Analog input voltage	V _{IAN}		AV _{SS}		AV _{REF0}	V
Reference voltage	AV _{REF0}		2.7		AV _{DD}	V
Resistance between AV _{REF0} and AV _{SS}	RA _{IREF0}		4			kΩ

Note Excludes quantization error (±1/2LSB). Shown as a percentage of the full scale value.

Remark f_{XX}: Main system clock frequency (f_X or f_X/2)
 f_X: Main system clock oscillation frequency

D/A Converter Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	bit
Overall error		R = 2 MΩ ^{Note 1}			1.2	%
		R = 4 MΩ ^{Note 1}			0.8	%
		R = 10 MΩ ^{Note 1}			0.6	%
Settling time		C = 30 pF ^{Note 1}	4.5 V ≤ AV _{REF1} ≤ 6.0 V		10	μs
			2.7 V ≤ AV _{REF1} < 4.5 V		15	μs
			2.0 V ≤ AV _{REF1} < 2.7 V		20	μs
Output resistance	R _{O0}	DACS0 = 55H		10		kΩ
	R _{O1}	DACS1 = 55H		10		kΩ
Analog reference voltage	AV _{REF1}		2.0		V _{DD}	V
AV _{REF1} current	AI _{REF1}	Note 2			1.5	mA

Notes 1. R and C are the load resistance and load capacitance of the D/A converter output pin.
 2. Value for one D/A converter channel.

Remark DACS0, DACS1: D/A conversion value setting register 0, 1

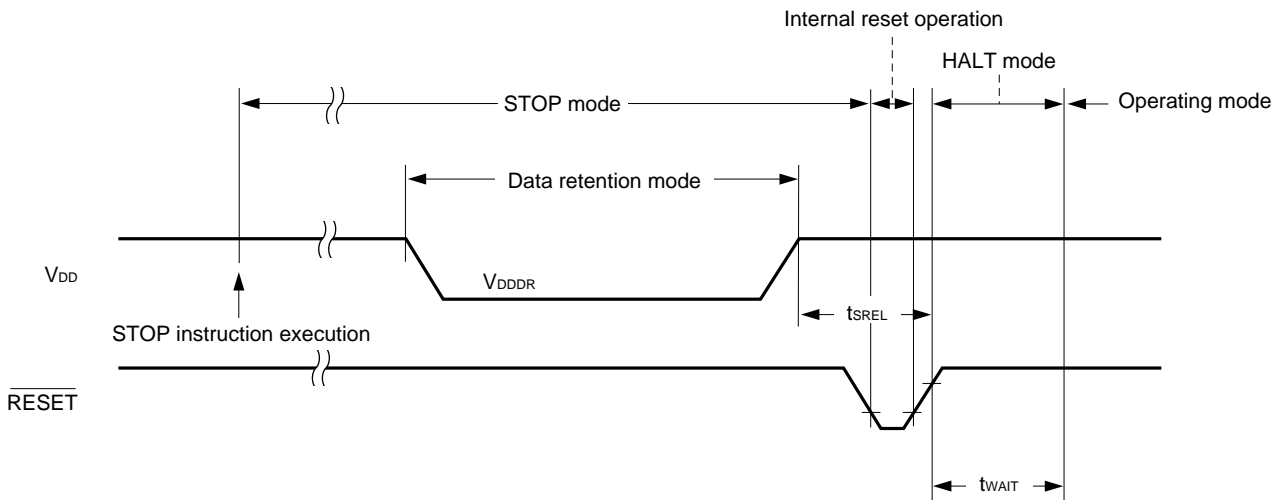
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.8		6.0	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.8 V Subsystem clock unused (XT1 = V _{DD}), feedback resistor disconnected		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt request		Note		ms

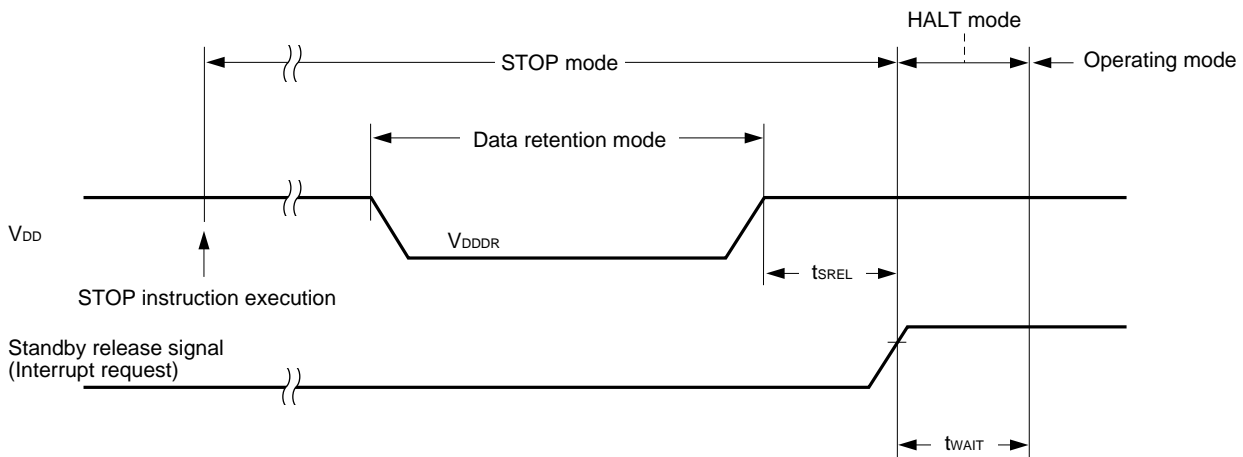
Note Selection of 2¹²/f_{xx}, or 2¹⁴/f_{xx} through 2¹⁷/f_{xx} is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_{xx}: Main system clock frequency (f_x or f_x/2)
f_x: Main system clock oscillation frequency

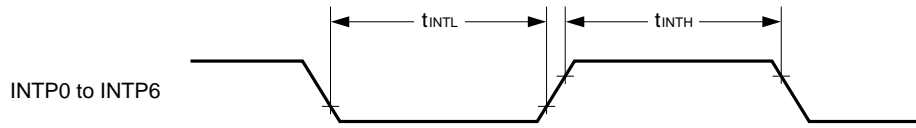
Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



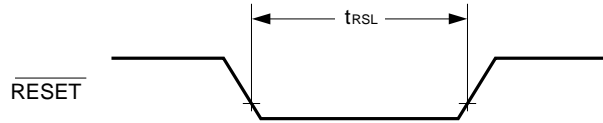
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM Programming Characteristics

DC Characteristics

(1) PROM write mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH}	V_{OH}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
Output voltage, low	V_{OL}	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM} = V_{IL}$			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM read mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 5.0 \pm 0.5\text{ V}$, $V_{PP} = V_{DD} \pm 0.6\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH1}	V_{OH1}	$I_{OH} = -1\text{ mA}$	$V_{DD} - 1.0$			V
	V_{OH2}	V_{OH2}	$I_{OH} = -100\ \mu\text{A}$	$V_{DD} - 0.5$			V
Output voltage, low	V_{OL}	V_{OL}	$I_{OL} = 1.6\text{ mA}$			0.4	V
Input leakage current	I_{LI}	I_{LI}	$0 \leq V_{IN} \leq V_{DD}$	-10		+10	μA
Output leakage current	I_{LO}	I_{LO}	$0 \leq V_{OUT} \leq V_{DD}$, $\overline{OE} = V_{IH}$	-10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		$V_{DD} - 0.6$	V_{DD}	$V_{DD} + 0.6$	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	$V_{PP} = V_{DD}$			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$			50	mA

Note Corresponding symbols for the μPD27C1001A.

AC Characteristics

(1) PROM write mode

(a) Page program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{OE}}\downarrow$)	t _{AS}	t _{AS}		2			μs
$\overline{\text{OE}}$ set time	toES	toES		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{OE}}\downarrow$)	t _{CES}	t _{CES}		2			μs
Input data setup time (to $\overline{\text{OE}}\downarrow$)	t _{DS}	t _{DS}		2			μs
Address hold time (from $\overline{\text{OE}}\uparrow$)	t _{AH}	t _{AH}		2			μs
	t _{AHL}	t _{AHL}		2			μs
	t _{AHV}	t _{AHV}		0			μs
Input data hold time (from $\overline{\text{OE}}\uparrow$)	t _{DH}	t _{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t _{DF}	t _{DF}		0		250	ns
V _{PP} setup time (to $\overline{\text{OE}}\downarrow$)	t _{VPS}	t _{VPS}		1.0			ms
V _{DD} setup time (to $\overline{\text{OE}}\downarrow$)	t _{VDS}	t _{VCS}		1.0			ms
Program pulse width	t _{PW}	t _{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	toE	toE				1	μs
$\overline{\text{OE}}$ pulse width during data latching	t _{LW}	t _{LW}		1			μs
$\overline{\text{PGM}}$ set time	t _{PGMS}	t _{PGMS}		2			μs
$\overline{\text{CE}}$ hold time	t _{CEH}	t _{CEH}		2			μs
$\overline{\text{OE}}$ hold time	toEH	toEH		2			μs

(b) Byte program mode ($T_A = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6.5 \pm 0.25\text{ V}$, $V_{PP} = 12.5 \pm 0.3\text{ V}$)

Parameter	Symbol	Symbol ^{Note}	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{\text{PGM}}\downarrow$)	t _{AS}	t _{AS}		2			μs
$\overline{\text{OE}}$ set time	toES	toES		2			μs
$\overline{\text{CE}}$ setup time (to $\overline{\text{PGM}}\downarrow$)	t _{CES}	t _{CES}		2			μs
Input data setup time (to $\overline{\text{PGM}}\downarrow$)	t _{DS}	t _{DS}		2			μs
Address hold time (from $\overline{\text{OE}}\uparrow$)	t _{AH}	t _{AH}		2			μs
Input data hold time (from $\overline{\text{PGM}}\uparrow$)	t _{DH}	t _{DH}		2			μs
Data output float delay time from $\overline{\text{OE}}\uparrow$	t _{DF}	t _{DF}		0		250	ns
V _{PP} setup time (to $\overline{\text{PGM}}\downarrow$)	t _{VPS}	t _{VPS}		1.0			ms
V _{DD} setup time (to $\overline{\text{PGM}}\downarrow$)	t _{VDS}	t _{VCS}		1.0			ms
Program pulse width	t _{PW}	t _{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{\text{OE}}\downarrow$	toE	toE				1	μs
$\overline{\text{OE}}$ hold time	toEH	—		2			μs

Note Corresponding symbols for the μPD27C1001A.

(2) PROM read mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

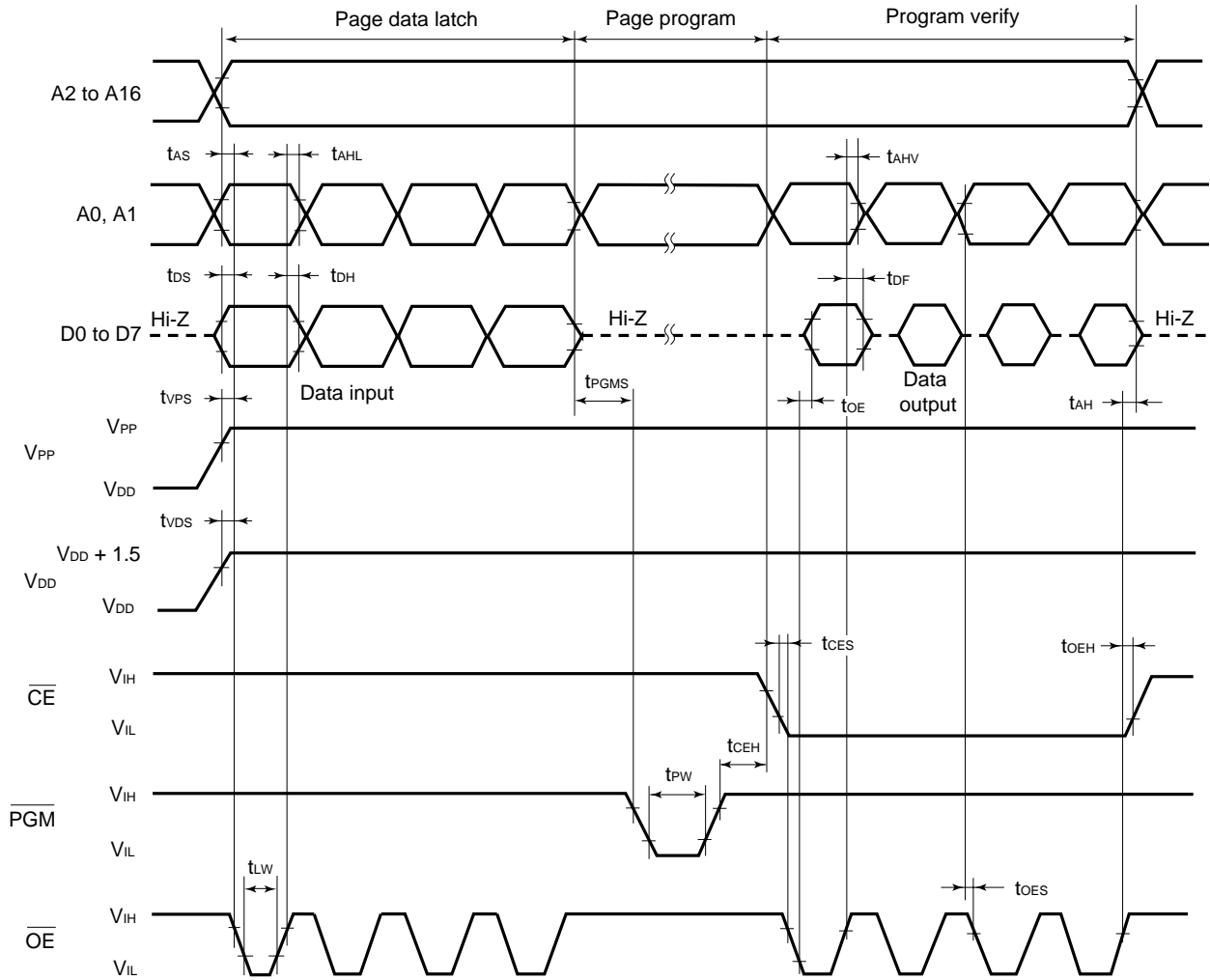
Parameter	Symbol	Symbol ^{Note}	Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t _{ACC}	t _{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{CE} \downarrow$	t _{CE}	t _{CE}	$\overline{OE} = V_{IL}$			800	ns
Data output delay time from $\overline{OE} \downarrow$	t _{OE}	t _{OE}	$\overline{CE} = V_{IL}$			200	ns
Data output float delay time from $\overline{OE} \uparrow$	t _{DF}	t _{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Data hold time from address	t _{OH}	t _{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note Corresponding symbols for the μPD27C1001A.

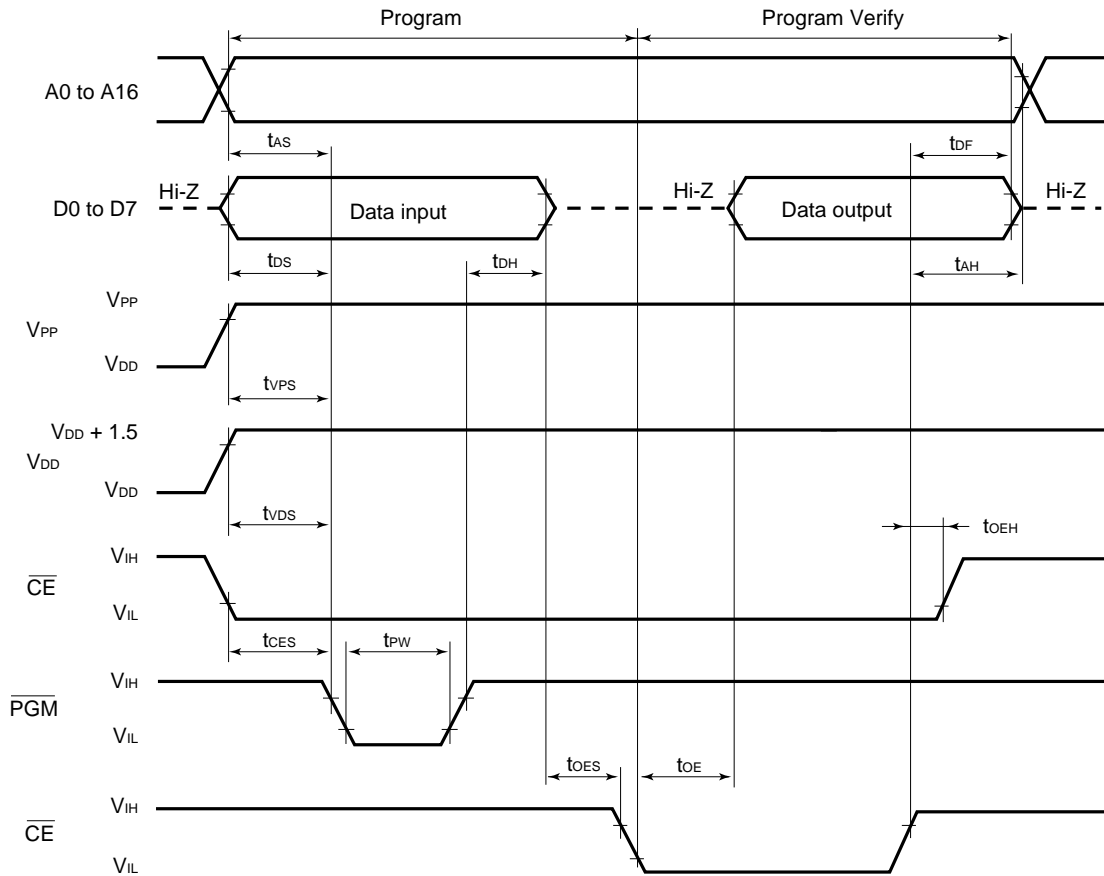
(3) PROM programming mode setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t _{SMA}		10			μs

PROM Write Mode Timing (Page program mode)

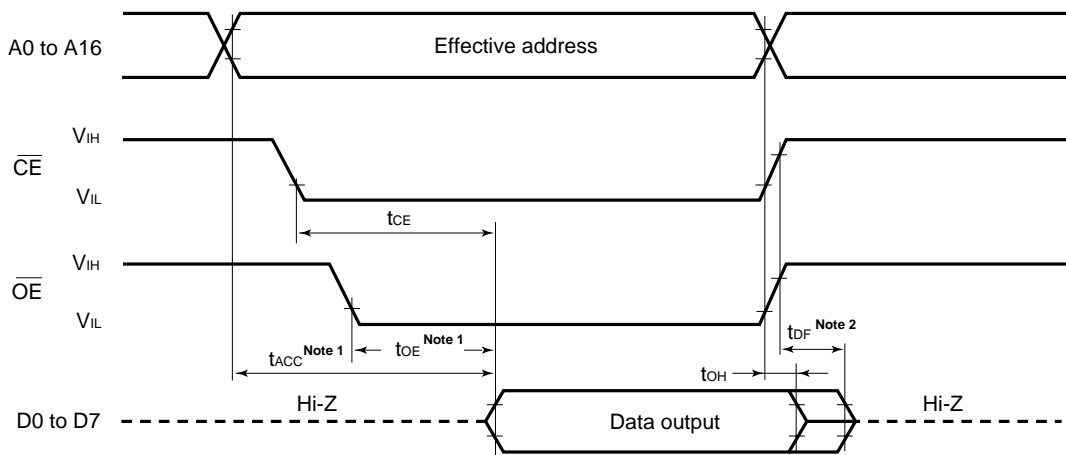


PROM Write Mode Timing (Byte program mode)



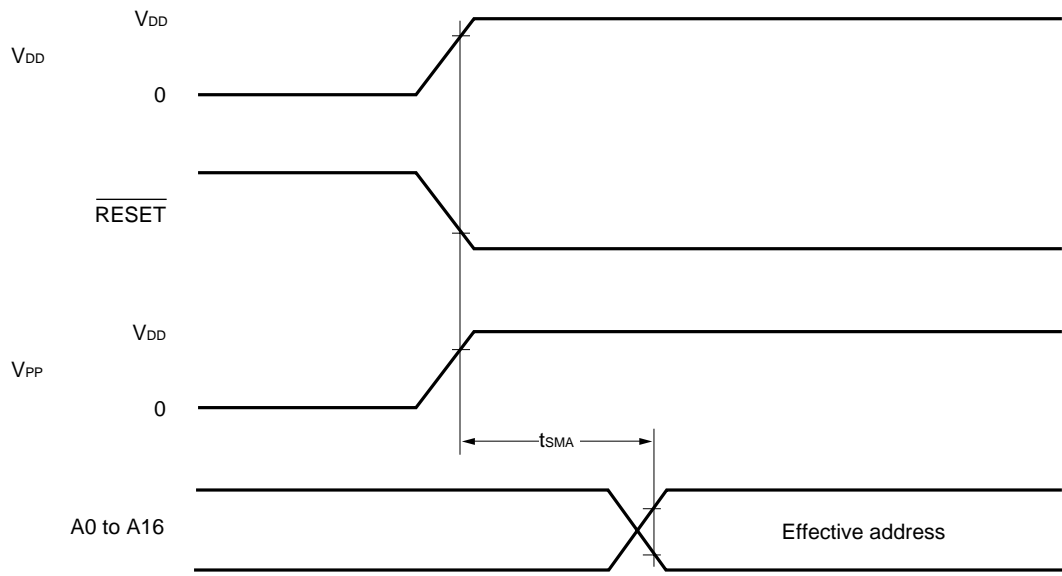
- Cautions**
1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.
 2. V_{PP} must not exceed +13.5 V including overshoot.
 3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

PROM Read Mode Timing



- Notes**
1. To read within the t_{ACC} range, make the delay time from the \overline{OE} input to the fall of \overline{CE} a maximum of $t_{ACC} - t_{OE}$.
 2. t_{DF} is the time from when either \overline{OE} or \overline{CE} first reaches V_{IH}.

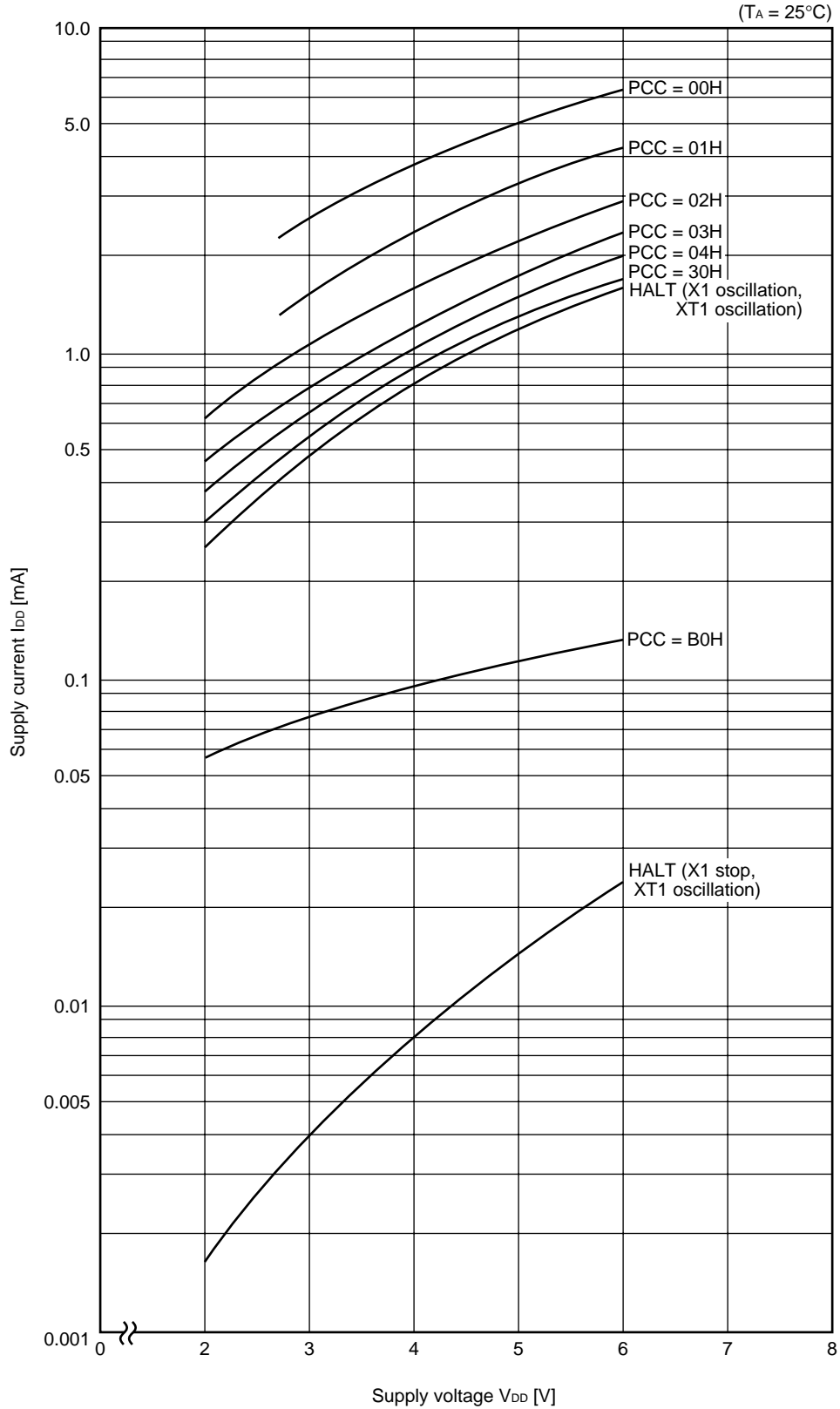
PROM Programming Mode Setting Timing



10. CHARACTERISTICS CURVES (FOR REFERENCE ONLY)

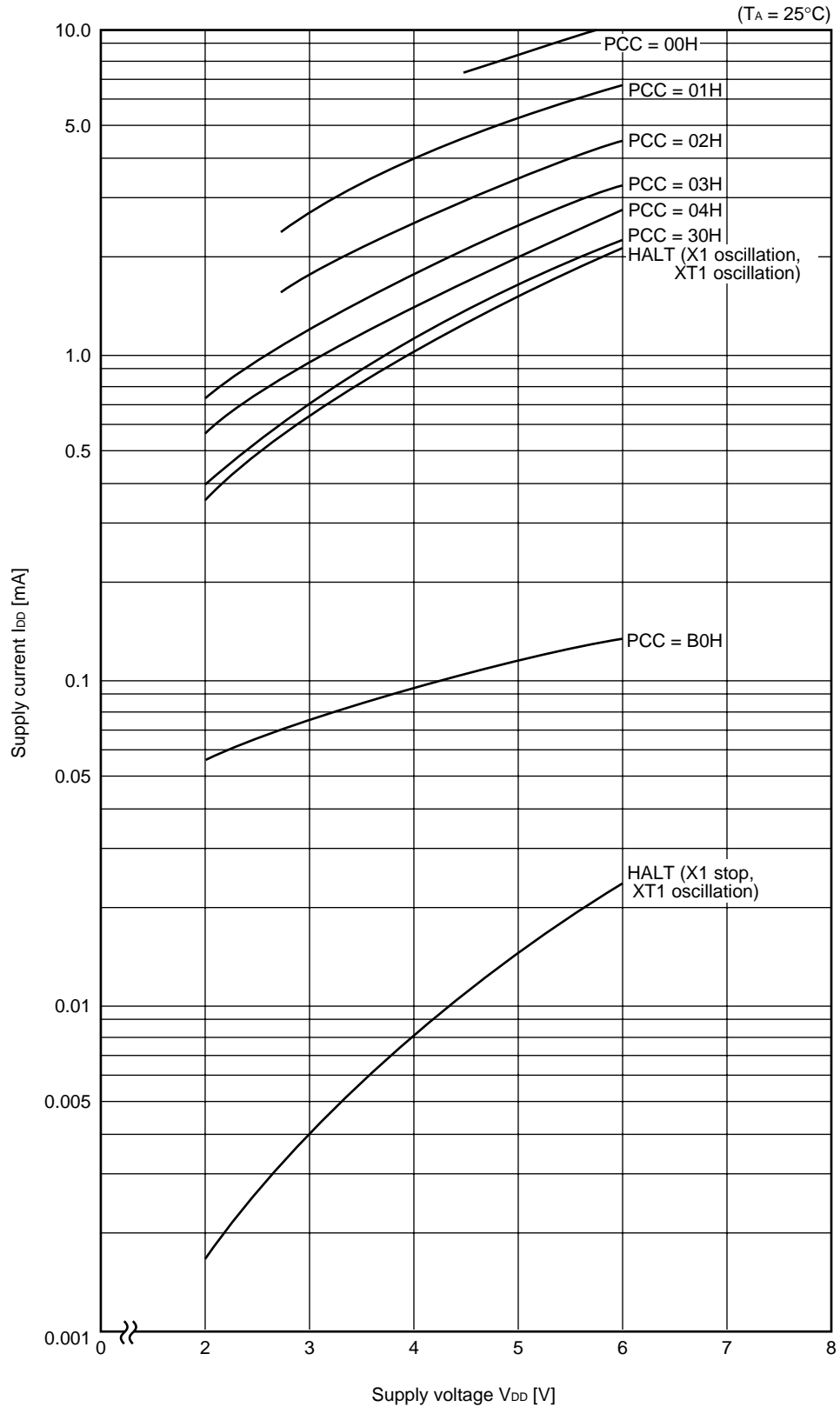
(1) Characteristics curves of μPD78P054 (1/2)

I_{DD} vs V_{DD} (f_x = 5.0 MHz, f_{xx} = 2.5 MHz)



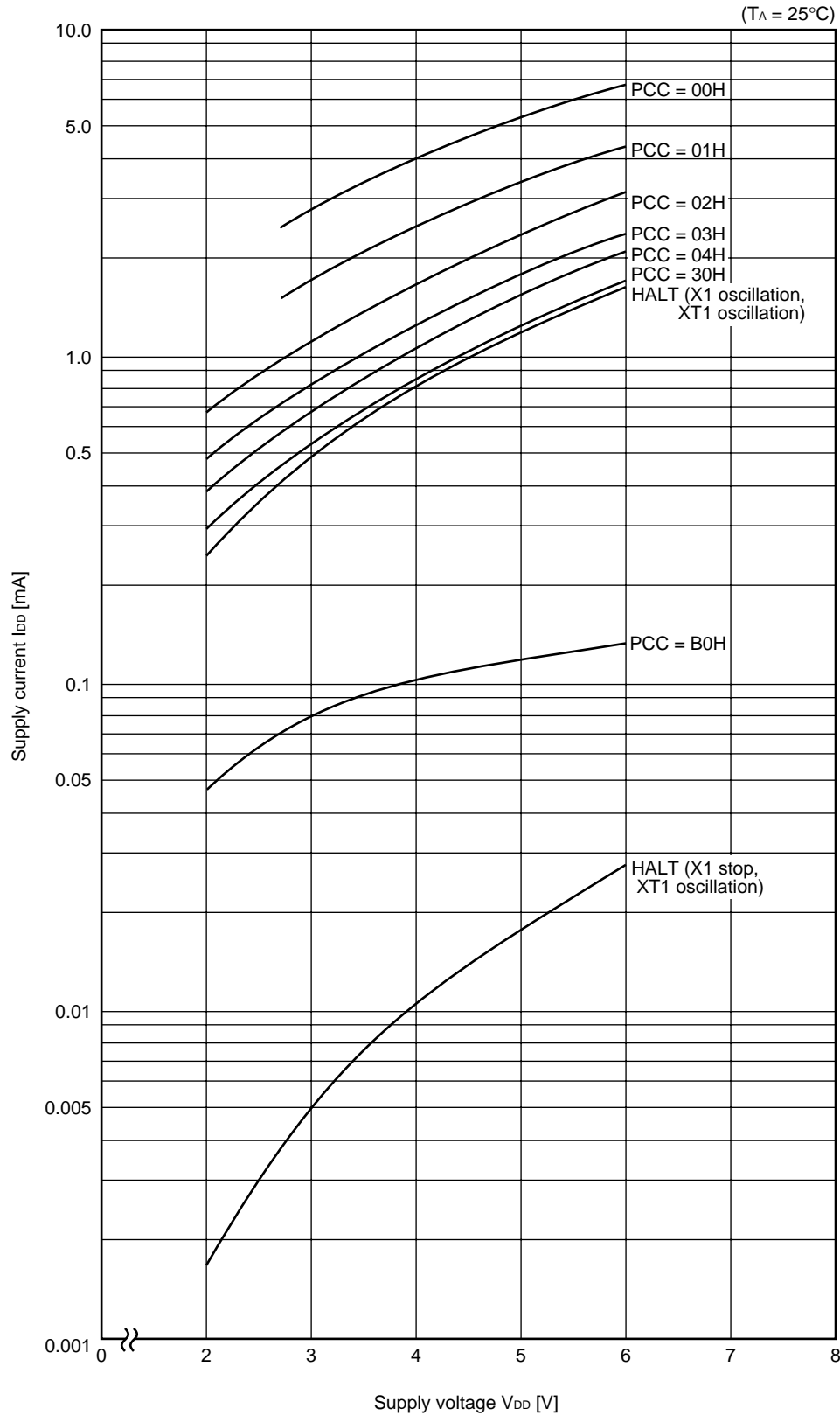
(1) Characteristics curves of μPD78P054 (2/2)

I_{DD} vs V_{DD} (f_x = f_{xx} = 5.0 MHz)



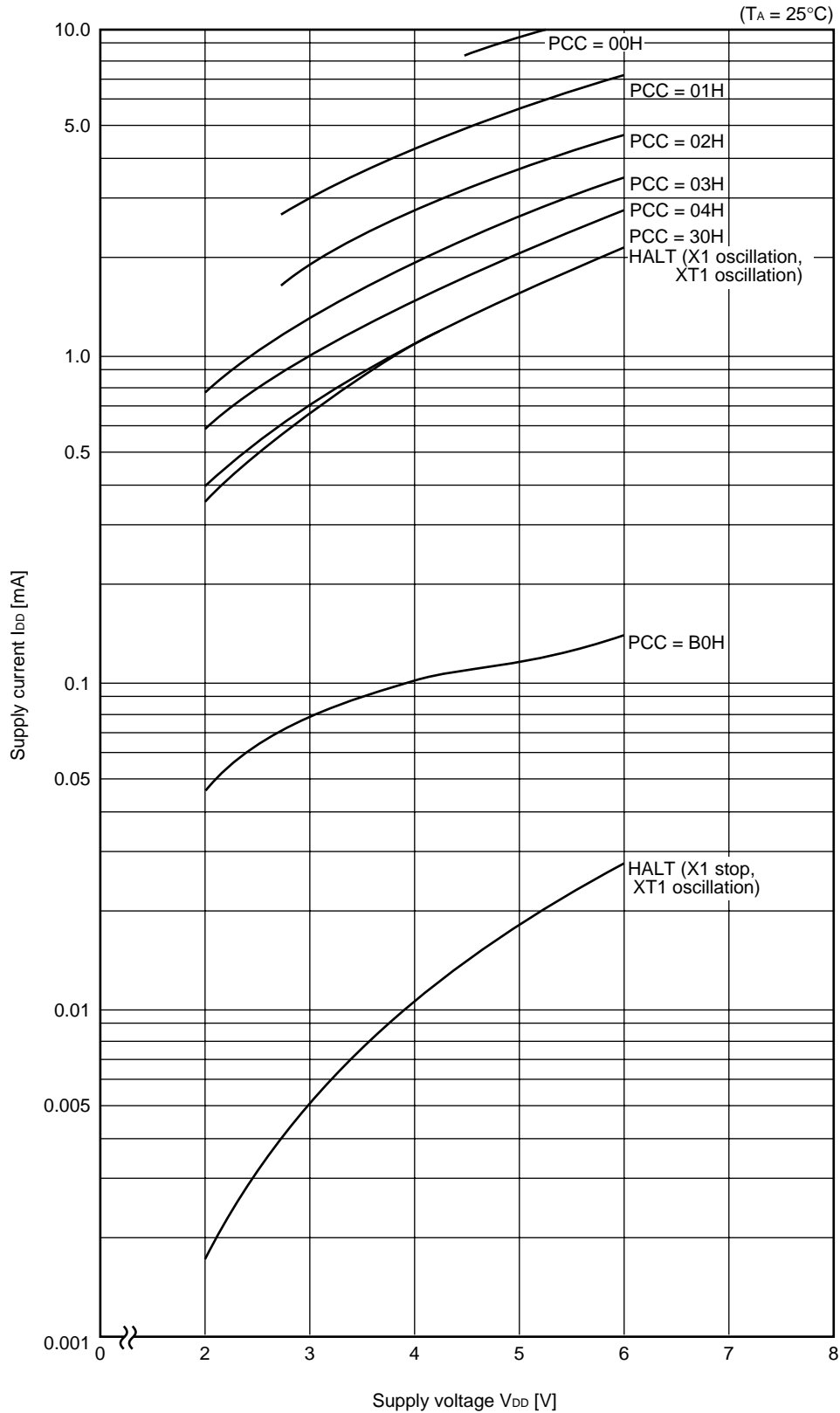
(2) Characteristics curves of μPD78P058 (1/2)

I_{DD} vs V_{DD} (f_x = 5.0 MHz, f_{xx} = 2.5 MHz)



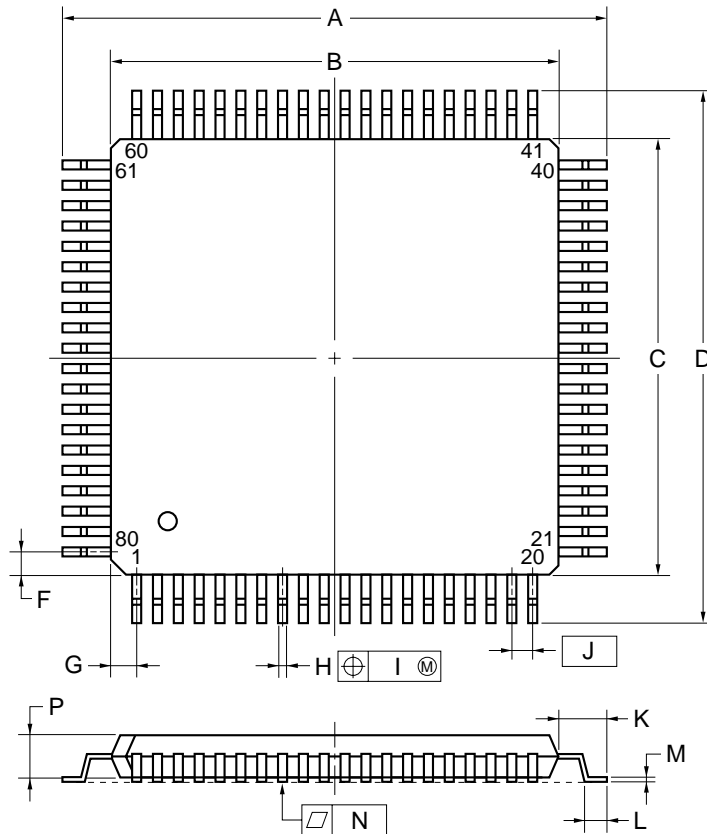
(2) Characteristics curves of μPD78P058 (2/2)

I_{DD} vs V_{DD} (f_x = f_{xx} = 5.0 MHz)

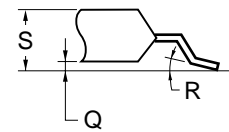


11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

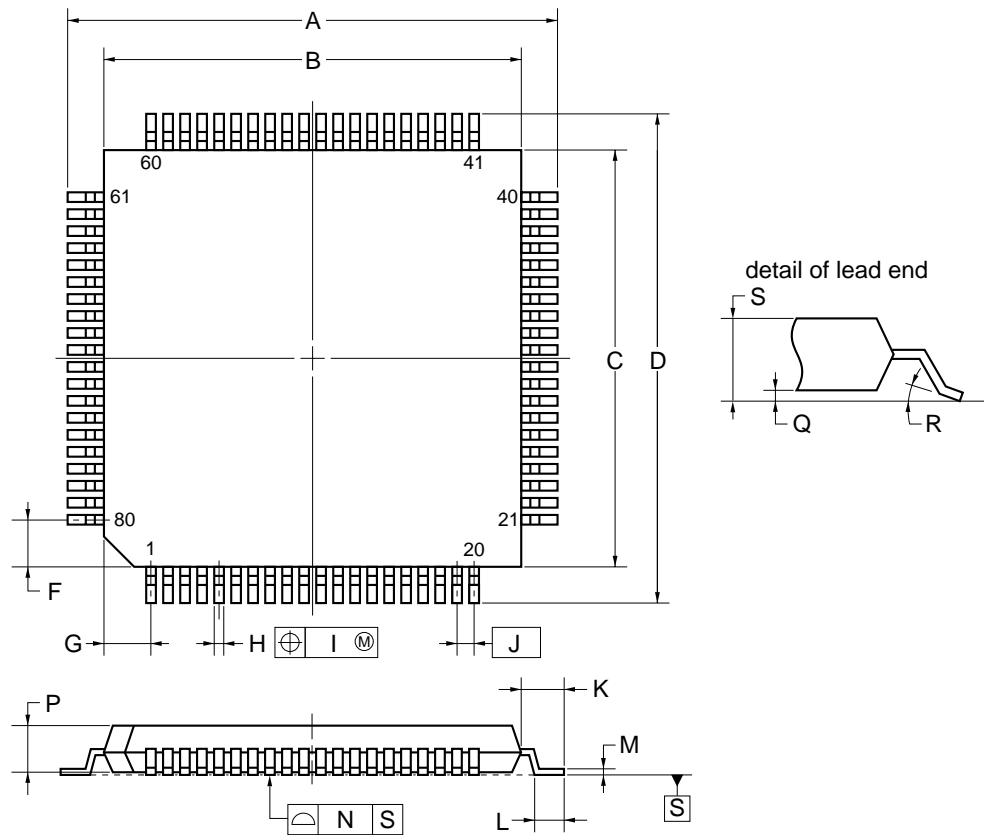
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	0.551 ^{+0.009} _{-0.008}
C	14.00±0.20	0.551 ^{+0.009} _{-0.008}
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	0.013 ^{+0.002} _{-0.003}
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	0.031 ^{+0.009} _{-0.008}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

Remark The dimensions and materials of ES products are the same as those of mass-production products.

80 PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

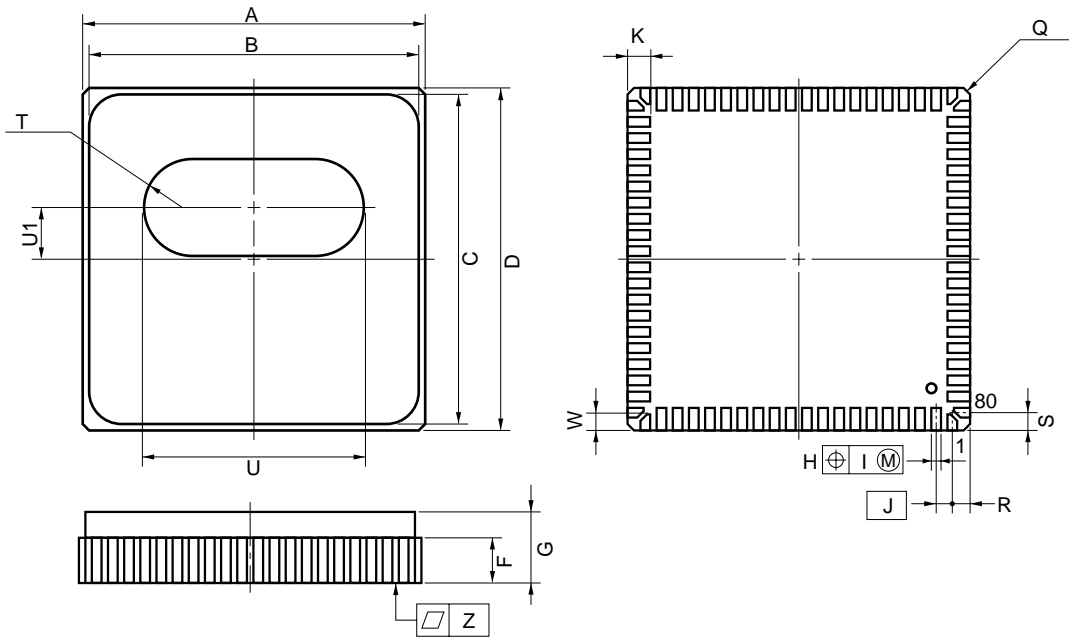
Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.00±0.20
B	12.00±0.20
C	12.00±0.20
D	14.00±0.20
F	1.25
G	1.25
H	0.22 ^{+0.05} _{-0.04}
I	0.10
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.145 ^{+0.055} _{-0.045}
N	0.10
P	1.05±0.07
Q	0.10±0.05
R	5°±5°
S	1.27 MAX.

P80GK-50-BE9-6

Remark The dimensions and materials of ES products are the same as those of mass-production products.

80 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X80KW-65A-1

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	0.018 ^{+0.004} _{-0.005}
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	0.039 ^{+0.007} _{-0.006}
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	0.030 ^{+0.006} _{-0.007}
Z	0.10	0.004

12. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, please contact your NEC sales representative.

Table 12-1. Surface Mount Type Soldering Conditions (1/2)

- ★ (1) μPD78P054GC-8BT : 80-pin plastic QFP (14 × 14 mm, resin thickness: 1.4 mm)
 μPD78P058GC-8BT : 80-pin plastic QFP (14 × 14 mm, resin thickness: 1.4 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: 2 times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 12-1. Surface Mount Type Soldering Conditions (2/2)

(2) μPD78P054GK-BE9 : 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: 3 times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: 3 times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

★ **APPENDIX A. DEVELOPMENT TOOLS**

The following support tools are available for system development using the μPD78P054 and 78P058.
Refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF78054	μPD78054 Subseries device file
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P054GC PA-78P054GK PA-78P054KK-T	Programmer adapter connected to a PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tools

• **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA ^{Note}	Performance board to enhance and expand the function of IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 Series (except notebook type computer) as a host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook type computer as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as the host machine
IE-70000-PCI-IF	Adapter necessary when using computer including PCI bus as the host machine
IE-780308-NS-EM1	Emulation board common to μPD780308 Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket to connect target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted and NP-80GC
TGK-080SDW	Conversion adapter to connect target system board on which 80-pin plastic TQFP (GK-BE9 type) can be mounted and NP-80GK
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF78054	Device file for μPD78054 Subseries

Note Under development

• When using in-circuit emulator IE-78001-R-A

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 Series (except notebook type computer) as the host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using computer including PCI bus as the host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as the host machine
IE-780308-NS-EM1 IE-780308-R-EM	Emulation board common to μPD780308 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780308-NS-EM1 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (GK-BE9 type)
EV-9200GC-80	Conversion socket to connect target system board on which 80-pin plastic QFP (GC-8BT type) can be mounted and EP-78230GC-R
TGK-080SDW	Conversion adapter to connect target system board on which 80-pin plastic TQFP (GK-BE9 type) can be mounted and EP-78054GK-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF78054	Device file for μPD78054 Subseries

(4) Real-Time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

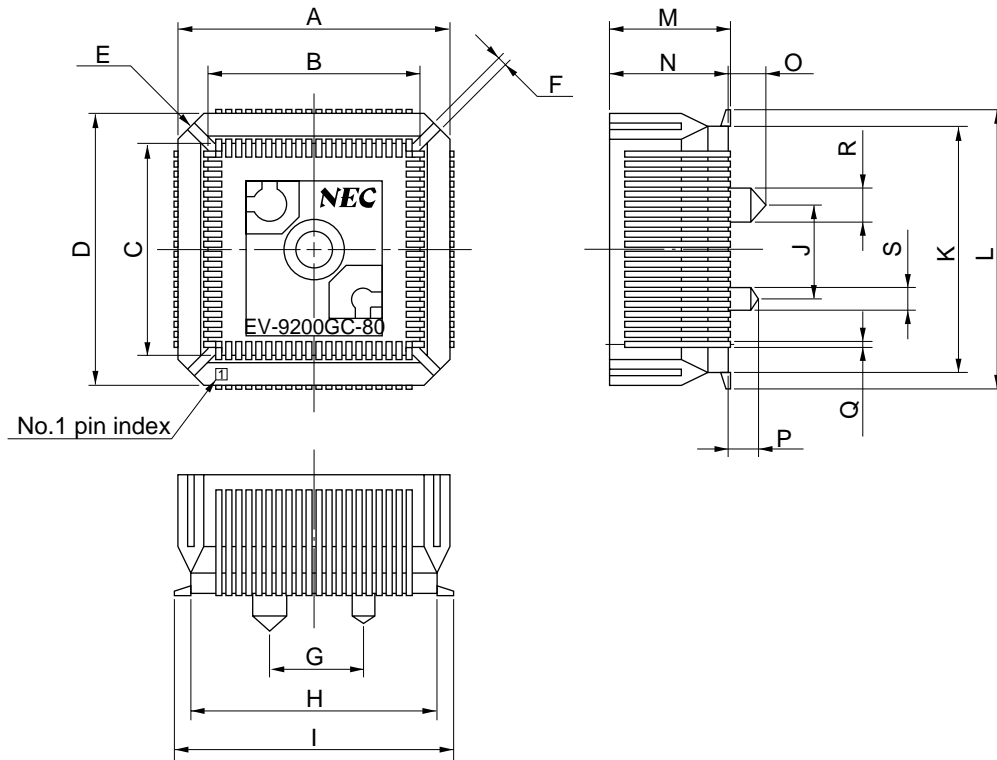
- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78054.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF78054.
- The NP-80GC and NP-80GK are the products of Naito Densai Machida Mfg. Co., Ltd. (TEL +81-44-822-3813).
Consult an NEC sales representative regarding purchase of these products.
- The TGK-080SDW is a product of TOKYO ELETECH CORPORATION.
Reference : Daimaru Kogyo Corporation Tokyo electronic (TEL +81-3-3820-7112)
Osaka electronic (TEL +81-6-6244-6672)
- For third party development tools, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machines and operating systems corresponding to each software are as follows.

Host Machine [OS]	PC	EWS
	PC-9800 Series [Windows™] IBM PC/AT compatibles [Japanese/English Windows]	HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
Software		
RA78K/0	√ Note	√
CC78K/0	√ Note	√
PG-1500 controller	√ Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√ Note	√
MX78K0	√ Note	√

Note DOS-based software

CONVERSION SOCKET (EV-9200GC-80) DRAWING AND FOOTPRINT

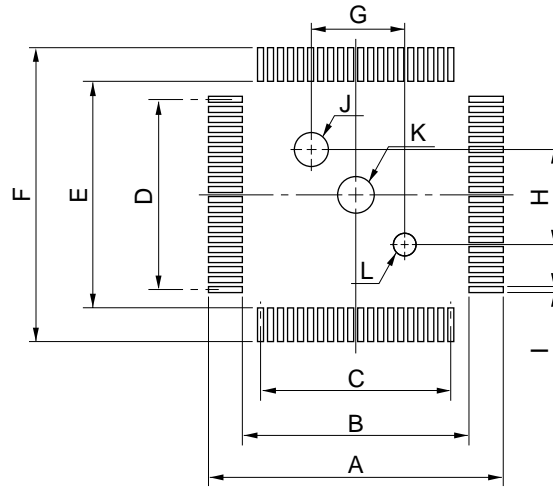
Figure A-1. EV-9200GC-80 Drawing (For Reference Only)



EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. EV-9200GC-80 Footprint (For Reference Only)



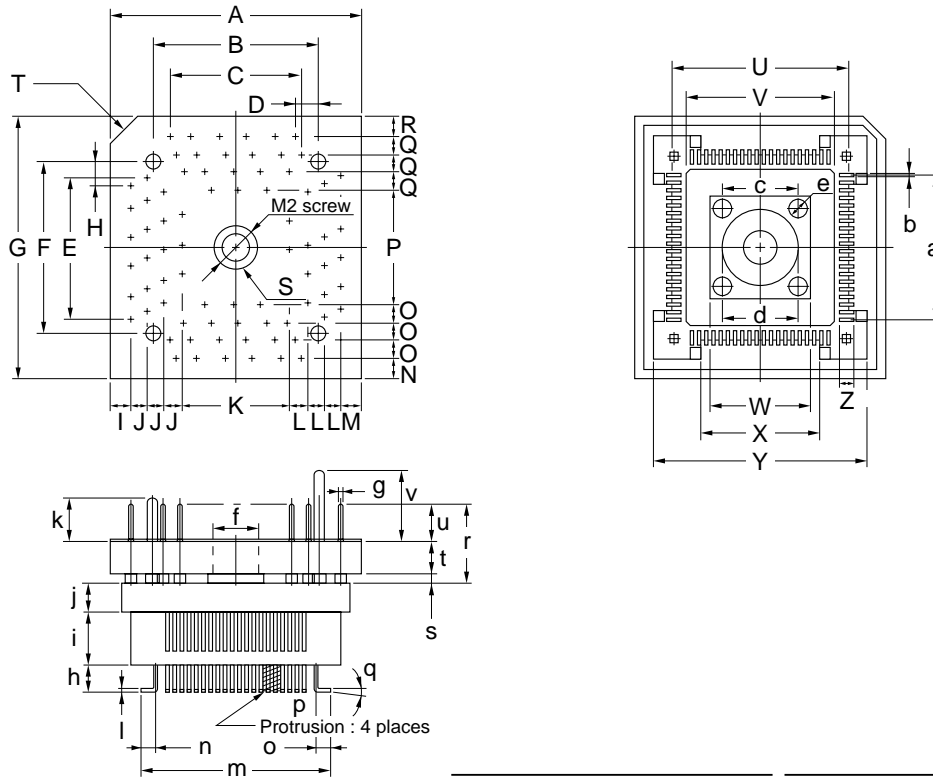
EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

CONVERSION ADAPTER (TGK-080SDW) DRAWING

Figure A-3. TGK-080SDW Drawing (For Reference Only)



ITEM	MILLIMETERS	INCHES	ITEM	MILLIMETERS	INCHES
A	18.0	0.709	a	0.5x19=9.5±0.10	0.020x0.748=0.374±0.004
B	11.77	0.463	b	0.25	0.010
C	0.5x19=9.5	0.020x0.748=0.374	c	φ5.3	φ0.209
D	0.5	0.020	d	φ5.3	φ0.209
E	0.5x19=9.5	0.020x0.748=0.374	e	φ1.3	φ0.051
F	11.77	0.463	f	φ3.55	φ0.140
G	18.0	0.709	g	φ0.3	φ0.012
H	0.5	0.020	h	1.85±0.2	0.073±0.008
I	1.58	0.062	i	3.5	0.138
J	1.2	0.047	j	2.0	0.079
K	7.64	0.301	k	3.0	0.118
L	1.2	0.047	l	0.25	0.010
M	1.58	0.062	m	14.0	0.551
N	1.58	0.062	n	1.4±0.2	0.055±0.008
O	1.2	0.047	o	1.4±0.2	0.055±0.008
P	7.64	0.301	p	h=1.8 φ1.3	h=0.071 φ0.051
Q	1.2	0.047	q	0-5°	0.000-0.197°
R	1.58	0.062	r	5.9	0.232
S	φ3.55	φ0.140	s	0.8	0.031
T	C 2.0	C 0.079	t	2.4	0.094
U	12.31	0.485	u	2.7	0.106
V	10.17	0.400	v	3.9	0.154
W	6.8	0.268	TGK-080SDW-G1E		
X	8.24	0.324			
Y	14.8	0.583			
Z	1.4±0.2	0.055±0.008			

note: Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No. (English)	Document No. (Japanese)
μPD78054, 78054Y Subseries User's Manual	U11747E	U11747J
μPD78052, 78053, 78054, 78055, 78056, 78058 Data Sheet	U12327E	U12327J
μPD78P054, 78P058 Data Sheet	This document	U10417J
78K/0 Series User's Manual Instructions	U12326E	U12326J
78K/0 Series Instruction Set	—	U10904J
78K/0 Series Instruction Table	—	U10903J
μPD78054 Subseries Special Function Register Table	—	U10102J
78K/0 Series Application Note	Basic (III)	U10182E
	Floating Point Arithmetic Programs	IEA-1289

Documents Related to Development Tools (User's Manuals)

Document Name	Document No. (English)	Document No. (Japanese)
RA78K0 Assembler Package	Operation	U11802E
	Assembly Language	U11801E
	Structured Assembly Language	U11789E
RA78K Series Structured Assembler Preprocessor	EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
CC78K0 C Compiler Application Note	Programming Know-how	U13034E
PG-1500 PROM Programmer	U11940E	U11940J
PG-1500 Controller PC-9800 Series (MS-DOS™) based	EEU-1291	EEU-704
PG-1500 Controller IBM PC Series (PC DOS™) based	U10540E	EEU-5008
IE-78K0-NS	To be prepared	To be prepared
IE-78001-R-EM	To be prepared	To be prepared
IE-780308-NS-EM1	To be prepared	To be prepared
IE-780308-R-EM	U11362E	U11362J
EP-78230	EEU-1515	EEU-985
EP-78054GK-R	EEU-1468	EEU-932
SM78K0 System Simulator Windows based	Reference	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
ID78K0-NS Integrated Debugger Windows based	Reference	U12900E
ID78K0 Integrated Debugger EWS based	Reference	—
ID78K0 Integrated Debugger PC based	Reference	U11539E
ID78K0 Integrated Debugger Windows based	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Microcomputer Product Series Guide	—	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.

Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH

Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.

Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.

Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH

Scandinavia Office
Taebly, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

FIP, IEBus, and QTOP are trademarks of NEC Corporation.

MS-DOS and Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.

PC/AT and PC DOS are trademarks of International Business Machines Corporation.

HP9000 Series 700 and HP-UX are trademarks of Hewlett-Packard Company.

SPARCstation is a trademark of SPARC International, Inc.

Solaris and SunOS are trademarks of Sun Microsystems, Inc.

NEWS and NEWS-OS are trademarks of Sony Corporation.

The export of these products from Japan is regulated by the Japanese government. The export of some or all of these products may be prohibited without governmental license. To export or re-export some or all of these products from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

License not needed: μPD78P054KK-T, 78P058KK-T

The customer must judge the need for license: μPD78P054GC-8BT, 78P054GK-BE9

μPD78P058GC-8BT

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
 - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
 - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
 - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
 - While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
 - NEC devices are classified into the following three quality grades:
 - "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
 - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.