TEXAS INSTRUMENTS

DRV593 and DRV594 PWM Power Driver Evaluation Module

User's Guide

MAY 2003

High Performance Linear

SLOU142A

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It is important to operate this EVM within the supply voltage range of 2.8 V to 5.5 V.

Exceeding the specified supply range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the supply range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Operating Instructions

Related Documentation From Texas Instruments

- ***DRV593, DRV594*** data sheet (SLOS401).

FCC Warning

This equipment is for use in a laboratory test environment only. It generates and uses radio frequency energy. It may also radiate such energy. The equipment has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the EVM in other environments may cause interference with radio communications, in which case users at their own expense must take whatever measures are required to correct this interference.

Contents

Figures

Tables

Chapter 1

Introduction

This chapter provides an overview of the Texas Instruments (TI) DRV593/594 high-efficiency power driver evaluation module. It includes a list of EVM features, a brief illustrated description of the module, and a list of EVM specifications.

Topic **Page**

1.1 Feature Highlights

The DRV593/594 evaluation module includes the following features:

- ❑ PWM operation with only one output filter required
- ❑ High efficiency
- ❑ Small solution size
- ❑ Low supply current in active and shutdown modes
- ❑ LEDs and test points for fault monitoring
- ❑ Jumpers for selecting device options
- ❑ Easy connections for inputs, outputs, and power supply

1.2 Description

The DRV593/594 PWM power driver evaluation module is a complete power stage solution. It consists of the TI DRV593/594 PWM power driver IC, along with a few discrete passive components required for operation. It also includes jumpers for configuring the features of the device, LEDs and test points for fault monitoring, and an output filter that is easily modified. The 5-way jacks for the inputs, outputs, and power supply provide ease of connection to any system, from an existing design to a bread-boarded prototype.

1.3 EVM Specifications

Supply voltage range, V_{DD} . . . . . 2.8 V to 5.5 V
Supply current, I_{DD} . . . . . 3.1 A max

Chapter 2

Operating Instructions

Follow the steps in this chapter to quickly prepare the DRV593/594 EVM for use.

Topic **Page**

2.1 Precautions

Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected V_{DD} power input connector J8 is correct. Overvoltage or reverse-polarity power applied to this terminal can damage the evaluation module.

2.2 Operating Instructions List (See Figures 2−2 and 2−3.)

Table 2−1. Typical Jumper Settings

J1(FREQ)	J2 (INT/$\overline{\text{EXT}}$)	J3 ($\overline{\text{SHUTDOWN}}$)
ON	ON	ON

❑ **Power supply**

1) Ensure that all external power sources are set to OFF.

2) Connect a 2.8-V to 5.5-V power supply to J8 (V_{DD}) and J9 (GND), taking care to observe proper polarity.

❑ **Inputs and outputs**

3) Connect a dc control voltage to J4 (IN+), ranging from ground to V_{DD}. The terminal J5 (IN−) is held to $V_{DD}/2$ with a resistor voltage divider, as shown in the schematic. Therefore, a dc control voltage of $V_{DD}/2$ provides 0-V output from PWM to H/C.

   If a different bias or offset is required, replace the voltage divider resistors R7 and R8. To minimize gain error due to imbalance in the impedance of the differential input stage, the value of R7 and R8 in parallel should not exceed 1 kΩ. Alternatively, the resistor divider may be removed and a different common voltage output (such as from an op-amp buffer or a power supply) may be connected to J5 (IN−).

Note:

The common mode input range of the DRV593 and DRV594 are 1.2 V to 3.8 V when using a 5-V supply, and 1.2 V to 2.1 V when using a 3.3-V supply. Refer to the DRV593/594 data sheet, SLOS401.

4) Connect a load across J6 (PWM) and J7 (H/C). The polarity of the connection depends on the operation of the dc control voltage. As the voltge at IN+ becomes greater than the voltage at IN−, the voltage at PWM increases and the H/C voltage remains at ground. The differential voltage created causes current to flow from PWM to H/C. Similarly, as the voltage at IN+ decreases lower than IN−, the voltage at H/C goes to V_{DD} and the PWM voltage decreases. The differential voltage increases in the opposite direction, causing current to flow from H/C to PWM.

For example, consider the load to be a TEC element and the dc control voltage to be the output of a temperature control circuit. In this example, as temperature increases the output of the temperature control circuit increases. The TEC element should therefore be connected with the anode at PWM and the cathode at H/C to ensure that the TEC element cools when the temperature increases.

❑ **Evaluation module jumpers, LEDs, and test points**

5) Jumper J1 (FREQ) should be ON for normal operation.

When J1 is ON, the device is configured for 500-kHz operation.

When J1 is OFF, the device is configured for 100-kHz operation. However, capacitor C9 must be removed and replaced with a 1-nF capacitor for proper operation.

6) Jumper J2 (INT/$\overline{\text{EXT}}$) should be ON for normal operation.

When J2 is ON, the internal oscillator is used to generate the switching outputs. When J2 is OFF, an external TTL-compatible clock signal can be driven into the COSC pins of DRV593 and DRV594. In that case, the capacitor C9 is removed and a wire is soldered to the pad closest to the IC for connecting the external clock.

7) Jumper J3 ($\overline{\text{SHUTDOWN}}$) should be ON for normal operation. (Remove J3 to place the DRV593 and DRV594 in shutdown mode.)

If an external shutdown control signal is to be used, it should be connected to the right-hand pin of J3 (which is connected to resistor R5). The control signal must be TTL-compatible; a logic high provides normal operation, a logic low places the DRV593 and DRV594 in shutdown.

8) The LED D1 lights if FAULT1 is active, and LED D2 lights if FAULT0 is active. If external fault monitoring is to be used, test point TP1 is connected to FAULT1 and test point TP2 is connected to FAULT0. The pins and test points go low when a fault is present, lighting the LEDs. The faults are shown in the table below. Refer to the DRV593/594 data sheet (SLOS401) for additional information on the fault indicators.

Table 2−2. Fault Indicators

FAULT1	FAULT0	
0	0	Overcurrent
1	0	Undervoltage
0	1	Overtemperature
1	1	Normal operation

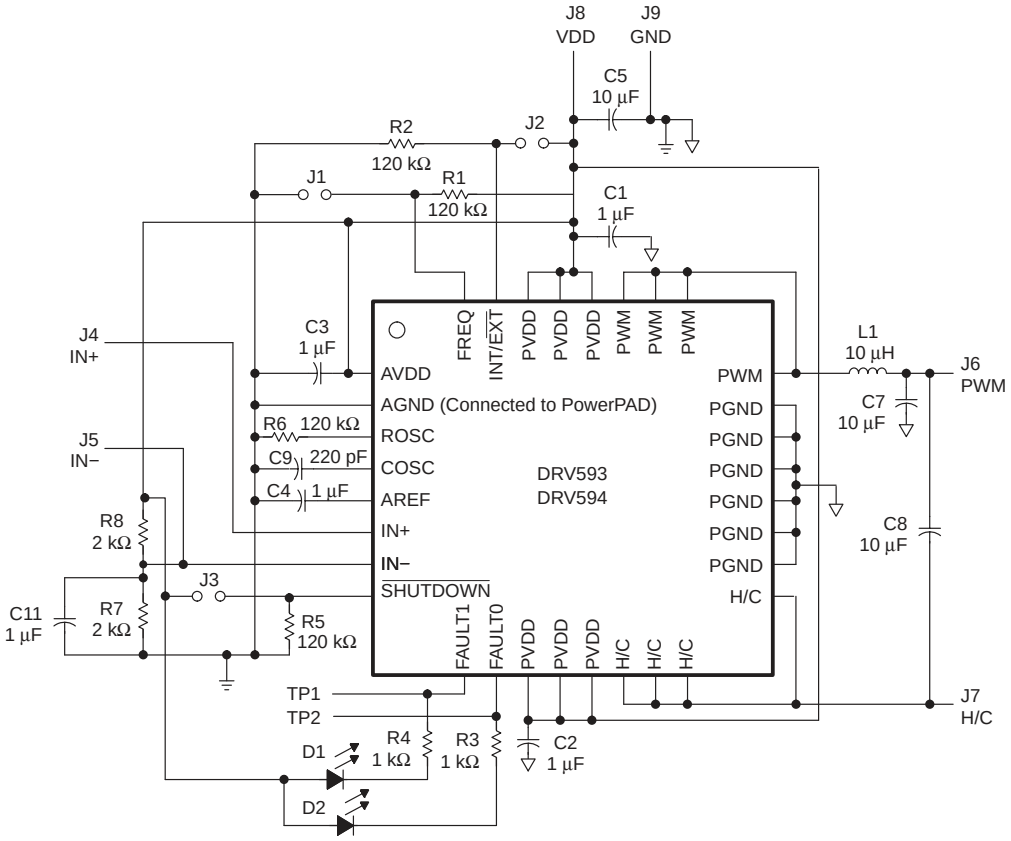
Note: 0 = LED ON (Fault) 1 = LED OFF (Normal)

❑ **Power up**

9) Verify correct voltage, verify input polarity, and set the external power supply to ON. The EVM begins operation.

2.2.1 DRV593/594 EVM Schematic

Figure 2−1. DRV593/594 EVM Schematic Diagram



2.2.2 DRV593/594 EVM Bill of Materials

Table 2−3. DRV593/594 EVM Bill of Materials

Reference	Description	Size	Qty.	MFG	Part #	Vendor/#
C1−4, C11	Capacitor, ceramic, 1 μF, ±10%, X5R, 6.3 V	0603	5	Panasonic	ECJ1VB0J105K	Digi-Key/ PCC1915CT-ND
C5	Capacitor, ceramic, 22 μF, ±10%, X5R, 16 V	1206	1	Panasonic	ECJ-4YB1C106K	Digi-Key/ PCC2169CT-ND
C6	Capacitor, ceramic (not assembled)	0603	1			
C7	Omitted					
C8	Capacitor, ceramic, 10 μF, ±10%, X5R, 16 V	1210	1	Panasonic	ECJ-4YB1C106K	Digi-Key PCC2169CT-ND
C9	Capacitor, ceramic, 220 pF, ±10%, X7R	0603	1	Panasonic	ECUV1J221KBV	Digi-Key/ PCC221BVCT-ND
R1, R2, R5, R6	Resistor, chip, 120 kΩ, 1/16 W, 1%	0603	4	Phycomp	9C06031A1203F KHFT	Digi-Key/ 311-120KHCT-ND
R3, R4	Resistor, chip, 1 kΩ, 1/16 W, 1%	0603	2	Phycomp	9C06031A1001F KHFT	Digi-Key/ 311-1.00KHCT-ND
R7, R8	Resistor, chip, 2 kΩ, 1/16 W, 1%	0603	2	Phycomp	9C06031A2001F KHFT	Digi-Key/ 311-2.00KHCT-ND
D1, D2	LED, red, 2 V, 140° view angle	0805	2	Lumex	SML−LXT0805IW	Digi-Key/ 67−1552−2−ND
L1	Inductor, SMT, 10 μH, 0.026 mΩ DCR (typical), 4.4 A max dc current		1	Sumida	CDRH104R-100	Harvey King/ CDRH104R−100
L2	Chip bead (not assembled)	1806	2			
J1, J2, J3	Header, 2 position	2 mm	3	Norcomp	2163-2-01-P2	Digi-Key/ 2163S-02-ND
	Shunts	2 mm	3	3M	953170-00	Digi-Key/ 953170-00
TP1, TP2	Test points		2			Farnell/240-333
IN−, IN+, V_{DD}, GND, OUT+, OUT− (J5−J9)	Uninsulated binding post with knurled thumb, nut-grounded type		6	Johnson Components	111-2223-001	Digi-Key/J587-ND
	Standoffs	4−40	4			Digi-Key/534-1804
U1	DRV593/DRV594, 32-pin Quad Flatpack		1	TI	DRV593/ DRV594VFP	TI/DRV593/ DRV594VFP

2.2.3 DRV593/594 EVM PCB Layers

Figure 2−2. DRV593 Top Layer

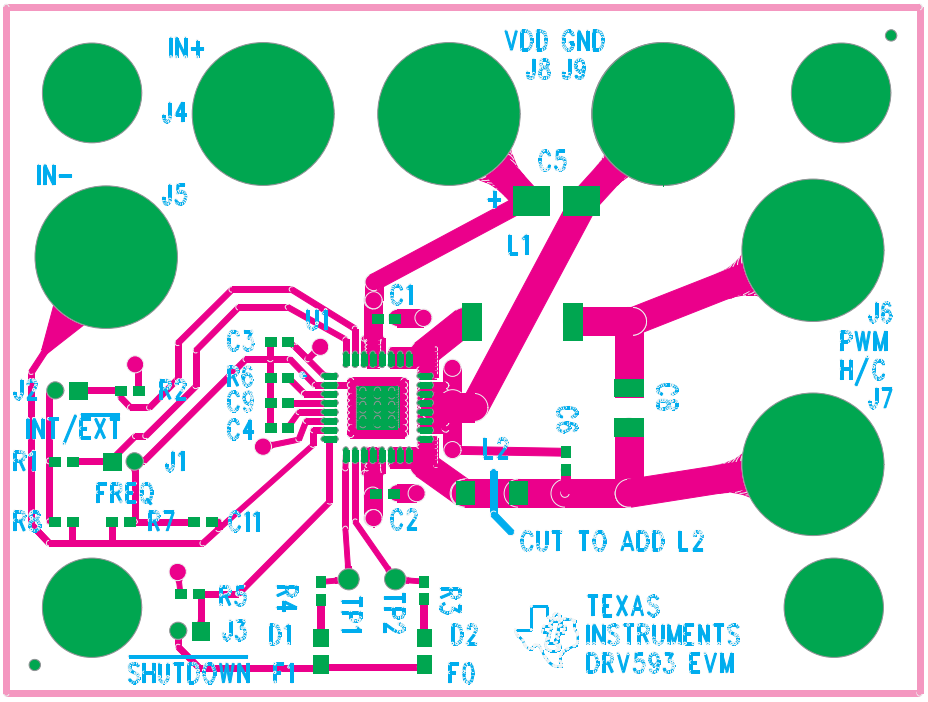


Figure 2−3. DRV594 Top Layer

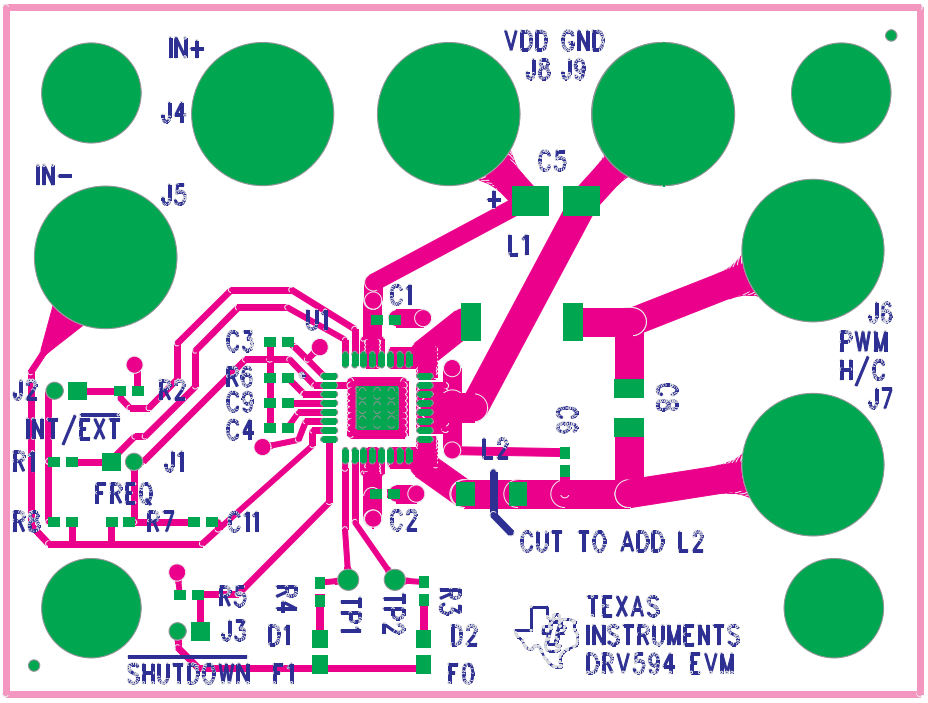


Figure 2−4. DRV593 and DRV594 Bottom Layer

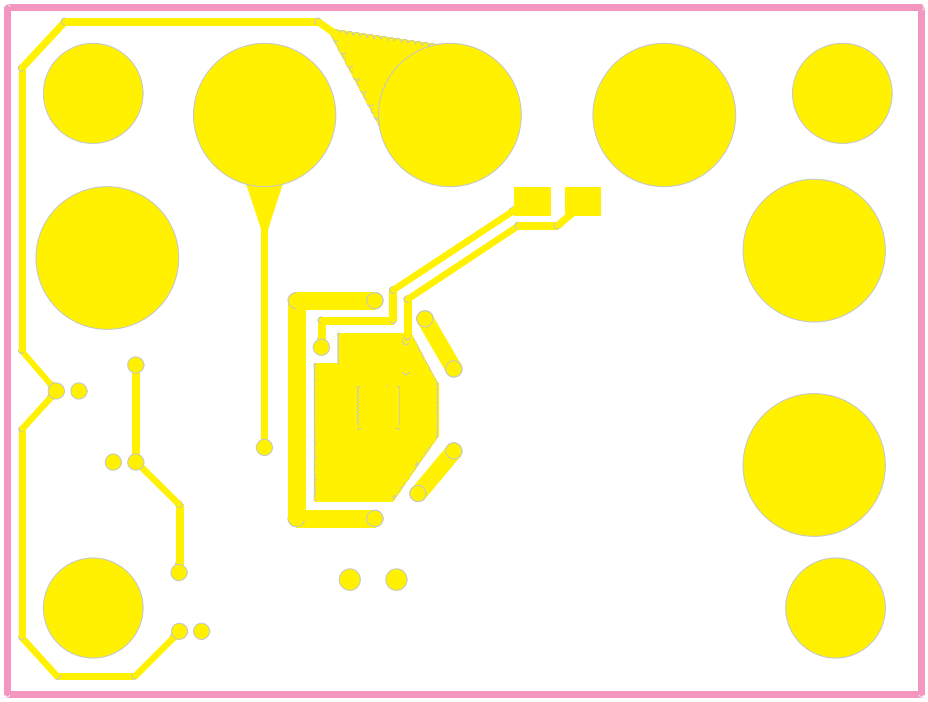


Figure 2−5. DRV593 and DRV594 Thermal Plane Layer