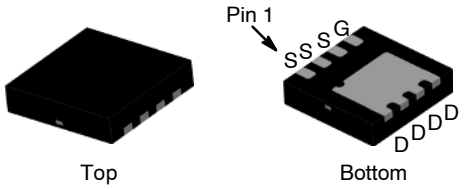
MOSFET - N-Channel, Shielded Gate, POWERTRENCH®

100 V, 24 mΩ , 22 A

FDMC86102LZ



WDFN8 MPL
CASE 511DH

Description

This N−Channel logic Level MOSFETs are produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance and yet maintain superior switching performance. G−S zener has been added to enhance ESD voltage level.

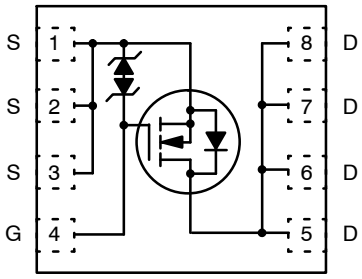
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 24 mΩ at V_{GS} = 10 V, I_D = 6.5 A
- Max $R_{DS(on)}$ = 35 mΩ at V_{GS} = 4.5 V, I_D = 5.5 A
- HBM ESD Protection Level > 6 kV Typical (Note 4)
- 100% UIL Tested
- RoHS Compliant

Applications

- DC−DC Switching

N−Channel

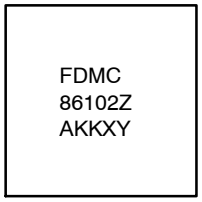


MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain−to−Source Voltage		100	V
V_{GS}	Gate−to−Source Voltage		±20	V
I_D	Drain Current − Continuous	T_C = 25°C	22	A
	− Continuous (Note 1a)	T_A = 25°C	7	
	− Pulsed		30	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		84	mJ
P_D	Power Dissipation	T_C = 25°C	41	W
	Power Dissipation (Note 1a)	T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



FDMC86102Z	= Specific Device Code
A	= Assembly Plant Code
KK	= Lot Run Traceability Code
XY	= Numeric Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMC86102LZ	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	71	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.6	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate−to−Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−6	–	mV/°C
$R_{DS(on)}$	Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 6.5 A	–	19	24	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A	–	25	35	
		V_{GS} = 10 V, I_D = 6.5 A, T_J = 125°C	–	31	40	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 6.5 A	–	24	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	969	1290	pF
C_{oss}	Output Capacitance		–	181	240	pF
C_{rss}	Reverse Transfer Capacitance		–	9	15	pF
R_g	Gate Resistance		–	0.4	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 50 V, I_D = 6.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	7.1	15	ns
t_r	Rise Time		–	2.3	10	
$t_{d(off)}$	Turn−Off Delay Time		–	19	35	
t_f	Fall Time		–	2.5	10	
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 6.5 A	–	15.3	22	nC
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V, V_{DD} = 50 V, I_D = 6.5 A	–	7.6	11	
Q_{gs}	Gate−to−Source Charge	V_{DD} = 50 V, I_D = 6.5 A	–	2.4	–	
Q_{gd}	Gate−to−Drain “Miller” Charge	V_{DD} = 50 V, I_D = 6.5 A	–	2.5	–	

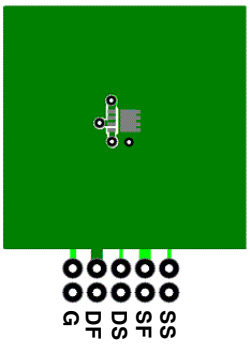
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6.5 A (Note 2)	–	0.80	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.72	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 6.5 A, di/dt = 100 A/μs	–	37	59	ns
Q_{rr}	Reverse Recovery Charge		–	27	43	nC

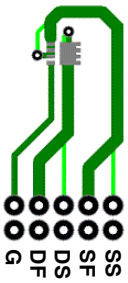
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 1 mH, I_{AS} = 13 A, V_{DD} = 90 V, V_{GS} = 10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

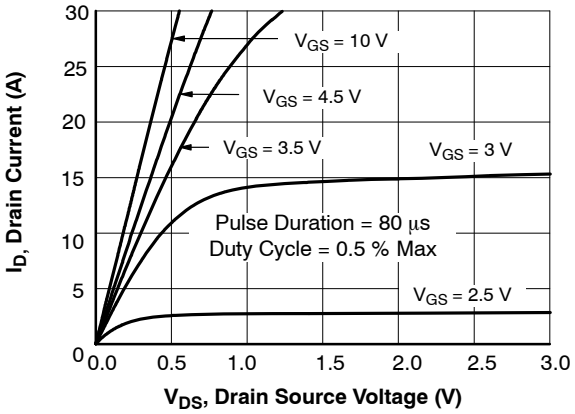


Figure 1. On−Region Characteristics

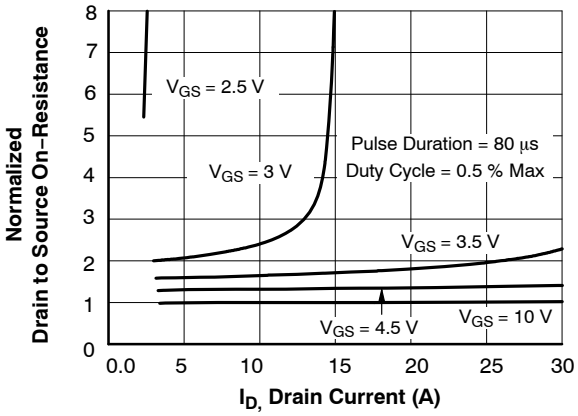


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

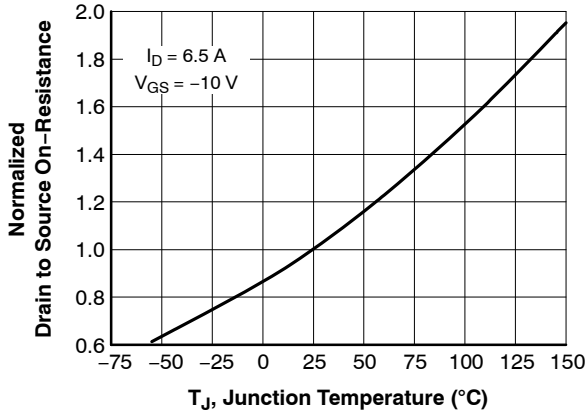


Figure 3. Normalized On−Resistance vs. Junction Temperature

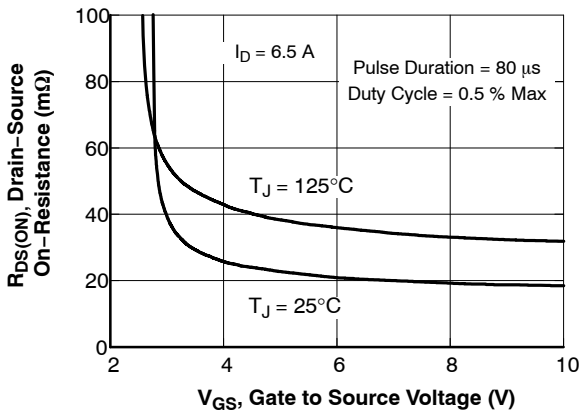


Figure 4. On-Resistance vs. Gate−to−Source Voltage

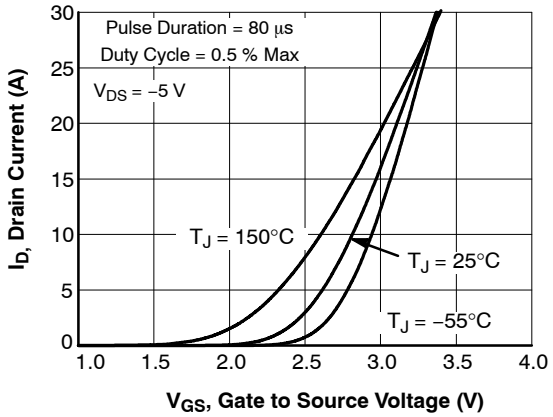


Figure 5. Transfer Characteristics

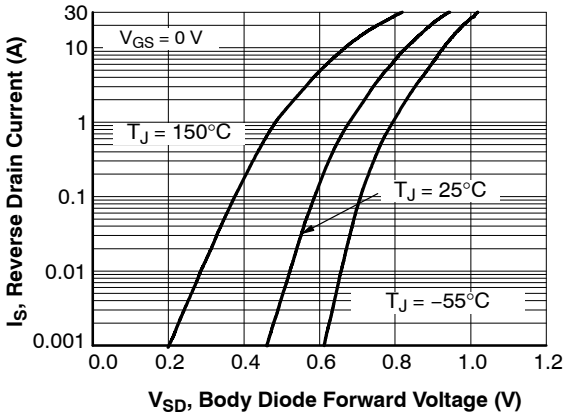


Figure 6. Source−to−Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

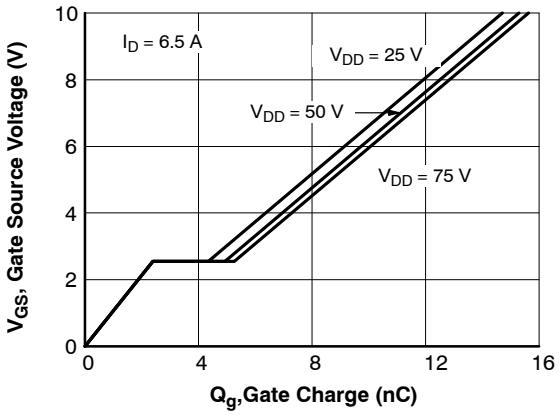


Figure 7. Gate Charge Characteristics

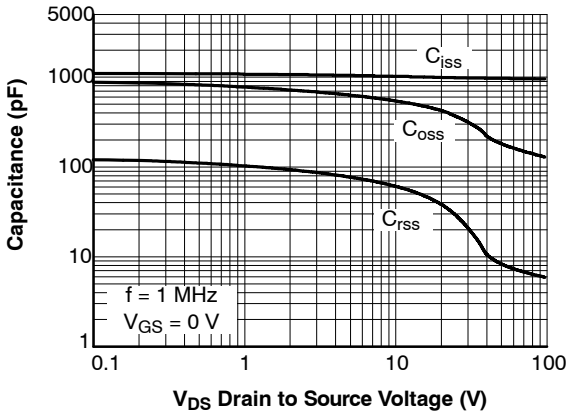


Figure 8. Capacitance vs Drain−to−Source Voltage

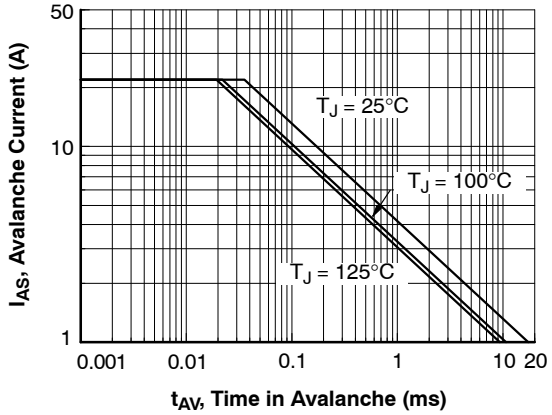


Figure 9. Unclamped Inductive Switching Capability

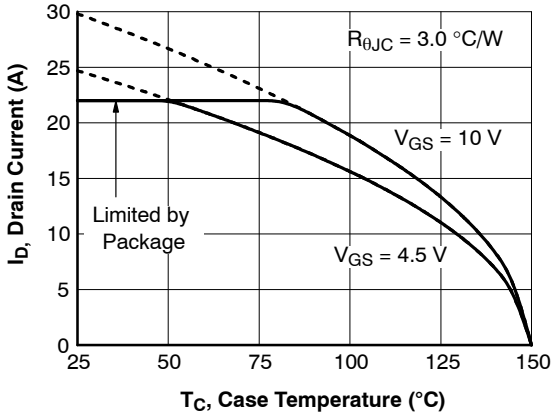


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

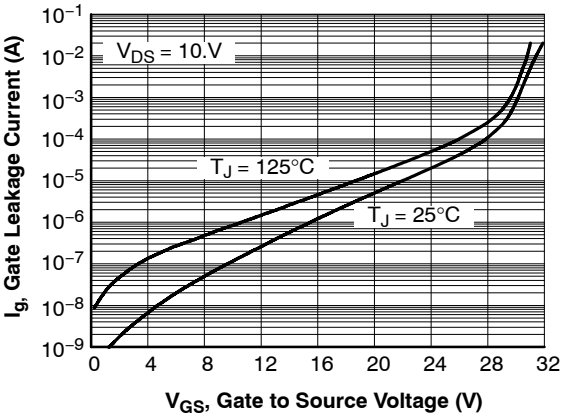


Figure 11. Gate Leakage Current vs. Gate−to−Source Voltage

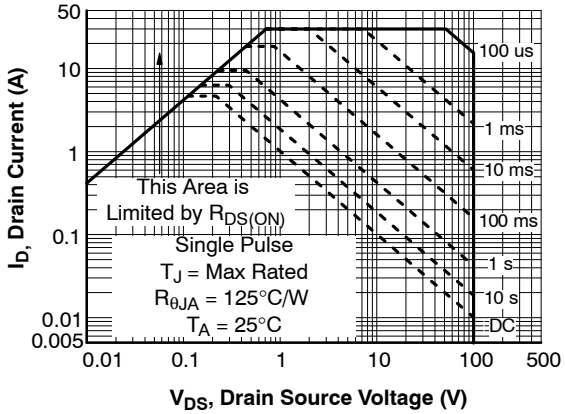


Figure 12. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

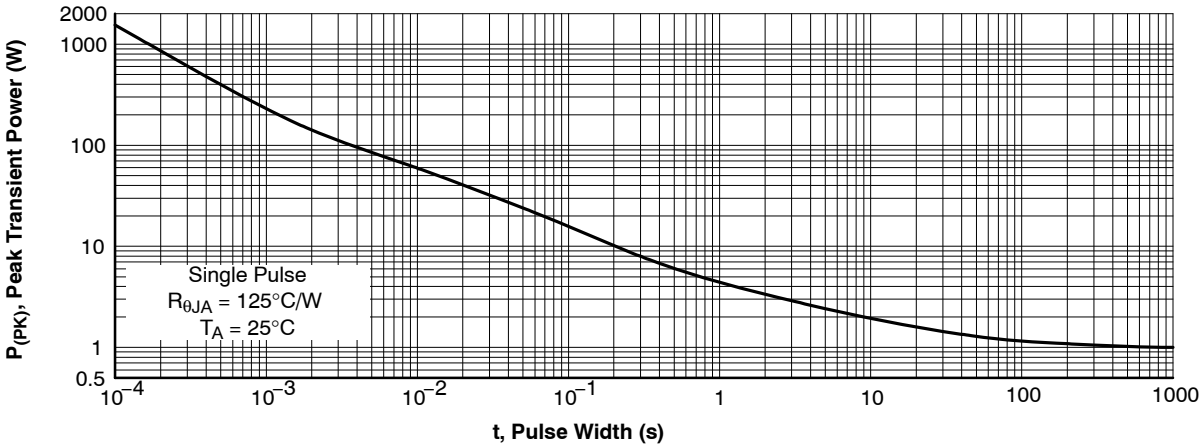


Figure 13. Single Pulse Maximum Power Dissipation

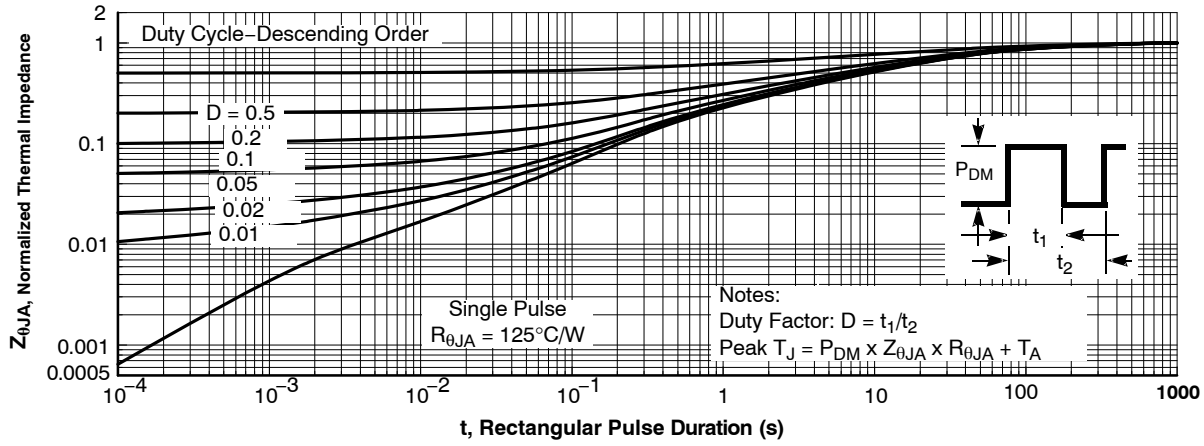
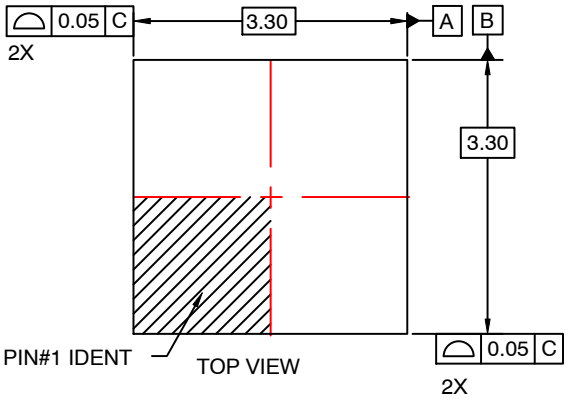
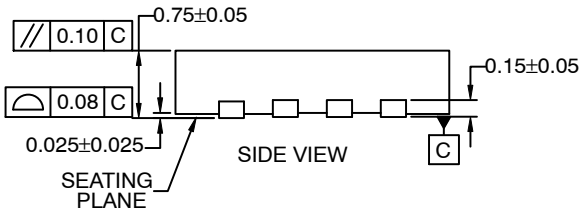


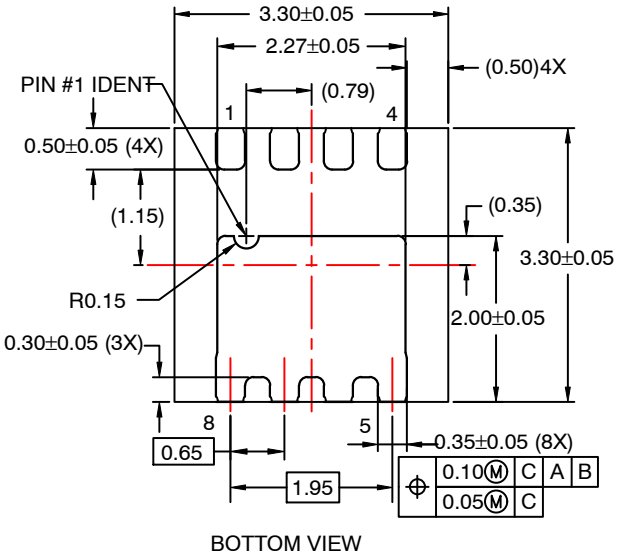
Figure 14. Junction−to−Ambient Transient Thermal Response

WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

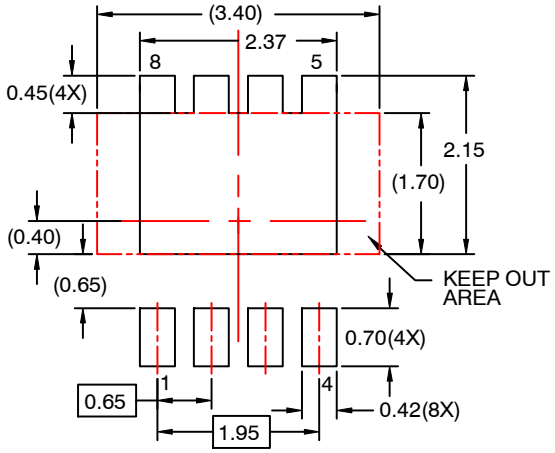
DATE 31 JUL 2016







BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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