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1 The ZIOL2xxx IC Family Overview

IDT provides a universal and IO-Link compatible cable driver IC by issuing the ZIOL2401 integrated circuit. The ZIOL2401 is highly configurable and suitable for a wide range of applications in process and factory automation. In order to fulfill the requirements of specific applications stripped down versions of the IC were required. The ZIOL2xxx IC family is derived from the ZIOL2401 by modification (elimination or disabling) of certain functional building blocks. In this combination the following building blocks or functions are affected:

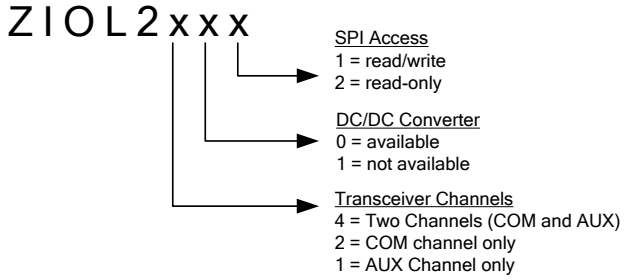
- The transceiver channels COM and AUX
- The availability of the integrated DC/DC converter
- The activation of a read-only data access via the SPI interface

This datasheet describes the entire IC family ZIOL2xxx. Respective notes or footnotes describe the availability the above mentioned building blocks or functionality with respect to certain IC family members. Table 1.1 shows an overview concerning the ZIOL2xxx IC family and the used naming convention.

Table 1.1 ZIOL2xxx Product Matrix and Product Naming Convention

ZIOL2xxx Member	Transceiver Channel	DC/DC Converter	SPI Access	Remarks
ZIOL2401	COM + AUX	yes	r/w	Base type - released
ZIOL2201	COM	yes	r/w	released
ZIOL2101	AUX	yes	r/w	1)
ZIOL2411	COM + AUX	no	r/w	released
ZIOL2211	COM	no	r/w	released
ZIOL2111	AUX	no	r/w	1)
ZIOL2402	COM + AUX	yes	r	1)
ZIOL2202	COM	yes	r	1)
ZIOL2102	AUX	yes	r	1)
ZIOL2412	COM + AUX	no	r	1)
ZIOL2212	COM	no	r	1)
ZIOL2112	AUX	no	r	1)

1) For future product releases, please contact IDT's sales representative



2 Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 2.1 Absolute Maximum Ratings

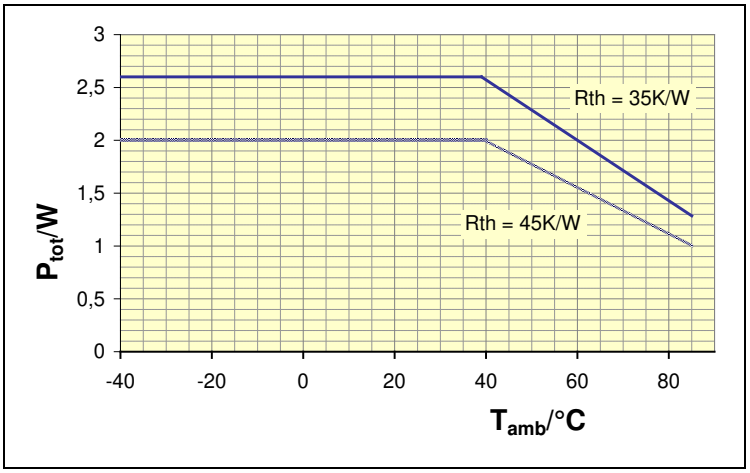
Symbol	Parameter	Min	Max	Unit	Conditions
V_{DD_HV}	Supply voltage	-0.3	40	V	
V_{HV}	Voltage at HV pins	-0.3	V_{DD_HV}+0.3	V	
V_{LV}	Voltage at LV pins	-0.3	V_{DD_LV}+0.3	V	2)
V_{imp}	Impulse voltage withstand	60		V	according to IEC 60947-5-2
V_{ESD}	Abs. ESD test voltage		2k	V	according to HBM
T_s	Junction temperature		125	°C	1)
T_a	Storage temperature	-50	150	°C	
P_{tot}	Average total power dissipation		2.6	W	integration period < 10ms 3)

1) Average die-temperature.

2) Exceptions are the digital input pins (µC interface) which tolerate 5V logic signals (refer to Table 5.1).

3) The allowed total power dissipation depends on the in the PCB design achieved thermal resistance R_{th} (package/ambient) and the ambient operation temperature as shown in Figure 2.1. In order to obtain optimal heat distribution (R_{th} < 35K/W) certain PCB layout rules shall be applied. Those rules are described in the application note for the used QFN package (refer to chapter 8, [4]).

Figure 2.1 Max. Total Power Dissipation



2.2. Operating Conditions

Table 2.2 Operating Conditions

Symbol	Parameter	Min	Typ[1)]	Max	Unit	Conditions
V_{DD_HV}	Supply voltage	8.0	24	36	V	
V_{in}	Linear regulator input voltage	4.75		36	V	LR_IN can be connected to V_{DD_HV} or DC/DC output voltage.
V_{DD_LV}	Linear regulator output voltage	3.0	3.3	3.6	V	Voltage LR_OUT → GND pin
I_{out}	Linear regulator output current			10	mA	LR_OUT provides supply current for external applications. [2)]
$t_{startup}$	Startup timing @ V_{DD_HV} = 8V			5	ms	Time for system start up including loading of configuration registers from EEPROM
T_{amb}	Operating ambient temperature	-40		+85	°C	
f_{osc}	Internal oscillator frequency	4.5		5.5	MHz	Internal clock is not available externally. All digital circuit timing parameters of the IC are derived from the internal clock.

1) The mentioned typical values of IC properties are provided for information only.
2) While start-up (until the voltage at LR_OUT has reached 1V) the output current may be limited to 5mA.

2.3. Electrical Parameters

All parameter values are valid under operating conditions specified in chapter 2.2 if no other conditions are mentioned.

Table 2.3 Electrical Characteristics

Symbol	Parameter	Min	Typ[1)]	Max	Unit	Conditions
Transmitter Output Stages (COM[1]/AUX[2])						
I_{DAL_0}	Alarm level threshold corresponding to configurable output current limitation [2)] Dual Driver Mode	50		I_{Dout_0}	mA	Dual mode The active setting is defined in the configuration registers
I_{DAL_1}		100		I_{Dout_1}	mA	
I_{DAL_2}		200		I_{Dout_2}	mA	
I_{DAL_3}		250		I_{Dout_3}	mA	
I_{MAL_0}	Alarm level threshold corresponding to configurable output current limitation [2)] Tandem Driver Mode	100		I_{Mout_0}	mA	Tandem mode The active setting is defined in the configuration registers.
I_{MAL_1}		200		I_{Mout_1}	mA	
I_{MAL_2}		400		I_{Mout_2}	mA	
I_{MAL_3}		500		I_{Mout_3}	mA	
I_{Dout_0}	Configurable output current limit[2)] Dual Driver Mode	56		95	mA	Dual mode The active setting is defined in the configuration registers.
I_{Dout_1}		112		180	mA	
I_{Dout_2}		224		330	mA	
I_{Dout_3}		280		410	mA	
I_{Mout_0}	Configurable output current limit[2)] Tandem Driver Mode	112		180	mA	Tandem mode The active setting is defined in the configuration registers.
I_{Mout_1}		224		360	mA	
I_{Mout_2}		448		660	mA	
I_{Mout_3}		560		820	mA	
SR_{38}	Slew rate [3)]	6	10	14[5)]	V/µs	referring to IO-Link Spec.: 38,4kBaud (COM2),
SR_{230}		40	60	80[5)]	V/µs	referring to IO-Link Spec.: 230.4kBaud (COM3)
$t_{TLHdelayCOM3}$	Propagation delay L-H edge			250	ns	Time from LV L-H edge till HV edge begins to rise (COM3 baud rate)
$t_{THLdelayCOM3}$	Propagation delay H-L edge			250	ns	Time from LV H-L edge till HV edge begins to fall (COM3 baud rate)
$t_{TLHdelayCOM2}$	Propagation delay L-H edge			700	ns	Time from LV L-H edge till HV edge begins to rise (COM2 baud rate)

[1] The COM transmitter is only available inside the products ZIOL24xx/22xx
[2] The AUX transmitter is only available inside the products ZIOL24xx/21xx

Symbol	Parameter	Min	Typ[1)]	Max	Unit	Conditions
$t_{THLdelayCOM2}$	Propagation delay H-L edge			700	ns	Time from LV H-L edge till HV edge begins to fall (COM2 baud rate)
Receiver Input Channels (COM[1]/AUX[2])						
V_{ih1}	IO-Link specific threshold, High	10.75		12.75	V	
V_{il1}	IO-Link specific threshold, Low	8.75		10.75	V	
V_{ihyst1}	IO-Link specific thresholds, Hysteresis	1.5		2.5	V	
V_{ih2}	Ratiometric threshold, High	52		57	%*V_{DD_HV}	
V_{il2}	Ratiometric threshold, Low	43		47.7	%*V_{DD_HV}	
V_{ihyst2}	Ratiometric thresholds, Hysteresis	7		11.6	%*V_{DD_HV}	
R_{in}	Input resistance	150			kOhms	
C_{in}	Input capacitance			20	pF	
t_{Rdelay}	Propagation delay without filtering			80 100 200	ns ns ns	No filter within signal path. Input edge with: >30V/µs (COM3) >5V/µs (COM2) >0.75V/µs (COM1)
$t_{FRdelay}$	Propagation delay with analog filtering	750	850	950	ns	@V_{DD_HV} = 24V, Input edge with: >30V/µs (COM3)
t_{Rpulse}	Minimal propagated pulse width without filtering		25		ns	
$t_{FRpulse}$	Minimal propagated pulse width with analog filtering		1.1		µs	
$t_{DIGdelay}$	Additional propagation delay with digital filtering	180		440	ns	
f_{cut}	Input filter – cut off frequency (-3dB) COM and AUX channel	100		250	kHz	filter characteristic: 1st order
I_{sink1}	Sink strength 1	2	2.5	3	mA	Line input voltage >5V
I_{sink2}	Sink strength 2	5	6	7	mA	According to IO-Link Specification
R_{pull}	Configurable pull-up/pull-down resistor @ COM_O/AUX_O	100k		250k	Ohms	

[1] The COM receiver is only available inside the products ZIOL24xx/22xx
[2] The AUX receiver is only available inside the products ZIOL24xx/21xx

Symbol	Parameter	Min	Typ[1)]	Max	Unit	Conditions
WURQ Detection						
t_{wurqL}	Lower pulse width limit of signal evaluated as IO-Link wake-up	60	68	75	µs	Refer to chapter 3.3.4
t_{wurqU}	Upper pulse width limit of signal evaluated as IO-Link wake-up	85	94	109	µs	Refer to chapter 3.3.4
DC/DC converter [1]						
V_{OUT}	Output voltage Range[6)]	3		15	V	@ $V_{DD\_HV} > V_{out} + 2V$ (step down function only)
I_{LOAD}	Output load current	5[4)]		50	mA	Current that flows to the application and the R-Divider
I_{PK}	Over current limit for output transistor		240		mA	Averaged current over complete short at DCDC converter output
f_{osc}	Operating frequency	2.25		2.75	MHz	
V_{ref}	Reference/feedback Voltage		1.225		V	at FB pin in steady state
ΔV_{OUT_Line}	DC Output Line Regulation		8		mV/V	@V_{out}=5V, I_{LOAD} = 5mA Filter: C=10µF, L=10µH
ΔV_{OUT_Load}	DC Output Load Regulation				mV/mA	Filter: C=10µF, L=10µH V_{OUT} = 5V
	@Vout=3.3V	0.7		1.4		
	@Vout=15V	3.3		6.9		
V_{ripple}	Ripple of Output Voltage				mV_{PP}	Filter: C=10µF, L=10µH V_{OUT} = 5V
	@ VDD_HV >= 24V		65[7)]			
	@ VDD_HV < 24V		25[7)]			
t_{strt}	Settling time after POR is released		1		ms	For C=10µF, L=10µH Higher C may result in higher t_{strt}
t_{DLY}	digital delay for DC_RDY signal	45	50	55	ms	If enabled in configuration
η	Efficiency	[8)]			%	Filter: C=10µF, L=10µH

[1] The DC/DC converter is only available inside the products ZIOL2401/2402/2201/2202/2101/2102

Symbol	Parameter		Min	Typ[1)]	Max	Unit	Conditions
Microcontroller Interface [9)]							
V_{LIH}	Voltage range for input "high" level		2.5		5.5	V	@ V_{DD_LV} = 3.6V, otherwise $V_{LIH\text{-}min} = 0.7 * V_{DD\_LV}$
V_{LIL}	Voltage range for input "low" level		-0.3		0.9	V	@ V_{DD_LV} = 3.0V, otherwise $V_{LIL\text{-}max} = 0.3 * V_{DD\_LV}$
I_{LIH}	Logic "high" input current	@ pins without pull-up/pull-down resistors: INT_L, WURQ_L	-1		1	µA	@ $V_{LIH} = V_{DD\_LV}$
I_{LIL}	Logic "low" input current		-1		1	µA	@ V_{LIL} = 0V
I_{LIH_PD}	Logic "high" input current	@ pins with pull-down resistors: TX_EN/SPI_CLK, TX/MOSI, AUX_EN, AUX_TX, DC_RDY	-300		-150	µA	@ $V_{LIH} = V_{DD\_LV\text{-}max}$ = 3.6V @ V_{LIH} = 5.5V, $V_{DD\_LV\text{-}max}$ = 3.6V
I_{LIL_PD}	Logic "low" input current		-1		1	µA	@ V_{LIL} = 0V, $V_{DD\_LV\text{-}max}$ = 3.6V @ V_{LIL} = 0V, $V_{DD\_LV\text{-}max}$ = 3.0V
I_{LIH_PU}	Logic "high" input current	@ pins with pull-up resistors: RST_L, SPI_EN_L	-1		1	µA	@ $V_{LIH\text{-}min} = V_{DD\_LV\text{-}max}$ = 3.0V @ $V_{LIH\text{-}max} = V_{DD\_LV\text{-}max}$ = 3.6V
I_{LIL_PU}	Logic "low" input current		-150		250	µA	@ V_{LIL} = 0V, $V_{DD\_LV\text{-}max}$ = 3.6V @ V_{LIL} = -0.3V, $V_{DD\_LV\text{-}max}$ = 3.6V
V_{LOL}	Logic "high" output voltage	@ output pins: RX/MISO, AUX_RX	0		5	%*V_{DD_LV}	@ I_{LIL} = 1mA
V_{LOH}	Logic "high" output voltage		95		100	%*V_{DD_LV}	@ I_{LIH} = -1mA
Internal Current Consumption [10)]							
I_{VDD}	Current into VDD			1.7	2.5	mA	SPI_EN=3.3V
I_{LR_IN}	Current into LR_IN			2.2	3.4	mA	SPI_EN=3.3V

1) The mentioned typical values of IC properties are provided for information only and shall not be considered as statistical guaranteed mean values. Typical values are not subject for measurement while the electrical test of each IC – they are correct by design.

2) If the output current exceeds the configured current limit, the IC will raise an overload signal which causes up-counting of the overload counter (if configured) and which definitely limits the output current. However, the current limit will be performed after a certain settling time in order to ensure the configured slope of the output signal.

3) Absolute edge rise and fall times are proportional to V_{DD_HV}

4) A minimum of the output current must be provided by the application circuit. Otherwise the DC/DC converter shall be unused by interconnecting the FB pin with the LR_OUT pin. The required voltage divider (refer to Figure 3.21) may provide this current partly or in full.

5) Slew-rate measured after settlement time of the output signal

6) Configurable with an external voltage divider (refer to chapter 3.5)

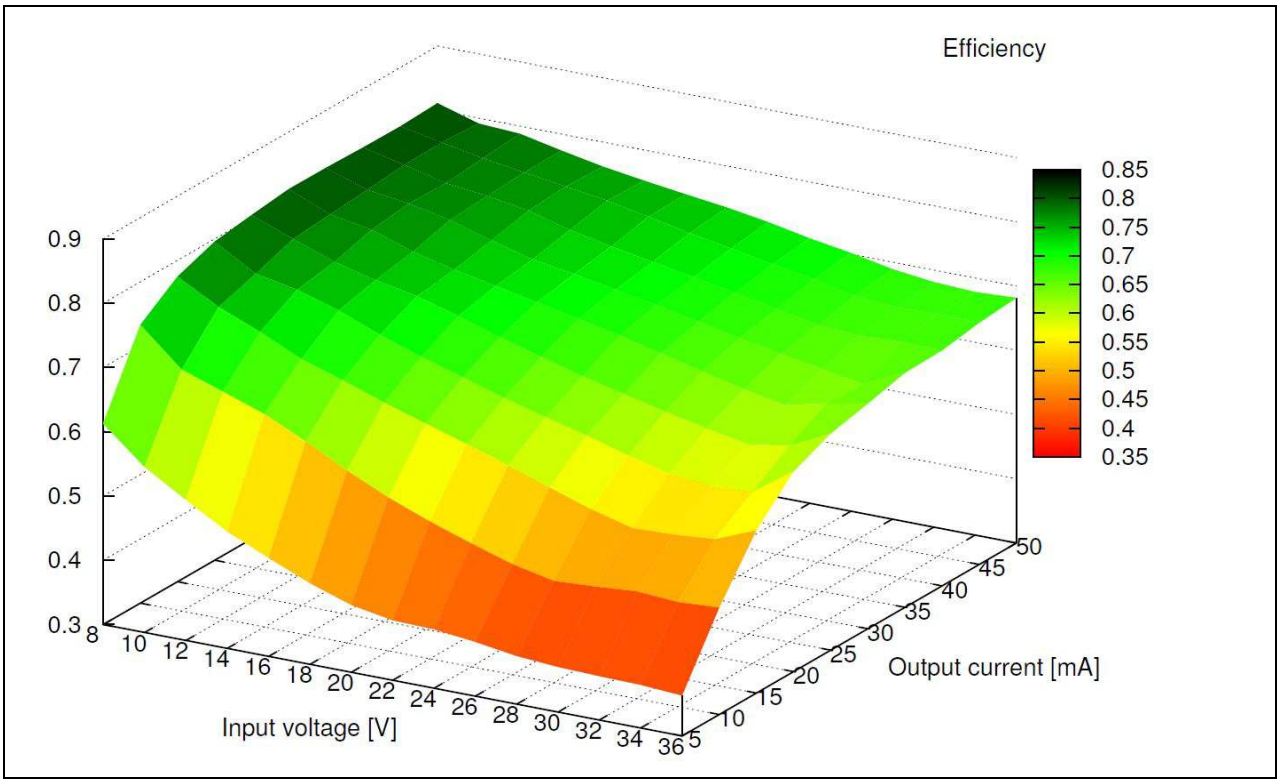
7) The ripple on the output voltage depends significantly on both the external components and the PCB layout. Reference PCB layouts are available from IDT. The layouts used in the application kits are shown in Figure 4.4; detailed layout data of the application kits are available from IDT upon request.

8) The efficiency of the DC/DC converter is depending on the external components and the used PCB layout. Moreover, there is an influence from several operational conditions which is illustrated in the diagram of Figure 2.2

9) Microcontroller interface pins are : RST_L, SPI_EN_L, INT_L, WURQ_L, TX_EN/SPI_CLK, TX/MOSI, RX/MISO, AUX_EN, AUX_TX, AUX_RX, DC_RDY

10) Current consumption is measured by applying the maximum supply voltage at the supply pins VDD and LR_IN (V_{VDD_HV}=36V, V_{in}=36V) and using a decoupling cap of 10µF between LR_OUT and ground. Both VDD and both VSS pins are interconnected, respectively. Pins TX_EN/SPI_CLK, AUX_TX, TX_EN, AUX_EN, PFD, COM_I, AUX_I are connected to ground.

Figure 2.2 Efficiency of the DC/DC[1] converter for VOUT=5V, C=10µF and L=10µH

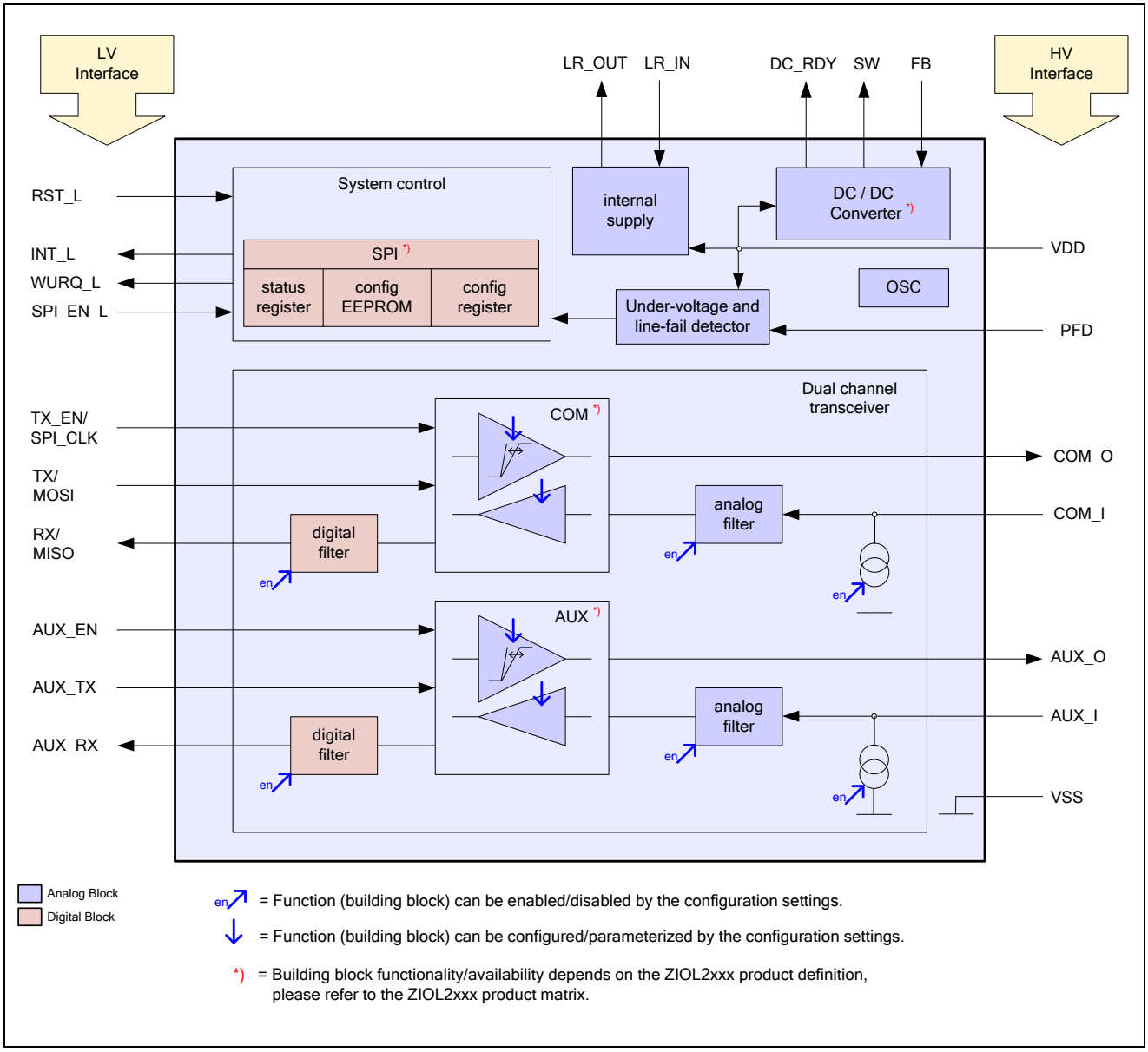


[1] The DC/DC converter is only available inside the products ZIOL2401/2402/2201/2202/2101/2102

3 Detailed Description

3.1. Block schematic

Figure 3.1 Functional Block Diagram of the ZIOL2xxx

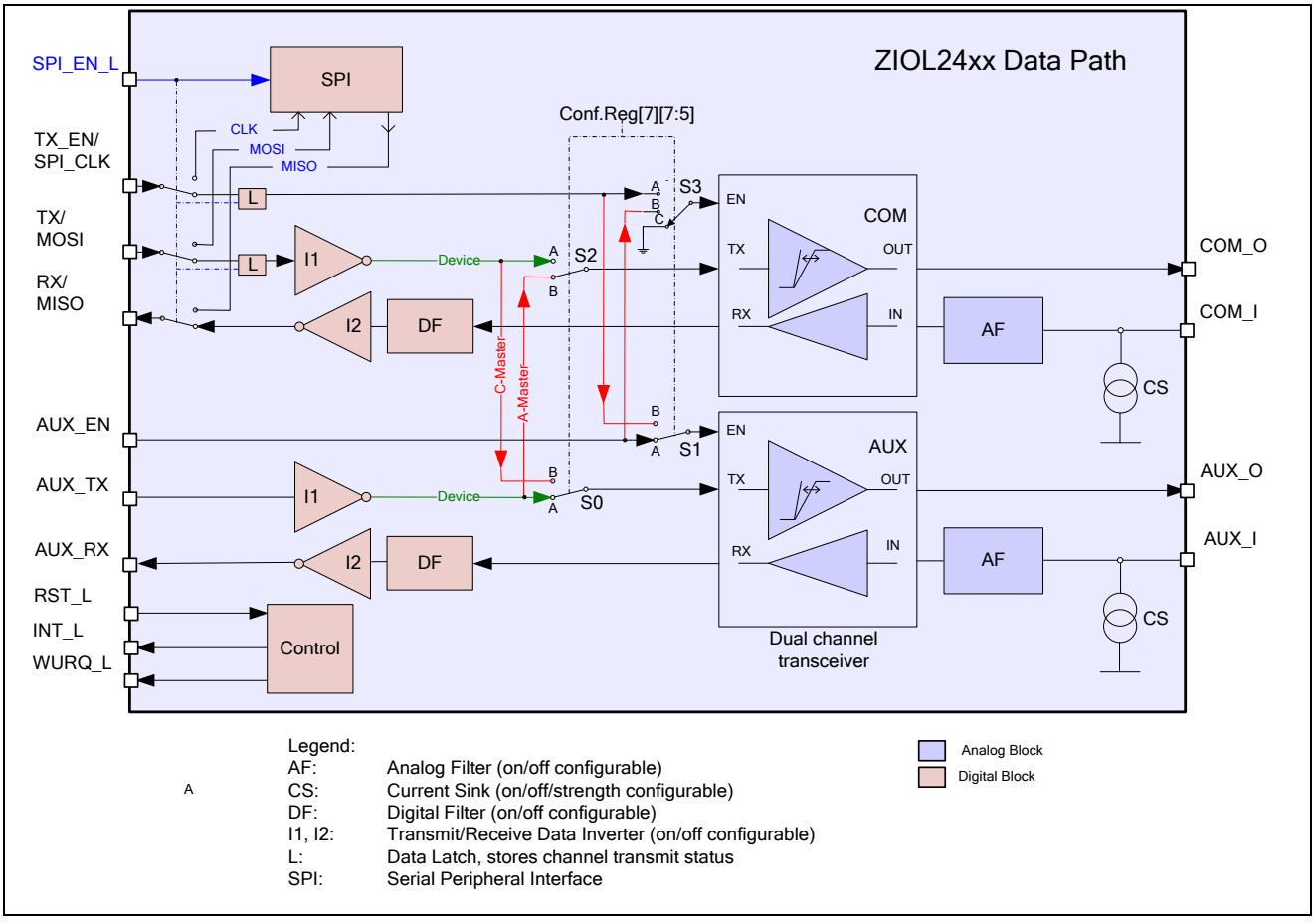


3.2. Dual Channel Transceiver

3.2.1. IC Data Path Configuration

The ZIOL2xxx ICs contains one (ZIOL22xx/21xx) or two (ZIOL24xx) transceiver channels. The channels inside the product versions with two channels can work independently in the “Dual Mode” or coordinated in “Tandem Mode”. The data path of the ZIOL24xx Ics is illustrated in Figure 3.2. Both channels, which are designed identically, are widely configurable. Due to configuration and the range of supported supply voltages the Ics can be used in a broad field of applications. Example applications can be level shifter for standard sensor applications or driver for resistive, capacitive or inductive loads.

Figure 3.2 ZIOL24xx Transceiver Data Path in Principle



Maximum driver capability of minimum 500mA can be achieved by combining both drivers. In this case the drivers work in parallel (Tandem Mode).

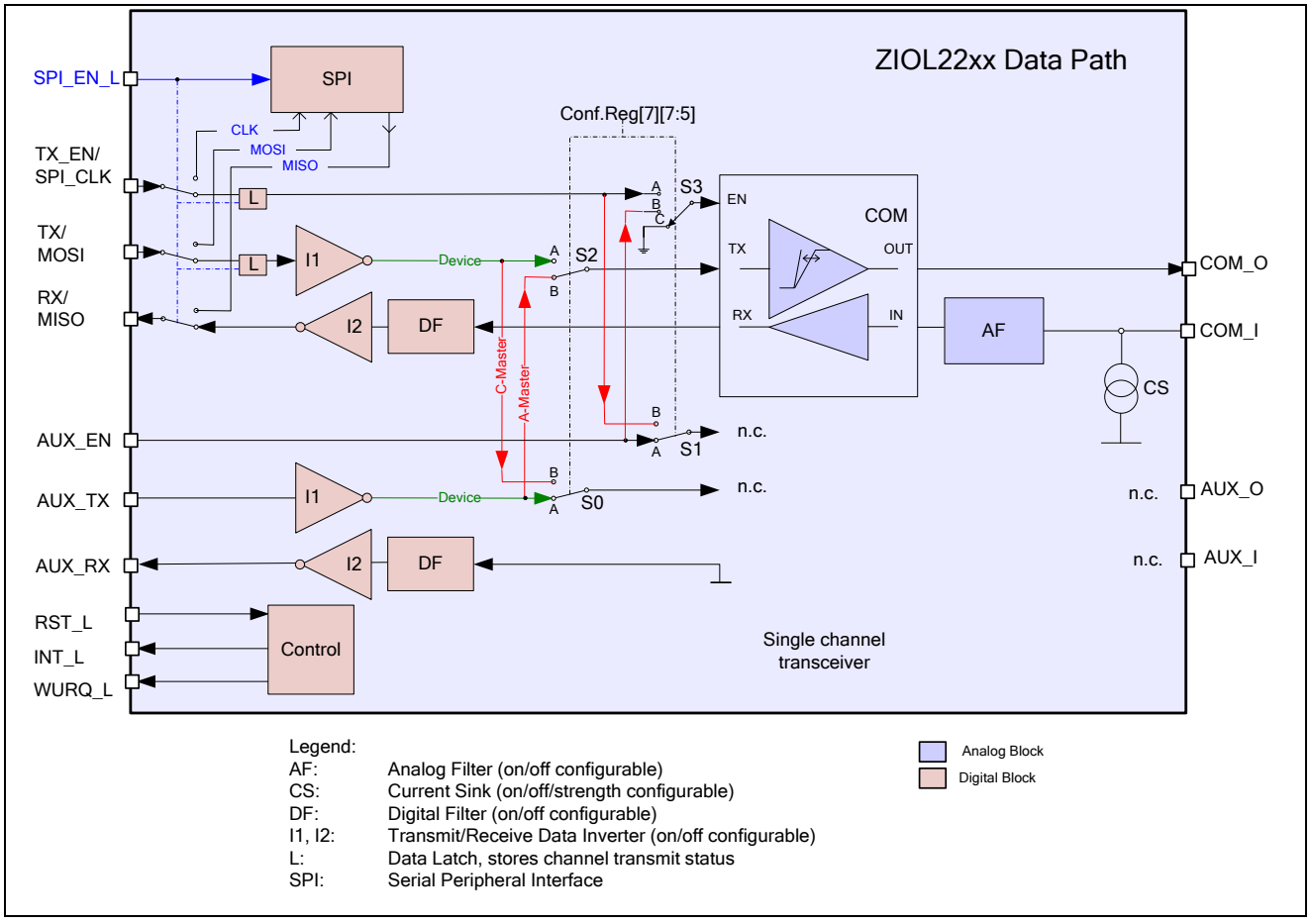
In order to gain optimal EMC behavior the slew rate of the output signals of both drivers can be adjusted. The input threshold levels of the receiver can be set to ratiometric or to IO-Link conform levels, which enables the IC to be used in applications having a wide supply voltage range.

The configuration of the transceiver can be changed during operation. After power-on this configuration is automatically loaded from the on-chip EEPROM.

Driver and receiver are kept totally separated, so full duplex mode in data communication systems is supported. The ability to enable/disable the drivers output also enables applications in half duplex mode, where output and input are connected. Having the I/O-pins separated also enables additional external input filtering.

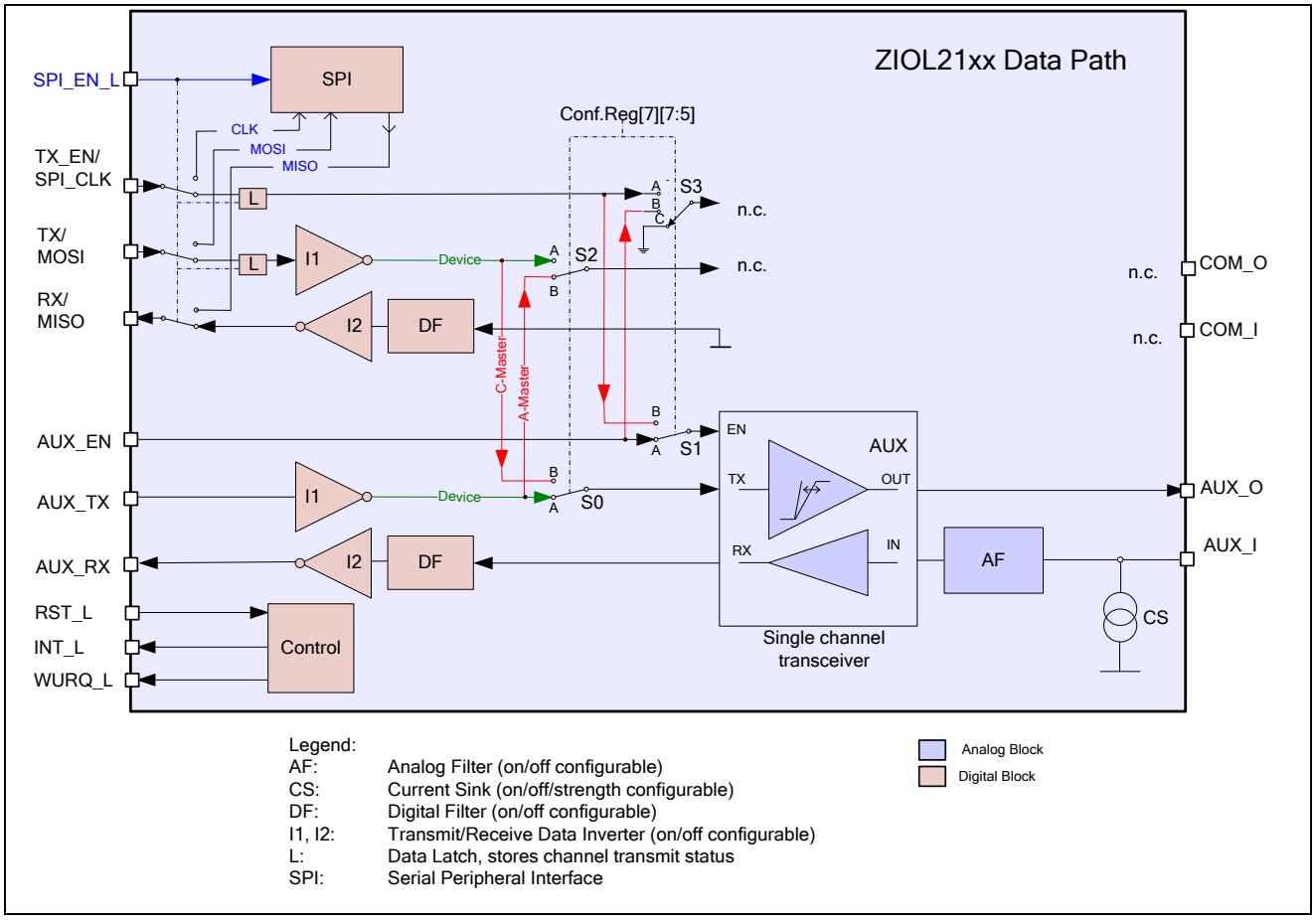
The COM channel send and receive signals (TX_EN, TX, RX) are multiplexed with the signals of the SPI functional unit of the IC (SPI_CLK, MOSI, MISO) as shown in Figure 3.2. The SPI unit is used for IC configuration and diagnostic purposes (refer to chapter 3.3.8). As long the SPI unit is active (SPI_EN_L = low), the send status of the COM channel is kept (for information refer to chapter 3.3.8 and Figure 3.10).

Figure 3.3 ZIOL22xx Transceiver Data Path in Principle



The (stripped down) IC versions ZIOL22xx/21xx contain only one channel. Figure 3.3 and Figure 3.4 show the data path of the ZIOL22xx versions and ZIOL21xx versions, respectively. The following chapters regarding details of the transmitter and receiver apply to IC versions with two channels (ZIOL24xx). The in the following described functionality applies to IC versions with one channel (ZIOL22xx/21xx) correspondingly. With the implicit understanding that one channel IC versions cannot perform tandem (master) mode operations or coordinated transceiver operations no explicit statement in the following chapters will reflect this.

Figure 3.4 ZIOL21xx Transceiver Data Path in Principle



The master mode configuration flags MASTER_MODE, EN_FOLLOW_PRIM_CH and PRIMARY_MASTER_CH located in the MASTER_SENS_CTRL configuration register (refer to Table 3.7) control the switches S0, S1, S2 and S3 (Figure 3.2, Figure 3.3 and Figure 3.4) thus they control the actually used data path. In principle, the ZIOL2xxx IC family supports five data path types which are mentioned in Table 3.1. In case the MASTER_MODE flag is cleared (=0), the IC operates in device mode. For more information about the operation in device/master mode, please refer to chapter 3.2.2.1.

Table 3.1 Master-Device-Mode Function Table

Data Path Configuration		MASTER_SENS _CTRL[7:5]	Data Path Switch Position				Receiver available [1]	RX/ MISO State control	REMARKS
Type	Global IC Function	[7] = MASTER_MODE [6] = EN_FOLLOW_PRIM_CH [5] = PRIMARY_MASTER_CH	S0	S1	S2	S3			
0	Device Mode	0 X X	A	A	A	A	COM[2] AUX	push/ pull	Equivalent to IC Rev A Device Mode
1	Master Mode, COM = prim channel, AUX enable not following prim-ch	1 0 0	B	A	A	A	COM[2] AUX	push/ pull	Equivalent to IC Rev A Master Mode
2	Master Mode, COM = prim channel, AUX enable is following prim-ch [1]	1 1 0	B	B	A	A	COM[2] AUX	push/ pull	Saves one interconnection wire (AUX_EN) to µC
3	Master Mode, AUX = prim channel, COM enable is following prim-ch [3]	1 1 1	A	A	B	B	AUX	push/ pull high-Z if SPI_EN_L = high	Process (IO-Link) and Service (SPI) data separation – SPI pin bus wiring!
4	Master Mode, AUX = prim channel, COM is disabled [4]	1 0 1	A	A	B	C			

[1] If AUX_EN is permanently wired to GND, the total driver strength can be controlled by toggling the MASTER_SENS_CTRL[6] bit (0: AUX disabled using just COM/ 1: AUX enabled if COM is enabled = double strength). → Switching between type 1 and 2 via SPI access.

[2] The logic value of the COM receiver output (RX) is available if the SPI communication is disabled (SPI_EN_L = 1).

[3] Driver strength is “double” – “WAKE_UP_MODE”. The total driver strength can be decreased by switching to type 4 (single strength).

[4] Driver strength is “single”. The total driver strength can be increased by switching to type 3 (double strength)

3.2.2. Transmitter

3.2.2.1. General functionality

The IC versions ZIOL24xx consists of two[1] independent driver stages. Each driver (COM/AUX) is configurable as regards the parameter

- Output current limitation
- Output slew rate
- Driver function (push, pull, pull ups/downs)

Several Modes of operation are supported – as independent or as combined driver outputs.

3.2.2.2. Modes of operation (IO-Link specific Operation)

Operating both on-chip drivers independently or in parallel ensures the IC utilization in a wide range of applications. An example can be the different requirements of driver capability in master or device mode regarding the IO-Link specification (refer also to chapter 3.3.2). Both modes are supported by the ZIOL2xxx Ics. The active mode is defined in the configuration register [7] bit 7. The chosen mode influences the IC's driver behavior as well as the handling of overload exceptions. Both input channels do not depend on the operational mode.

In master mode[2] the data inputs (TX) of both drivers are connected internally. As regards their functionality both drivers work in parallel. Therefore, the driver outputs have to be interconnected externally in master mode.

In device mode both drivers are working independently. A respective current overload signal will be generated if at one or at both drivers the output current exceeds the set current limit for longer than the configured amount of time.

Figure 3.5 shows a simplified application circuit including ZIOL24xx Ics in device and in master mode, respectively. Although both drivers are controlled by the same "TX" signal in master mode, the driver strength can be influenced with the COM_EN and AUX_EN signal thus the resulting driver strength can be reduced in this mode.

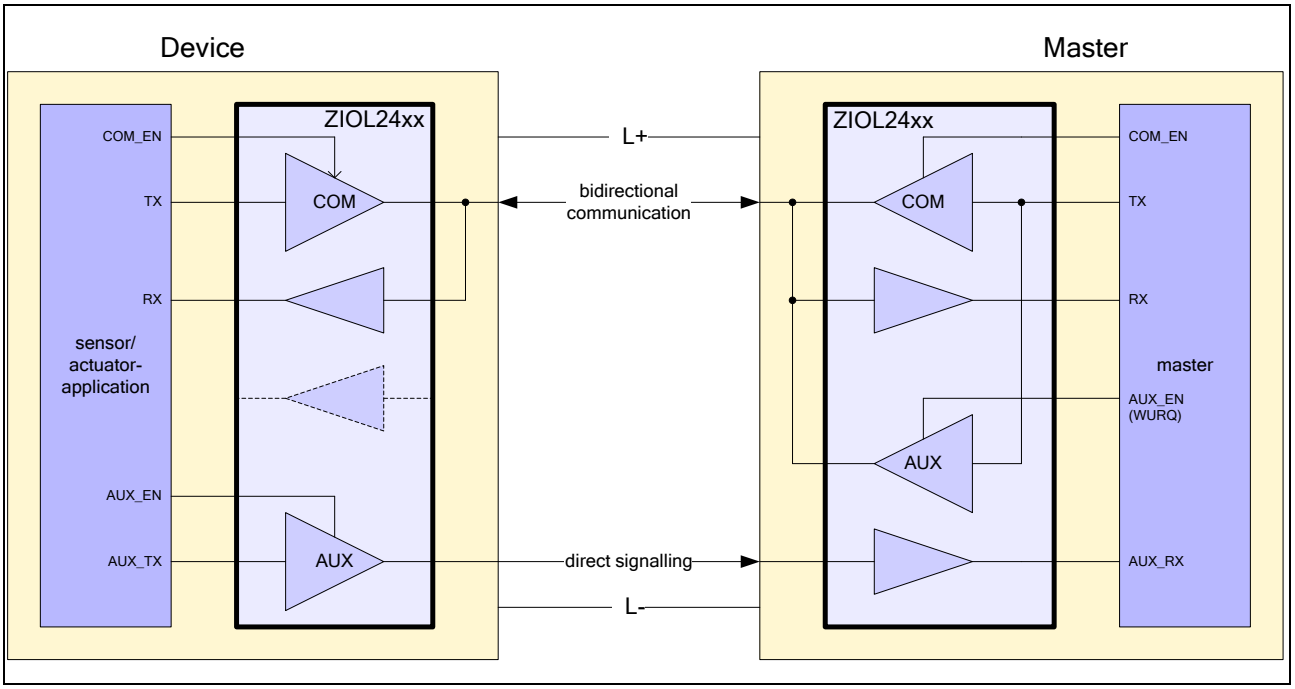
Starting with Rev B of the IC the MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] replaces the formerly used control via an input pin. Summarizing the above, the MASTER_MODE flag controls:

- The Data path; it controls whether both channels use an individual or common TX signal
- The current sinks at the receiver's inputs in the IO-Link sink mode (refer to Table 3.4)

For more information about the data path configuration of the IC in device and in mode master, please refer to chapter 3.2.1.

[1] Note: The IC versions ZIOL22xx/21xx have just one channel. With respect to those IC versions the statements concerning the existence of two channels shall be ignored or interpreted analogously.
[2] Not applicable for the IC versions ZIOL22xx/21xx

Figure 3.5 ZIOL24xx in Device and Master Mode Application



The illustration in Figure 3.5 shows the principal way of using the ZIOL2xxx integrated circuit in master and device mode. Figure 3.5 does not include all required electronic components of the application circuit which are mentioned in chapter 4 (Figure 4.1 and Figure 4.2).

3.2.2.3. Configuration

The COM and AUX drivers are built identically. Their features can be configured in a wide range. The behavior of the output stages can be set to push, pull or push/pull. Current limitation and the overload timing can be set individually. In order to improve the EMC system behavior the slew rate of the output signal is controlled and can be set according to the needs of the application. The following table gives an overview of the possible configurations for the COM and AUX driver in master and device mode, respectively.

Table 3.2 Driver configurations

Parameter	Config.-Register	Reg.-Addr.	Bit-Field	Ranges & Coding	Unit	Remarks[1)]
COM and AUX driver output current limitation	COM_PARAM, AUX_PARAM	2 4	4:2	0b000: 50 0b010: 100 0b100: 200 0b110: 250 0bxx1: limitation off[2)]	mA mA mA mA	IC in Device mode: both drivers work independently
Combined driver output current limitation	COM_PARAM, AUX_PARAM	2 4	4:2	0b000: 100 0b010: 200 0b100: 400 0b110: 500 0bxx1: limitation off[2)]	mA mA mA mA	IC in Master mode: both drivers work in parallel Both drivers shall be set to identical driver capability.
Slew Rate Control	COM_CTRL, AUX_CTRL	1 3	4:3	0b00: 10 0b10: 60 0b01: slow control off 0b11: fast control off	V/µs V/µs	Limitation of maximal edge steepness. Limitation turned off! Limitation turned off!
Output characteristic	COM_CTRL, AUX_CTRL	1 3	1:0	0b00: off 0b01: pull 0b10: push 0b11: push+pull		
Overload time base – COM, AUX	COM_MON_CTRL, AUX_MON_CTRL	11 13	6:5	0b00: 0.2 0b01: 1000 0b10: 8000 0b11: 16000	µs	Defines the clock frequency for COM/AUX overload counters
Overload counter compare value – COM, AUX	COM_ASSERT_TIME, AUX_ASSERT_TIME	10 12	7:0	Byte		If overload counter value equals compare value an overload will be asserted
Pull up/down enable – COM, AUX	COM_PARAM, AUX_PARAM	2 4	6:5	Bit 6: pull-up Bit 5: pull-down		Enables resistor of typical 150kOhms

[1)] For a summary of all configuration registers, please refer to Table 3.7.
[2)] Not recommended due to chance of overheating

3.2.3. Receiver

3.2.3.1. General Functionality

In principle, the ZIOL2xxx IC family has two[1] identical input channels with a configurable feature set. The input threshold levels can be set ratiometric or absolute. The absolute values are compatible with definition of Type 1 digital inputs in IEC61131-2 and conform to the IO-Link specification. The ratiometric levels[2] are proportional to the HV power supply voltage. The ratiometric level configuration allows the input channels to function down to a

[1] Note: The IC versions ZIOL22xx/21xx have only one receiver.
[2] Note: Ripple on the supply voltage may have influence to the trip-point of the input stage. Another influence to be considered is that an enabled analog input filter is reducing the ripple on the on the received signal.

supply voltage of 8V. For each input channel an analog and a digital filter are implemented, which can separately be enabled.

3.2.3.2. Configuration

The following table gives an overview of the possible configurations for the COM and AUX input channels.

Table 3.3 Receiver configurations

Parameter	Config.-Register	Reg.-Addr.	Bit-Field	Setting / Range	Unit	Remarks[1)]
Threshold level for COM and AUX	COM_CTRL, AUX_CTRL	1 3	5	0b0: absolute 0b1: ratiometric		Absolute = IO-Link compliant thresholds
Analogue filter	COM_CTRL, AUX_CTRL	1 3	2	0b0: disabled 0b1: enabled		
Digital filter	COM_CTRL, AUX_CTRL	1 3	7	0b0: disabled 0b1: enabled		
I_{sink}, sink strength	COM_PARAM, AUX_PARAM	2 4	7	0b0: 2 – 3 0b1: 5 – 7	mA	
Sink mode	COM_PARAM, AUX_PARAM	2 4	1:0	0b00: off 0b01: IO-Link 0b10: follow driver 0b11: on		Following driver: if driver is enabled then sink = off if driver is disabled then sink = on

[1)] For a summary of all configuration registers, please refer to Table 3.7.

3.2.3.3. Sink Modes

The IO-Link standard defines a possible configuration option, in which the device drives the signal line only with a high side driver thus the logic low level will be generated with a current sink on the master side (Figure 3.6). The ZIOL2xxx supports the current sinks in different modes on master side (for details refer to Table 3.4).

Figure 3.6 Typical IO-Link Device Configuration with HS driver only

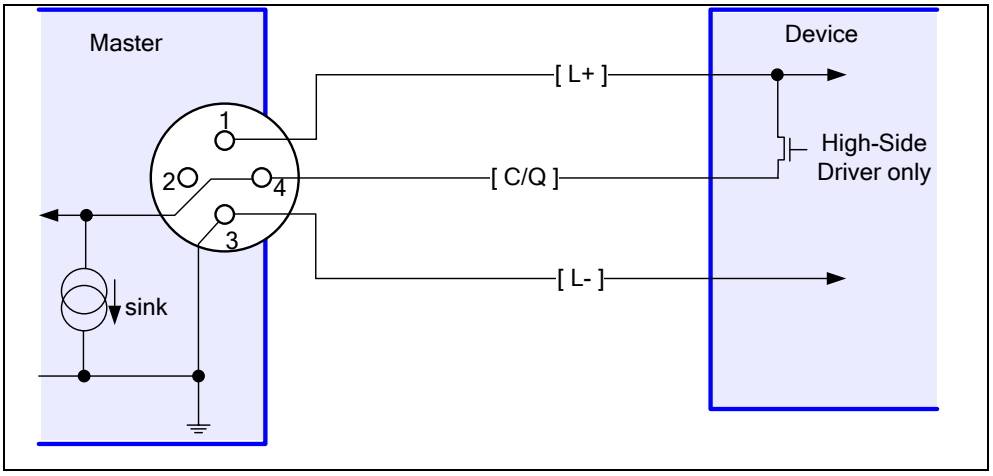


Table 3.4 Sink Mode Configuration in Detail

Register[2][1:0] Register[4][1:0]	Mode	Sink enabling	Remark
00	n.a.	Sink steady disabled	OFF
01	Device Mode [1]	Sink steady disabled	Typical application mode for the IO-Link channel: **device**: no sink **master**: sink enabled contrary to the corresponding driver enable signal
	Master Mode [2]	Sink enabled if: • TX_EN/SPI_CLK = low (COM) • AUX_EN = low (AUX)	
10	n.a.	Sink enabled if: • TX_EN/SPI_CLK = low (COM) • AUX_EN = low (AUX)	Enabling contrary to the driver enable signal; sink is only enabled while the driver is disabled. (helps to reduce the system's power dissipation)
11	n.a.	steady enabled	ON

[1] MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] is cleared (=0).
[2] MASTER_MODE flag (configuration register MASTER_SENS_CTRL[7] is set (=1).

3.3. System Control

3.3.1. General

The system control provides device configuration, status signaling and SPI data transfer functionality. Implemented are several register areas which contain configuration data and which provide status information. In order to gain read/write access to these register areas, the standard serial peripheral interface (SPI) is implemented. Since the pin count of the package is limited to 24 pins, the SPI specific pins (CLK, MOSI, and MISO) are multiplexed with IO-pins of the COM driver. A dedicated pin SPI_EN_L is used to switch between SPI

(logic low) and COM transceiver functionality (logic high). The low voltage (LV) interface works with 3.3V supply voltage (refer to Figure 3.1). The LV outputs drive 3.3V as high level, the inputs are 5V tolerant.

If the SPI communication channel of the ZIOL2xxx Ics is active (SPI_EN_L = low), the status of the COM channel drivers is kept. This means while SPI_EN_L = low the output driver status (driving low, driving high, or high-z) is the same as defined by the pins TX_EN/SPI_CLK and TX/MOSI at the point of time of the SPI_EN_L high-low transition. The AUX channel is not affected by the activity of the SPI communication. For more information, please refer to chapter 3.3.8 and Figure 3.10.

3.3.2. IO-Link Master[1] and Device Mode

The IC architecture is suitable for both IO-Link application cases, the physical layer transceiver at an IO-Link master port and at an IO-Link device port. In the first case the IC shall operate in its “master mode” which is the case if configuration register [7] bit 7 is set (=1). If the IC shall operate in “device mode”, configuration register [7] bit 7 shall be cleared (=0). Details regarding the control of both driver channels are described in chapter 3.2.1, 3.2.2.2 and 3.2.3.3.

The IO-Link specific WURQ detection (detection of an IO-Link master’s wake-up request, refer to IO-Link Communication Specification – chapter 8, [2]) works only in device mode.

3.3.3. Internal Exceptions

Depending on the IC configuration the ZIOL2xxx can detect several critical situations and rise internal exceptions accordingly. Also depending on the IC configuration an occurred internal exception can be indicated externally by changing the logic level of the INT-L pin to “low”. The situations that cause an internal exception are channel locks (channel driver protection), detected IO-Link specific Wake-Up pulses and several issues concerning the internal EEPROM as described in chapter 3.3.10.

3.3.4. IO-Link specific Wake-Up (WURQ)

In device mode the IC can detect the IO-Link specific wake-up request (WURQ) of the IO-Link master and can therefore help to save resources in the microcontroller of IO-Link device. As regards the IO-Link specific “Wake-Up (WURQ)” specification, please refer to the IO-Link Communication Specification issued by the IO-Link consortium (refer to chapter 8, [2]).

The WURQ can be detected on the COM or on the AUX channel. The chosen channel is defined in a configuration register (IRQ_WURQ_CTRL, refer to chapter 3.3.9).

In order to establish an IO-Link specific communication, the master will generate the WURQ event. In this case the master overdrives the devices output level for a determined period. The ZIOL2xxx can detect that event which physically occurs in two ways:

- A current overload in the drivers output for a certain period
- A contradiction of the TX and RX lines of the device for a certain period

The IC configuration register (IRQ_WURQ_CTRL, refer to chapter 3.3.9) defines if the “overload” or the “contradiction” or both events shall be chosen for the WURQ detection. Both ways of detection can be enabled

[1] Not applicable for the IC versions ZIOL22xx/21xx.

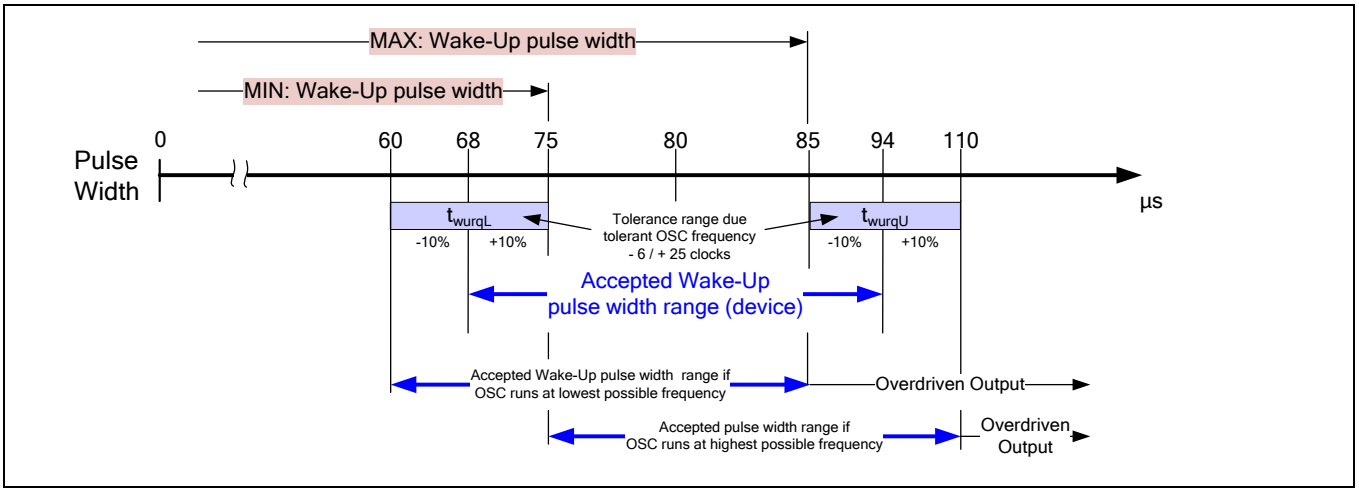
independently. If at least one of both events appears for a specific time, the incident will be regarded as WURQ request from master side and the IC will generate an internal exception (issue an interrupt) in order to signal this to the interconnected µC. Besides the configurable signaling on the INT_L pin (refer to chapter 3.3.10.1) this special exception will be displayed on the therefore dedicated WURQ_L pin. Details of the signaling via the WURQ_L and/or the INT_L pin and the pin driver configuration of the WURQ_L pin can be defined in the configuration registers which are described in detail in chapter 3.3.9.

The logic level of the WURQ_L pin (a wake-up causes logic low) or the stored WURQ event will be reset as soon as the drivers direction is set to input (TX_EN=0), which equals the WURQ acknowledge from the IO-Link device side.

The on logic level based WURQ detection works only for level-changes which are driven by the master. That means a WURQ will not be detected if a level change has been initiated by the device itself, even if the signal timing is equivalent to a WURQ event. This prevents the in SIO mode operating IO-Link device to misinterpret the situation caused for instance by capacitive loads.

If the ZIOL2xxx operates in master mode (physical interface for IO-Link master port) and a Wake-Up pulse (WURQ) shall be issued, the µC has to control the required driver strength by activating both channels (via COM_EN and AUX_EN, refer to Figure 3.5) and has to provide the correct timing.

Figure 3.7 Wake-Up Signal Recognition



The WURQ pulse recognition of the ZIOL2xxx in device mode is – in contrast to that – based on a time base derived from the internal oscillator (OSC). Therefore the as WURQ recognized pulse width range of an received Wake-Up signal is dependent on the frequency tolerance of the internal oscillator as illustrated in Figure 3.7. A Wake-Up signal (pulse width according to the IO-Link Communication Specification, refer to chapter 8, [2]) shall have a pulse width between 75µs and 85µs (variation 10µs). The ZIOL2xxx Wake-Up signal detection will always recognize such a signal securely considering a frequency tolerance of the internal oscillator of ±10% (refer to parameter f_{osc} in Table 2.3).

3.3.5. IC Self-Protection – Lock Mode

In order to prevent serious IC damage due to overloaded or overheated driver transistors, the IC has a build-in protection mechanism. If a critical situation occurs for a certain configurable time, the IC can protect itself in transferring its control in a special mode, called lock mode, in which the driver of the related channel is turned-off in case of over-current, or in case of over-temperature the drivers of both channels are turned-off, respectively.

Figure 3.8 shows the basic scheme of the IC self protection. In principle, this scheme is five times implemented in order to tread:

- Over-current situations separately at the high side and at the low side switch of the COM channel as described in Figure 3.15
- Over-current situations separately at the high side and at the low side switch of the AUX channel as described in Figure 3.16
- Over-temperature situations of the silicon die as described in Figure 3.17

In case of an over-current or over-temperature situation occurs (in the following called overload) the related over-current/over-temperature counter (overload counter) will count up. Since the overload counter counts down to zero in case of no overload is existent, the circuit performs an integrator function. This integrator function makes sure that overloads which temporarily occur are not accumulated thus will not lead to an unwanted driver locks.

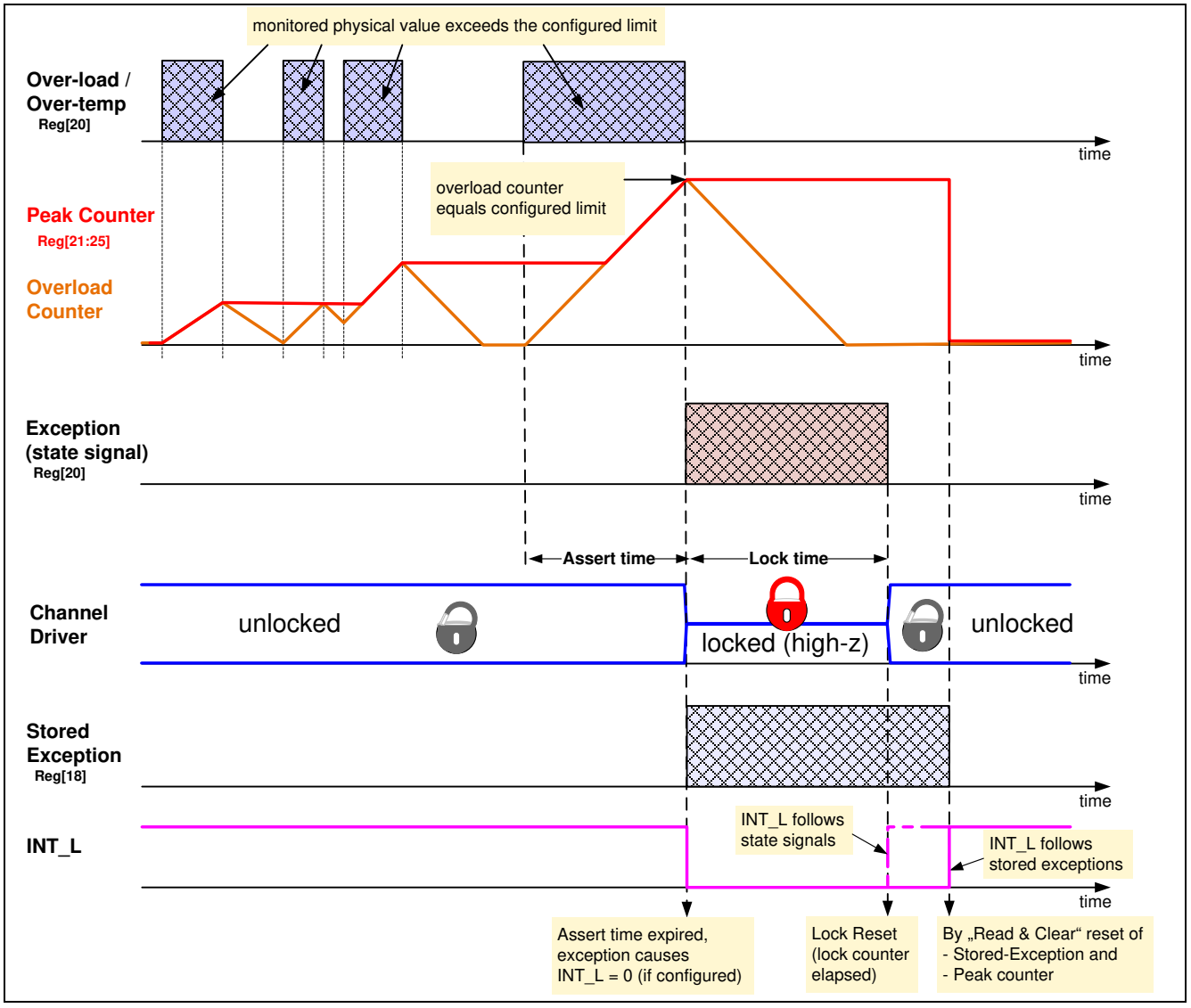
If the overload counter has reached the (in the related configuration register) defined maximum value, the IC will generate an internal exception. This exception will lock the associated channel or both channels in case of an over-temperature situation. The “assert Time” (refer to Figure 3.8) which is the elapsed time in until reaching the configured maximum of the overload counter depends on the used clock period for the overload counter. This clock period can be defined separately for the lock control circuit of each channel (Figure 3.15, Figure 3.16) and the temperature lock control circuit (Figure 3.17) in the associated configuration register.

To each overload counter is a peak register associated. The value of the overload counters can not be retrieved via the SPI port. However, the value of the overload counter will be copied in the related peak register if the value of the overload counter is greater than the value of the peak register. The peak registers can be read via the SPI port. The content of the peak register will be cleared after each read access. However, within the next cycle of the IC control circuit the peak register will be set to the overload counter value again if this value is greater than zero.

The above described peak register update is only performed if an overload situation is present. In case of overload situation the peak register is an important instrument to perform an IC diagnostic. For more information about techniques to operate the peak, please refer to Appendix A.

A due to an overload raised internal exception will cause in case of over-current a lock of the related channel or a lock of both channels in case of a over-temperature situation. There are three signals (displayed in status register[20] which indicate the lock activator. The other five bits of this status register indicate what IC sensor has detected an over-current or if the configured maximum of the die temperature has been exceeded.

Figure 3.8 The Basic Scheme of the IC Self Protection



Any internal exception will be stored in status register[18]. This status register will be cleared by reading the register but the appropriated bit will be set again (within the next cycle of the IC control circuit) if an exception is still present.

A lock can be reset by using the build-in and configurable lock counter (defined in the associated configuration registers). As shown in Figure 3.8 the lock reset will be performed when the lock time has been elapsed. The lock counter is using the same clock as the associated overload counter(s). Alternatively a lock can be reset by performing an write access to status register[16] (for more details refer to Appendix A).

Depending on the IC configuration the any exception or stored exception can cause the INT_L pin to logic low. As shown in Figure 3.8 INT_L can follow the state signals (internal exceptions) or the stored exception which is also depending on the IC configuration.

3.3.6. Channel Locking in Master/Device Mode

There are three independent lock mechanisms implemented. For each channel (COM and AUX) a separate lock can be generated if an over-current at the high side or low side switch has occurred. Therefore it is implied that for the considered switch a current limit had been configured. The third lock mechanism which is affecting both channels is related to over-temperature situations.

As regards the IC operation as IO-Link master or device PHY (master/device mode, refer to chapter 3.3.2) the lock mechanisms of both channels are really separated or coordinated as following described:

Master[1] mode (COM and AUX driver work in parallel – Tandem Mode):

- Assumed that both channels (COM and AUX) are enabled and the configuration flag BOTH_CHANNEL_LOCK (register[14]) is set (=1), both HS or both LS driver of both channels need to be overloaded simultaneously for longer as a configured time in order to generate an IC-internal overload exception which is indicated at the INT_L pin (logic low).
- In the case the IC works in tandem mode and the configuration flag BOTH_CHANNEL_LOCK (register 14) is set (=1), but only one of the channels (COM or AUX) is enabled, the protection of the enabled channel is performed analogous to the device mode.
- If single HS or a single LS driver is disabled, then its overload signal is not needed to create a general overload signal, in that case just the other (enabled) HS or LS driver can generate the overload exception.
- If the die temperature exceeds the configured limit thus a temperature overload exception is detected, the IC locks both channels and signals and according to the IC's configuration an interrupt can be signaled at the INT_L pin.

Device mode:

- Any single overloaded HS or LS driver of the COM or AUX channel leads to a lock and an interrupt signaling (INT_L pin) according to the configuration of the IC.
- If the die temperature exceeds the configured limit thus a temperature overload exception is detected, the IC locks both driver channels and signals and according to the IC's configuration an interrupt is signaled at the INT_L pin.
- If both drivers are configured parallel, the interrupt behavior equals the master mode

The lock mode is associated with IC-internal exceptions that are signaled to the interconnected µC as an interrupt. The details for building and clearing an exception are described in the chapter 3.3.10 which deals with the interrupt handling and lock mode operation.

3.3.7. Memory Unit

The memory unit of the IC provides several IC configuration options. Those configuration options define the properties of the Ics driver channels and define the IC monitoring and protection functions with respect to the over-current and over-temperature handling.

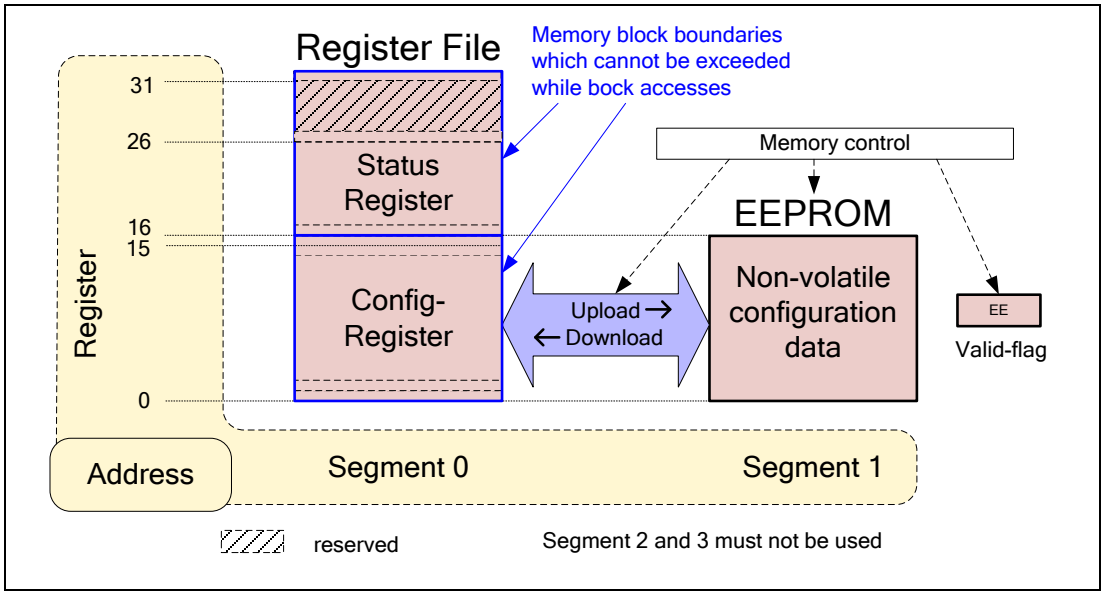
[1] Not applicable for the IC versions ZIOL22xx/21xx

The currently applied configuration data of the IC is stored in the configuration-register area which is implemented as a register file. The configuration-register area can be uploaded via SPI command into an on-chip EEPROM for non-volatile storage. While power-on-reset or also via SPI command the EEPROM content will be downloaded to the configuration-register area.

Besides data for IC configuration the IC has certain status registers that can be used to monitor the internal status of the IC. The status registers reflect the IC status as regards the occurrence of different driver channel overload situations and their duration. Moreover, four alert phases (green, yellow, orange and red) indicate the die temperature of the IC and in this combination the die temperature margin prior a thermal shut down of certain IC building blocks. In principle, status registers are read-only registers. Some status registers are reset by reading the register's value. Furthermore, a write access to some status registers will cause certain control actions (for more information refer to Table 3.7).

The read/write access to the Ics memory unit is provided by an SPI interface (refer to chapter 3.3.8). In order to access a certain register or range of consecutive registers (block access) an 8-bit-address has to be applied which consists of segment address (2bits) and register address (6 bits) as illustrated in Figure 3.9.

Figure 3.9 Memory Unit



In case of a collapsing supply voltage while writing data into the EEPROM, the EEPROM data shall be suspected to be corrupt. There is an additional build-in security feature to indicate this situation and to avoid that corrupt EEPROM data is used for the IC configuration. In this combination a non-volatile flag (one bit EEPROM) is used to indicate possibly not valid (corrupt) EEPROM data. This flag which is called valid-flag is set if the data are valid or is cleared if the data are suspected to be corrupt. As shown in Figure 3.14 corrupt EEPROM data or any other EEPROM problems can cause an internal exception.

The above mentioned feature is using the following procedure while performing an EEPROM write access:

1. Clearing the valid-flag.

2. Write access to the EEPROM. This is the critical step which can lead to corrupt data if interrupted at certain points in time. Since the valid-flag is cleared the IC can detect this and make sure that no corrupt data are going to be used unintentionally.
3. Set the valid-flag. From now on the data are declared as valid.

If the power supply of the IC collapses while writing to the EEPROM or the write access is interrupted by any other reason, the IC can detect this while power-up due to the cleared valid-flag and can and block the EEPROM data against further use. Just in case the IC has detected possibly corrupt EEPROM data the configuration registers will be load with default values which are equal to the initial state (reset values) mentioned in Table 3.7.

3.3.7.1. EEPROM Error Correction Features

The physical memory array of the EEPROM contains 16 words of 13 bits. In addition to the eight “real” data bits there are five parity bits which are used as error correction code (ECC). In case one of the data bits changes its information an automatic single-error correction will be done. Thus the data word (read by the IC system control) is still correct if this one-bit-error occurs. In order to signal this incident the exception “Eeprom-error” is generated (stored in bit 4 of the status register[18]).

If a two-bit-error occurs (two bits of the data word are wrong) the ECC cannot correct the memory failure. This means the in such a situation read data is corrupt. In order to signal this non-recoverable memory failure the exception “Eeprom_2_error” is generated (stored in bit 3 of the status register[18]).

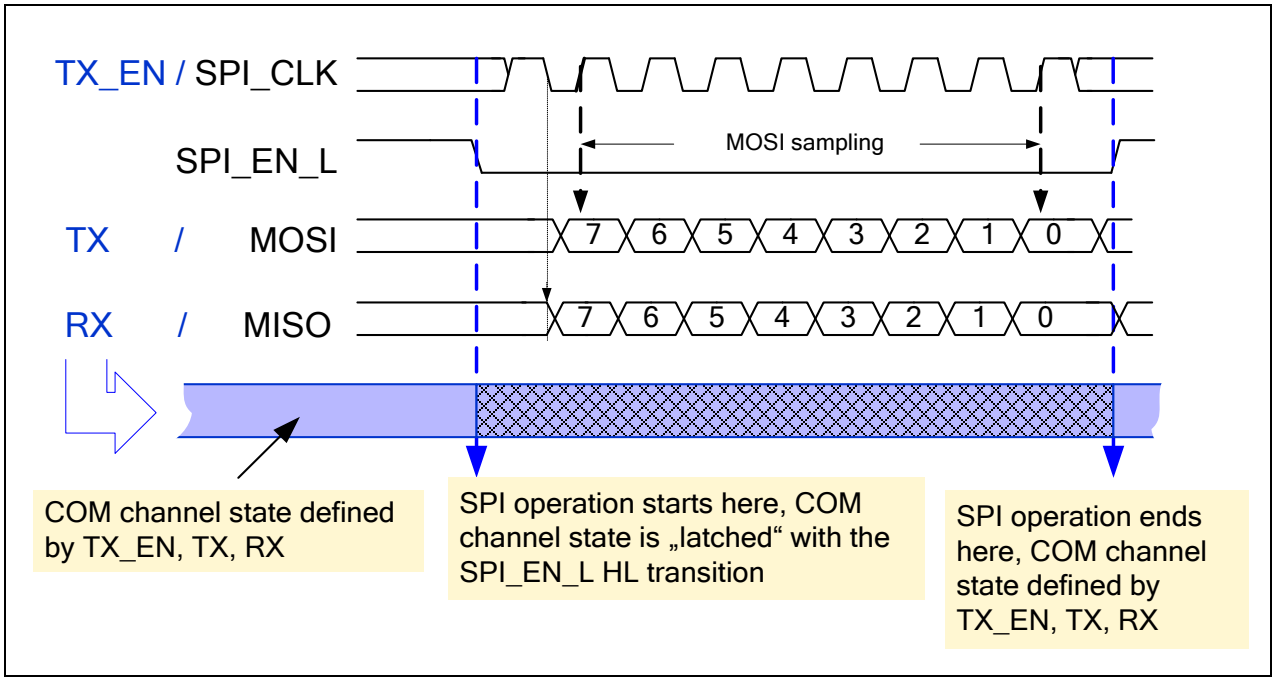
In summary the ECC features of the EEPROM allow to recognize problems (single bit errors) of the EEPROM (Eeprom_error exception) without jeopardizing the entire system application. Only for the case that there are multiple-bit-errors, which are signaled with the “Eeprom_2_error” exception, it is recommended to stop the application and maintain the application circuit.

3.3.8. Serial Peripheral Interface (SPI)

3.3.8.1. SPI Features

The purpose of the SPI interface is to provide access to the memory unit of the IC. Within communication pauses of the transceiver channels the SPI can be used to retrieve diagnostic data from the IC and/or to reconfigure the IC, respectively. An active SPI communication causes that the COM communication channel, which shares its control pins with the SPI interface, cannot change its output value and output status and cannot forward received signals for exactly the period SPI_EN_L is low (refer to Figure 3.10).

Figure 3.10 General timing of a byte transfer



SPI feature summary:

- The interface works in SPI-slave mode only
- The timing follows the scheme in Figure 3.10 which defines
  - Clock Polarity CPOL = 1 (clock is idle high)
  - Clock Phase CPHA = 1 (data captured with 2nd clock edge after SPI_EN_L went low; data are read on clock's rising edge and data are changed on a falling edge)
- Maximum clock frequency of the SPI_CLK shall not exceed 4 MHz for accessing the on-chip EEPROM and 10 MHz for other SPI accesses
- SPI clock duty cycle: 40…60%
- MSB will be transmitted first
- If access exceeds last byte, a wrap will NOT happen – the last byte will be written correctly, rest will be disregarded
- Block write (access to more than one address location) is only supported for the configuration-register area but not for the EEPROM area.
- Block read is supported for both the EEPROM and configuration-register area.
- During enabling the SPI (SPI_EN_L = low) the input lines of the COM driver are latched, so the COM driver does not change its output state while SPI is enabled.

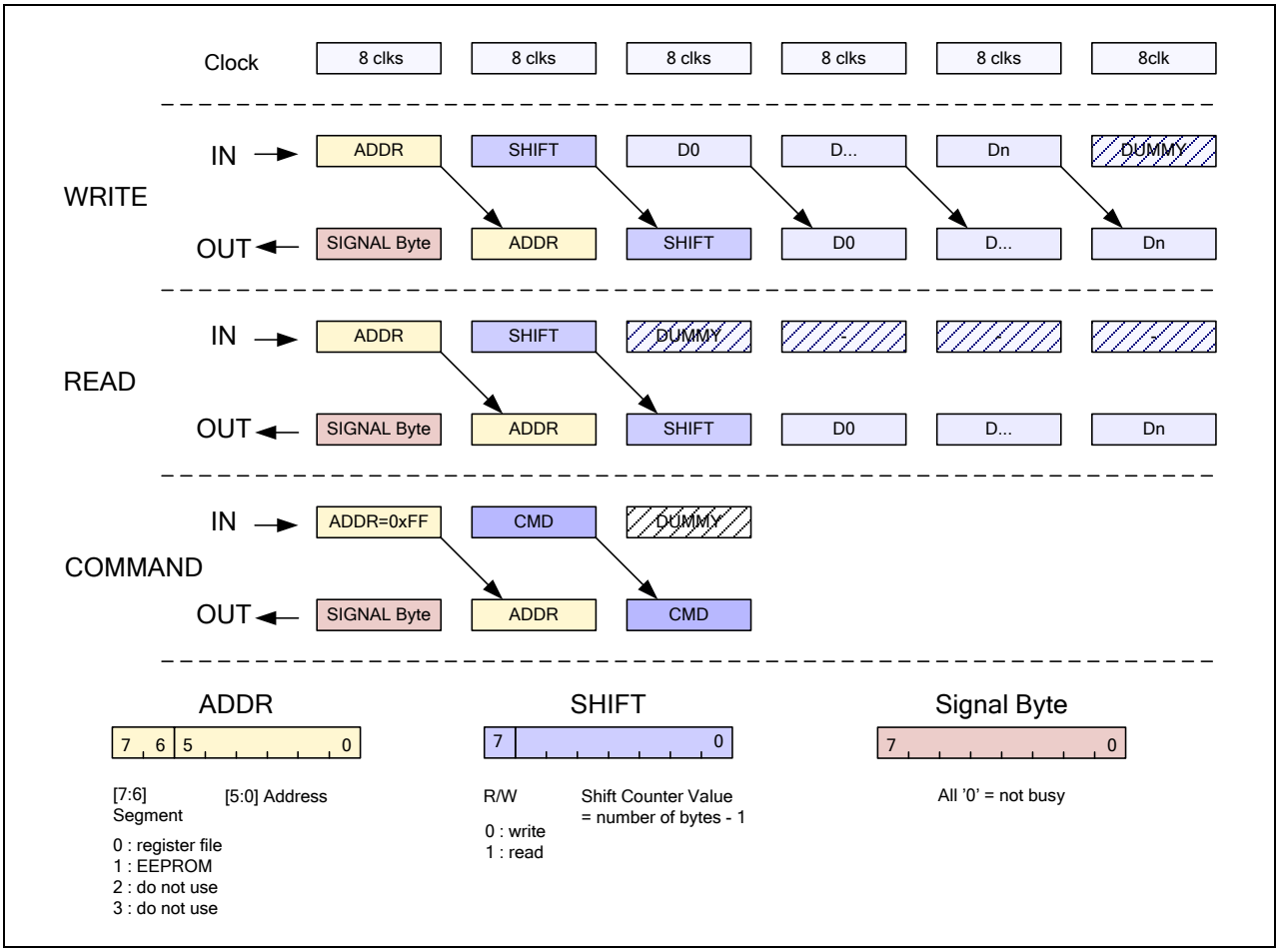
The SPI telegram structure can be divided into three types of SPI accesses:

- **READ:** read access to register file or EEPROM, block access possible

- **WRITE**[1]**:** write access to register file (if applicable) or EEPROM, block access only supported with the access to register file
- **COMMAND:** Commands to achieve an IC (soft-)reset or up- or download of configuration data

Figure 3.11 illustrates the structure of supported SPI accesses. The in this figure illustrated write access works only with the IC versions ZIOL2xx1

Figure 3.11 Structure of SPI accesses



3.3.8.2. SPI access details

The timing of the three SPI access types is illustrated in Figure 3.13. As shown in this figure the 1st byte, which is called destination byte, is composed out of the segment address (bit 7:6) and the register address (bit 5:0). A command is always using the address 0xFF which is a not physically implemented memory location within the IC memory unit.

[1] Note: IC versions ZIOL2xx2 do not allow any write access.

The READ and WRITE[1] access is defined in the value of bit 7 (0=write; 1=read) of the 2nd byte which is called the SHIFT byte. Bit 6:0 represent the repeat count. This value defines the number of additional consecutive bytes to be accessed. In case of a write access the SHIFT byte following bytes are the actual data to be written into the memory location(s). Table 3.5 illustrates the building of the SHIFT byte in using an example.

Table 3.5 Example for building the SHIFT Byte

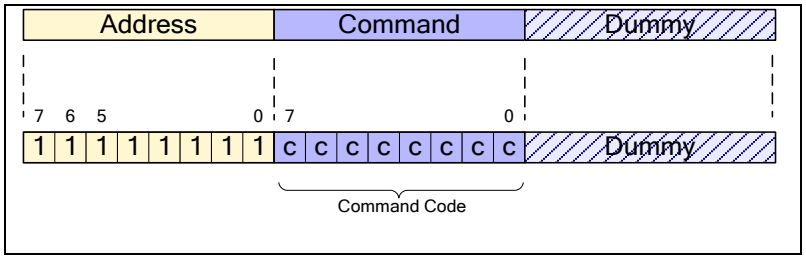
Number of bytes to be accessed	SHIFT byte value In case of a write access	SHIFT byte value In case of a read access
1	0000 0000	1000 0000
2	0000 0001	1000 0001
3	0000 0010	1000 0010
…	…	…
16	0000 1111	1000 1111

If the transferred data stream of one telegram exceeds the border line of the chosen memory block, all following accesses will be disregarded. No wrap will happen! For more details refer to Table 3.6.

Table 3.6 Valid Address and Length Combinations

Segment	Address	Length = SHIFT[6:0]	Comment
00	00 0000 … 00 1111	000 0000…000 1111 … 000 0000…000 0000	Configuration-register block
	01 0000 … 01 1001 01 1111	000 0000…000 1111 … 000 0000…000 0101 000 0000…000 0000	Status register block Although status registers can be accessed up to address 31 the useful range is only up to address 25
01	00 0000 … 00 1110	000 0000 … 000 0000	EEPROM is directly accessible via SPI but there is no block operation allowed

Figure 3.12 SPI Command Structure



[1] Note: IC versions ZIOL2xx2 do not allow any write access.

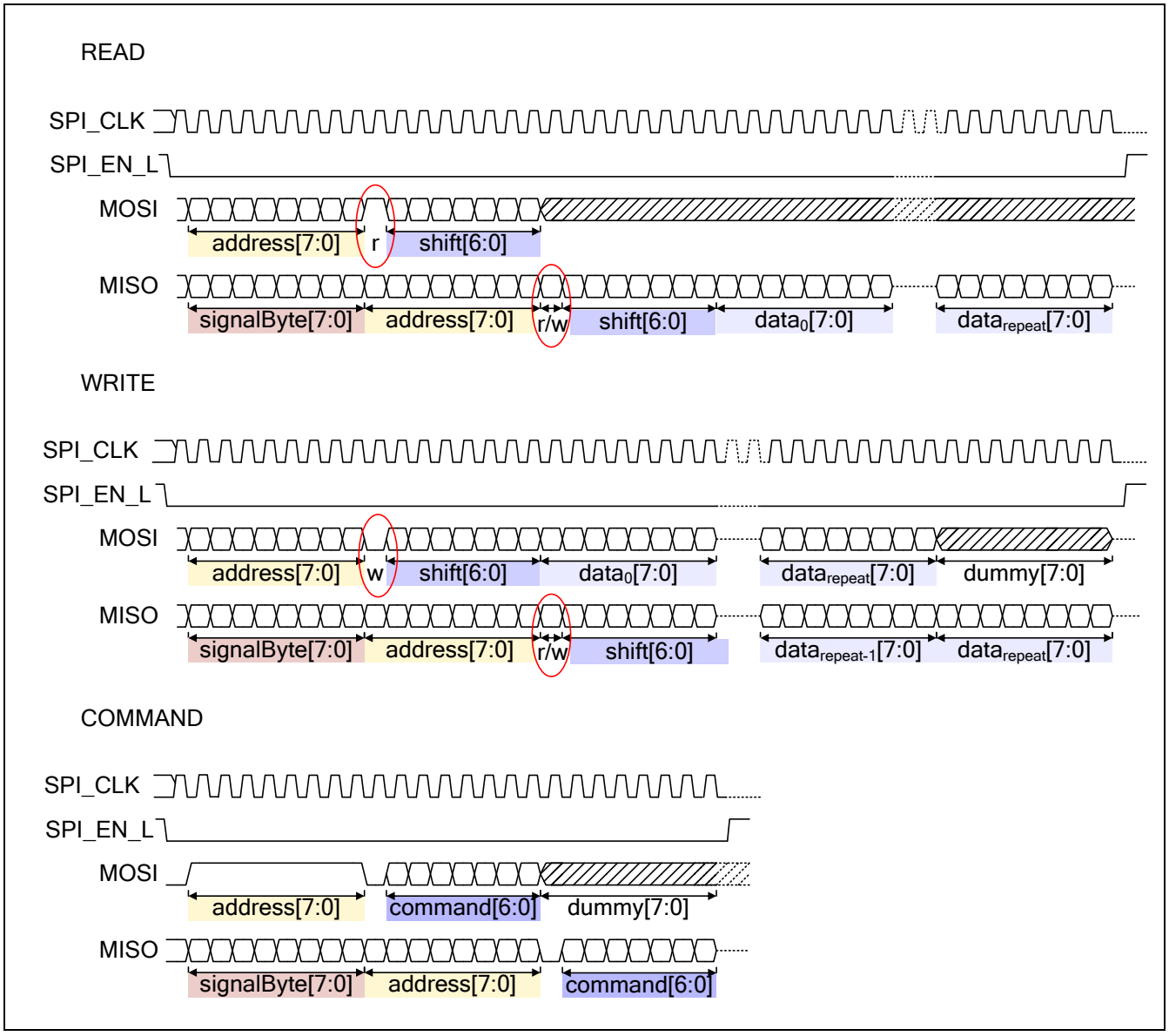
The structure of an SPI command is shown in Figure 3.12. There are three commands implemented which are:

- **MEM_DOWNLOAD**
  Code: 0x01
  Description: If the EEPROM data is valid (valid-flag = 1 → data is not corrupt) the MEM_DOWNLOAD copies the EEPROM data into the configuration registers. If the data are suspected to be corrupt (valid-flag = 0), the EEPROM data are not downloaded and an interrupt (INT_L pin) will be asserted.

- **MEM_UPLOAD**
  Code: 0x02
  Description: The command copies the entire configuration register data into the EEPROM memory. The command execution starts with clearing the valid-flag and then with reading the configuration registers and writing the data into the EEPROM. At the end of cycle the valid-flag is set to 1.

- **SOFT_RESET**
  Code: 0x07
  Description: The command execution generates a reset for the entire IC. This reset occurs asynchronously with reference to the system clock but is released synchronously. When this SPI command is being executed, the system is hold in the reset state for about 2µs. The system reset state is indicated with active low on the INT_L pin.

Figure 3.13 SPI Timing[1]



3.3.9. Register Table / Registers for IC Configuration and Monitoring

The following Table 3.7 shows a summary of the configuration- and status registers of the ZIOL2xxx. The address space from address 0 to 15 is implemented in both the register file area and the EEPROM area. Registers with addresses greater than 15 (status registers) are implemented in the register file area only.

[1] Note: IC versions ZIOL2xx2 do not allow any write access.

As regards the access type to a particular register the following four types have been implemented:

1. **r/w** normal read/write[1]
2. **r** read only
3. **r/rst** read only, clear by read
4. **w/pulse** writing to such type of registers causes a partial reset of certain IC functions which correspond to the assigned bit of the write accessed register; reading is possible but will return no useful information

In order to illustrate for instance the w/pulse type a write access to status register MON_RST_LOCK_WURQ shall be explained. The bits of this register are assigned to

- the power fail event (bit 4) and
- the IO-Link specific wake-up request event (bit 3) and
- the COM/AUX driver over-current event (bit 2 and 1) and
- the over-temperature event (bit 0).

Writing the value 0x08 (MON_RST_WURQ = 1) to the register would cause a reset of the previously detected and stored wake-up request. In doing so the to the IC interconnected µC acknowledges the occurred wake-up request thus the IC is ready to detect the next wake-up request.

Table 3.7 Register Table

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
CONFIGURATION REGISTER							
IRQ_ENABLE	0		7:0	255	r/w		Figure 3.14
	0	IRQ_EN_POWER_FAIL	7	1	r/w	Power fail interrupt enable	Added in Rev B
	0	IRQ_EN_WURQ	6	1	r/w	WURQ interrupt enable	
	0	IRQ_EN_VALID_FLAG_ERR	5	1	r/w	Valid-flag error interrupt enable	
	0	IRQ_EN_EEPROM_ERR	4	1	r/w	Single bit error interrupt enable	
	0	IRQ_EN_EEPROM2_ERR	3	1	r/w	Multiple bit error interrupt enable	
	0	IRQ_EN_LOCK_AUX	2	1	r/w	interrupt enable for over-load lock of AUX line driver	

[1] Note: IC versions ZIOL2xx2 do not allow any write access.

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
	0	IRQ_EN_LOCK_COM	1	1	r/w	interrupt enable for over-load lock of COM line driver	
	0	IRQ_EN_LOCK_OVT	0	1	r/w	interrupt enable for over-temperature lock of both, AUX and COM, line drivers	
COM_CTRL	1		7:0	0	r/w	IOLINK-control-register	
	1	COM_DIG_FILTER	7	0	r/w	Enable digital RX-Filter	
	1	COM_INV_SEND	6	0	r/w	invert receive and send (implemented in digital part)	
	1	COM_RATIO	5	0	r/w	Disables the receiver IO-Link levels and enables ratiometric	
	1	COM_COM3	4	0	r/w	COM3-Mode (slope-control), 0: COM2 1: COM3	
	1	COM_NOEDGE	3	0	r/w	Disables Edge control	
	1	COM_FILTER	2	0	r/w	Filter-enable 0=off / 1 = on	
	1	COM_LS_ON	1	0	r/w	LowSide-Driver 0=off / 1=on	
	1	COM_HS_ON	0	0	r/w	HighSide-Driver 0=off / 1=on	
COM_PARAM	2		7:0	0	r/w	IOLINK-Control-Parameters	
	2	COM_SINK_STRENGTH	7	0	r/w	Sink_strength	
	2	COM_PULLUP_EN	6	0	r/w	Pull-Up Enable for COM-Channel	
	2	COM_PULLDOWN_EN	5	0	r/w	Pull-Down Enable for COM-Channel	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
	2	COM_CULI	4:3	0	r/w	Current Limit	
	2	COM_NOCULI	2	0	r/w	Current-Limiting disabled	
	2	COM_SINK_MODE	1:0	0	r/w	Sink-Mode	
AUX_CTRL	3		7:0	0	r/w	IOLINK-control-register	
	3	AUX_DIG_FILTER	7	0	r/w	digital RX-Filter	
	3	AUX_INV_SEND	6	0	r/w	invert receive and send (implemented in digital part)	
	3	AUX_RATIO	5	0	r/w	Disables the receiver IO-Link levels and enables ratiometric	
	3	AUX_COM3	4	0	r/w	COM3-Mode (slope-control)	
	3	AUX_NOEDGE	3	0	r/w	Disables Edge control	
	3	AUX_FILTER	2	0	r/w	Filter-enable 0=off / 1 = on	
	3	AUX_LS_ON	1	0	r/w	LowSide-Driver 0=off / 1=on	
	3	AUX_HS_ON	0	0	r/w	HighSide-Driver 0=off / 1=on	
AUX_PARAM	4		7:0	0	r/w	IOLINK-Control-Parameters	
	4	AUX_SINK_STRENGTH	7	0	r/w	Sink strength	
	4	AUX_PULLUP_EN	6	0	r/w	Pull-Up Enable for AUX-Channel	
	4	AUX_PULLDOWN_EN	5	0	r/w	Pull-Down Enable for AUX-Channel	
	4	AUX_CULI	4:3	0	r/w	Current Limit	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
	4	AUX_NOCULI	2	0	r/w	Current-Limiting disabled	
	4	AUX_SINK_MODE	1:0	0	r/w	Sink-Mode	
OVT_LOCK_TIME	5		7:0	200	r/w	Over-temperature: time until lock is released	Figure 3.17
COM_LOCK_TIME	6		7:0	100	r/w	Overload: time until Lock is released	Figure 3.15 Figure 3.16
MASTER_SENS_CTRL	7		7:0	1	r/w	Over-temperature	Figure 3.18
	7	MASTER_MODE	7	0	r/w	Master mode enabled, influences the data path and the receiver's current sinks in IO-Link mode	Added in Rev B
	7	EN_FOLLOW_PRIM_CH	6	0	r/w	The secondary channel: 0 = uses a separate enable signal 1 = uses the enable of the prim. ch.	Added in Rev B
	7	PRIMARY_MASTER_CH	5	0	r/w	Defines the primary channel: 0 = COM 1 = AUX	Added in Rev B
	7	RESERVED	4	0	r/w	RESERVED	
	7	OVT_RED	3	0	r/w	OVT level set to "Red"	
	7	OVT_ORANGE	2	0	r/w	OVT level set to "Orange"	
	7	OVT_YELLOW	1	0	r/w	OVT level set to "Yellow"	
	7	OVT_GREEN	0	1	r/w	OVT level set to "Green"	
OVT_ASSERT_TIME	8		7:0	100	r/w	Over-temperature: time until lock is asserted	Figure 3.17

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
OVT_PFD_CTRL	9		6:0	15	r/w	OVT and Power-Fail control	Figure 3.17
	9	LINE_FAULT_EN	6	0	r/w	Enables Line-fault (LF) detection	Added in Rev B
	9	UNDER_VOLTAGE_EN	5	0	r/w	Enables Under-Voltage (UV) detection	Added in Rev B
	9	OVT_TBASE	4:3	1	r/w	Over-temperature: time base	
	9	OVT_LOCK_TIME_RST	2	1	r/w	Over-temperature: reset lock (also) time based	
	9	OVT_LOCK_EN	1	1	r/w	Over-temperature: enable lock	
	9	OVT_EN	0	1	r/w	Over-temperature: enable OVT-measurement and control	
COM_ASSERT_TIME	10		7:0	50	r/w	COM-Overload: time until lock is asserted	Figure 3.15
COM_MON_CTRL	11		6:0	63	r/w		Figure 3.15
	11	COM_OVL_TBASE	6:5	1	r/w	COM-Overload: time base	
	11	COM_LOCK_TIME_RST	4	1	r/w	COM-Overload: reset lock (also) time based	
	11	COM_HS_LOCK_EN	3	1	r/w	COM-Overload: enable HighSide-lock	
	11	COM_LS_LOCK_EN	2	1	r/w	COM-Overload: enable LowSide-lock	
	11	COM_OVL_HS_EN	1	1	r/w	COM-Overload: enable HighSide-control, to be set if wake-up shell be detected via over-current activity	
	11	COM_OVL_LS_EN	0	1	r/w	COM-Overload: enable LowSide-control, to be set if wake-up shell be	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
						detected via over-current activity	
AUX_ASSERT_TIME	12		7:0	50	r/w	AUX-Overload: time until lock is asserted	Figure 3.17
AUX_MON_CTRL	13		6:0	63	r/w		Figure 3.17
	13	AUX_OVL_TBASE	6:5	1	r/w	AUX-Overload: time base	
	13	AUX_LOCK_TIME_RST	4	1	r/w	AUX-Overload: reset lock (also) time based	
	13	AUX_HS_LOCK_EN	3	1	r/w	AUX-Overload: enable HighSide-lock	
	13	AUX_LS_LOCK_EN	2	1	r/w	AUX-Overload: enable LowSide-lock	
	13	AUX_OVL_HS_EN	1	1	r/w	AUX-Overload: enable HighSide-control, to be set if wake-up shell be detected via over-current activity	
	13	AUX_OVL_LS_EN	0	1	r/w	AUX-Overload: enable LowSide-control, to be set if wake-up shell be detected via over-current activity	
IRQ_WURQ_CTRL	14		7:0	35	r/w		Figure 3.14
	14	IRQ_PAD_MODE	7	0	r/w	IRQ_PAD_MODE: 0 = open-drain / 1 = push-pull	
	14	WURQ_PAD_MODE	6	0	r/w	WURQ_PAD_MODE: 0 = open-drain / 1 = push-pull	
	14	DCDC_READY_DELAY	5	1	r/w	DCDC-Ready-delay-enable / 0 = No delay / 1 = delay 50 ms	
	14	BOTH_CHANNEL_LOCK	4	0	r/w	lock only, when both channel are in OVL-alarm Recommended to be	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
						set (=1) in tandem mode	
	14	IRQ_NOREG	3	0	r/w	0 = IRQ-Port follows state-reg / 1 = IRQ follows state-signals	
	14	WURQSOURCE	2	0	r/w	Source for WURQ-detection 0 = COM / 1 = AUX	
	14	WURQDETECT_CURRENT	1	1	r/w	WURQ detection on current (overload)	
	14	WURQDETECT_LVL	0	1	r/w	WURQ detection on levels (can be combined with current)	
AUX_LOCK_TIME	15		7:0	100	r/w	Overload: time until Lock is released	Added in Rev B
STATUS REGISTER							
MON_RST_LOCK_WURQ	16		4:0	0	w/pulse		Figure 3.14
	16	MON_RST_POWER_FAIL	4	0	w/pulse	Reset for power fail due to line-fault or under-voltage	Added in Rev B
	16	MON_RST_WURQ	3	0	w/pulse	Reset for Wake Up Request	
	16	MON_RST_AUX_LOCK	2	0	w/pulse	Reset for Channel 2 Lock	
	16	MON_RST_COM_LOCK	1	0	w/pulse	Reset for Channel 1 Lock	
	16	MON_RST_OVT_LOCK	0	0	w/pulse	Reset for Temperature Lock	
MON_RST_COUNTER	17			0			
	17	MON_RST_AUX_HS	4	0	w/pulse	Reset Channel2 OVL-HS-Counter	
	17	MON_RST_AUX_LS	3	0	w/pulse	Reset Channel2 OVL-LS-Counter	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
	17	MON_RST_COM_HS	2	0	w/pulse	Reset Channel1 OVL-HS-Counter	
	17	MON_RST_COM_LS	1	0	w/pulse	Reset Channel1 OVL-LS-Counter	
	17	MON_RST_OVT	0	0	w/pulse	Reset OVT Counter	
IRQ_STATUS	18		7:0	0	r/rst	Interrupt-Status	Figure 3.14
	18	IRQ_POWER_FAIL	7	0	r/rst	POWER_FAIL interrupt request	Added in Rev B
	18	IRQ_WURQ	6	0	r/rst	wake-up request	
	18	IRQ_VALID_FLAG_ERR	5	0	r/rst	Valid-flag error occurred	
	18	IRQ_EEPROM_ERR	4	0	r/rst	Single error has been corrected	
	18	IRQ_EEPROM2_ERR	3	0	r/rst	Multiple bit error occurred	
	18	IRQ_LOCK_AUX	2	0	r/rst	over-load lock of AUX line driver	
	18	IRQ_LOCK_COM	1	0	r/rst	over-load lock of COM line driver	
	18	IRQ_LOCK_OVT	0	0	r/rst	over-temperature LOCK of both line drivers, AUX and COM	
MON_DEVICE_TEMP	19		3:0	0	r	Device Temperature	
MON_STAT	20		7:0	0	r		
	20	MON_AUX_LOCK	7	0	r	Lock on AUX due to AUX-Overload	
	20	MON_COM_LOCK	6	0	r	Lock on COM due to COM-Overload	

Reg.-Name	Addr.	Bit-Field	Bit	Reset-Value	r/w	Comment	Reference
	20	MON_OVT_LOCK	5	0	r	Lock on COM + AUX due to Over-temperature	
	20	MON_STAT_AUX_HS_OVL	4	0	r	AUX-HighSide-OVL	
	20	MON_STAT_AUX_LS_OVL	3	0	r	AUX-LowSide-OVL	
	20	MON_STAT_COM_HS_OVL	2	0	r	COM-HighSide-OVL	
	20	MON_STAT_COM_LS_OVL	1	0	r	COM-LowSide-OVL	
	20	MON_STAT_OVT	0	0	r	Over-temperature	
MON_COM_LS_PEAK	21		7:0	0	r/rst	Longest COM-LS-Overload	
MON_COM_HS_PEAK	22		7:0	0	r/rst	Longest COM-HS-Overload	
MON_AUX_LS_PEAK	23		7:0	0	r/rst	Longest AUX-LS-Overload	
MON_AUX_HS_PEAK	24		7:0	0	r/rst	Longest AUX-HS-Overload	
MON_OVT_PEAK	25		7:0	0	r/rst	Longest over-temperature duration	
MON_POW_DETECT	26		1:0	0	r/rst	Power Monitor	Added in Rev B
	26	RESERVED	7:2	0	r/rst	RESERVED	
	26	MON_LINE_FAULT		0	r/rst	Line fault occurred	
	26	MON_UNDER_VOLTAGE		0	r/rst	Under voltage occurred	
Manufacture Use Only	27:30		7:0	0	r	Read returns 0	
PRODUCT_ID	31		7:0	ID	r	Allows to retrieve product and revision information	Added in Rev B

3.3.10. Interrupt and IC Lock Mode Control

3.3.10.1. Interrupt Handling

The INT_L pin provides indication functionality for a set of IC-internal exceptions. Once an exception had occurred, expressed as logic low of the INT_L signal, the actual cause can be evaluated by reading the IC's status register via the SPI interface. Depending on the condition – a reset of the exception by reading the corresponding status register can be performed.

The following exceptions are combined in the INT indication functionality:

- Lock caused by power fail detector (refer to chapter 3.5)
- Lock caused by COM-Overload (refer to chapter 3.3.10)
- Lock caused by AUX-Overload (refer to chapter 3.3.10)
- Lock caused by over-temperature (refer to chapter 3.3.10)
- EEPROM-single-bit-error (refer to chapter 3.3.7)
- EEPROM-2bit-error (refer to chapter 3.3.7)
- Valid-flag-cleared due to possibly corrupt EEPROM (refer to chapter 3.3.7)
- WURQ detected (refer to chapter 3.3.4)

Figure 3.14 illustrates the handling of the above mentioned exceptions and their monitoring. It also shows how to configure the interrupt (INT_L pin) and wake-up (WURQ_L pin) signal generation. Besides several exceptions concerning channel overload, die over-temperature and IO-Link specific wake-up situations the IC can also signal problems as regards the EEPROM.

Since the configuration registers get their content initially from the EEPROM, the data should be correct. The following described features make sure that no corrupt EEPROM data can cause unwanted IC configurations.

An EEPROM single bit error indicates a one bit problem in the content of the EEPROM. Since the EEPROM includes a self correction, one bit errors will be detected and corrected automatically. However, the indication shall trigger a rewrite[1] of the entire EEPROM content.

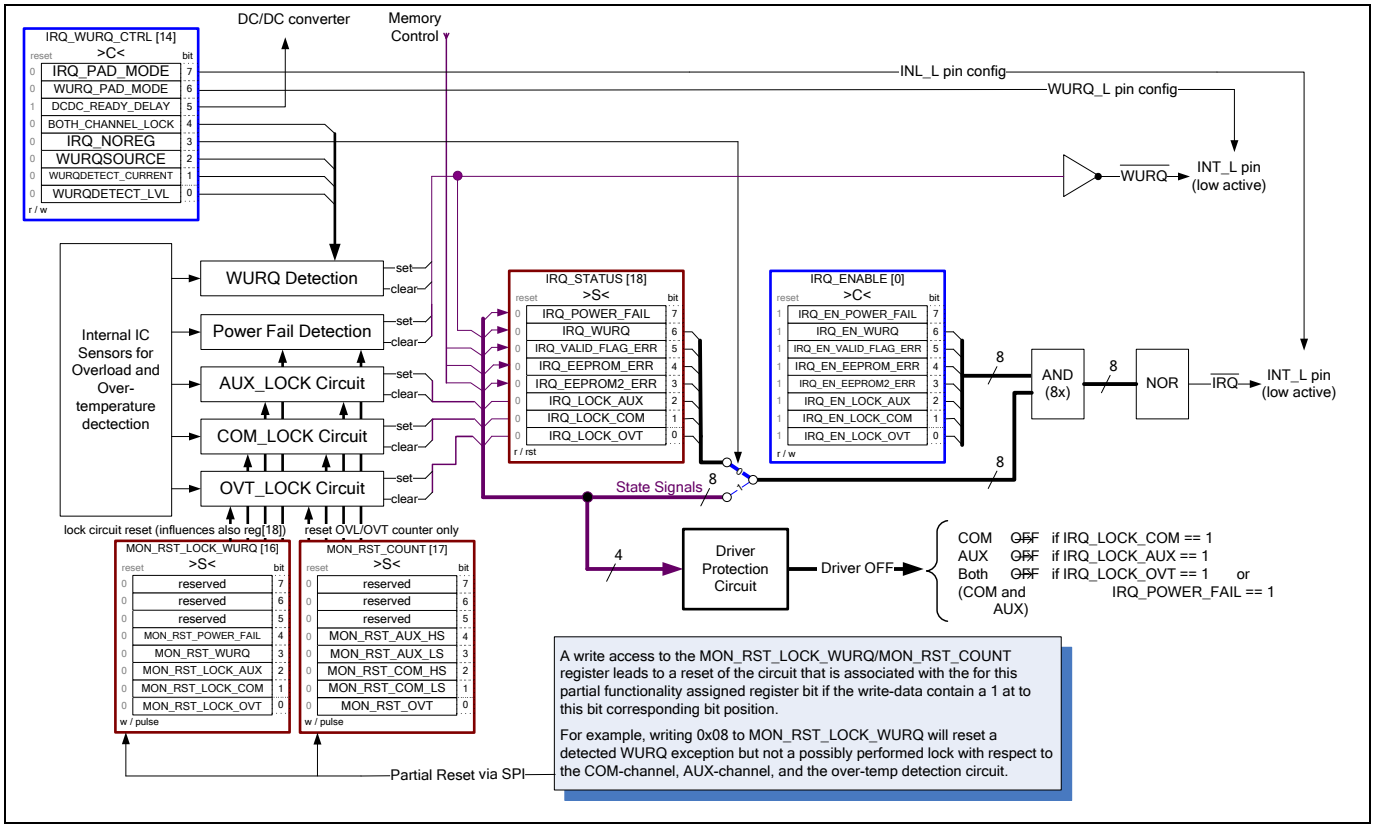
The EEPROM 2-bit error indicates a two bit problem in the content of the EEPROM. That error is not automatically corrected, so the content of the EEPROM can not be considered as correct. Thus a reprogramming is absolutely required.

The valid-flag is used to indicate that the last write access to the EEPROM was successful. If the valid-flag indicates a problem, then the chip configuration has to be regarded as faulty – no save IC function can be guaranteed. Rewriting of the entire EEPROM content is necessary. In case of a regular write process to the EEPROM is not completed, for instance by an interruption of the IC supply power within the ongoing write process, the valid-flag will indicate this as a problem because of the EEPROM content might be corrupt.

Besides the signalization of IC-internal exceptions the IN_L pin signals also the system reset state. The system reset state is indicated with active low on the INT_L pin.

[1] Note: IC versions ZIOL2xx2 do not allow any write access.

Figure 3.14 Interrupt (INT_L pin) and Wake-up (WURQ_L pin) Signaling[1]



The WURQ indication is a dedicated IO-Link functionality. A WURQ event is indicated if an over current situation with a determined timing – regarding to IO-Link Communication Specification happened on one of the output driver stages (refer to chapter 3.3.4, 3.3.10.1 and 8). A WURQ event will be created if there is either a timely limited (typical 80µs) different logical value between the logical output value of the driver and the received logical value from the line or an also timely limited (typical 80µs) over-current at the considered channel. It can be configured whether the first or the last or both conditions lead to a WURQ event.

3.3.10.2. IC Lock Mode Configuration and Monitoring

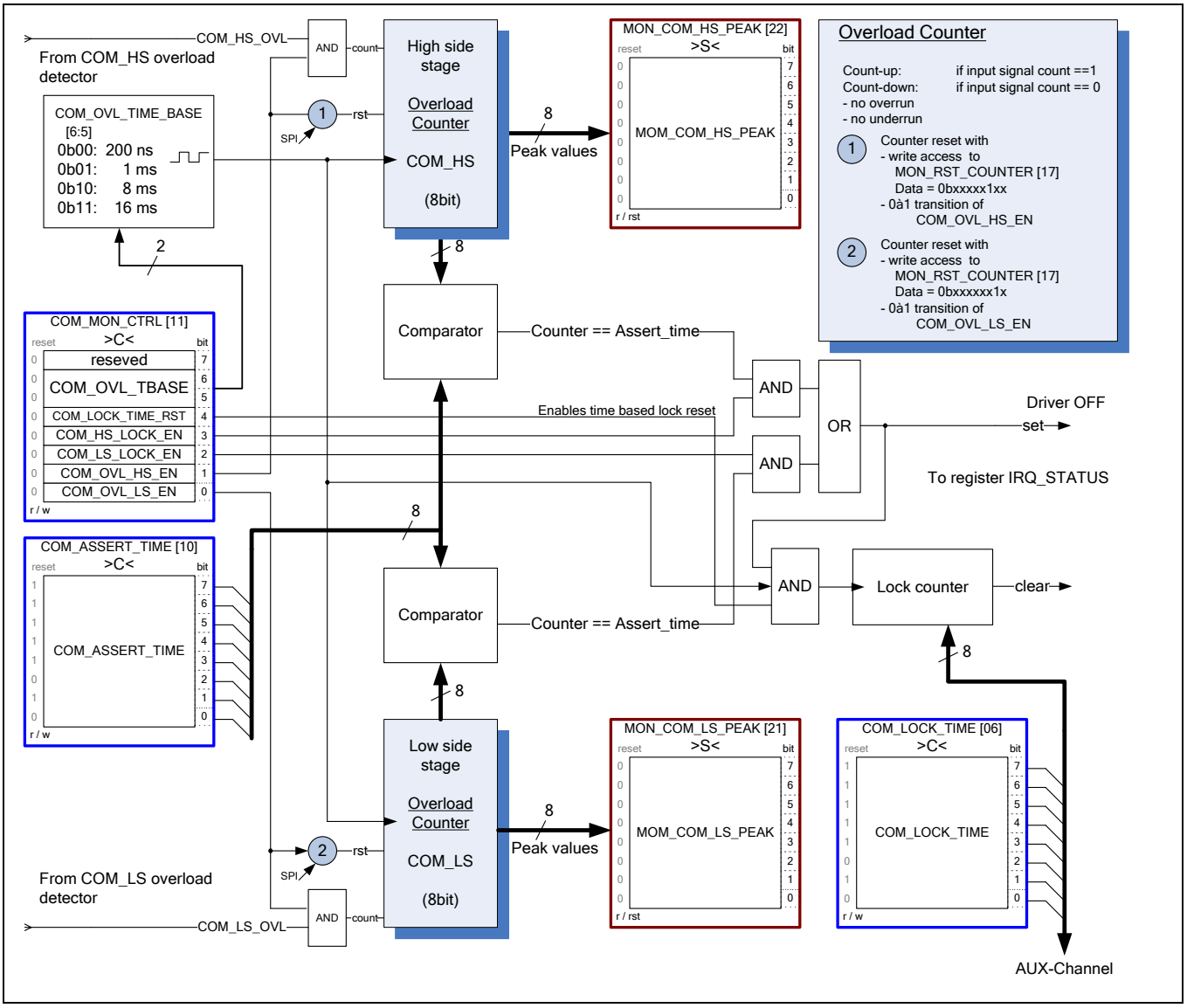
If the current through the output driver exceeds the configured limit, an exception will be generated. In addition to that and depending on the Ics configuration, the lock mode operation which corresponds to the overloaded channel can be performed (refer to Figure 3.15 and Figure 3.16). The above mentioned lock mode operation is activated if either one driver stage (HS or LS) or both drivers stages (HS and LS stage) are overloaded, means the output current exceeds the configured limit.

If the event occurs, the corresponding driver stage will be set to a save state, meaning it will be disabled.

The Lock mode configuration as shown in the following figures (Figure 3.15, Figure 3.16, Figure 3.17) is based on configurable current limits and time periods.

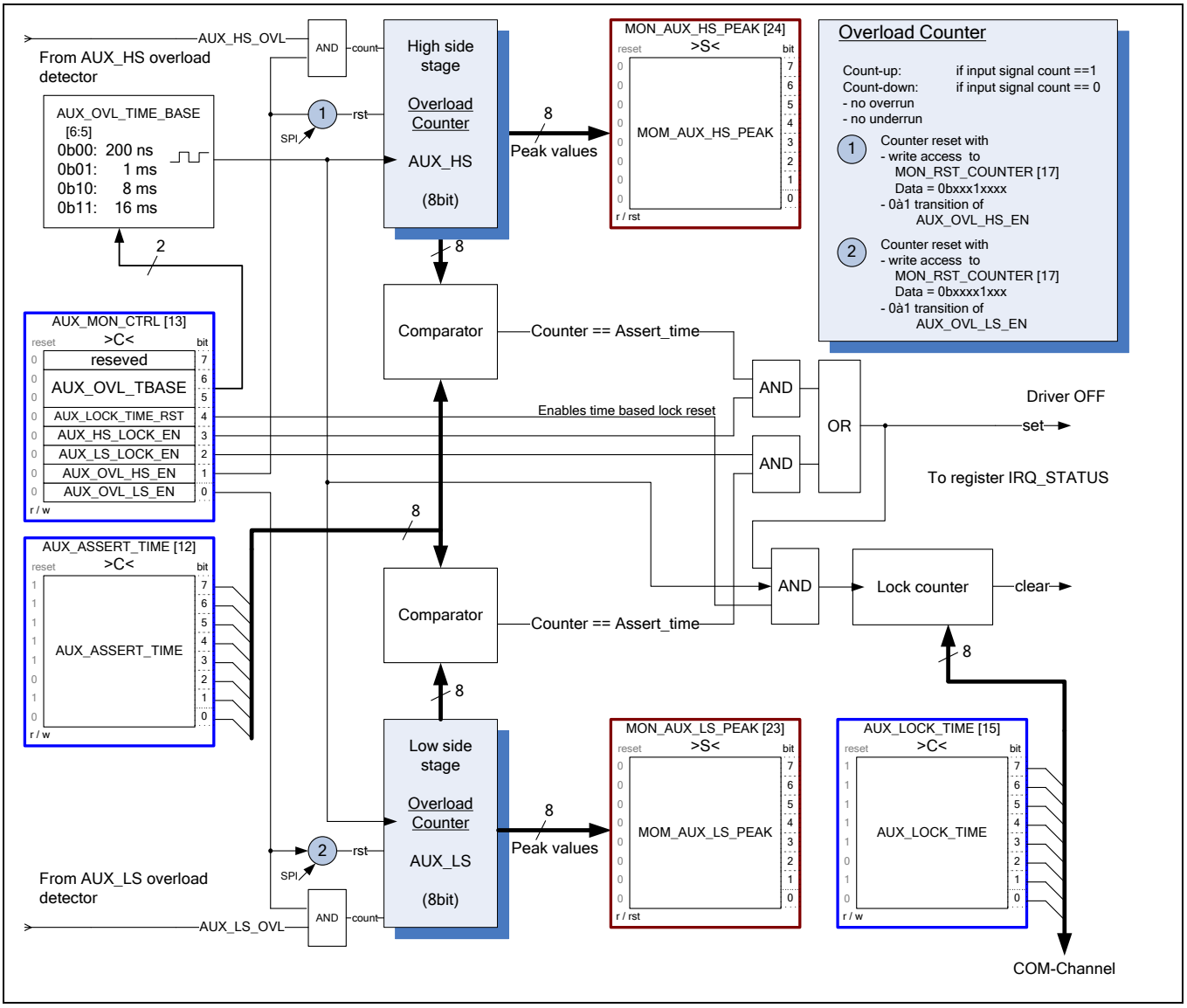
[1] The in this an in the following figures used symbols for the IC registers are explained in Figure 9.1.

Figure 3.15 COM Channel Lock Control[1]



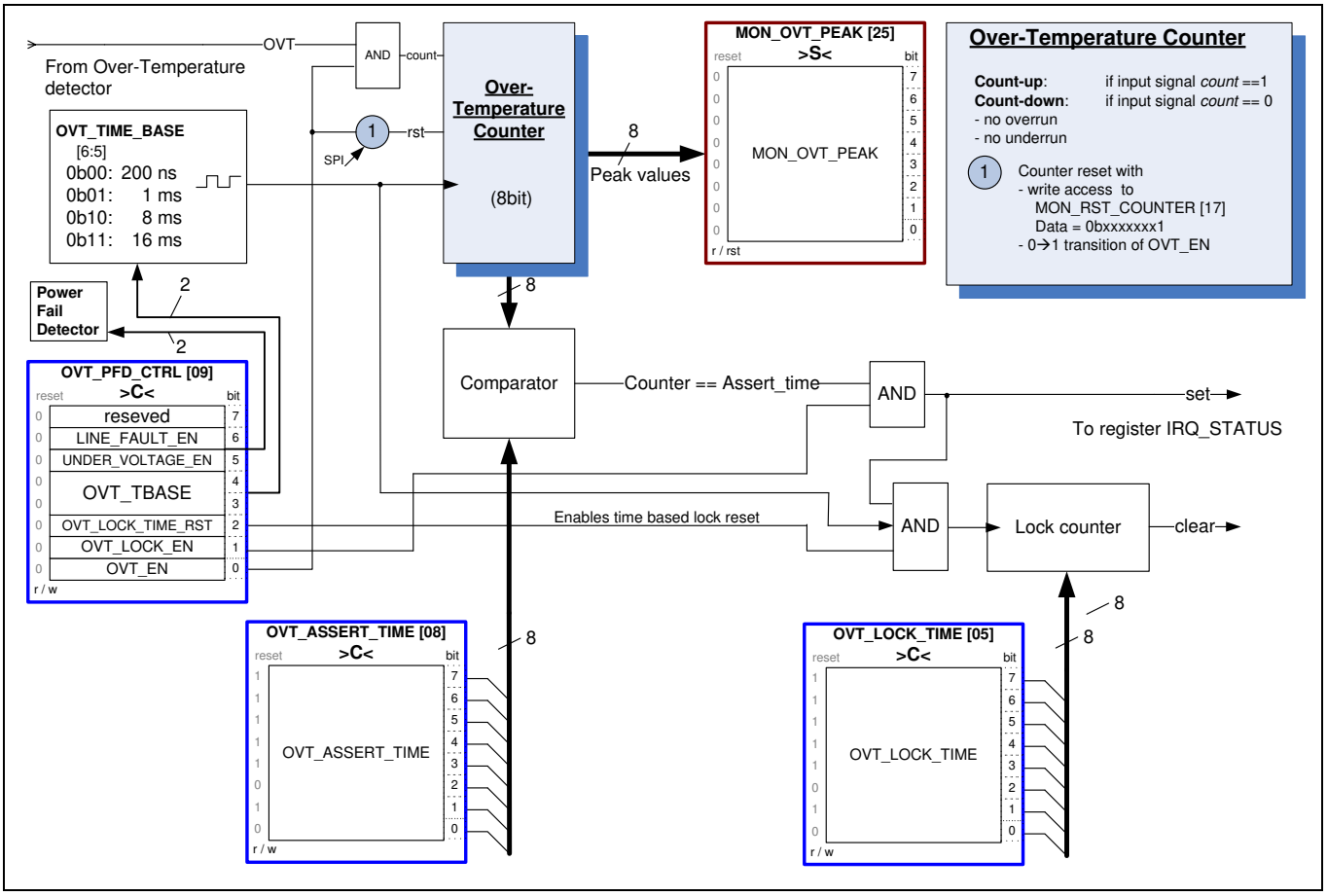
[1] The COM transmitter is only available inside the products ZIOL24xx/22xx

Figure 3.16 AUX Channel Lock Control[1]



[1] The AUX transmitter is only available inside the products ZIOL24xx/21xx

Figure 3.17 Over-Temperature Lock Control



The Lock caused by an over-temperature displays that the die temperature has reached a critical level. That forces a self protecting save state, it causes disabling the COM and the AUX channel by turning off all the HV driver output stages (Figure 3.17).

The IC configuration allows disabling the lock mode operation for overload exceptions from both channels (COM/AUX) and the exception from the die over-temperature detector. Since the lock mode operation prevents the IC to be destroyed due to physical stress situation, the disabling is not recommended or shall be done with particular caution only.

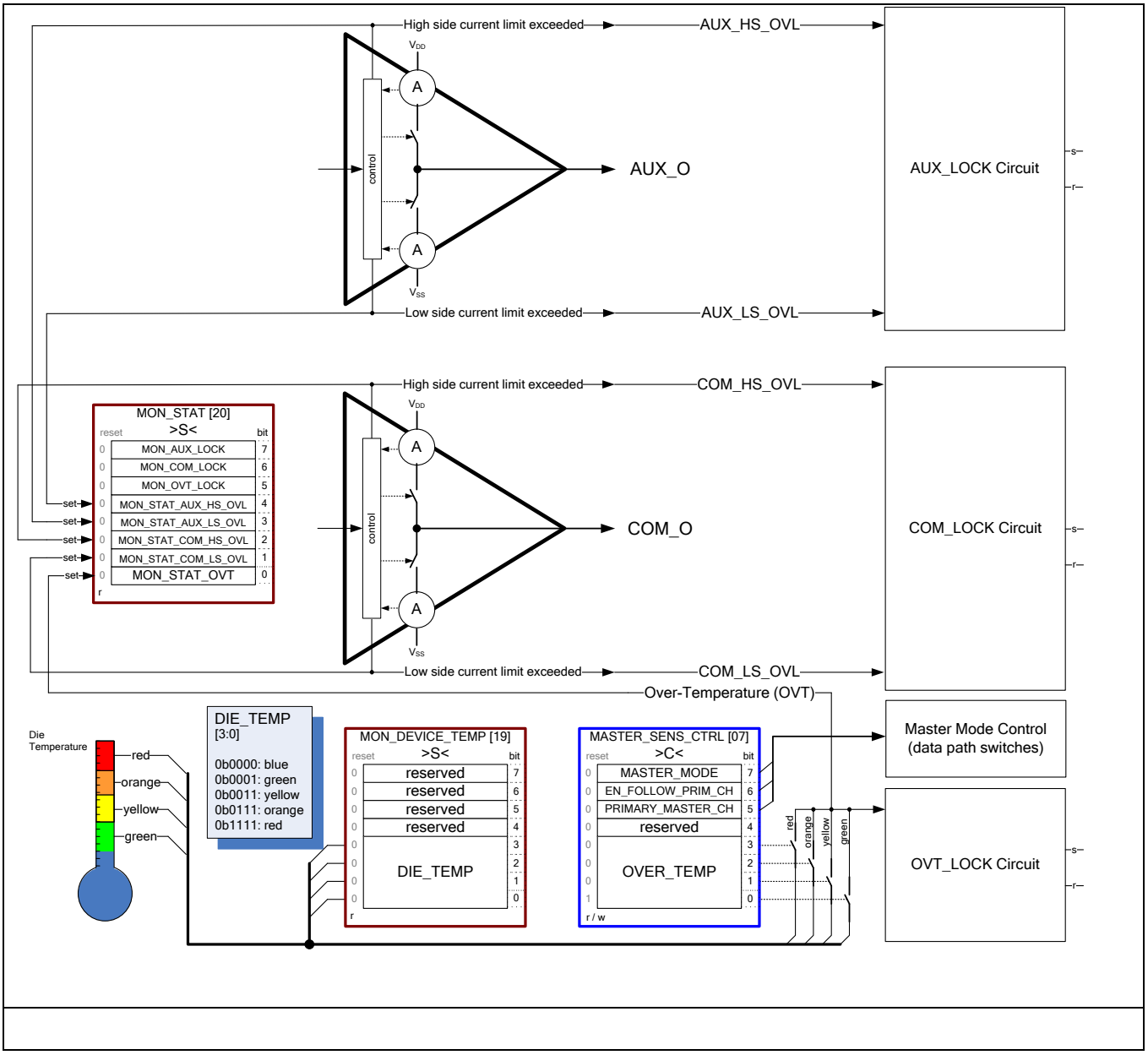
Disabled lock mode operations for the above mentioned building blocks will prevent generating the related contribution to the interrupt signal at the INT_L pin. However, those exceptions can be retrieved by reading the status register MON_STAT[20] (refer to chapter 3.3.9 and/or Figure 3.18).

Not depending on the lock mode operation the IC allows retrieving diagnostic information about the duration of an exception (peak values). The corresponding IC configuration that is required for retrieving such diagnostic data is illustrated above figures (Figure 3.15, Figure 3.16, and Figure 3.17).

3.3.10.3. Overload and Over-Temperature Configuration and Monitoring

The ZIOL2xxx is dedicated to work in harsh industrial environments. Several situations can cause serious stress to the IC which may lead to partly or complete damage of the IC. In order to minimize the impact of physical stress the IC generates exceptions if the HV drivers exceed the configured current limits or if finally the die temperature exceeds a certain configured value (for more details refer to chapter 3.3.11). The status register MON_STAT[20] reflects all currently occurred exceptions. Status register MON_DEVICE_TEMP[19] allows reading of the current die temperature.

Figure 3.18 Internal IC Sensors and related Overload and Over-Temperature Detection Circuits[1]



[1] The COM transmitter is only available inside the products ZIOL24xx/22xx and the AUX transmitter is only available inside the products ZIOL24xx/22xx, respectively

3.3.11. Die Temperature Measurement

Figure 3.18 illustrates the die temperature measurement of the ZIOL2xxx IC. The die temperature is measured with an on-chip sensor right in the center of the silicon die. Since there is one temperature sensor which has a certain distance to all the different locations that produce heat (due to dissipated electrical power), the sensor can only indicate a rough average value of the die temperature. This shall be considered in defining the alarm values for the over-temperature counter and in defining the over-temperature lock mode duration.

In combination with four comparators the temperature sensor circuit provides five temperature levels that correspond to certain temperatures as described in Table 3.8. The current die temperature (level) can be retrieved in reading the status register MON_DEVICE_TEMP[19].

Table 3.8 Temperature Sensor Levels

Temperature Level	Typical Trigger Temperature Value[1)]	Min. Trig. [2)]	Max. Trig. [2)]	Unit	MON_DEVICE_TEMP[19] value	Remarks / OVER_TEMP value for over-temperature exception
Blue	< 95			°C	0b0000	No comparator level reached
Green	> 100	95	105	°C	0b0001	0b0001
Yellow	> 110	105	115	°C	0b0011	0b0010
Orange	> 120	115	125	°C	0b0111	0b0100
Red	> 130	125	135	°C	0b1111	0b1000
Software-Test	n.a.	n.a.	n.a.	n.a.	0bxxxx	0b0000 [4)]

[1)] The mentioned typical values of IC properties shall not be considered as statistical guaranteed mean values.
[2)] The tolerance (deviation from the typical trigger value) is ±5°C. The deviation is for all trigger values the same. This means for example that in extreme situations all trigger levels equal the min. temperature or the max. temperature trigger value.
[3)] Setting configuration register[7][3:0] = 0b1111 will cause an over-temperature exception immediately. This setting is supposed to be used while software development and not supposed to be used in regular operation.
[4)] There is a deviating code 0b1111for the software test which valid for Rev A only.

The configuration-register OVT_TEMPERATURE defines what temperature level causes an over-temperature exception (Figure 3.18/Table 3.8). This configuration feature ensures a flexibility of the IC in various application cases.
Depending on the IC configuration an over-temperature can cause disabled HV drivers in order to prevent the IC against damage. Besides the DC/DC converter all other IC building feature will still function, also if a over-temperature exception has been detected[1]. Thus all control and diagnostic functions are still available if the IC is being overheated.

3.4. Smart Power Supply

The internal low voltage supply of the chip is 3.3V and generated by an on chip linear regulator. In order to decouple this voltage a capacitor needs to be connected externally. Since the regulator supports more load current than the IC requires itself, a certain current can be drawn by the external application (Table 2.2).

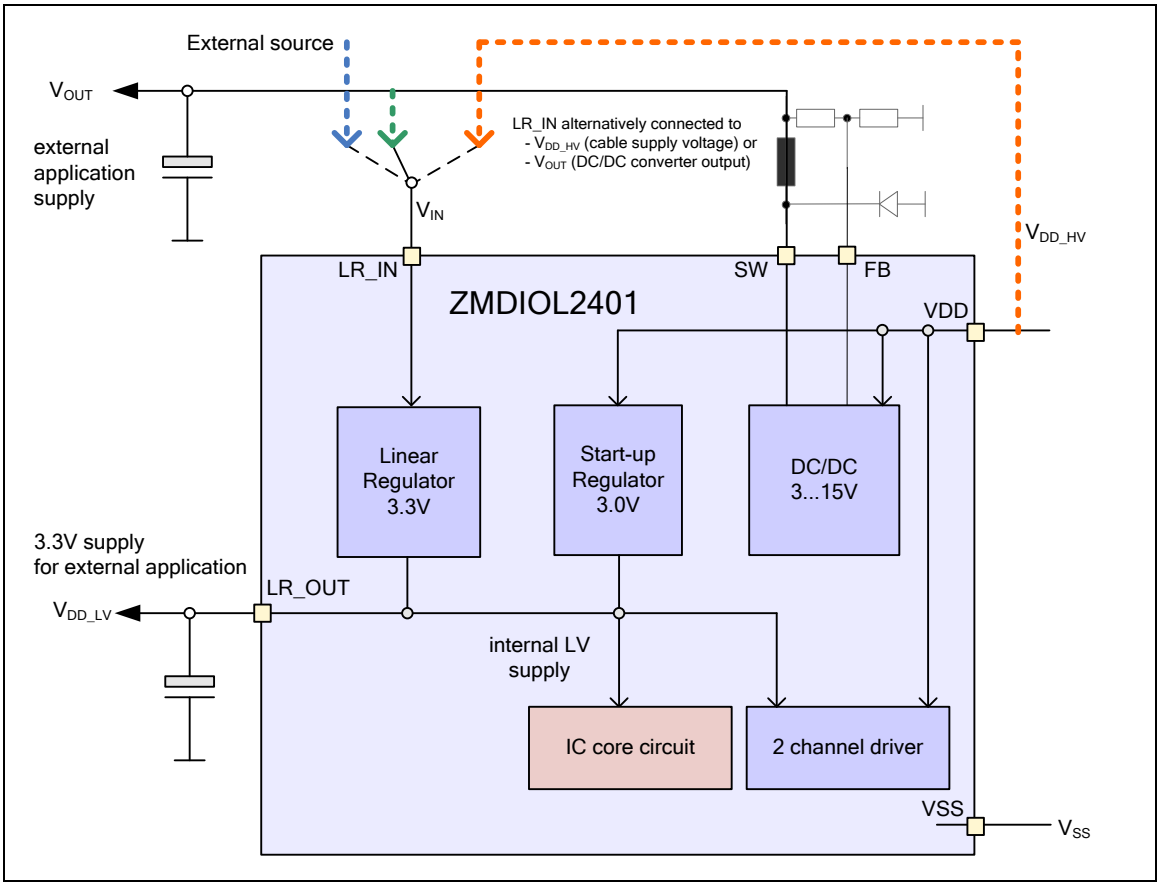
[1] This security shutdown of the DC/DC converter is not implemented in the IC revision A but prearranged for later easy implementation.

In order to reduce power dissipation, caused by the voltage drop above the regulating transistor, the regulator can be powered with an input voltage less than V_{DD_HV}. If for example the on-chip DC/DC converter is in use and its output voltage is set to at least 5V, then the linear regulator can be powered with this output voltage.

The electrical characteristics are shown in the chapter “operating conditions” (chapter 1).

The following block schematic (Figure 3.19) shows the principle of the low voltage generation in conjunction with a possible usage of the on chip DC/DC converter. For more information about required external components refer to chapter 4.

Figure 3.19 Low Voltage Supply Concept



3.5. The Power Fail Detector

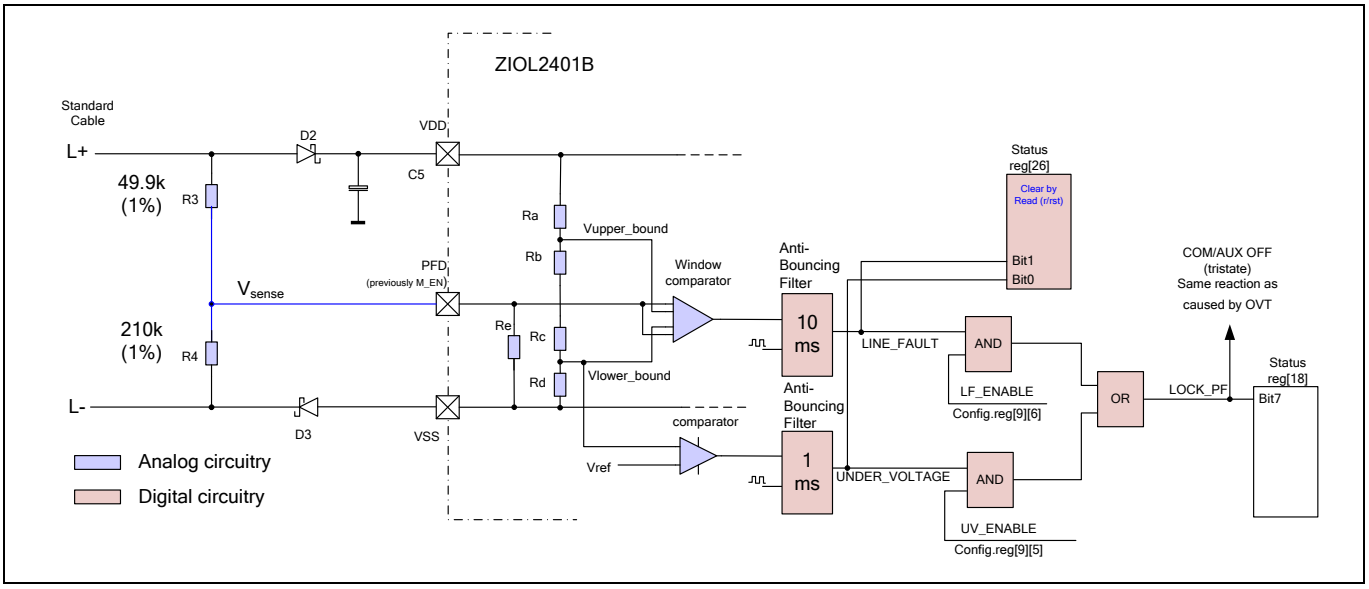
3.5.1. Overview

The Power-Fail detector function is split into two tasks. The first task is the “Line-Fault” (LF) detection which shall recognize a situation in which the ZIOL2xxx is not powered regularly. This situation can happen if for instance the wiring between device and host port is not performed in the right way (interchanged wires, broken wires).

The second task is the “Under-Voltage” (UV) detector which monitors the supply voltage at the VDD pin of the ZIOL2xxx. The purpose of this detector is ensure a proper working of the HV drivers COM and AUX which is not guaranteed if the supply voltage at VDD drops below the allowed minimum value.

Figure 3.20 illustrated the working principle of both the LF and the UV detector in combination with the further processing to the detected events (LINE_FAULT and UNDER_VOLTAGE). Based on the IC configuration (LF_ENABLE, UV_ENABLE flags) each event (or both events) may activate the lock for both channels exactly for the period the respective event is present. The new status register [26] allows diagnosing what event is present or was present in the past.

Figure 3.20 PFD Working Principle



3.5.2. Line-Fault Detector

The Line-Fault (LF) detection feature assumes the utilization of both channels in device mode. In the case one channel is used only, the number of detectable failures be reduced accordingly. For more information about detectable failures, please refer to the Appendix C.

The optional (configurable) detection of the situation of an abnormal power supply of the IC will be achieved by a ratiometric working voltage sensor. As sensor input works the PFD pin (formerly M_EN) in combination with two

"sense" resistors which are interconnected to the L+ and L- pin of the sensor/actuator device. Those resistors provide a voltage divider. The so downscaled supply voltage (voltage at the pin PFD) is compared with the output voltage of an IC-internal voltage divider. In case of abnormal power supply of the IC (refer to Figure 3.20) a window comparator will detect this situation as LINE_FAULT event. The further processing of the LINE_FAULT event depends on the LF_ENABLE configuration flag (Figure 3.20). A Power-Fail Lock (LOCK_PF) will be generated only if the duration of the so detected abnormal power supply (or break of power supply) is longer than 10ms (Figure 3.20).

3.5.3. Under-voltage Detector

The IC has a Power-on-reset circuit which puts the IC in RESET state while power-on, or if the internal (core) supply voltage of 3.3V (voltage at LR_OUT) drops below a critical value. For example with VDD = 5V the internal 3.3V power supply may not be jeopardized thus the IC control will work as usual. In this situation the under-voltage detection shall protect the HV driver which may not work correctly with VDD < 8V and which might have a chance to get damaged in this situation. If configured the Under-Voltage detector will avoid this situation by locking both driver channels.

3.5.4. Channel Locking and Interrupt Generation

As mentioned in chapter 3.5.1 both channels can be locked if one or both of the events LINE_FAULT and UNDER_VOLTAGE occur. In this case the resulting signal LOCK_PF (refer to Figure 3.20) will be stored in the IRQ_STATUS status register [18][7] (refer to Table 3.7). Depending on the IRQ_ENABLE configuration register [0][7] or on IRQ_NOREG (configuration register [14][3]) and interrupt (pin INT_L) can be issued.

3.5.5. Downward Compatibility

The introduction of the PFD in IC Rev B goes in parallel with the conversion of the formerly master enable (M_EN) pin to a voltage sense pin (PFD pin). Therefore the master enable /disable function must be defined by using a configuration flag. Since old PCB designs are using the M_EN interconnection either to VDD/LR_OUT or VSS (enabling/disabling the master functionality), the LF feature cannot be used.

3.6. DC/DC Converter[1]

3.6.1. Principle of Operation

The on chip DC/DC converter is a constant frequency (2.5MHz) buck converter with an adjustable output voltage. The wide input voltage range of 8V to 36V, a minimized output ripple (< 25mVpp), and the maximum output current of 50mA make the converter suitable for standard sensor/actuator applications. The output voltage can be adjusted with an external voltage divider.

The electrical characteristics are shown in the chapter "operating conditions" (chapter 1).

The DC/DC converter can be disabled if the application does not require this functionality. In order to do this the FB pin shall be connected to the 3.3V LV power supply output (pin LR_OUT).

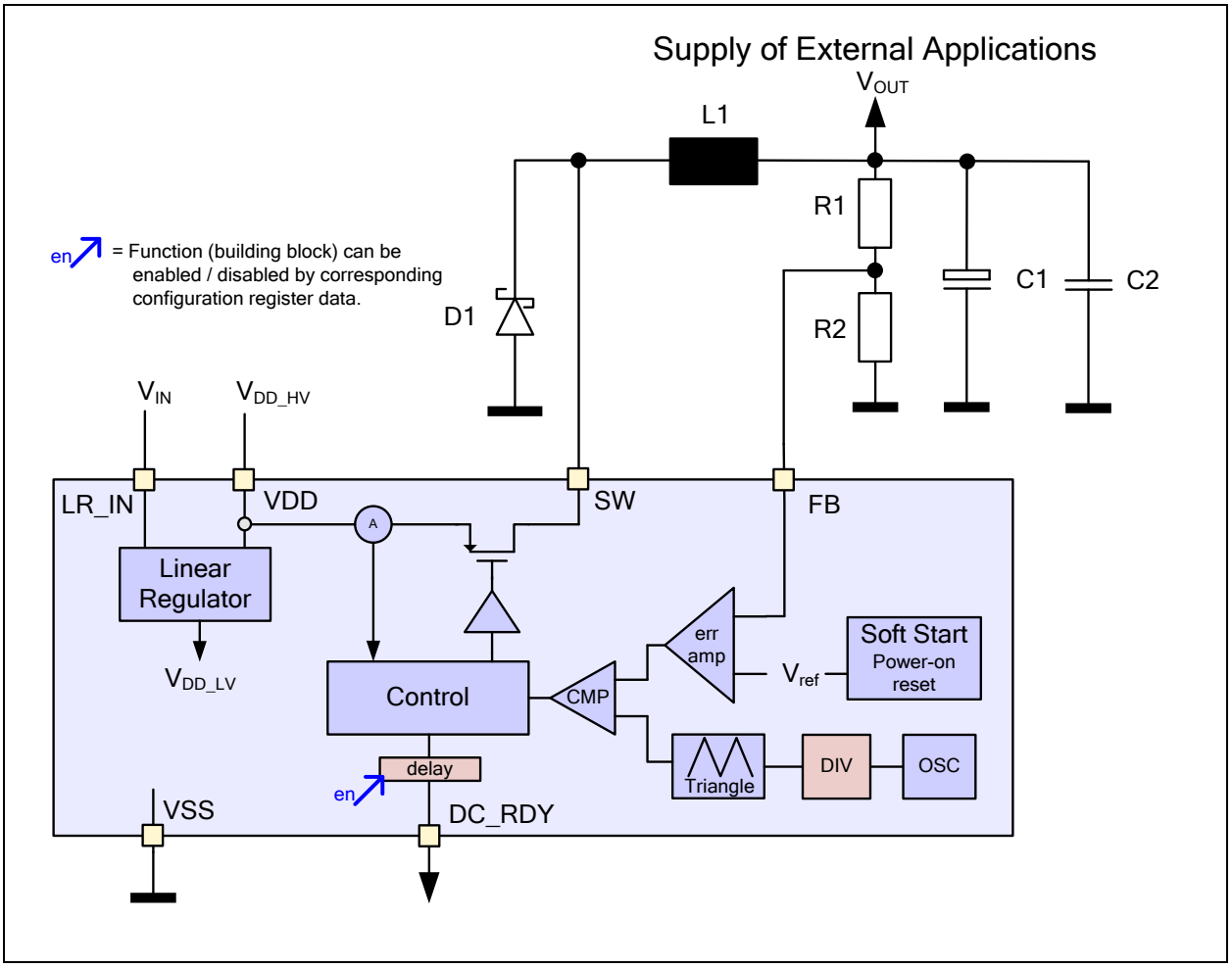
[1] Only available with IC versions ZIOL240x/220x/210x

The converter runs independently from the two driver channels (COM/AUX) and their digital control state machine. A reset has no influence on the DC/DC converter.

3.6.2. Principle of Operation

Figure 3.21 shows the working principle of the DC/DC converter. Required external components are described in chapter 3.6.3.

Figure 3.21 DC/DC Converter in Principle



The DC/DC converter senses the output voltage divided by the resistors R1 and R2 at pin FB. The difference between this signal and the reference voltage is amplified and then transformed into a PWM signal by comparing it with a triangular waveform. The PWM signal now enables and disables the output transistor. This results in a pulse length modulated signal with an amplitude of V_{DD_HV} and $-V_D$ (the Schottky diode forward drop) which is then been filter via a second order LC filter to generate the output voltage V_{OUT}.

The capability of the output driver of the DC/DC converter is limited to 200mA (refer to parameter I_{PK} in Table 2.3). Operating at this limit must be limited in time. Since the DC/DC is not shut down when the die-temperature exceeds the configured limit, the application circuit hardware and software design must make sure that no IC damage can occur.

In the start-up phase of the IC (power-on-reset) the DC/DC converter control moves to a soft-start regime which limits the current that charges the capacitor at the V_{OUT} voltage. This is done by increasing the reference voltage and thus the output voltage follows that reference in a controlled manner.

The DC_RDY pin provides information on the state of the output voltage. If the DC/DC converter is overloaded (V_{OUT} drops below 85% of the nominal value), DC_RDY is low. In addition to that DC_RDY is kept on logic low level if the IC is in power-on-reset. In this power-on-reset case and only in this case the converter is restarted.

The rising edge of DC_RDY signal can be delayed by 50ms (+/- 5%). This delay function is configurable with bit 5 of the configuration-register IRQ_WURQ_CTRL[14] (refer to Figure 3.14). The IC manufacturer default value for this bit is '1' thus the delay function is enabled by default. If DC_RDY is low during re-configuration of the IC and the delay is not yet finished, it stays low. The falling edge of the DC_RDY signal will not be delayed thus is not affected by bit 5 of the configuration-register IRQ_WURQ_CTRL[14].

3.6.3. Dimensioning of external Devices

The output capacitor C1 acts as filter capacitor. It has to have low equal series resistance (ESR) thus a ceramic capacitor with a 10µF capacitance has to be chosen. The ESR has influence on the output ripple. The higher the ESR the higher is the output ripple. The self-resonant frequency of the capacitor shall be as high as possible. It is possible to have a 100nF block capacitor (C2) in parallel to C1 to increase its frequency behaviour.

The Schottky diode acts as freewheeling diode. Therefore, it shall have a low voltage drop to increase efficiency. A low parasitic capacity or a fast reverse recovery time increase the efficiency by preventing a large shoot-through current through the output transistor and the diode when switching on the transistor.

The voltage divider provides the feedback voltage for the DC/DC converter. R2 shall be ~10kΩ. R1 can be calculated by

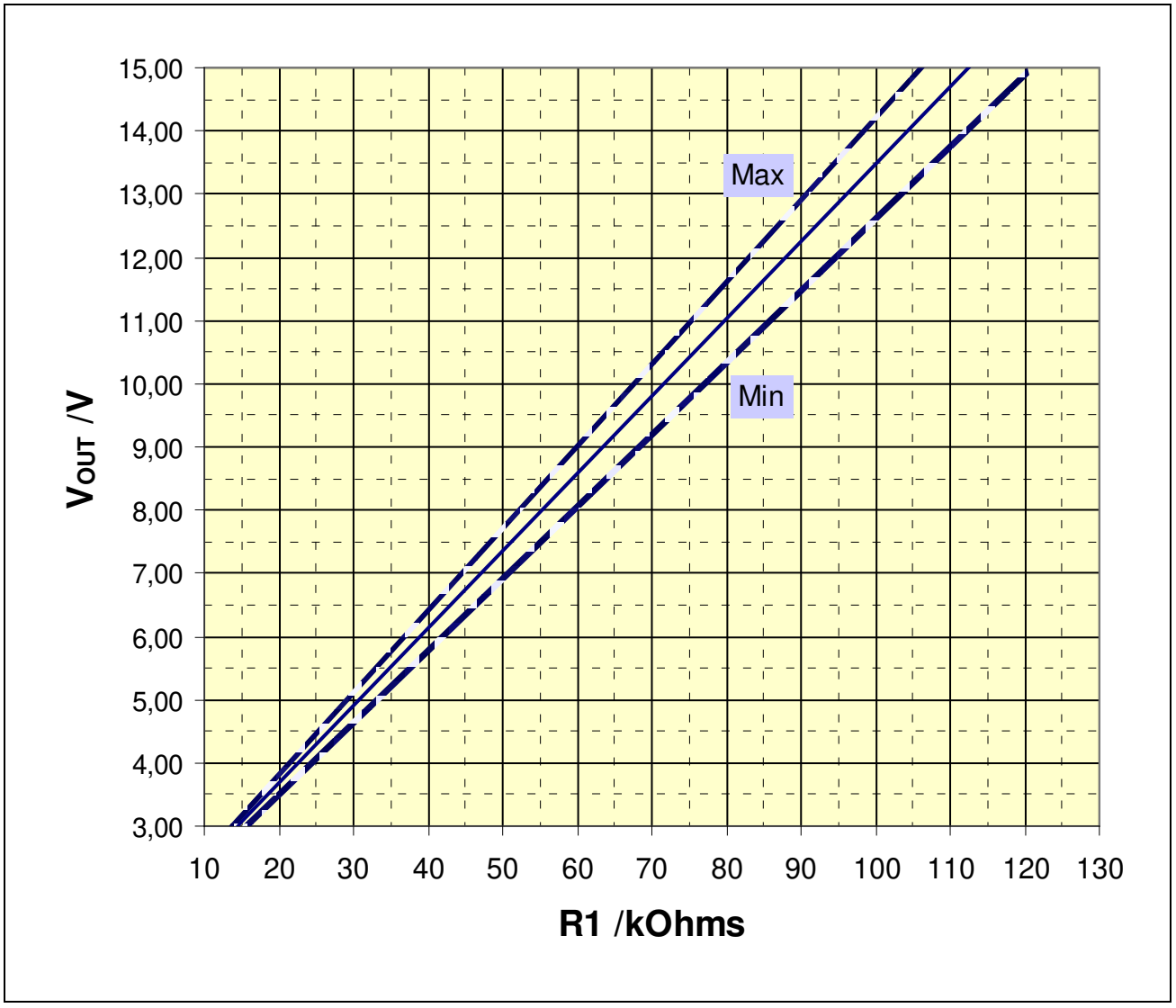
$$R_1 = R_2 \cdot \left(\frac{V_{OUT,set}}{1{,}225V} - 1 \right).$$

The tolerance of the resistors affect the tolerance of the output voltage thus resistors with 1% tolerance are preferred. Figure 3.22 illustrates the DC/DC converter output voltage (including its tolerance range) as function of R1 for R2 = 10kOhms.

Table 3.9 Examples for the resistors R1 and R2 using E96 resistor series

$V_{OUT,set}$	R1	R2
3.3V	18.2kΩ	10.5 kΩ
5V	38.3 kΩ	12.4 kΩ

Figure 3.22 DC/DC Converter Output Voltage as Function of R1 (R2 = 10kOhms)



The inductor stores energy when the output transistor is conducting and releases the energy if the transistor is switched off. For most applications a 10µH inductor is sufficient. To reduce the electromagnetic interference or to reduce the ripple voltage of the output voltage, the required inductance is calculated by

$$L_{\min} > \left(1 - \frac{V_{OUT,set}}{V_{DD\_HV,\max}}\right) \cdot \frac{V_{OUT,set}}{2 \cdot f_{Sw} \cdot I_{OUT,\min}},$$

where $I_{OUT,min}$ is the lowest output current, $V_{DD\_HV,max}$ is the highest input voltage and f_{Sw} is the switching frequency of the DC/DC converter.

3.6.4. PCB Layout considerations

To achieve optimal parameters for the DC/DC converter (e.g. efficiency or ripple voltage), attention has to be given to the PCB layout. Figure 3.23 shows the DC/DC converter, its external elements and two high frequency loops. The length of each loop has to be as short as possible. Furthermore, the distance between SW and FB has to be as large as possible to decrease the interference. It is recommended to have ground planes in between each signal line.

Figure 3.23 High frequency critical loops of DC/DC converter for PCB layout

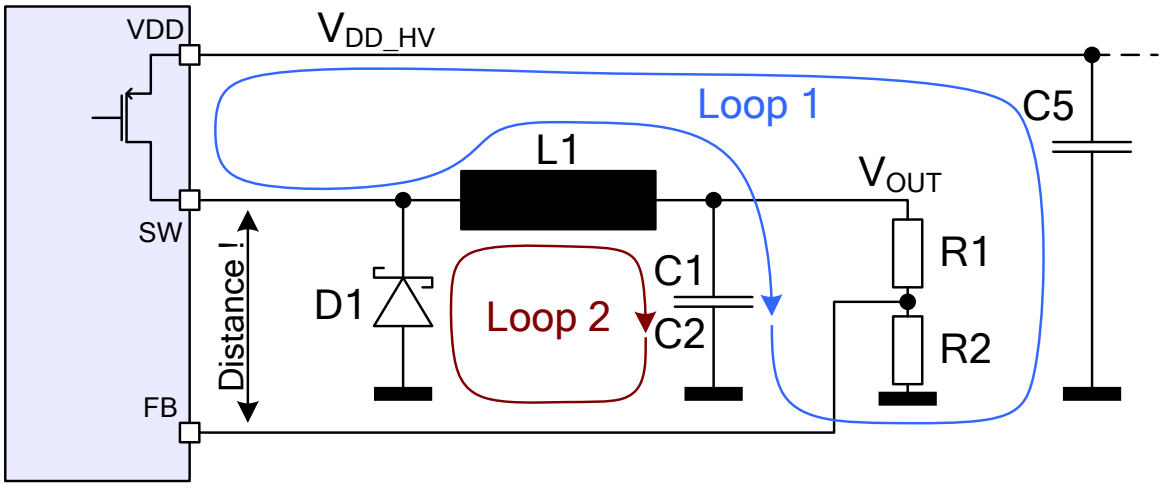
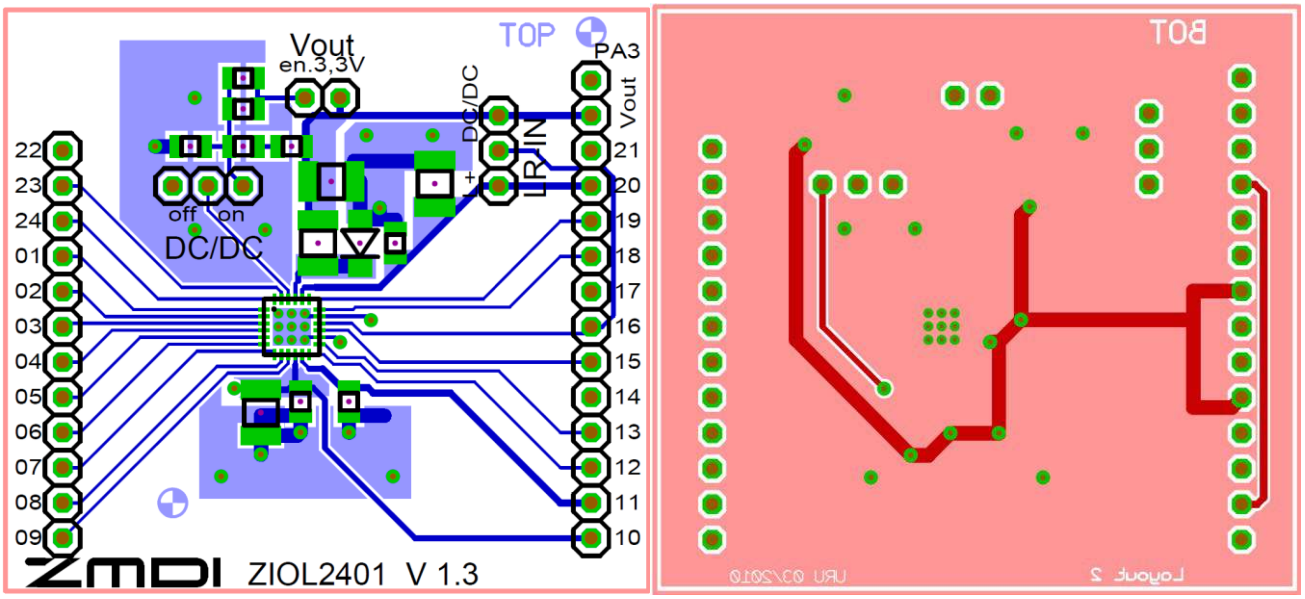


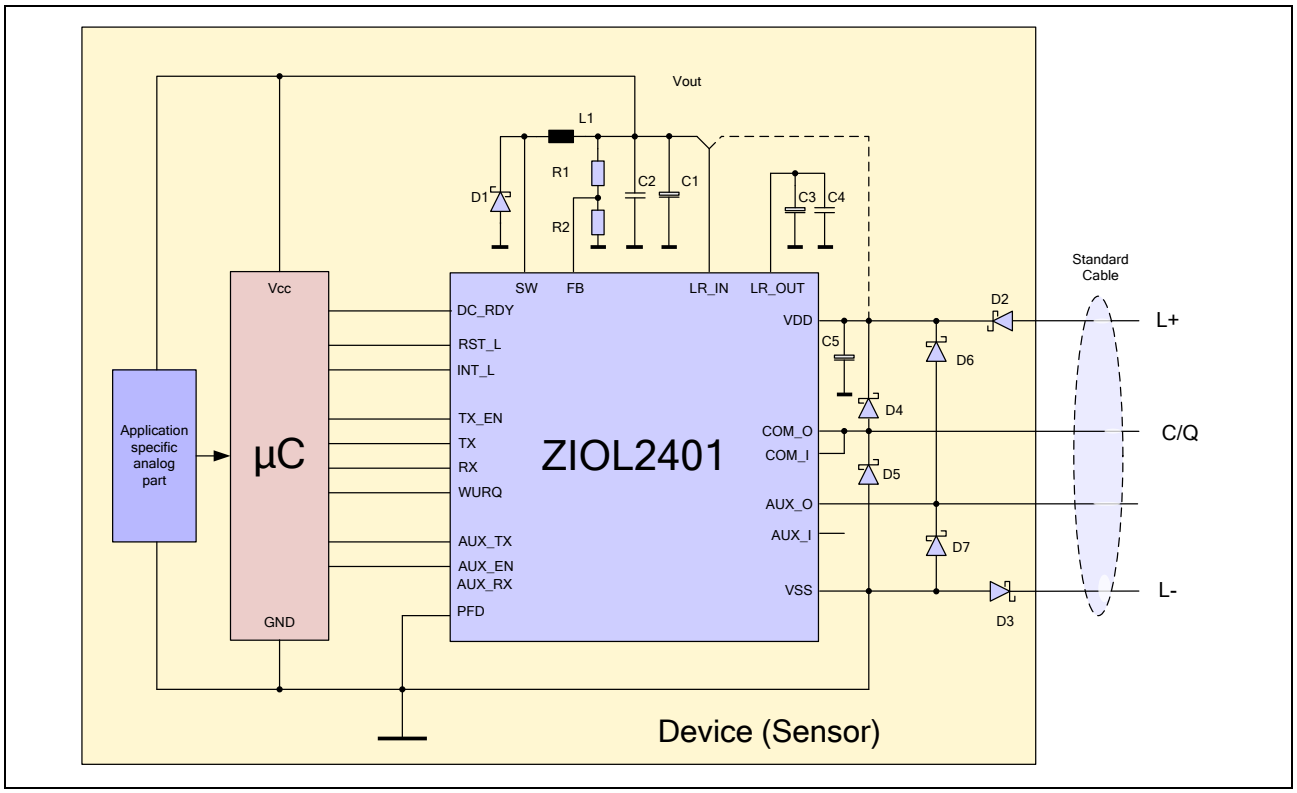
Figure 3.24 PCB layout of Evaluation board as an example



4 Application Information

ZIOL2xxx application circuits contain usually external components, which are required for overvoltage and reverse polarity protection. Table 4.1 provides a summary about requires components. The in the following figures used external components, in particular the special component type and it parameters are mentioned in this table.. The following schematics show standard application circuits in principle with the focus to the interface part of the physical level transceiver performed by the ZIOL2xxx Ics..

Figure 4.1 Simplified Application Circuit with the ZIOL2xxx in Device Mode

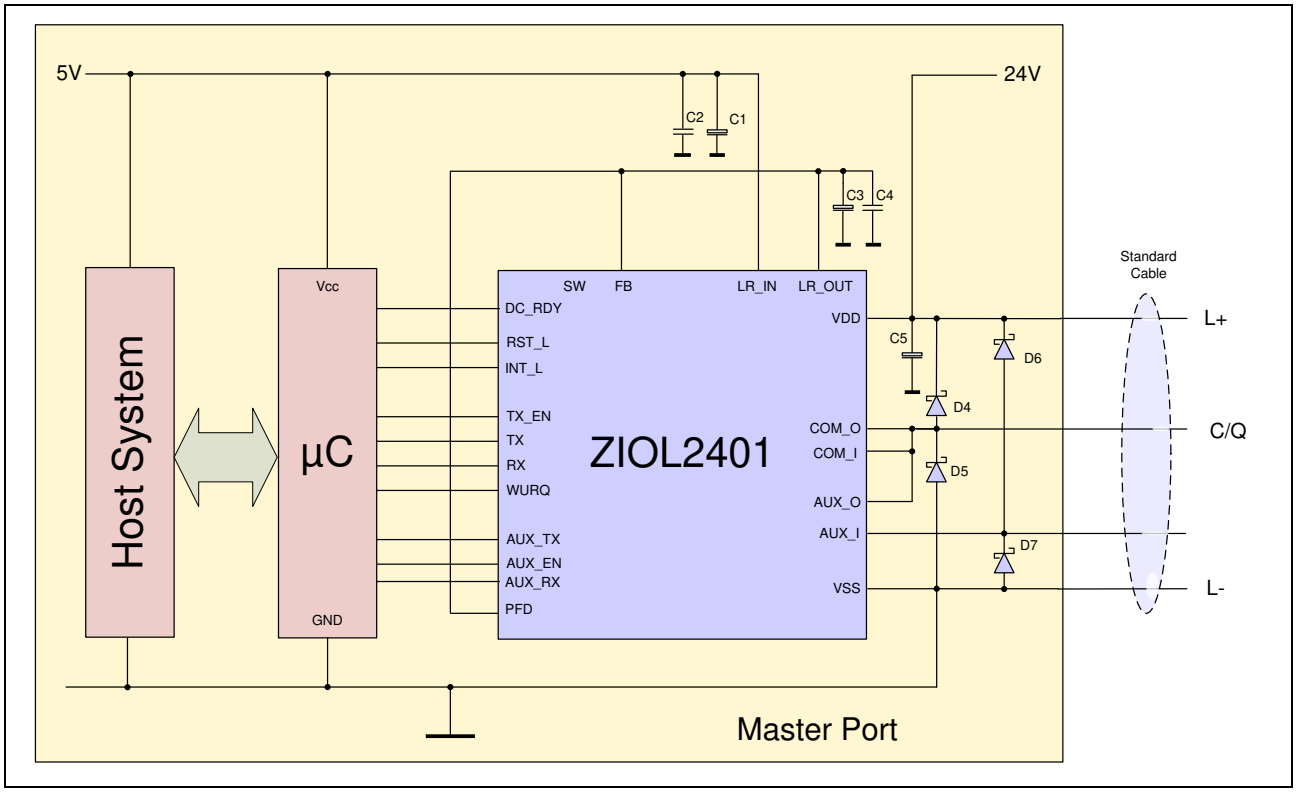


In principle an IO-Link device cable interface (or the interface for a standard sensor/actuator) requires four (one channel) or six (Two channels) protection diodes. The diodes D4 … D7 are fast clipping schottky diodes. Those highly recommended diodes damp signal overshoots and make sure that in IO-Link device applications the device can detect supply power failures as illustrated in Figure 4.3. D2 and D3 provide the reverse polarity protection for the device unit as shown in Figure 4.1.

Since there is normally no chance in IO-Link master applications to apply the supply voltage in reverse manner, the reverse polarity protection diodes D2 and D3 can be omitted in master applications (Figure 4.2). With respect to Figure 4.1 and Figure 4.2 the PFD pin (prior IC Rev B called M_EN pin) is connected to power or ground as it was required in using Rev A. Using this way of interconnections of the PFD pin requires disabling of the line-fail

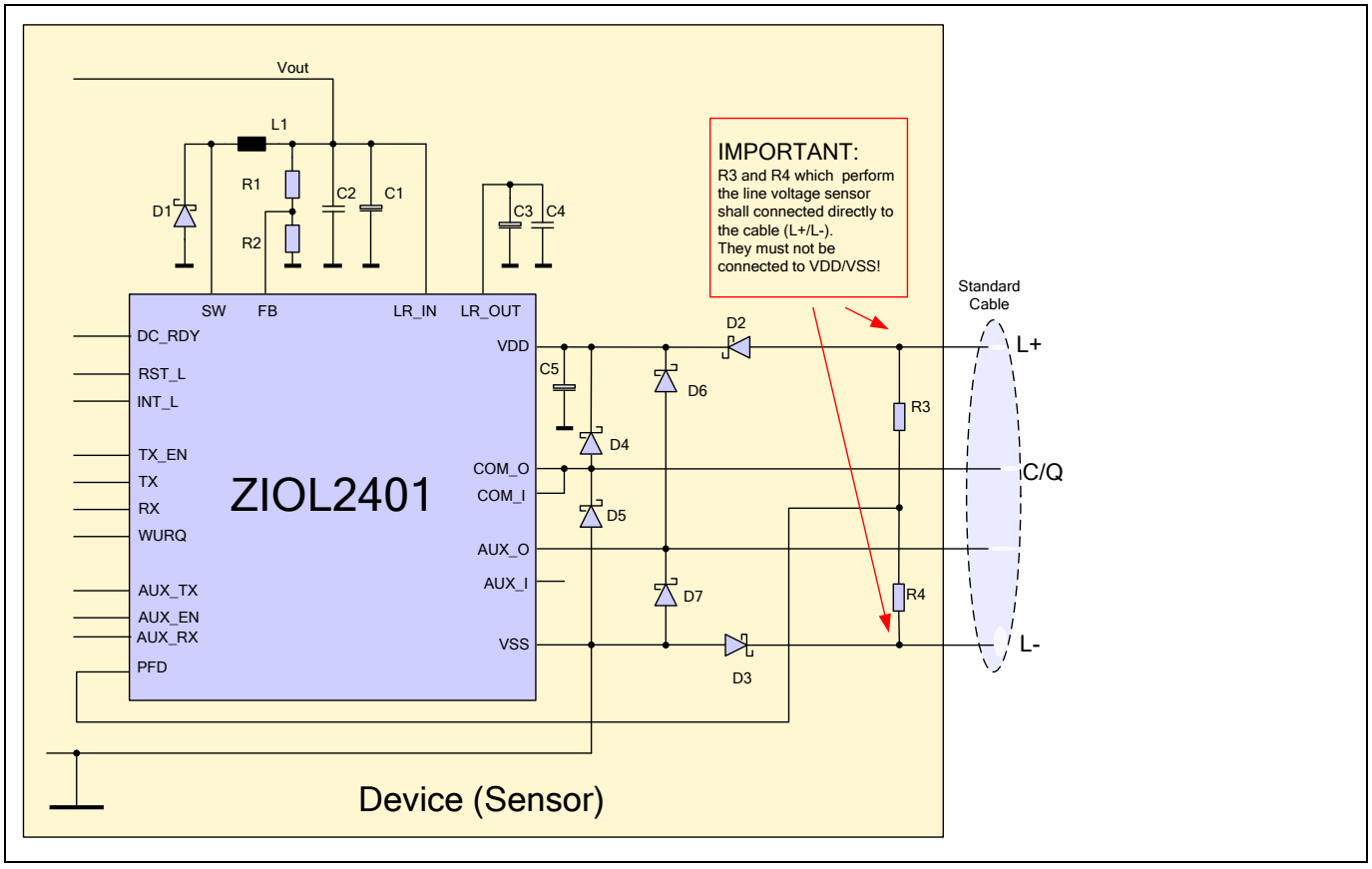
feature (refer to chapter 3.5). In case the line fail feature is intended to be use the PFD shall be connected to a voltage divider as described in chapter 3.5 or illustrated in Figure 4.3.

Figure 4.2 Simplified Application Circuit with the ZIOL2xxx in Master Mode



In case of (IO-Link) device applications the IC might be powered not correctly via the L+/L- line. The circuit in Figure 4.3 illustrates how to detect this power fail situation by using a voltage divider as “sensor”. Since the voltage at the PFD pin is compared with an internal voltage divider resistors with low tolerace range (<= 1%) shall be used.

Figure 4.3 Power Line Fail Detection



The PCB layout design requires considering several recommendations. In particular the placement of decoupling capacitors and the placement external components that perform the DC/DC converter circuits shall be done carefully. Recommendations are:

- Low resistive and low inductive ground interconnections due to metal ground areas surrounding the IC or/and using a special “Ground” PCB layer.
- The wiring of the channel driver output shall consider that the wires are designed for currents up to 500mA (depending on the IC configuration) and in combination with that wiring for VDD and VSS shall designed for currents up to 1A.
- Decoupling capacitors related to the IC pins VDD and LR_OUT (and LR_IN if applicable) shall placed as close as possible to the IC pin.
- The DC/DC converter requires an external Schottky-diode as free-wheel diode. Its anode shall be interconnected to the SW pin. It is important that its cathode has good (short) ground connection. With respect to all to the SW pin interconnected devices (free-wheel diode and inductor L1) all wires have to be kept as short as possible. Moreover, the PCB design shall make sure that the parasitic coupling between the node belonging to the SW pin and the node belonging to the FB pin of the IC is minimized.
- The voltage divider R1/R2 shall interconnected to the FB (feedback pin) in that way that the electromagnetic coupling to the wire interconnected to the SW pin is low as possible.

- In order to achieve an optimal heat distribution form the IC to the environment it is strongly recommended to place via's underneath the QFN package. An example as regards this PCB design detail is illustrated in Figure 4.4 (2-layer PCB example). Please refer to applications notes of the package manufacturer AMKOR for more details how to place cooling via's underneath the IC package (please visit the link mentioned in chapter 8, [4]).

Figure 4.4 PCB Layout Recommendations

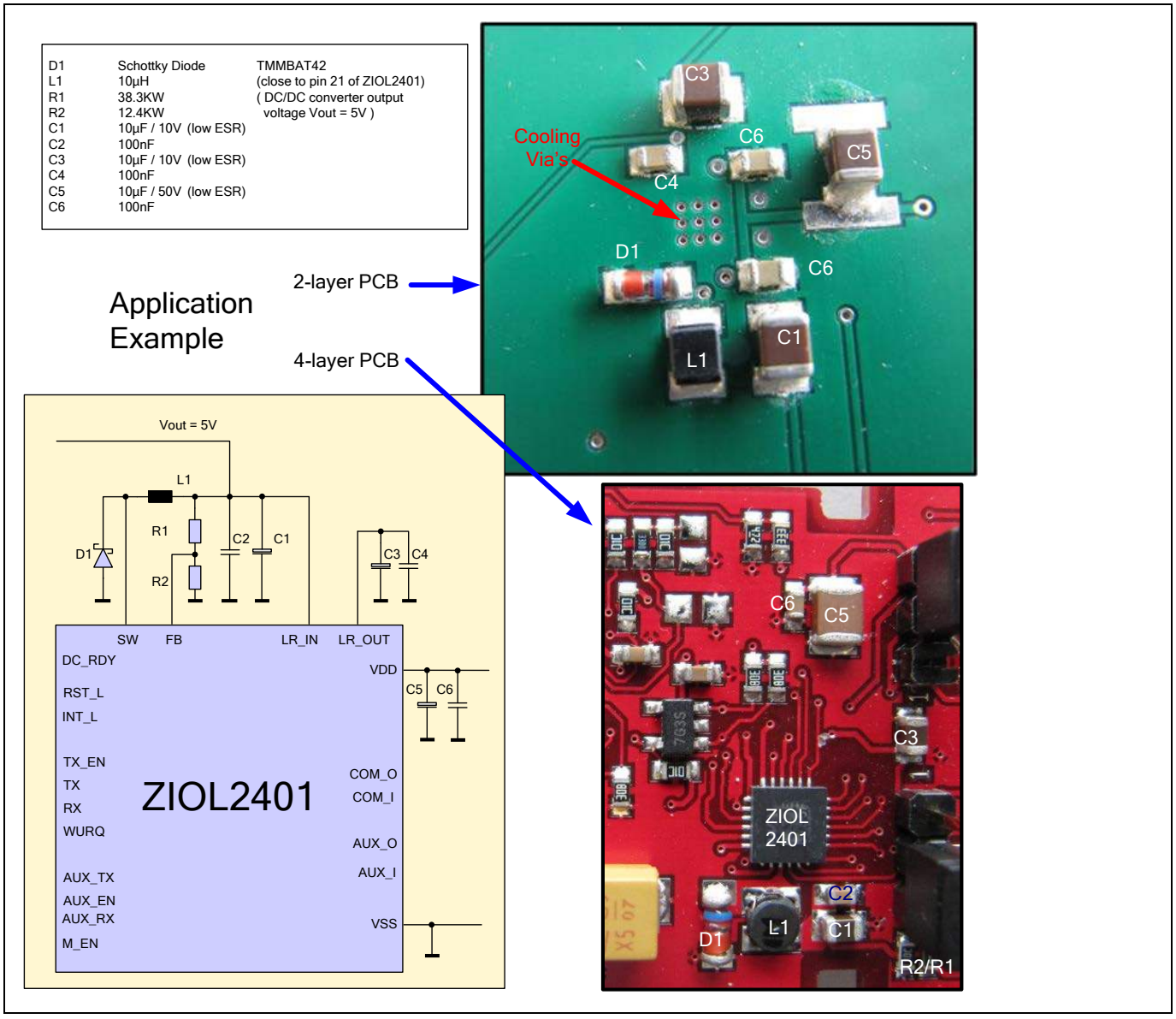


Figure 4.4 shows two layout variants as regards the component placement in the case the DC/DC converter is used in the application circuit. The in this figure shown PCBs are the PCBs of the ZIOL2xxx application kits (ZIOL2xxx LabKit: 2-layer-PCB/ ZIOL2xxx USB-Stick: 4-layer-PCB). The complete PCB documentation of the applications kit is available at IDT upon request and is part of the documentation package of the application kits.

Another more optimized PCB layout recommendation for utilizing the on-chip DC/DC-converter shows Figure 3.24 in chapter 3.6.4. An appropriated explanation about the considerations behind this recommendation is give in this chapter as well and illustrated in Figure 3.23.

Table 4.1 Recommended External Components

Symbol	Parameter	Min	Typ	Max	Unit	Notes
R1	R	14 [1)]		112 [2)]	kΩ	Value depends on desired output voltage.
R2	R		10		kΩ	
R3	R	-1%	49.9	+1%	kΩ	Low tolerance range resistor (1% class)
R4	R	-1%	210	+1%	kΩ	Low tolerance range resistor (1% class)
L1	L	10		50	µH	Optimal value depends on application requirements.
C1	C	10		50	µF	Low ESR recommended
C2	C		100		nF	Low ESR required
C3	C		10		µF	Low ESR recommended
C4	C		100		nF	Low ESR required
C5	C		10		µF	Low ESR recommended
D1	Schottky Diode					Recommended: small signal low cap schottky diode, e.g. TMMBAT48 (SGS-THOMSON) or similar device
	V_{RRM}	40			V	
	I_F	0.2			A	
D2, D3	Schottky Diode					Only in device applications
	V_{RRM}	40			V	Recommended: 10BQ040PBF (Vishay) or similar device
	I_F	1.0 [3)]			A	
D4 – D7	Schottky Diode					Recommended:
	V_{RRM}	40			V	BAT64-04W (□nfineon) or similar device,
	I_F	0.1			A	The BAT64-04W has a SOT323 package with two diodes in series. Thus there only one component for one channel (one dual diode for D4/D5 and one dual diode for D6/D7).
Q1	Optocoupler					ACPL-217 (Avago Technologies)

[1)] R2 = 10kΩ, please refer to minimum output voltage V_{out} in Table 2.3
[2)] R2 = 10kΩ, please refer to maximum output voltage V_{out} in Table 2.3
[3)] Two channels in operation, each channel drives max. current
[4)] IMPORTANT: The ratio R4/R3 shall be 4.2084 +/- 2%

5 Pin Configuration, Latch-Up and ESD Protection

5.1. Pin Configuration and Latch-up Conditions

Table 5.1 Pin Configuration and Latch-Up Conditions

Pin	Name[1)]	Description	Remarks	Usage[1)] / Connection [3)]	Application Circuit Restrictions and/or Remarks
11, 20	VDD (x2)	Positive external supply voltage pins (HV[4)])	Supply IN	Required/-	Both pins must be interconnected using a low impedance wiring
14, 17	VSS (x2)	Negative external supply voltage pins	Ground	Required/-	Both pins and the exposed die paddle must be interconnected using a low impedance wiring
n.a.	VSS	Exposed die paddle	Ground	Required	Requirements: - to be connected to VSS - cooling via's underneath the die paddle (refer to application note from Amkor (refer to [4] in chapter 8)
24	RST_L	Reset Input	Digital IN L-active	Required or open/-	Pin tolerates 5V logic signals
15	PFD	Power Fail Detector (sense input of the line-fail detector)	Analog IN	Required/ VDD, LR_OUT or VSS (Rev A compatibility) or Voltage divider	HV analog input pin, avoid long wires in order to optimize the EMC behavior
7	SPI_EN_L	SPI enable	Digital IN L-active	Required/-	Pin tolerates 5V logic signals
8	INT_L	Overload indication	Digital OUT L-active	Required or open/-	
9	WURQ_L	Wake up detect signal	Digital OUT L-active	Required or open/-	
4	TX_EN/SPI_CLK	COM driver enable	Digital IN H-active	Required/-	Pin tolerates 5V logic signals
5	TX/MOSI	TX: Data input MOSI: SPI IN	Digital IN	Required or open/-	Pin tolerates 5V logic signals
6	RX/MISO	RX: Data output MISO: SPI OUT	Digital OUT	Required or open/-	
12	COM_I	COM driver IN	HV[4)] IN	Required or open/-	
13	COM_O	COM driver OUT	HV[4)] OUT	Required or open/-	
1	AUX_EN	AUX driver enable	Digital IN H-active	Required/-	Pin tolerates 5V logic signals

Pin	Name[1)]	Description	Remarks	Usage[1)] / Connection [3)]	Application Circuit Restrictions and/or Remarks
2	AUX _TX	TX: Data input	Digital IN	Required or open/-	Pin tolerates 5V logic signals
3	AUX _RX	RX: Data output	Digital OUT	Required or open/-	
18	AUX_O	AUX driver OUT	HV[4)] OUT	Required or open/-	
19	AUX _I	AUX driver IN	HV[4)] IN	Required or open/-	
23	DC_RDY	DC/DC ready signal	Digital OUT	Required or open/-	
21	SW	DC/DC switch OUT	HV OUT	Required or open/-	
22	FB	DC/DC feed back	Analog IN	Required / either interconnected voltage divider or to LR_OUT	In operation mode of the DC/DC converter the voltage divider shall provide 1.225V at the FB pin. Interconnecting FB to LR_OUT will disable the DC/DC converter.
16	LR_IN	Linear regulator Input Voltage (HV[4)])	Supply IN HV	Required/-	
10	LR_OUT	Linear regulator Output Voltage (LV [5)])	Supply OUT LV	Required/ Block Cap to VSS	

[1)] Names of low active digital I/O pins end with "_L"
[2)] Usage: If "Required" is specified, an electrical connection is necessary – refer to the application circuits
[3)] Connection: To be connected to this potential, if not used or no application/configuration related constraints are given
[4)] HV: High voltage – The primary supply voltage of the IC or the voltage swing of the cable signal, typically 24V (>8V, <36V)
[5)] LV: Low voltage – The supply voltage for the internal building blocks of the IC or control signals of the IC, typically 3.3V

5.2. ESD-Protection

All pins have an ESD protection of >2000 V.

ESD protection referred to the Human Body Model (HBM) is tested with devices in QFN24 packages during product qualification. The ESD test follows the Human Body Model with 1.5 kΩ/100 pF, based on MIL 883, Method 3015.7.

6 Package

6.1. Package Details QFN24 4x4mm

6.1.1. Pin Hardware Configurations

In contrast to the integrated circuit product ZIOL2xxx which is base IC for the ZIOL2xxx IC family, not all derived ICs provide all electrical pin interconnections as provided with the ZIOL2xxx. Table 6.1 shows what pins are not connected (n.c.).

Table 6.1 Availability of Pin Interconnections

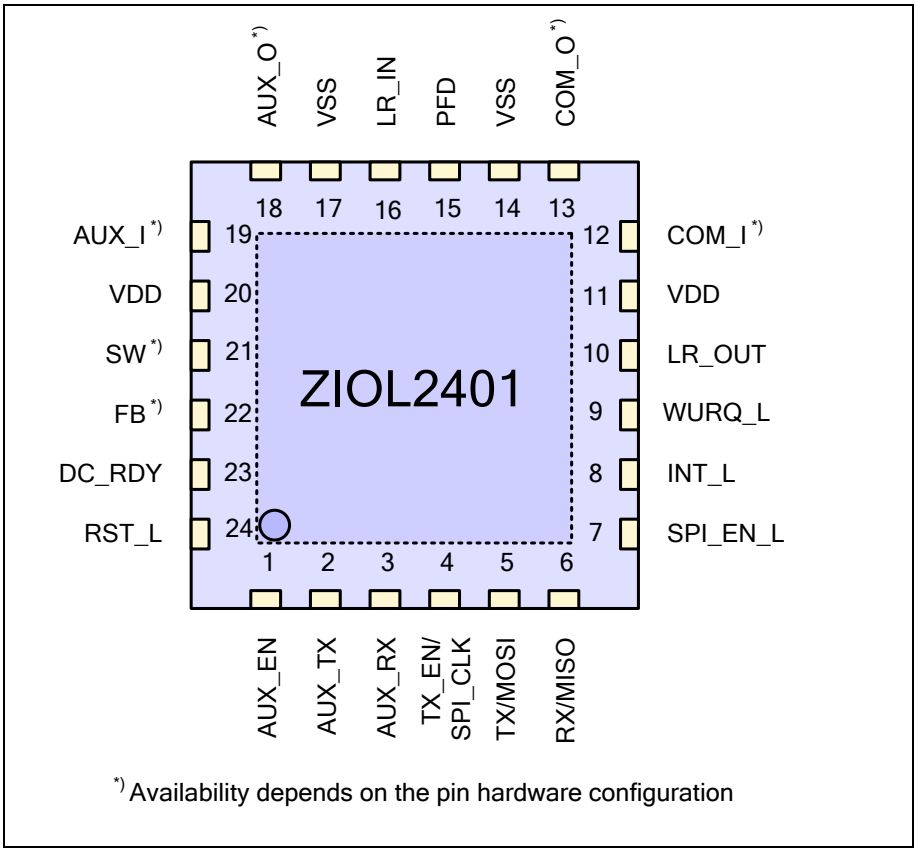
Pin Number (QFN package)	Pin Name	ZIOL 240x [2) 3)]	ZIOL 241x [2) 3)]	ZIOL 220x [2) 3)]	ZIOL 221x [2) 3)]	ZIOL 210x [2) 3)]	ZIOL 211x [2) 3)]	PCB Design Recommendations for not connected (n.c.) Pins
12	COM_I	+	+	+	+	n.c.	n.c.	Connect to VSS
13	COM_O	+	+	+	+	n.c.	n.c.	Connect to VSS
19	AUX_I	+	+	n.c.	n.c.	+	+	Connect to VSS
18	AUX_O	+	+	n.c.	n.c.	+	+	Connect to VSS
21	SW	+	n.c.	+	n.c.	+	n.c.	Do not connect
22	FB	+	n.c.	+	n.c.	+	n.c.	Do not connect
1)	2) "+": Pin is in connected, regular use as mentioned in this datasheet 3) "n.c.": Pin is not connected, the PC design recommendations shall be considered							

6.1.2. Pin Diagram

The standard package of the ZIOL2xxx is a "sawn type" 24 pin MicroLeadFrame package (Amkor, QFN24): It is a green package having a 4mm body width and a lead pitch of 0.5 mm (refer to [3] in chapter 8).

With respect to the different pin hardware configurations of certain ICs of the product family ZIOL2xxx not all pins are interconnected with the silicon die (for more information refer to Table 6.1). The pin diagram shown in Figure 6.1 does not reflect this or can be considered as the pin diagram of the ZIOL2xxx.

Figure 6.1 Pin Diagram of the ZIOL2xxx



6.1.3. Optimal PCB Layout

In order to obtain optimal heat distribution (minimized thermal resistance between package and board) certain PCB layout rules shall be applied. Those rules are described in the application note for the used QFN package (refer to chapter 8, [4]). Crucial for optimal heat distribution is the correct number, diameter and placement of via's underneath the exposed die paddle as described in the above mentioned application note.

6.1.4. Package Outline

The IC is packaged in a 24 pin QFN package (Figure 6.2, based on JEDEC MO-220) having dimensions as shown in Table 6.2.

Figure 6.2 Package Dimensions

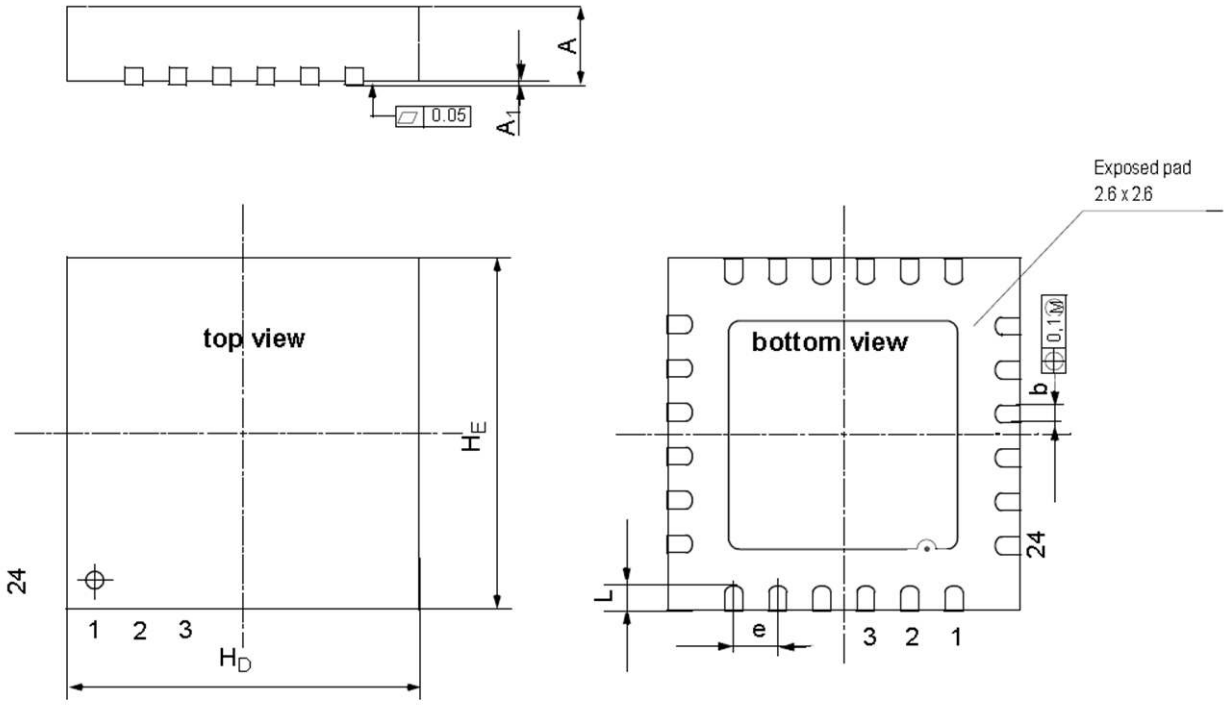


Table 6.2 Package Dimensions in mm

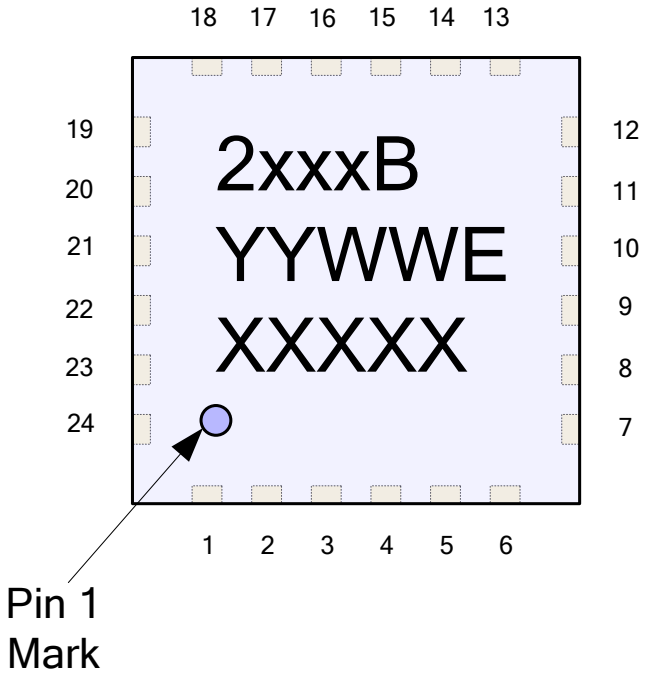
Dimensions	min	max
A	0.80	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0,5nom	
H_D	3.90	4.10
H_E	3.90	4.10
L	0.35	0.45

6.1.5. Device Marking

Figure 6.3 illustrates the device top marking which reflects:

- First line: The **product type** (ZIOL2xxx, xxx: refer to Table 1.1)
  and
  product **revision** identification (last letter, e.g. “B” for Rev B)
- Second line: The **date code** (“YYWW” = Year / Workweek),
  “E” stands for “engineering sample” if applicable
- Third line: IC manufacture’s **traceability code** (XXXXX)

Figure 6.3 Top Marking of the ZIOL2xxx



The ZIOL2xxx has no bottom marking.

6.2. Package Details WL-CSP

6.2.1. Pin Hardware Configurations

In contrast to the integrated circuit product ZIOL2xxx which is base IC for the ZIOL2xxx IC family, not all derived ICs provide all electrical pin interconnections as provided with the ZIOL2xxx. Table 6.1 shows what pins of the Wafer-Level Chip Scale Package are not connected (n.c.).

Table 6.3 Availability of Pin Interconnections

Pin Number (QFN package)	Pin Name	ZIOL 240x 2) 3)	ZIOL 241x 2) 3)	ZIOL 220x 2) 3)	ZIOL 221x 2) 3)	ZIOL 210x 2) 3)	ZIOL 211x 2) 3)	PCB Design Recommendations for not connected (n.c.) Pins
F1	**COM_I**	+	+	+	+	n.c.	n.c.	Connect to VSS
E2+F1	**COM_O**	+	+	+	+	n.c.	n.c.	Connect to VSS
A2	**AUX_I**	+	+	n.c.	n.c.	+	+	Connect to VSS
A1+B2	**AUX_O**	+	+	n.c.	n.c.	+	+	Connect to VSS
A4	**SW**	+	n.c.	+	n.c.	+	n.c.	Do not connect
A6	**FB**	+	n.c.	+	n.c.	+	n.c.	Do not connect
	2) "+": Pin is connected, regular use as mentioned in this datasheet 3) "n.c.": Pin is not connected, the PC design recommendations shall be considered							

6.2.2. Pin Diagram

Table 6.4 shows the standard Pin configuration of the ZIOL2401 in Wafer-Level Chip Scale Package (WL-CSP). As mentioned under paragraph 6.2.1 the pin connection depends on the derivative of the ZIOL2xxx family.

Figure 6.4 Package Dimensions

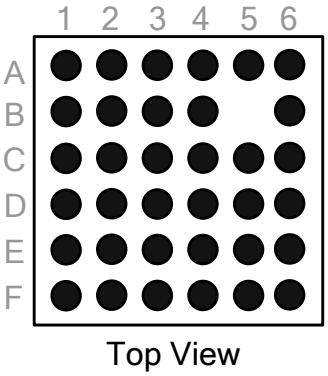


Table 6.4 Bump Pin Configuration

	1	2	3	4	5	6	
A	AUX_O	AUX_I	VDD	SW	DC_RDY	FB	A
B	VSS	AUX_O	VDD	RST_L		AUX_EN	B
C	LR_IN	VSS	VSS	VSS	AUX_TX	AUX_RX	C
D	PFD	VSS	VSS	VSS	TX_EN/SPI_CLK	VSS	D
E	VSS	COM_O	VDD	WURQ_L	RX/MISO	TX/MOSI	E
F	COM_O	COM_I	VDD	LR_OUT	INT_L	SPI_EN_L	F
	1	2	3	4	5	6	

6.2.3. Optimal PCB Layout

In order to obtain optimal heat distribution (minimized thermal resistance between package and board) certain PCB layout rules shall be applied.

6.2.4. Package Outline

The IC is packaged as a 35-pin Wafer-Level Chip Scale Package (Figure 6.5) having dimensions as shown in Table 6.5.

Figure 6.5 Package Dimensions WL-CSP

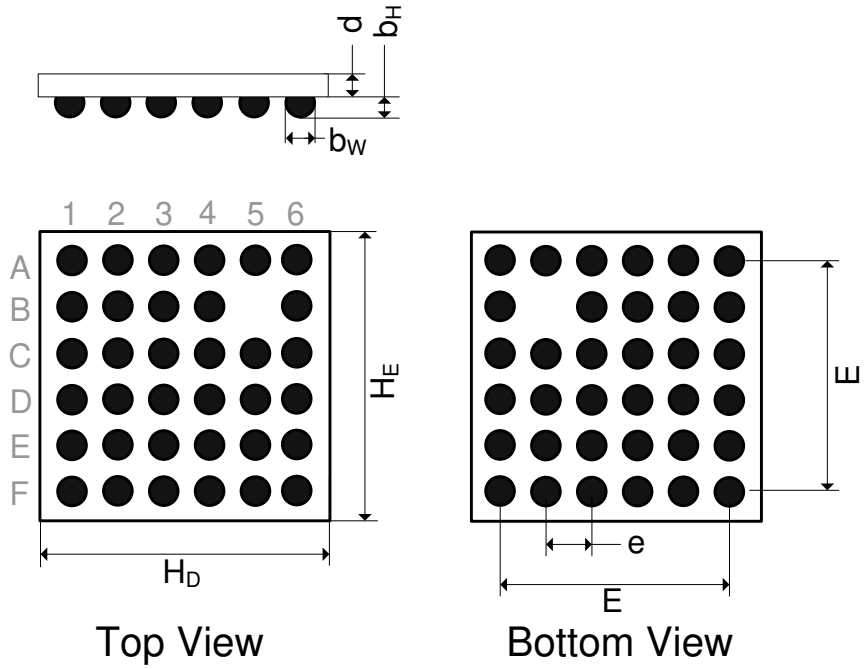


Table 6.5 Package Dimensions in mm

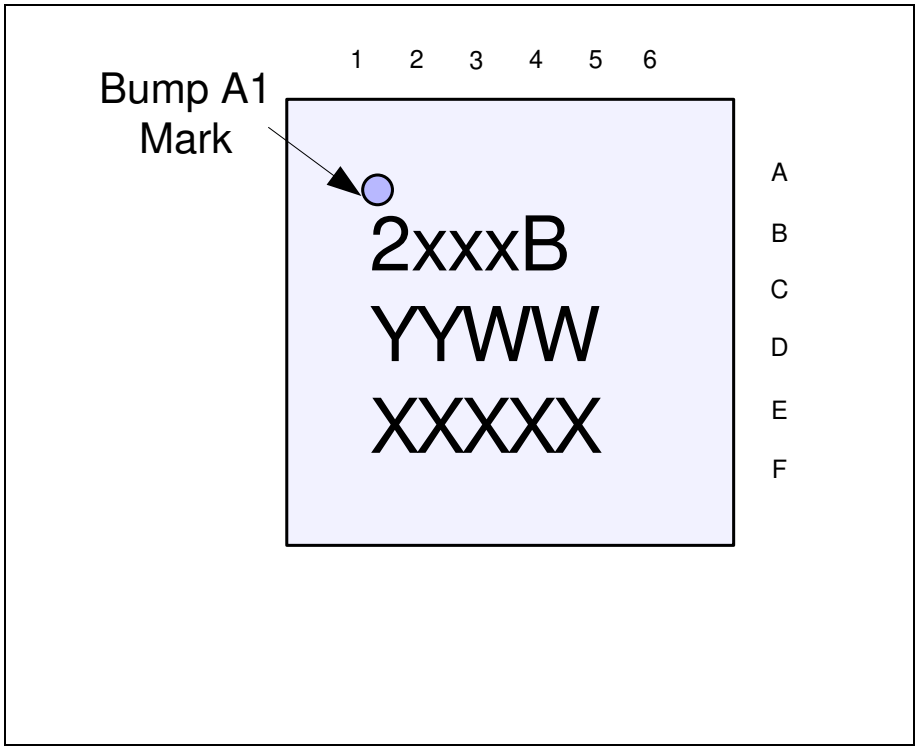
Dimensions	min	nom	max
b_W	0.230	0.255	0.280
b_H	0.185	0.200	0.215
d	0.190	0.200	0.210
E		2.000	
e		0.400	
H_D	2.500	2.525	2.550
H_E	2.500	2.525	2.550

6.2.5. Device Marking

Figure 6.6 illustrates the device top marking which reflects:

- First line: The **product type** (ZIOL2xxx)
  and
  product **revision** identification (last letter, e.g. “B” for Rev B)
- Second line: The **date code** (“YYWW” = Year / Workweek)
- Third line: IC manufacture’s **traceability code** (XXXXX)

Figure 6.6 Top Marking of the ZIOL2xxx CSP



The ZIOL2xxx CSP has no bottom marking.

7 Ordering Information

Product Sales Code[1]	Description	Package
ZIOL2xxx***#I1R*** [1)]	ZIOL2xxx, packing: 13'' reel	QFN24, 4x4
ZIOL2xxx***#I1W*** [1)]	ZIOL2xxx, packing: 7'' reel	QFN24, 4x4
ZIOL2xxx#I2R [1)]	ZIOL2xxx, WL-CSP35, 2.5x2.5	WL-CSP35, 2.5x2.5
ZIOL2xxx***-Lab Kit***	ZIOL2xxx LabKit for detailed lab evaluation (suitable for ZIOL2xxx) (configurable IC-/Communication/Controller PCB, software, USB-cable)	
ZIOL2xxx***-Starter Kit***	ZIOL2xxx Introduction tool (USB stick, extension board, software) (suitable for ZIOL2xxx)	
[1)] # stands for the device revision xxx stands for the device derivate (refer to chapter 1)		

8 Related Documents

Document		Reference/File Name
[1]	IEC61131-2	IEC61131-2, third edition 2007-7
[2]	IO-Link Communication Specification	IOL-Comm-Spec_10002_V10_090118.pdf, downloadable from www.io-link.com
[3]	Datasheet MicroLeadFrame (QFN package)	MicroLeadFrame.pdf, downloadable form www.amkor.com
[4]	Application Note QFN Package	MLFApplicationNotes0908RevG.pdf , downloadable form www.amkor.com

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9 Glossary

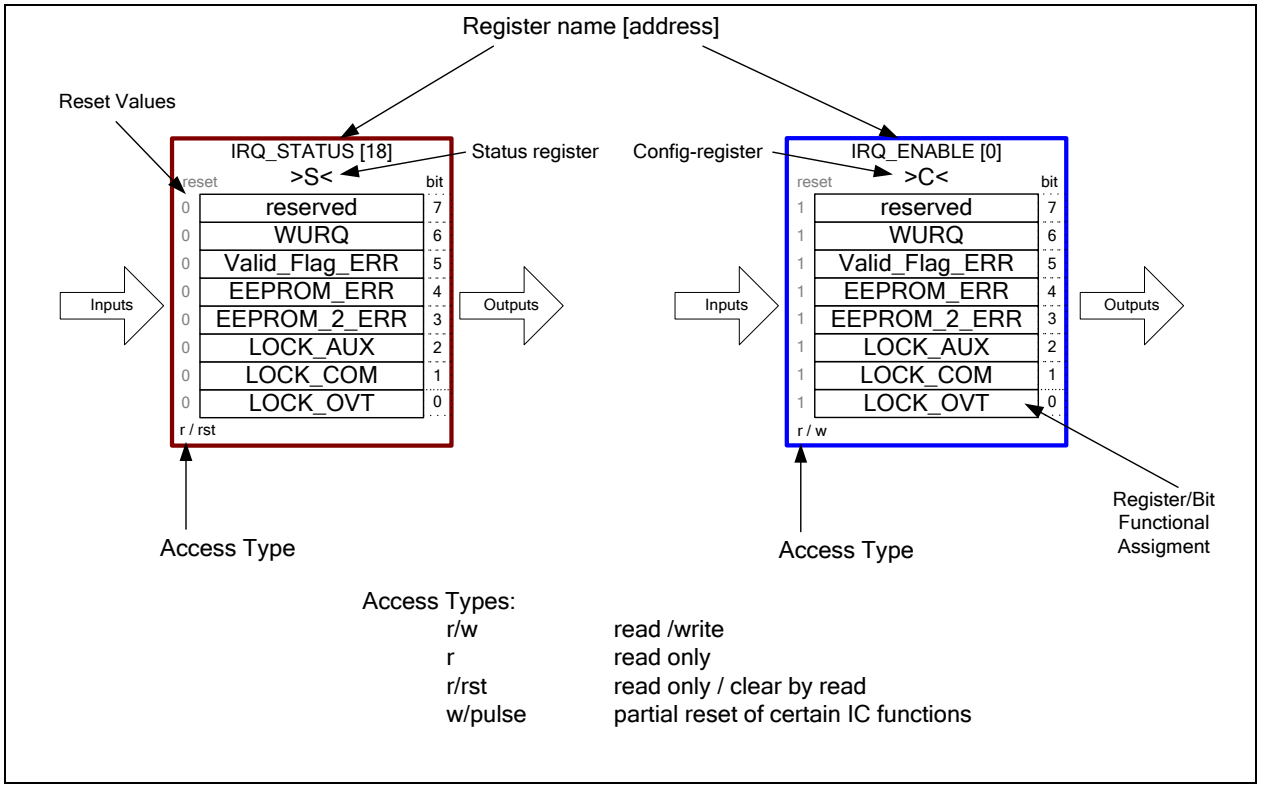
9.1. Terms and Abbreviations

Term	Description
AUX	Auxiliary communication channel of the IC ZIOL2xxx
COM	Default communication channel of the IC ZIOL2xxx
COM1	IO-Link specific communication channel speed
COM2	IO-Link specific communication channel speed
COM3	IO-Link specific communication channel speed
CSP	Chip Scale Package
HS	High-side, meant is the high side switch of a driver channel (push function)
LS	Low-side, meant is the low side switch of a driver channel (pull function)
OVL	Overload (current or temperature) exception
OVL_HS	Current overload exception at HS
OVL_LS	Current overload exception at LS
OVT	Over-temperature exception
PFD	Power fail detection
PHY	Physical Layer Transceiver

9.2. Symbols used in this Datasheet

Symbol	Description
XX_{yy}	Physical value (physical variable) as used in operation conditions, IC parameters and functional descriptions
XX_YY_**L**	Digital I/O low active IC Pin
XX_YY	Any other IC Pin (analog, supply or digital I/O high active IC Pin)
XX_YY[nn]	Register names, nn = address
Selected examples for physical values:	
V_{DD_HV}	Primary IC supply voltage of nominal 24V (called High_voltage) = Cable supply voltage
V_{DD_LV}	Secondary supply voltage for all analog and digital building blocks of the IC of nominal 3.3V. VDD_LV is equivalent to the supply voltage provided by the internal linear regulator. It can also be used to supply external electronic circuits.

Figure 9.1 Register Representation in Principle (Example)



10 Document Revision History

Revision	Date	Description
0.6	December 8, 2008	First draft
0.7-0.9		internal revisions
1.0	July 2009	Completely reworked datasheet
1.0.1 1.0.2	August 2009	Developer feedback processed
1.0.3	August 2009	Internal revision
1.0.4	August 2009	1st release under NDA
1.0.5	September 2009	Internal revision
1.0.6	November 2009	Reworked due to internal/external feedback
1.0.7	December 2009	Reworked due to internal/external feedback (correction of typing errors and wrongly described IC functions) - Register description in overview drawings - IC properties - External components DCDC converter
1.0.8	December 2009	Channel configuration coding tables and figure concerning the description of channel locking corrected;
1.1.0 .. 1.1.4	February 2010	Internal revisions
1.1.5 1.1.6 1.1.8	March 2010	Significant re-work of all datasheet chapters - Parameters DC/DC converter and COM/AUX driver adjusted - External clamping diodes changed from z-diodes to schottky diodes - IC configuration more in detail - Detailed application examples
1.1.8 1.1.9	April 2010	Internal revisions
1.1.10	April 2010	Update of package related information, improvement of comprehensibility
1.1.11	May 2010	- Improvement of comprehensibility on base of a detailed data path description - Typing error correction reg[18] (interrupt and wake-up signaling - More detailed descriptions in register list - Electrical interconnection of exposed paddle of the Ics package
1.1.12	May 2010	- Text Layout
1.1.13	June 2010	- Pin name error correction in Figure 5-1 Pin Diagram of the ZIOL2401 - recommendation for the external diode D1 of the DC/DC converter changed from TMMBAT42 to TMMBAT48
1.2.0	June 2010	Final Version for IC Revision A - Consequently using the term IO-Link “device”, term “slave” replaced - DC/DC converter parameters
1.2.1 1.2.2	June 2010	Internal revision

Revision	Date	Description
1.2.3	July 2010	General change (rework) of the DC/DC-converter description and adding of further PCB layout recommendation in combination with the utilization of the DC/DC-converter
1.2.4	August 2010	- Changes regarding ZMDI's corporate identity police - DC/DC Converter: more detailed DC_RDY description
2.0.1	September 2010	- Datasheet ZIOL2401 rev1.2.4 transferred to IC family datasheet ZIOL2xxx - Included all IC Rev B enhancements (upgrades)
2.0.2	November 2010	- Considered feedback from the IC development team, in particular as regards the Rev B functionality and functionality of the different IC family members - Revised the description of the transceivers in order to higher the comprehensibility (focusing to the terms: device/master mode and dual/tandem mode
2.0.3	January 2011	Internal review results considered - New (more comprehensive) description of the driver channel and their configuration and operating modes - Both Channels: Introduction of separated descriptions of alarm levels (causing an exception) and the corresponding current limitation of the considered driver.
2.1.0	April 2011	First release of ZIOL2xxx IC family data sheet
2.2.0	October 2011	Just for internal reviews
2.2.1	January 2012	- Changed upper limits for configurable output current limits (Table 2.3) - Added power consumption information (current into VSS, LR_IN) - Added package drawing
2.3.0	August 2012	- Added Wafer-Level Chip Scale Package (WL-CSP) information
	April 26, 2016	- Changed to IDT branding.

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Appendix A ZIOL2xxx Diagnostic Techniques

A.1. General Remarks

Since chapter 3.3 described the basic principles in terms of IC control circuit, this chapter deals with details of techniques for analyzing the internal IC state in order to prevent IC damage or unwanted system operation. The following description references to Figure 3.8 (The Basic Scheme of the IC Self Protection) of the ZIOL2xxx datasheet.

A.2. Overload Counter Behavior and Peak Register Access

The ZIOL2xxx contains five peak registers (status registers) which are associated with overload counters as follows:

- Over-current counter assigned to the LS driver of the COM channel – register[21]
- Over-current counter assigned to the HS driver of the COM channel – register[22]
- Over-current counter assigned to the LS driver of the AUX channel – register[23]
- Over-current counter assigned to the HS driver of the AUX channel – register[24]
- Over-temperature counter– register[25]

Only in case an overload is present, thus the overload counter is in the count up mode, the value of the overload counter will be copied into the peak register if the overload counter value is greater than the peak register value. This conditional copy operation is performed within each cycle of IC control circuit as illustrated in Figure 10.1.

Figure 10.1 shows two different scenarios of the behavior of a peak register. Scenario A shows the development of the peak register value if no read access happened. In contrast to that scenario B shows several read accesses within the same sequence of consecutive overload periods. Since the peak register is cleared after each read access, it resumes within the next cycle of the IC control circuit to the present overload counter value only if overload is present.

A lock will be generated if the overload counter reaches a configured maximum value which is representing according to the following formula the related “Assert time” of the lock circuit (refer to Figure 3.15, Figure 3.16, Figure 3.17).

$$T_{AssertTime} = T_{clk} * AssertTimeVal$$

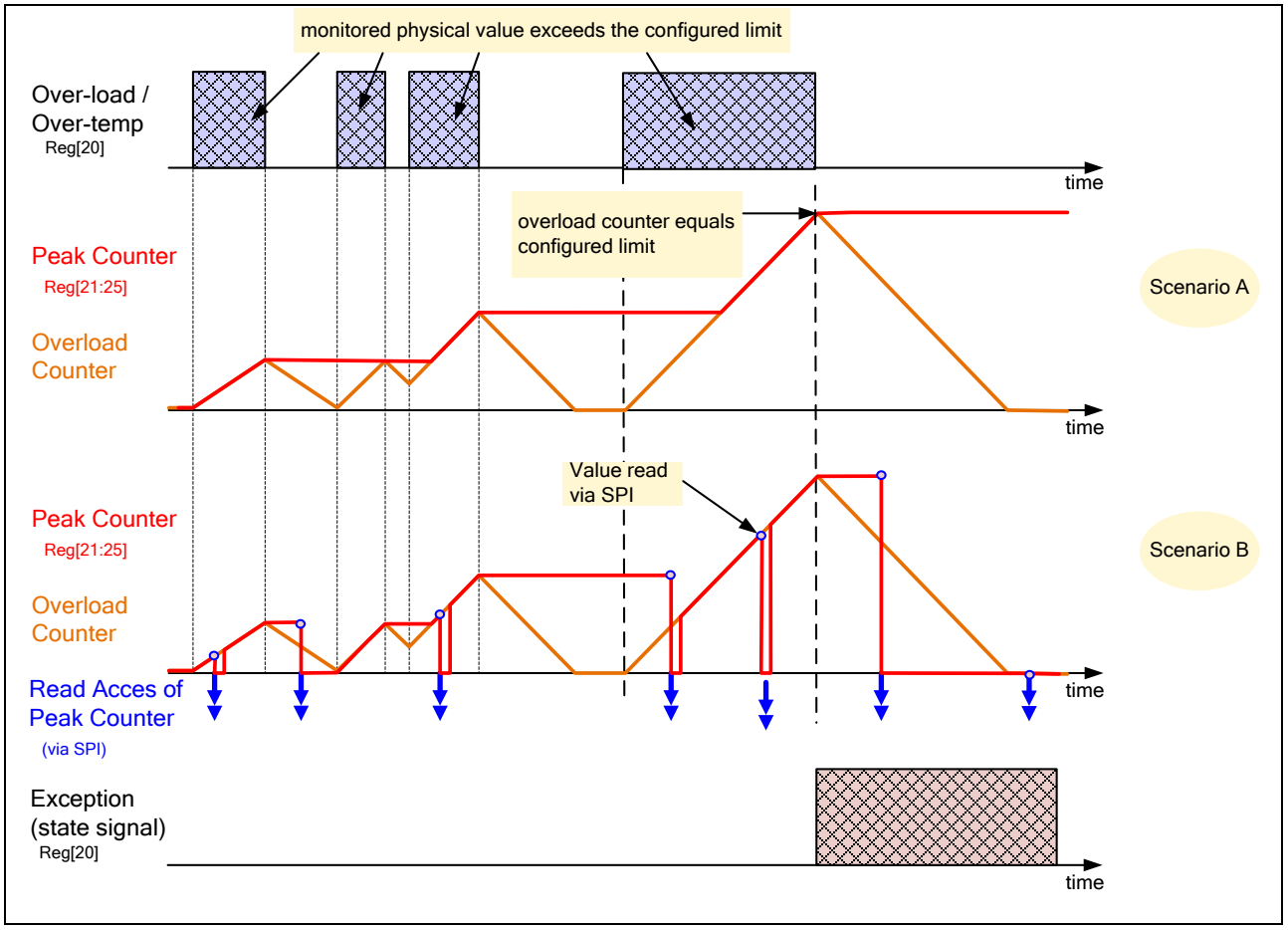
Where T_{clk} is the for the lock circuit configured counter clock (refer to Figure 3.15, Figure 3.16, Figure 3.17) having a period of 200ns, 1ms, 8ms, or 16ms and where *AssertTimeVal* is the in the related assert time register stored value.

Similarly to that, thus using a similar formula the lock time of the related lock circuit (refer to Figure 3.15, Figure 3.16, Figure 3.17) can be calculated.

$$T_{LockTime} = T_{clk} * LockTimeVal$$

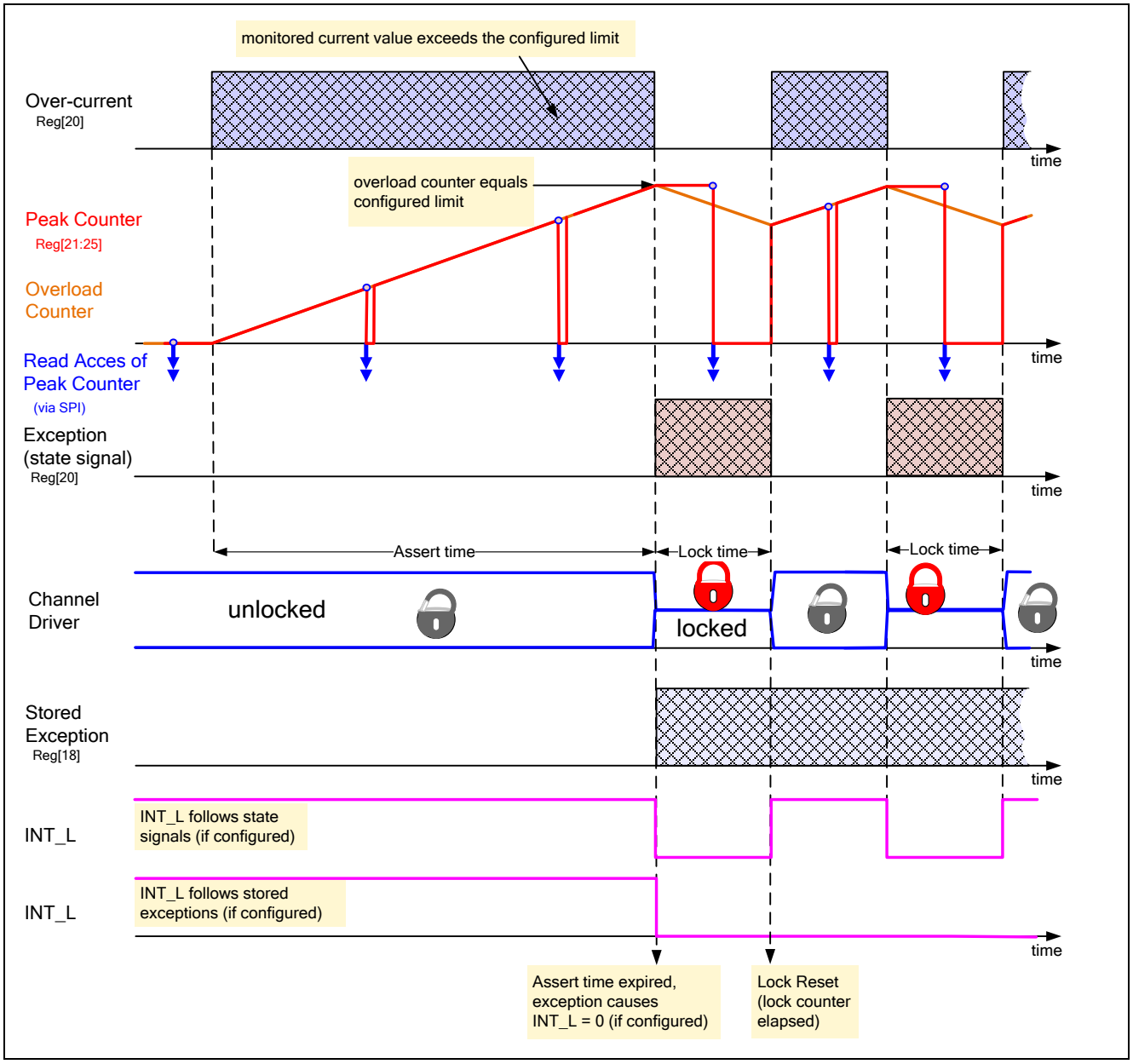
Where T_{clk} is the for the lock circuit configured counter clock (which is the same clock as used for the overload counter, refer to Figure 3.15, Figure 3.16, Figure 3.17) having a period of 200ns, 1ms, 8ms, or 16ms and where *LockTimeVal* is the in the related assert time register stored value.

Figure 10.1 Peak Register Access Scenarios



In contrast to Figure 10.1 in where the overload situation stops at the point in time in which the driver has been locked Figure 10.2 shows a situation in which the overload situation, especially an over-current situation is kept. This situation occurs for instance due to a low impedance load which is permanently interconnected to the driver output. In addition to that the lock reset is configured in that way that its period is significantly shorter compared with the assert time period. In this case the overload counter does not reach the zero value at the point in time the lock is reset. This in the following time the assert time is shortened and equals approximately the lock time that even passed by.

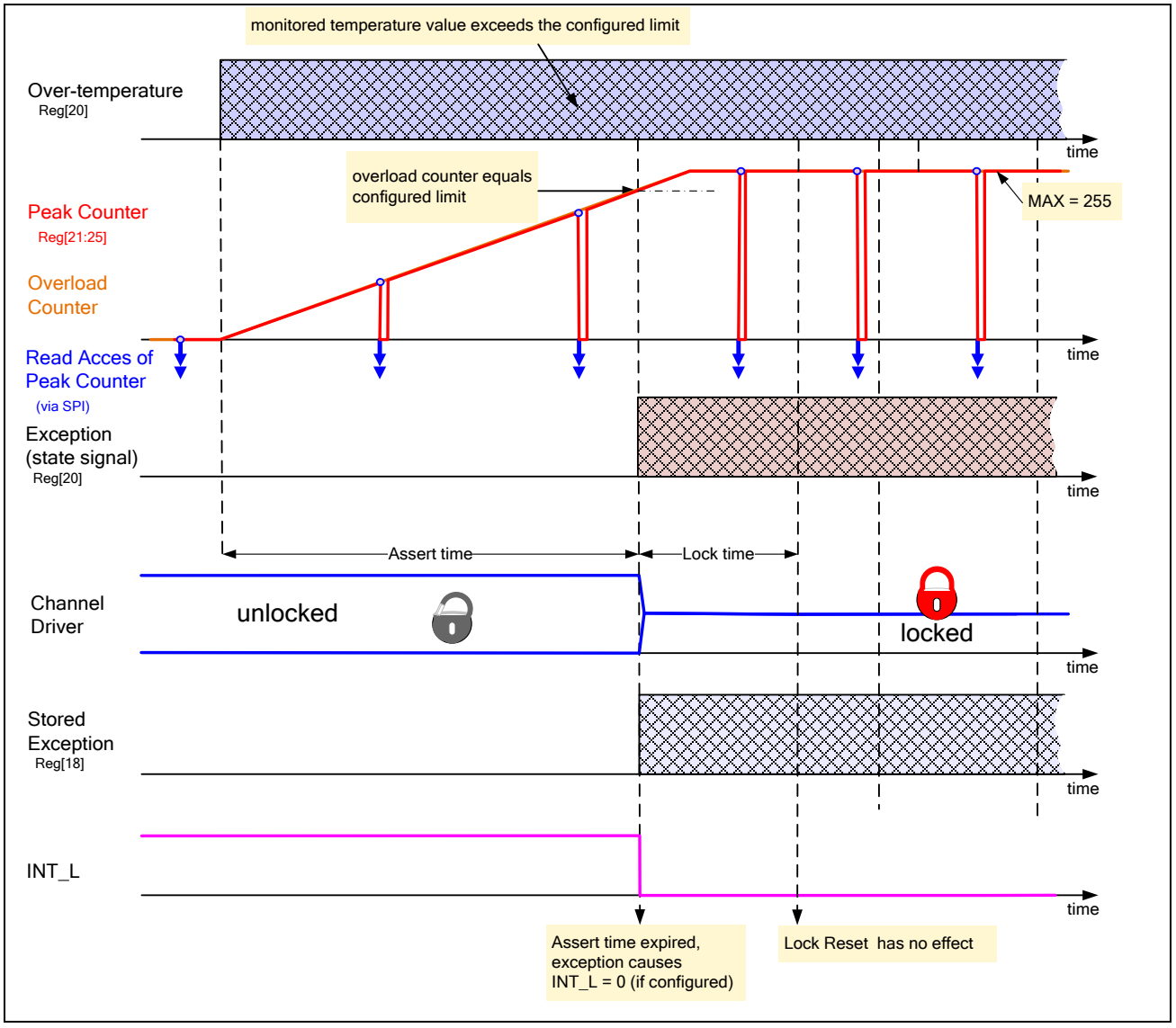
Figure 10.2 Overload Counter Behavior in permanent Over-Current Situations



Since a locked channel is in high-impedance (high-z) state, no over-current can occur while a channel is locked. Therefore overload counter starts immediately counting down when the lock is enabled.

In case of a permanent over-temperature situation the die temperature may not decrease at the point in time the channel control started locking both channels as shown in Figure 10.3. In this case the overload counter does not stop counting up if the configured assert time is expired. Finally the overload counter reaches its maximum value of 255 (0xFF).

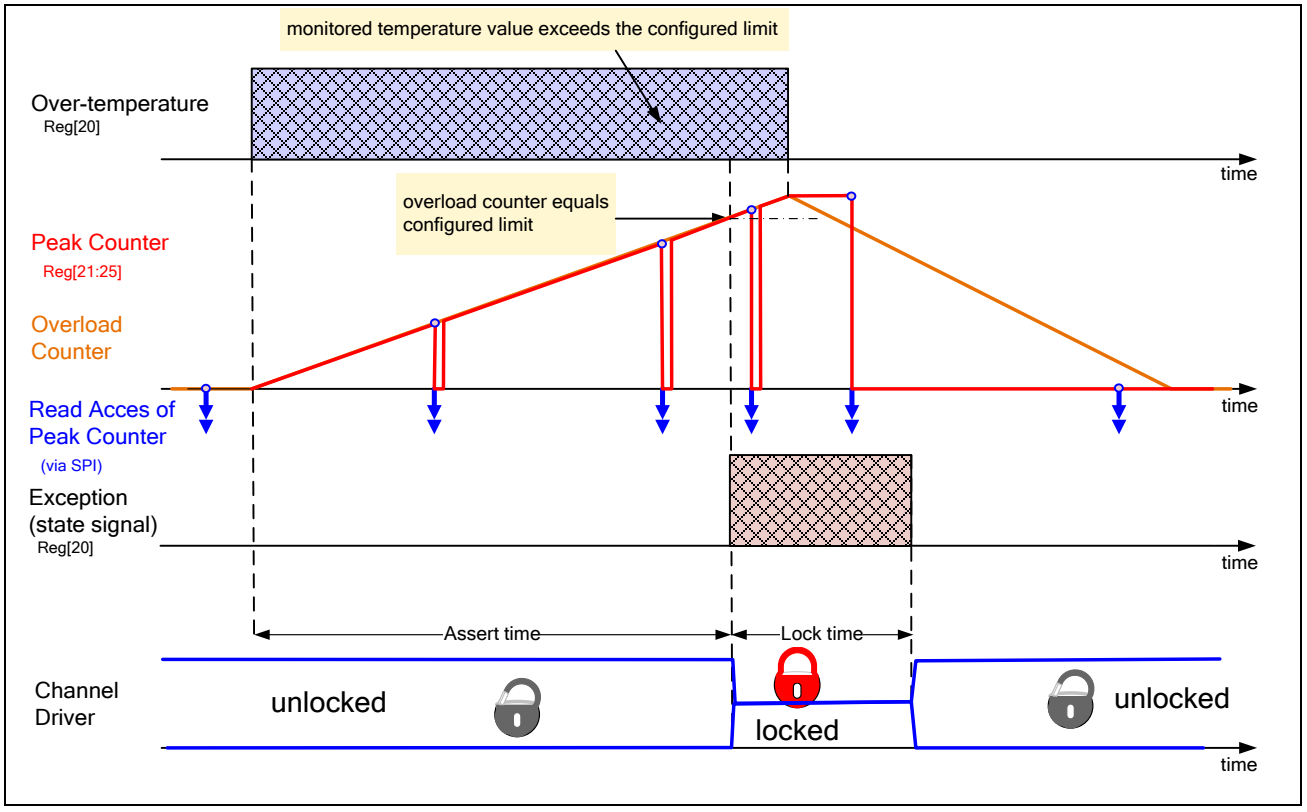
Figure 10.3 Overload Counter Behavior in permanent Over-Temperature Situations



In this situation a lock reset due to an elapsed internal lock counter of the temperature lock control circuit (Figure 3.17) will not release the locks which are in effect on both channels. However, the locks can be released by writing into register[16] (write pulse function).

In typical over-temperature situations the overload counter may reach a value that is greater as the configured limit. This is due to the thermal inertia of the system since the temperature sensor and the thermal sources are not on the same place on the silicon die. When the lock has been released, the there is a little difference in the behavior when reading the peak register as shown in Figure 10.4. The peak register is loaded with the overload counter value again as long the over-temperature situation is present.

Figure 10.4 Overload Counter Behavior in typical Over-Temperature Situations



A.3. Overload Counter and Lock Reset Methods

The ZIOL2xxx has two special status registers (register[16:17]). Those status registers do not contain information about the IC status. Thus reading those registers will always result to the value zero for each register. However those registers are used to perform special resets within the COM, AUX, and temperature lock circuits. In addition to that register[16] can also reset the WURQ exception.

The way to perform a particular reset operation is writing into the register (write[24] pulse access; please refer to chapter 3.3.9) the bit-value “1” at a certain bit position which is assigned to the desired reset operation.

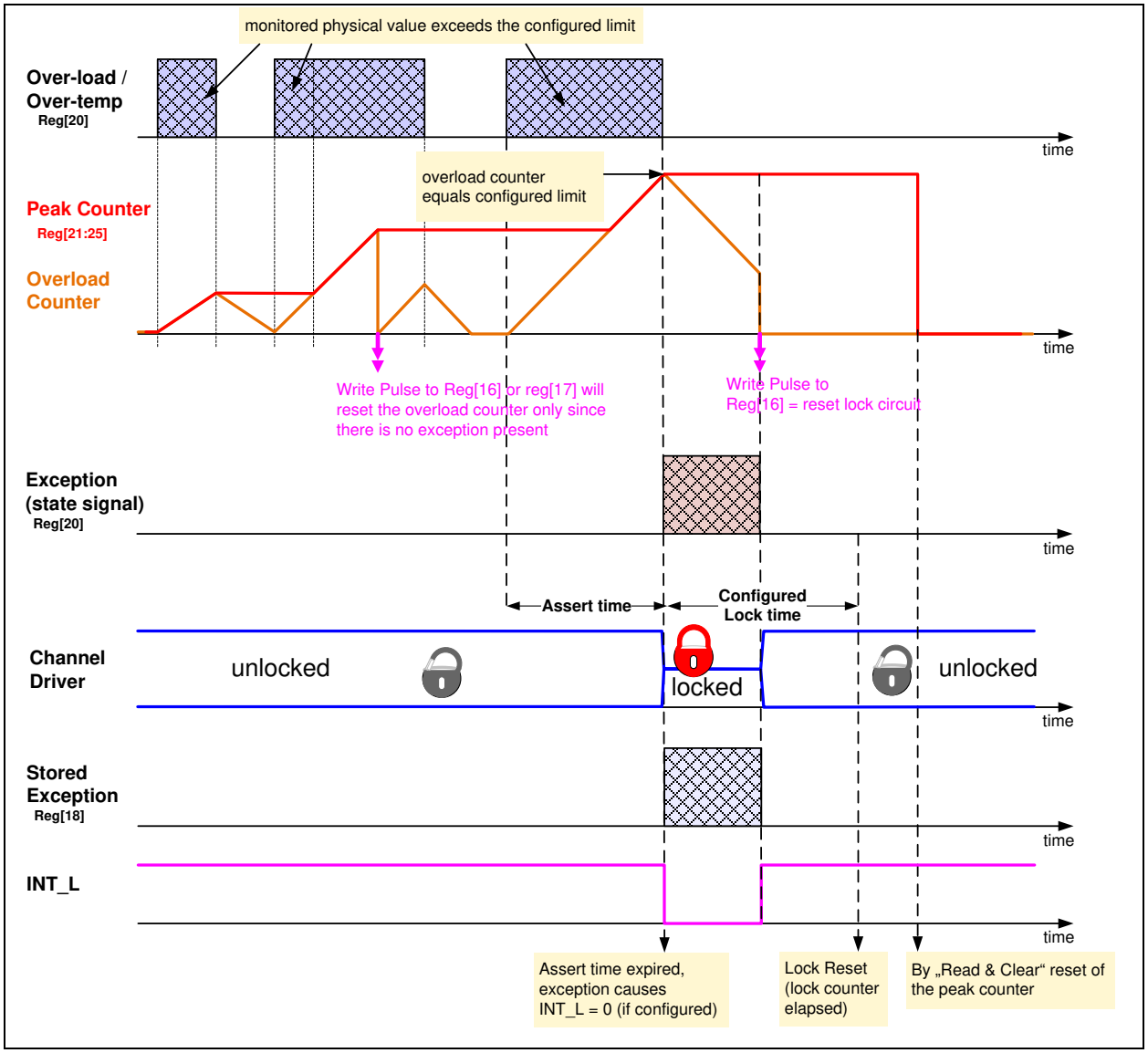
Register[16] performs the following reset operations by writing a “1” into the following bit positions:

- Bit[0]: Reset over-temperature counter and reset of the internal and stored over-temperature (OVT) exception
- Bit[1]: Reset the COM over-current counter and reset of the internal and stored COM over-current (OVT) exception
- Bit[2]: Reset the AUX COM over-current counter and reset of the internal and stored AUX over-current (OVT) exception

[24] Note: IC versions ZIOL2xx2 do not allow any write access.

- Bit[3]: Reset of the stored WURQ exception

Figure 10.5 Partial Reset of Overload Counter or the entire Lock circuit



A write pulse access to **register [17]** works similar but performs only a partial reset of the overload counter as in the following described:

- Bit[0]: Reset of the over-temperature counter
- Bit[1]: Reset of the over-current counter assigned to the COM LS driver
- Bit[2]: Reset of the over-current counter assigned to the COM HS driver

- Bit[3]: Reset of the over-current counter assigned to the AUX LS driver
- Bit[4]: Reset of the over-current counter assigned to the AUX HS driver

Figure 10.5 illustrates the effect of a write[25] pulse access to register[16] and register[17]. As shown in this figure a write pulse to register[16] does only reset the overload counter if no exception is present. If an exception is present (or still stored in register[18]) the write pulse access to register[16] will also reset related exceptions.

In the special case the write pulse access to register[16] is performed while a temperature overload is still present the exception will by cleared but set again within the next cycle of the IC control circuit. Accordingly to the configuration of the INT_L pint the INT_L pin will perform the configured transitions again (refer to chapter A.2).

Depending on the byte-value written in register[16] or register[17] the above mentioned reset operation are performed separately or in parallel.

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[25] Note: IC versions ZIOL2xx2 do not allow any write access.

Appendix B ZIOL2xxx Configuration Techniques

The ZIOL2xxx allow various configurations to work optimal in several applications. Basically the ZIOL2xxx can be configured to work in applications with or without µC.

Figure 10.6 Configuration Checker Report of the ZIOL2xxx Application Kit (Example)

Application Kit - ZIO2401 (c) ZMDI - V2.1, built 28.04.2011 10:06:42 (UTC)

ZIOL2211 Rev.B - Configuration Check
on: 29-Apr-2011 09:52:11

Number of Warnings: 1
Number of Errors: 1

IO-Link Wake-up (WURQ) Detection
WURQ detection is assigned to channel: COM
WURQ detection method:
- WURQ detection on current (overload)
- WURQ detection on antivalent levels

COM Channel Transmitter
Current Limit: 50 ... 65 mA
High-Side: enabled
Low-Side: enabled
Slew Rate Control: 10 V/µs
150k-Resistor usage: OFF
Signal inverter: OFF

COM Channel Receiver
Receiver logic input levels: absolute (IO-Link conform)
Analog filter: OFF
Digital filter: OFF
Signal inverter: OFF
Sink Mode: OFF
Sink strength: 2 ... 3 mA

COM channel protection settings
Assert time (persist overload during this period will lead to locked driver): 0 ms
>>> Warning: zero assert time can lead to immediately locked driver!
Lock time (period after lock will be removed automatically): 100 ms
High-Side:
Overload and wake-up detection: enabled
Driver lock due to HS overload exceeds assert time: enabled
Low-Side:
Overload and wake-up detection: enabled
Driver lock due to LS overload exceeds assert time: enabled

AUX Channel Transmitter
Current Limit: 50 ... 65 mA
High-Side: enabled
Low-Side: enabled
Slew Rate Control: 10 V/µs
150k-Resistor usage: OFF
Signal inverter: OFF

AUX Channel Receiver
Receiver logic input levels: absolute (IO-Link conform)
Analog filter: OFF
Digital filter: OFF
Signal inverter: OFF
Sink Mode: OFF
Sink strength: 2 ... 3 mA

AUX channel protection settings
Assert time (persist overload during this period will lead to locked driver): 50 ms
Lock time (period after lock will be removed automatically): 0 ms
High-Side:
Overload and wake-up detection: enabled
Driver lock due to HS overload exceeds assert time: enabled
Low-Side:
Overload and wake-up detection: enabled
Driver lock due to LS overload exceeds assert time: enabled

Over-temperature protection settings
Over-temperature protection: enabled
Channel locking: enabled
Max. allowed die temperature: >>> Error: Multiple or no temperature level selected
Assert time (persist over-temperature during this period will lock both drivers): 100 ms
Lock time (period after lock will be removed automatically): 200 ms

Power-Fail protection settings
Under-Voltage protection (channel locking): disabled
Line-Fail protection (channel locking): disabled

Master/Device mode settings
IC Mode: Device Mode

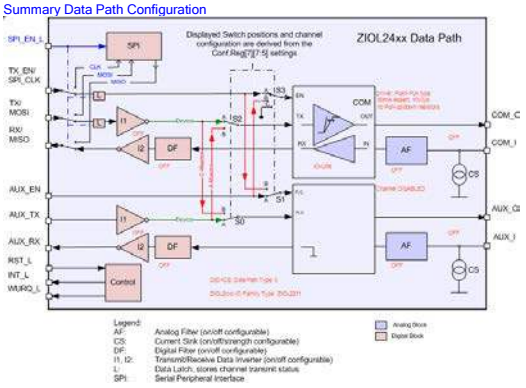
Pin Configuration Settings
WURQ_L pin (IO-Link wake-up signaling): push/pull
INT_L pin (for exception signaling settings refer below): push/pull
DC_RDY pin: delay 50 ms

Exception Signaling
Interrupt (INT_L) will be active if one of the following exceptions occurred:
- Both channels are locked due to Power-Fail
- Wake-up has been detected (WURQ)
- The EEPROM is corrupt (valid-latch error)
- There is a general EEPROM error
- There is a 2-bit EEPROM error
- The AUX channel is locked due to over-current
- The COM channel is locked due to over-current
- Both channels are locked due to over-temperature

IRQ_Port (INT_L pin) follows: state signals

Configuration Register Summary
ConfigReg[0] = 0xFF
ConfigReg[1] = 0x03
ConfigReg[2] = 0x00
ConfigReg[3] = 0x03
ConfigReg[4] = 0x00
ConfigReg[5] = 0xC8
ConfigReg[6] = 0x64
ConfigReg[7] = 0x06
ConfigReg[8] = 0x64
ConfigReg[9] = 0x0F
ConfigReg[10] = 0x00
ConfigReg[11] = 0x3F
ConfigReg[12] = 0x32
ConfigReg[13] = 0x3F
ConfigReg[14] = 0xEB
ConfigReg[15] = 0x00

Summary Data Path Configuration



Recommendations as regards the optimal configuration of the IC are provided by IDT in application notes and associated XML-Data-Files. Those XML-Data can be loaded into the IC using the also by IDT provided ZIOL2xxx application kits. Moreover, the user interface program of the ZIOL2xxx application kit provides a “configuration checker tool” which allows reviewing the IC configuration in a plain text report and which provides error and warning messages in case of wrong or critical IC configurations as illustrated in Figure 10.6.

The following configurations are considered as critical thus not recommended to use:

- Assert time = 0
- Set both the
- driver no-current-limit bit and in parallel one or two bit that define current limits
-

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Appendix C ZIOL2xxx Line Fail Detector

The following description of the Line-Fail (LF) Detection feature assumes the utilization of both channels in device mode. In the case one channel is used only, the number of failures that can be detected with the LF detector will be reduced accordingly. The following supply failures (Table 10.1) shall be detected or shall not cause undefined or malfunctions of the device (sensor/actuator). For more information about the Line-Fail detector as part of the Power-Fail detection feature of the ZIOL2xxx ICs, please refer to chapter 3.5.

Table 10.1 Abnormal Power Supply Situations

Number	Failure	IC Supply	IC function
F1	L+ break	After the break occurred the IC is supplied by the decoupling caps which are between VDD and VSS and LR_OUT and VSS, respectively. In addition to that the IC might get “supply power” via incoming (toggling) cable signals.	As long as the IC has sufficient supply power (which is normally - at least for some milliseconds - the case), the LF function will detect this as LINE_FAULT event and will rise an exception. This exception can be signaled to the µC via the INT_L signal if configured accordingly. Customer recommendation: Subsequently the µC shall stop any communication and shall handle (e.g. signal) the power fail situation.
F2	L- break		
F3	L+ and L- break		
F4	24V power supply falsely interconnected to COM/AUX in combination with F1, F2, or F3.	The IC is permanently powered via the COM/AUX external protection diodes (and internal parasitic diodes).	The LF function will detect this as LINE_FAULT event and will raise an exception. This exception can be signaled to the µC via the INT_L signal if configured accordingly. Customer recommendation: Subsequently the µC shall stop any communication and shall handle (e.g. signal) the power fail situation (e.g. by influencing signaling LEDs).
F5	Correct interconnection of the 24V power supply to L+ and L- but in addition to that is the 24V power supply falsely interconnected to COM/AUX.	No difference to the regular power supply situation.	The LF detector will not act in this situation. However, the IC protection is provided by the overload and over temperature protection feature.

Number	Failure	IC Supply	IC function
F6	Reverse interconnection of the 24V power supply to L+ and L-.	The reverse polarity protection diodes prevent a power supply of the IC.	No power – no function.
F7	Reverse interconnection of the 24V power supply to L+ and L- but in addition to that is the 24V power supply falsely interconnected to COM/AUX. Also in combination with F1 or F2.	The IC is permanently powered via the COM/AUX external protection diodes (and internal parasitic diodes). A similar situation is if the IC gets “supply power” via incoming (toggling) cable signals.	The LF function will detect this as LINE_FAULT event and will raise an exception. This exception can be signaled to the µC via the INT_L signal if configured accordingly. Customer recommendation: Subsequently the µC shall stop any communication and shall handle (e.g. signal) the power fail situation.
F8	The voltage of the regular 24V power supply drops under 8V	The control circuit of the IC is powered regularly but the HV driver may cause malfunction since the voltage at the VDD pin dropped below 8V.	The UV function will detect this as UNDER_VOLTAGE event and will raise an exception unconditionally.

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