CY7C1328A/GVT71256F18
CY7C1348A/GVT71128F36

128K x 36/256K x 18 Synchronous-Pipelined Cache RAM

Features

- **Fast access times: 3.5, 3.8, and 4.0 ns**
- **Fast clock speed: 166, 150, 133, and 117 MHz**
- **Provide high performance 3-1-1-1 access rate**
- **Fast OE access times: 3.5 ns and 3.8 ns**
- **Optimal for performance (double cycle chip deselect, depth expansion without wait state)**
- **3.3V –5% and +10% core power supply**
- **2.5V or 3.3V I/O supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **High-density, high-speed packages**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1348A/GVT71128F36 and CY7C1328A/GVT71256F18 SRAM integrate 262,144x18 and 131,072x36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables (CE2 and $\overline{CE2}$), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables (BW1, BW2, BW3, BW4, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$) and Burst Mode Control (MODE). The data outputs (Q), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

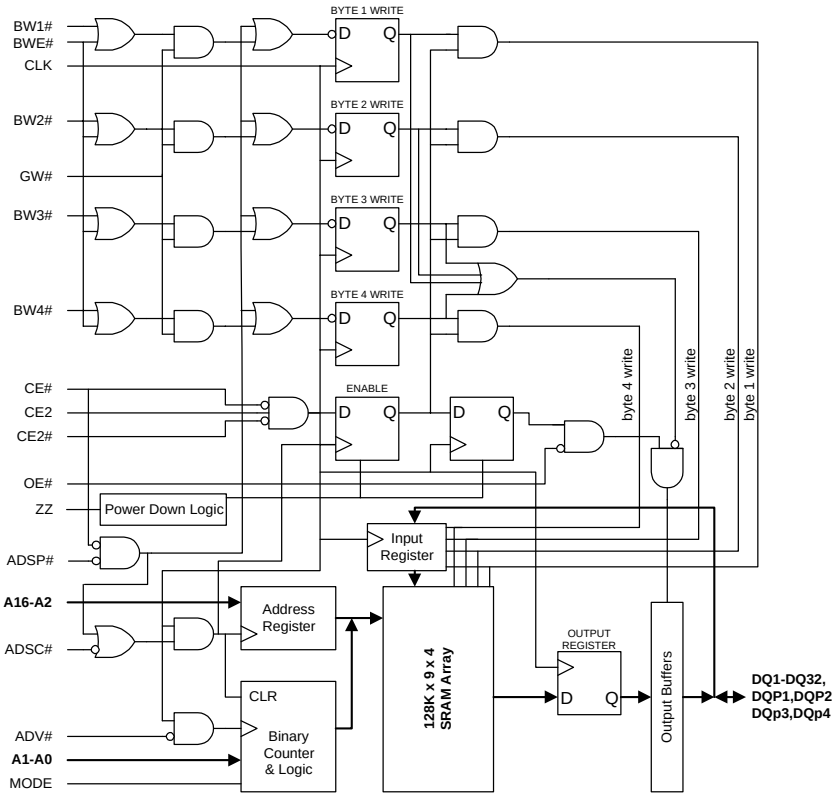
Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BW1 controls DQ1–DQ8 and DQP1. BW2 controls DQ9–DQ16 and DQP2. BW3 controls DQ17–DQ24 and DQP3. BW4 controls DQ25–DQ32 and DQP4. BW1, BW2, BW3, and BW4 can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the immediately next READ cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The CY7C1348A/GVT71128F36/CY7C1328A/GVT71256F18 operates from a +3.3V core power supply and all outputs operate on a +2.5V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible. The device is ideally suited for 486, Pentium®, 680x0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

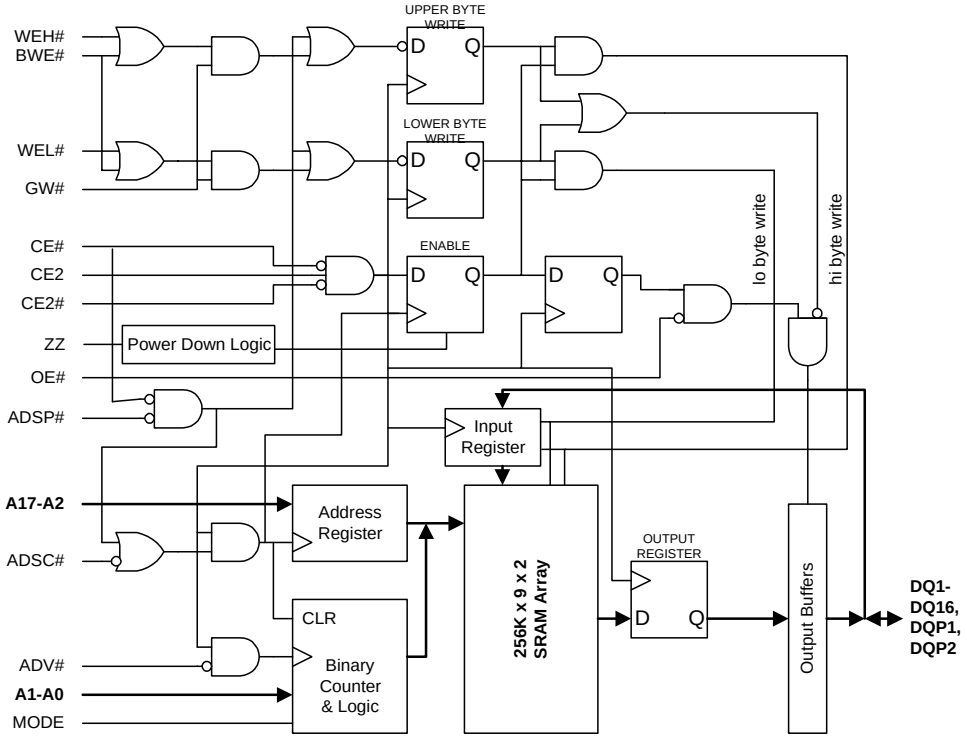
Selection Guide

	7C1328A-166 71256F18-3 7C1348A-166 71128F36-3	**7C1328A-150 71256F18-4 7C1348A-150 71128F36-4**	**7C1328A-133 71256F18-5 7C1348A-133 71128F36-5**	**7C1328A-117 71256F18-6 7C1348A-117 71128F36-6**
Maximum Access Time (ns)	3.5	3.8	4.0	4.0
Maximum Operating Current (mA)	425	400	375	350
Maximum CMOS Standby Current (mA)	10	10	10	10

Functional Block Diagram—128Kx36[1]



Functional Block Diagram—256Kx18[1]

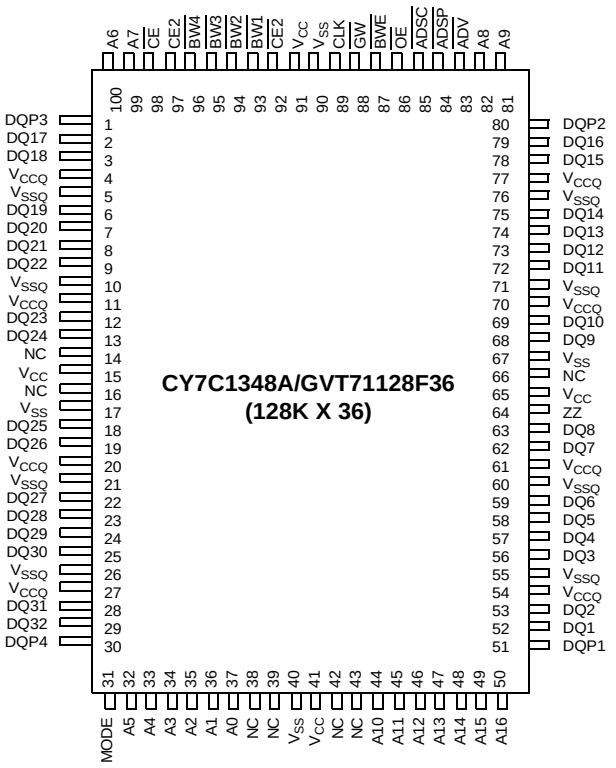


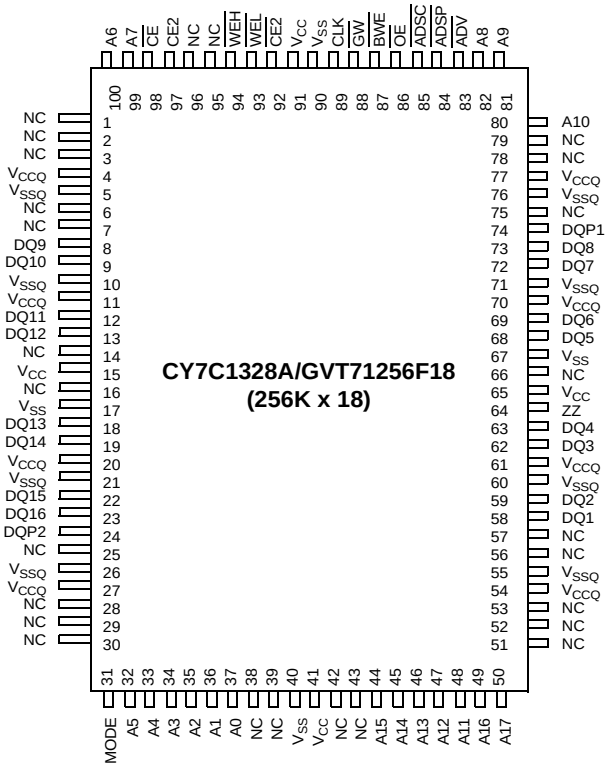
Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP
Top View





Pin Descriptions

Name	Type	Description
A0 A1 A2–A17 (A17 for X18)	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
$\overline{BW1}$ $\overline{BW2}$ $\overline{BW3}$ $\overline{BW4}$	Input-Synchronous	Byte Write Enables: A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1–DQ8 and DQP1. $\overline{BW2}$ controls DQ9–DQ16 and DQP2. $\overline{BW3}$ controls DQ17–DQ24 and DQP3. $\overline{BW4}$ controls DQ25–DQ32 and DQP4. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW. $\overline{BW1}$ is equal to $\overline{WEL}$ and $\overline{BW2}$ is equal to $\overline{WEH}$ for X18 device.
$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 38-bit (18-bit for X18 device) WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
CE2	Input-Synchronous	Chip Enable: This active HIGH input is used to enable the device.
$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
$\overline{ADSC}$	Input-Synchronous	Address Status Controller: This active LOW input causes device to be deselected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
ZZ	Input-Asynchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
DQ1–8 DQ9–16 DQ17–24 DQ25–32	Input/Output	Data Inputs/Outputs: Byte one is DQ1–DQ8. Byte two is DQ9–DQ16. Byte three is DQ17–DQ24. Byte four is DQ25–DQ32. Input data must meet set-up and hold times around the rising edge of CLK. X18 only has two bytes (Byte one and Byte two).
DQP1–DQP4	Input/Output	Parity Inputs/Outputs: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16. DQP3 is parity bit for DQ17–DQ24 and DQP4 is parity bit for DQ25–DQ32.
V_{CC}	Supply	Power Supply: +3.3V –5% and +10%.
V_{SS}	Ground	Ground: GND.
V_{CCQ}	I/O Supply	Output Buffer Supply: +2.5V (from 2.375V to V_{CC}).
V_{SSQ}	I/O Ground	Output Buffer Ground: GND.
NC	-	No Connect: These signals are not internally connected. User can connect them to V_{CC}, V_{SS}, or any signal. They can be left unconnected as floating.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes:

2. X = "Don't Care." H = logic HIGH, L = logic LOW.
   WRITE = L means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$]*$\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means [$\overline{BWE}$ + $\overline{BWa}$*$\overline{BWb}$]*$\overline{GW}$ equals HIGH.
3. BWa enables write to DQa. BWb enables write to DQb.
4. All inputs except $\overline{OE}$ must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

Partial Truth Table for READ/WRITE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) .....–55°C to +150°

Junction Temperature .....+150°

Power Dissipation..... 1.0W

Short Circuit Output Current..... 50 mA

Operating Range

Range	Ambient Temperature[9]	V_{CC}[10,11]
Com'l	0°C to +70°C	3.3V –5%/+10%

Note:
9. T_A is the case temperature.
10. Please refer to waveform (c)
11. Power Supply ramp-up should be monotonic.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[12, 13]	Data Inputs (DQxx)	1.7	V_{CC}+0.3	V
V_{IH}		All Other Inputs	1.7	4.6	V
V_{Il}	Input Low (Logic 0) Voltage[12, 13]		–0.3	0.7	V
IL_I	Input Leakage Current[14]	$0V \le V_{IN} \le V_{CC}$	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–2	2	µA
V_{OH}	Output High Voltage[12, 15]	I_{OH} = –2.0 mA	1.7		V
V_{OL}	Output Low Voltage[12, 15]	I_{OL} = 2.0 mA		0.7	V
V_{CC}	Supply Voltage[12]		3.135	3.6	V
V_{CCQ}	I/O Supply Voltage[12]		2.375	V_{CC}	V

Parameter	Description	Conditions	Typ.	-4	-4.4	-5	-6	Unit
I_{CC}	Power Supply Current: Operating[16, 17, 18]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} = Max.; outputs open	150	425	400	375	350	mA
I_{SB2}	CMOS Standby[17, 18]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	10	20	20	20	20	mA
I_{SB4}	Clock Running[17, 18]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ min.	40	90	80	70	60	mA

Capacitance[19]

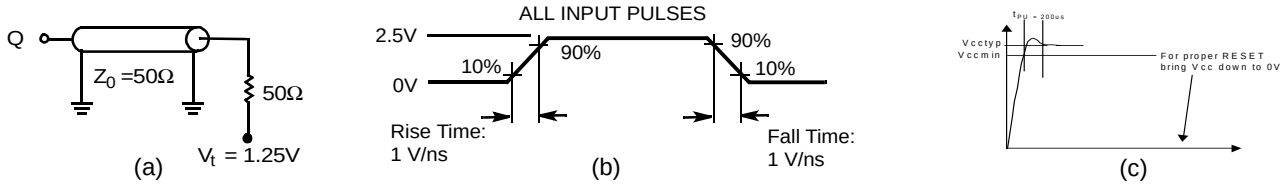
Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	7	pF
C_O	Input/Output Capacitance (DQ)		7	8	pF

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB	Θ_{JA}	25	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	9	°C/W

Note:
12. All voltages referenced to V_{SS} (GND).
13. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot: $V_{IL} \le -2.0V$ for $t \le t_{KC}/2$
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. AC I/O curves are available upon request.
16. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
17. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
18. Typical values are measured at 3.3V, 25°C, and 8.5-ns cycle time.
19. This parameter is sampled.

AC Test Loads and Waveforms[20]



Switching Characteristics Over the Operating Range[21]

Parameter	Description	-3 166 MHz		-4 150 MHz		-5 133 MHz		-6 117 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	6.0		6.7		7.5		8.5		ns
t_{KH}	Clock HIGH Time	2.4		2.6		2.8		3.4		ns
t_{KL}	Clock LOW Time	2.4		2.6		2.8		3.4		ns
Output Times										
t_{KQ}	Clock to Output Valid		3.5		3.8		4.0		4.0	ns
t_{KQX}	Clock to Output Invalid	1.5		1.5		1.5		1.5		ns
t_{KQLZ}	Clock to Output in Low-Z[19, 22, 23]	0		0		0		0		ns
t_{KQHZ}	Clock to Output in High-Z[19, 22, 23]	1.5	6.0	1.5	6.7	1.5	7.5	1.5	8.5	ns
t_{OEQ}	OE to Output Valid[24]		3.5		3.5		3.8		3.8	ns
t_{OELZ}	OE to Output in Low-Z[19, 22, 23]	0		0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[19, 22, 23]		3.5		3.5		3.8		3.8	ns
Set-up Times										
t_S	Address, Controls, and Data In[25]	1.5		1.5		1.5		2.0		ns
Hold Times										
t_H	Address, Controls, and Data In[25]	0.5		0.5		0.5		0.5		ns

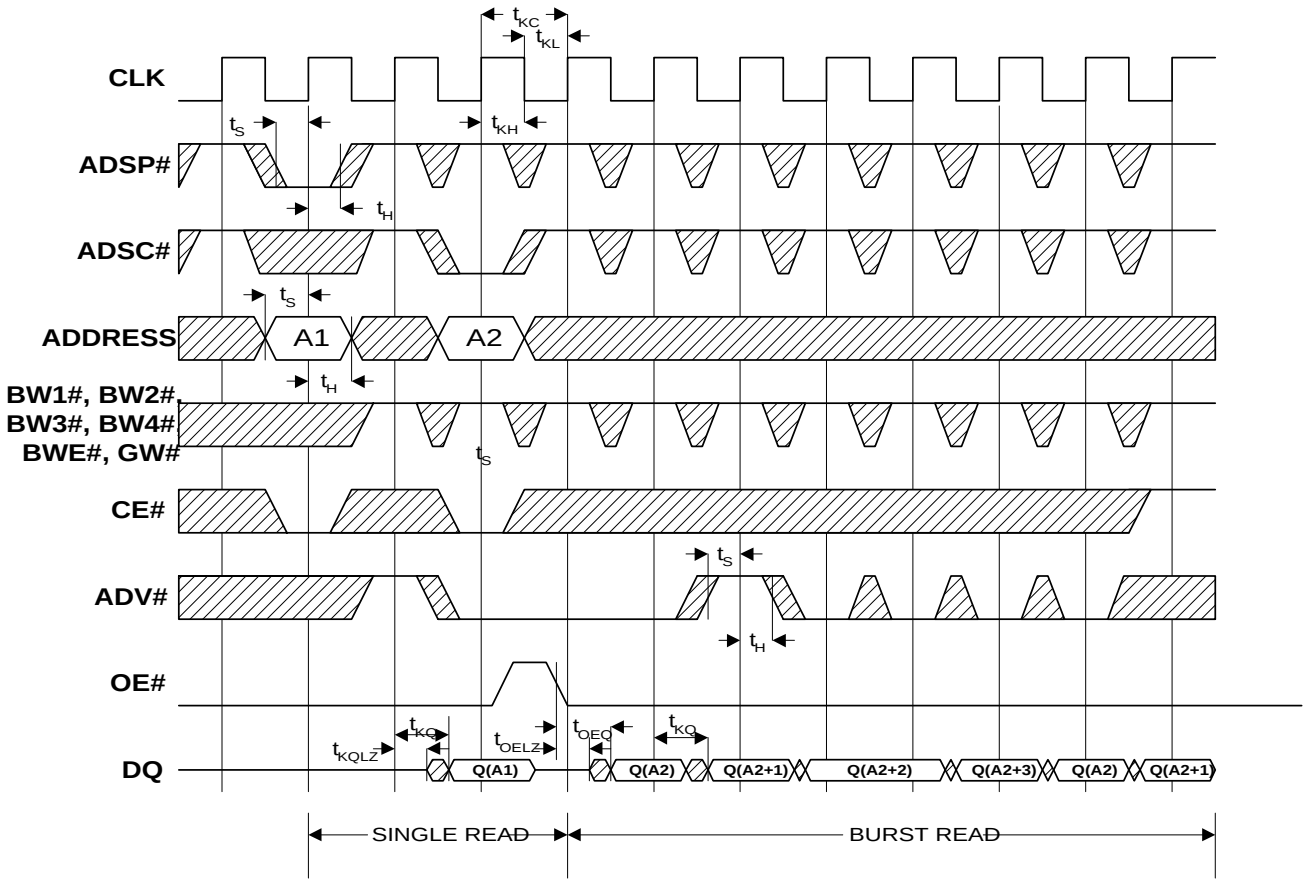
Typical Output Buffer Characteristics

Output High Voltage	Pull-Up Current			Output Low Voltage	Pull-Down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.		V_{OL} (V)	I_{OL} (mA) Min.	I_{OL}(mA) Max.
–0.5	–38	–105		–0.5	0	0
0	–38	–105		0	0	0
0.8	–38	–105		0.4	10	20
1.25	–26	–83		0.8	20	40
1.5	–20	–70		1.25	31	63
2.3	0	–30		1.6	40	80
2.7	0	–10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

Notes:
20. Overshoot: VIH(AC) <VDD + 1.5V for t <tTCYC/2; undershoot: VIL(AC) < 0.5V for t <tTCYC/2; power-up: VIH < 2.6V and VDD <2.4V and VDDQ < 1.4V for t<200 ms.
21. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
22. Output loading is specified with C_L = 5 pF as in AC Test Loads.
23. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
24. OE is a “Don’t Care” when a byte write enable is sampled LOW.
25. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “Don’t Care” as defined in the truth table.

Switching Waveforms

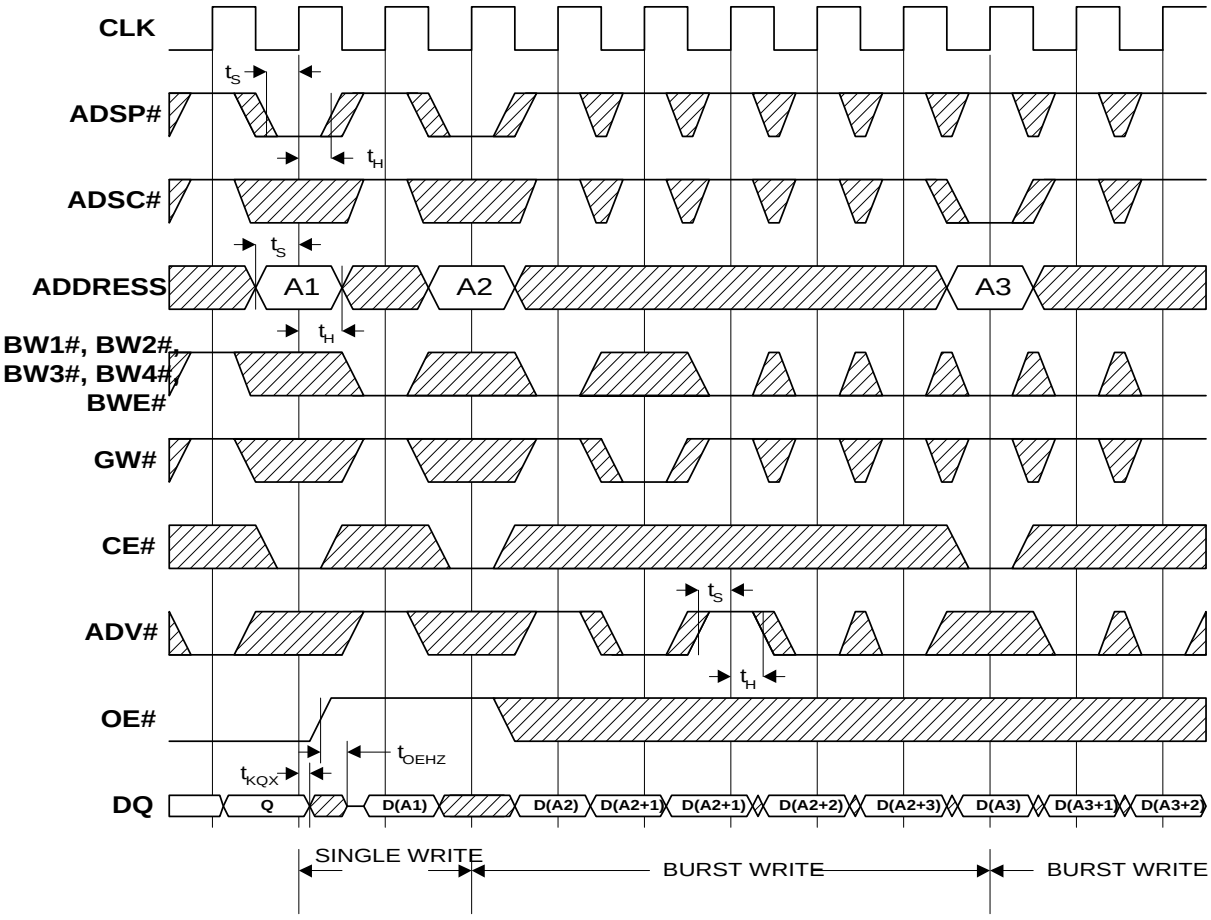
Read Timing[26, 27]



Notes:
26. $\overline{CE}$ active in this timing diagram means that all chip enables $\overline{CE}$, CE2, and $\overline{CE2}$ are active.
27. For X18 product, there are only BW1 (i.e., $\overline{WEL}$) and BW2 (i.e., $\overline{WEH}$) for byte write control.

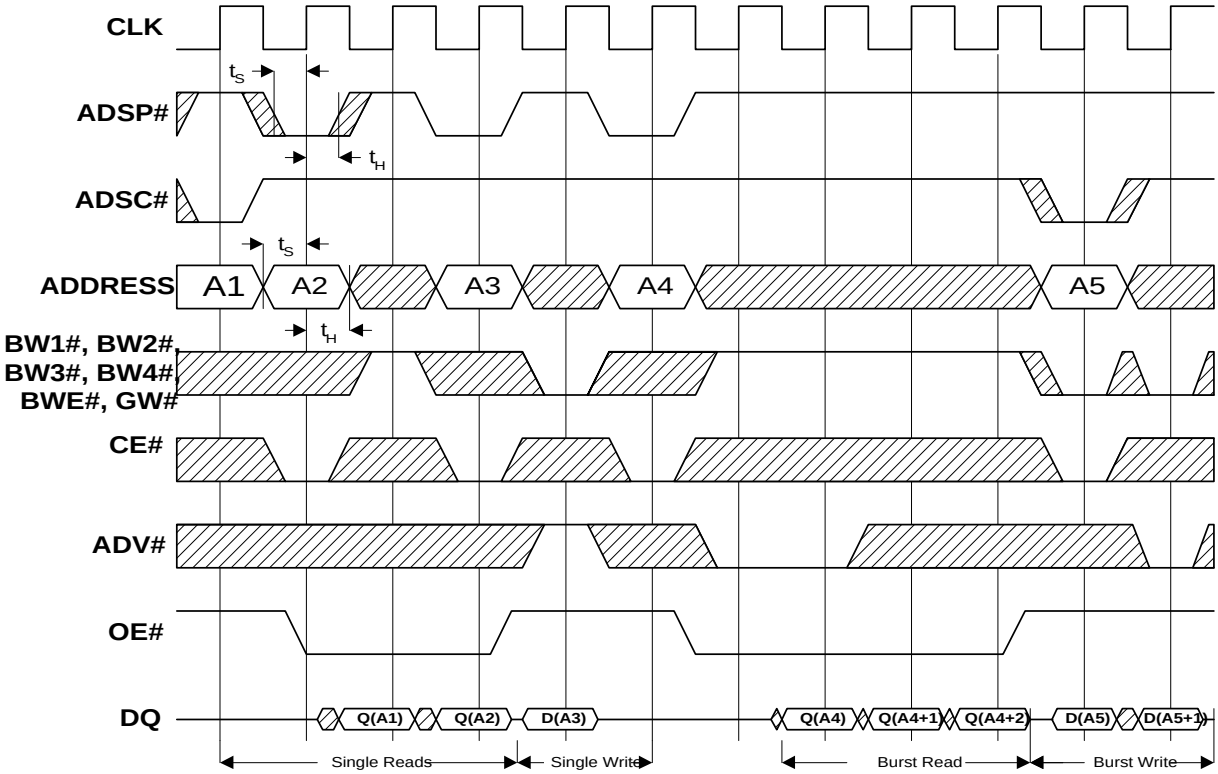
Switching Waveforms (continued)

Write Timing[26, 27]



Switching Waveforms (continued)

Read/Write Timing[26, 27]

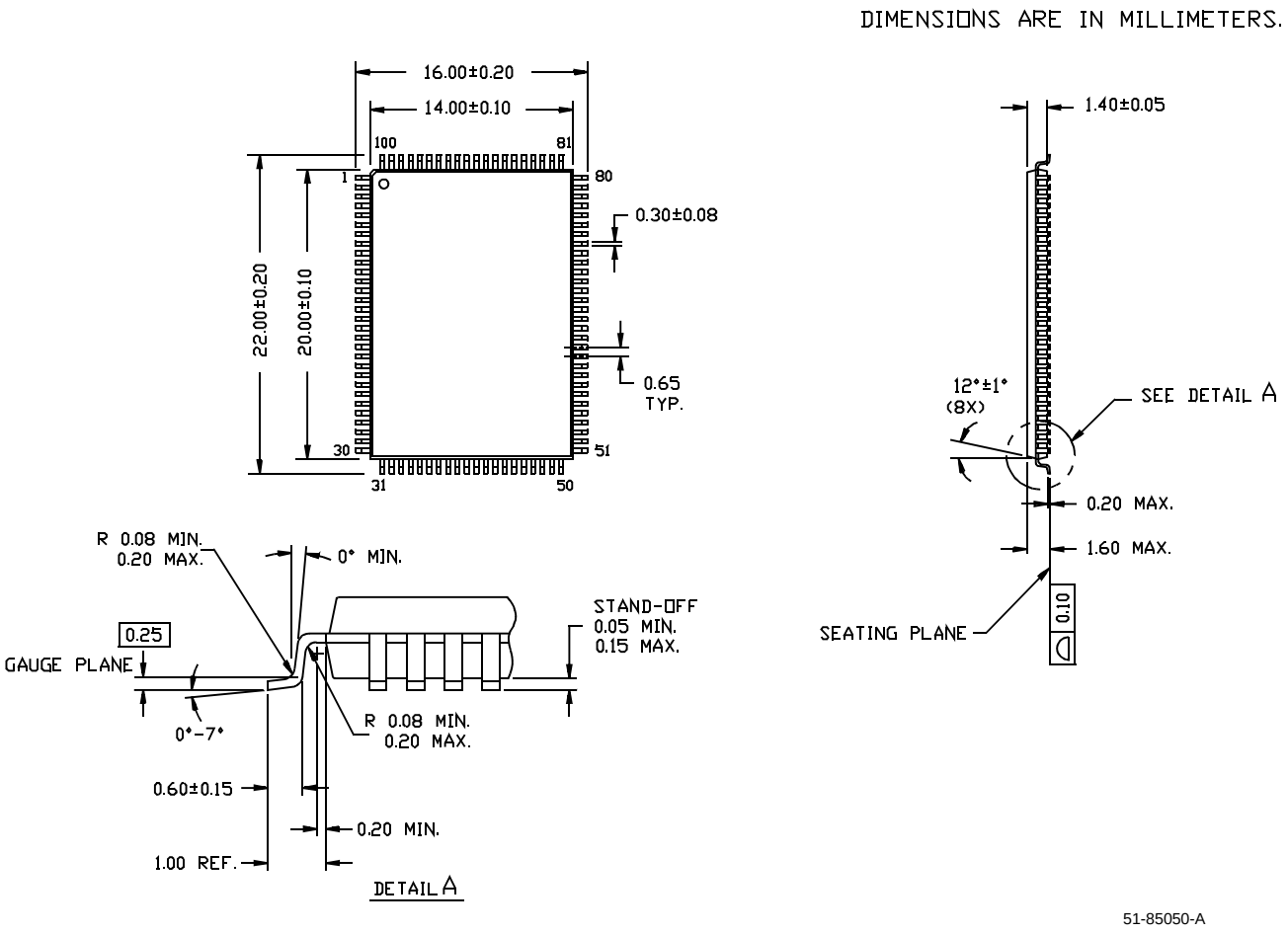


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1328A-166AC/ GVT71256F18T-3	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
150	CY7C1328A-150AC/ GVT71256F18T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
133	CY7C1328A-133AC/ GVT71256F18T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
117	CY7C1328A-117AC/ GVT71256F18T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
166	CY7C1348A-166AC/ GVT71128F36T-3	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
150	CY7C1348A-150AC/ GVT71128F36T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
133	CY7C1348A-133AC/ GVT71128F36T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
117	CY7C1348A-117AC/ GVT71128F36T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Document Title: CY7C1328A/GVT71256F18, CY7C1348A/GVT71128F36 128K x 36/256K x 18 Synchronous-Pipelined Cache RAM Document Number: 38-05152				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109896	09/22/01	SZV	Change from Spec number: 38-00999 to 38-05152
*A	111423	01/31/02	GLC	Removed preliminary from data sheet.
*B	123138	01/20/03	RBI	Add power up requirements to operating conditions information