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## **DS1200HE**

### 1200 Watts

### **Distributed Power System**

Front-end Bulk Power
Total Output Power:
180 to 264Vac: 1200W continuous
90 to 140Vac: 1000W/1200W<sup>1</sup> continuous







### **Special Features**

- 1200W output power
- High-power
- 1U x 2U power supply
- High-density design: 21.66W/in3
- Active Power Factor Correction
- EN61000-3-2 Harmonic compliance
- Inrush current control
- 80plus Platinum Efficiency
- N+1 or N+N Redundant
- Hot plug operation
- N + 1 redundant
- Active current sharing
- Full Digital control
- PMBus Compliant
- Input power reporting
- Compatible with Emerson's Universal PMBus GUI
- Reverse airflow option
- Two-year Warranty

## Compliance

- Conducted/Radiated EMI Class B
- ROHS

### Safety

- UL/cUL 60950 (UL Recognized)
- NEMKO+ CB Report EN60950
- CE Mark
- China CCC

Electrical Specifications					
Input					
Input Voltage range:	90-140Vac: 1000W / 1200W <sup>1</sup> 180-264Vac: 1200W				
Frequency:	47Hz - 63 Hz				
Efficiency:	94.0% peak				
Max Input Current:	15 Arms				
Inrush Current:	55Apk at 240Vac, cold start				
Conducted EMI:	Class B				
Radiated EMI:	Class B				
Power Factor:	0.9 typical				
ITHD:	10%				
Leakage Current:	1.4mA				
Hold-up Time:	12ms				

 $<sup>^{\</sup>mbox{\scriptsize 1}}$  1000W at forward air, 1200W at reverse air. See power derating table

Ordering Information						
DS1200-3	3.3V Stby, Forward airflow					
DS1200-3-002	5.0V Stby, Forward airflow					
DS1200-3-003	3.3V Stby, Reverse airflow					
DS1200-3-004	5.0V Stby, Reverse airflow					



ain DC Output	MIN	NOM	MAX
Nominal Setting:	-0.50%	12	0.50%
Total Output Regulation Range:	11.4V		12.6V
Dynamic Load Regulation Range:	11.4V		12.6V
Output Ripple:			120mVp-p
Output Current:	0A <sup>4</sup>		100.0A
Current Sharing:	Within +/-5% of full load rating		
Capacitive Loading:	2,000uF		40,000uF
Start-up from AC to Output:			2000ms
Output Rise Time:	5ms		50ms
tandby DC Output (VSB)			
Output Setpoint Range:	-1%	3.3V (5.0V)	1%
Total Output Regulation Range:	+5%		-5%
Dynamic Load Regulation Range:	+5%		-5%
Output Ripple:			50mVp-p
Output Current:	0		6.0A (4A)
Current Sharing:		N/A	
Capacitive Loading:	0uF		680uF
Start-up from AC to Output:			1000ms
Output Rise Time:	2ms		50ms
ROTECTIONS			
lain Output			
Over-Current Protection <sup>2</sup> :	120%		150%
Over-Voltage Protection 1:	13.5V		15.0V
Under-Voltage Protection:	10.5V		11.0V
Over-Temperature Protection:		Yes	
Fan Fault Protection:		Yes	
tandby Output			
Over-Current Protection <sup>3</sup> :			
Over-Voltage Protection <sup>3</sup> :			

<sup>1</sup>Latch mode
2Autorecovery if the overcurrent is less than 130% and last only for <1000ms. Otherwise, latch mode
3Standby protection is auto-recovery
4For output transient testing, the minimum load shall be at 10A

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put Signals			
PSON_L			
ctive LOW signal which enables/disables the 1 100pF decoupling capacitor is recommended	main output. Pulling this signal LOW will turn-on the main of at the system side.	output.	
		MIN	MAX
V <sub>II</sub>	Input logic level LOW		0.8V
	Input logiv level HIGH	2.0V	5.0V
I <sub>SOURCE</sub>	Current that may be sourced by this pin		2mA
ISINE	Current that may be sunk by this pin at low state		0.5mA
PSKILL_L			
irst break/Last Mate active LOW signal which or. A 100pF decoupling capacitor is also recon	enables/disables the main output. This signal will have to b nmended.	e pulled to ground at the syst	tem side with a 2200hm resis-
		MIN	MAX
V <sub>II</sub>	Input logic level LOW		0.8V
V <sub>II</sub> -	Input logic level HIGH	2.0V	5.0V
Isource	Current that may be sourced by this pin		2mA
	Current that may be sunk by this pin at low state		0.5mA
VSENSE+, VSENSE-, STBY_VSENSE+			
	e the remote sense lines for regulation. Each line will comp	ensate for a maximum of 100	mV.
Output Signals ACOK_L			
Output Signals  ACOK_L  Signal used to indicate the presence of AC inpurchase to the signal used to indicate the presence of AC inpurchile a logic level HIGH will indicate that AC hat his is an open collector/drain output. This pin	ut to the power supply. A logic level LOW will indicate that	the AC input to the power sup	pply is within the operating ra
Output Signals  ACOK_L  Signal used to indicate the presence of AC inpurchase to the signal used to indicate the presence of AC inpurchile a logic level HIGH will indicate that AC hat his is an open collector/drain output. This pin	ut to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V insi	the AC input to the power sup	pply is within the operating ra
Output Signals  ACOK_L  Signal used to indicate the presence of AC inputhile a logic level HIGH will indicate that AC haths is an open collector/drain output. This pintonnected to a 100pF decoupling capacitor and	ut to the power supply. A logic level LOW will indicate that is been lost. is pulled high by a 1.0kohm resistor connected to 3.3V insid pulled down by a 100kohm resistor at the system side.	the AC input to the power sup de the power supply. It is reco	pply is within the operating ra
Output Signals  ACOK_L  Signal used to indicate the presence of AC inputy while a logic level HIGH will indicate that AC haths is an open collector/drain output. This pind connected to a 100pF decoupling capacitor and V	at to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW	the AC input to the power sup de the power supply. It is reco	pply is within the operating ra ommended that this pin be MAX
Output Signals  ACOK_L  Signal used to indicate the presence of AC inputhile a logic level HIGH will indicate that AC haths is an open collector/drain output. This pintonnected to a 100pF decoupling capacitor and VIL	ut to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V insid pulled down by a 100kohm resistor at the system side.  Output logic level LOW Output logic level HIGH	the AC input to the power sup de the power supply. It is reco	pply is within the operating ra ommended that this pin be MAX 0.6V
Dutput Signals  ACOK_L  Signal used to indicate the presence of AC inputy while a logic level HIGH will indicate that AC hath has is an open collector/drain output. This pintonnected to a 100pF decoupling capacitor and VIII  VIII  VIII  VIII  SOURCE	at to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW Output logic level HIGH Current that may be sourced by this pin	the AC input to the power sup de the power supply. It is reco	pply is within the operating radiommended that this pin be  MAX  0.6V  5.0V  3.3mA
Output Signals  ACOK_L  Signal used to indicate the presence of AC inputhile a logic level HIGH will indicate that AC har in the signal of the	ut to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V insid pulled down by a 100kohm resistor at the system side.  Output logic level LOW Output logic level HIGH	the AC input to the power sup de the power supply. It is reco	pply is within the operating rate of the properties of the propert
Output Signals  ACOK_L  Signal used to indicate the presence of AC inputhile a logic level HIGH will indicate that AC hat has an open collector/drain output. This pin connected to a 100pF decoupling capacitor and VIII  VIII  VIII  SOURCE  ISINK  PWR_GOOD / PWOK_H	out to the power supply. A logic level LOW will indicate that his been lost.  It is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW  Output logic level HIGH  Current that may be sourced by this pin  Current that may be sunk by this pin at low state	the AC input to the power sup de the power supply. It is reco MIN 2.0V	pply is within the operating rate operating rate operating management of the properties of the propert
Dutput Signals  ACOK_L  Signal used to indicate the presence of AC inputyhile a logic level HIGH will indicate that AC hath is is an open collector/drain output. This pint connected to a 100pF decoupling capacitor and VIL  VIII  VIII  SOURCE  PWR_GOOD / PWOK_H  Signal used to indicate that main output volta will be driven LOW when the output falls below this signal also gives an advance warning when	at to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW Output logic level HIGH Current that may be sourced by this pin Current that may be sunk by this pin at low state  ge is within regulation range. The PWR_GOOD/PWOK_H side of the pulled high by a 1.0kohm resistor connected to	the AC input to the power sup de the power supply. It is reco MIN 2.0V gnal will be driven HIGH wher or system shutdown request.	pply is within the operating radiommended that this pin be  MAX 0.6V 5.0V 3.3mA 0.7mA  In the output voltage is valid and More details in the Timing
Dutput Signals  ACOK_L  signal used to indicate the presence of AC inputy while a logic level HIGH will indicate that AC haths is an open collector/drain output. This pintonnected to a 100pF decoupling capacitor and VIL  VIL  VIL  ISOURCE  ISINK  PWR_GOOD / PWOK_H  Signal used to indicate that main output volta will be driven LOW when the output falls below this signal also gives an advance warning when section. This is an open collector/drain output.	at to the power supply. A logic level LOW will indicate that as been lost. is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW Output logic level HIGH Current that may be sourced by this pin Current that may be sunk by this pin at low state  ge is within regulation range. The PWR_GOOD/PWOK_H side of the pulled high by a 1.0kohm resistor connected to	the AC input to the power sup de the power supply. It is reco MIN 2.0V gnal will be driven HIGH wher or system shutdown request.	pply is within the operating radiommended that this pin be  MAX 0.6V 5.0V 3.3mA 0.7mA  The output voltage is valid a
Dutput Signals  ACOK_L  ignal used to indicate the presence of AC inpuvhile a logic level HIGH will indicate that AC habis is an open collector/drain output. This pin onnected to a 100pF decoupling capacitor and VIL  VIH  ISOURCE  ISINK  PWR_GOOD / PWOK_H  Signal used to indicate that main output volta vill be driven LOW when the output falls below his signal also gives an advance warning where ection. This is an open collector/drain output. bin be connected to a 100pF decoupling capacitation.	out to the power supply. A logic level LOW will indicate that as been lost. It is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW  Output logic level HIGH  Current that may be sourced by this pin  Current that may be sunk by this pin at low state  ge is within regulation range. The PWR_GOOD/PWOK_H side in there is an impending power loss due to loss of AC input This pin is pulled high by a 1.0kohm resistor connected to citor and pulled down by a 10kohm resistor."	the AC input to the power sup de the power supply. It is reco MIN 2.0V gnal will be driven HIGH wher or system shutdown request. 3.3V inside the power supply.	pply is within the operating radiommended that this pin be  MAX 0.6V 5.0V 3.3mA 0.7mA  The output voltage is valid an More details in the Timing It is recommended that this
Dutput Signals  ACOK_L  Isignal used to indicate the presence of AC input while a logic level HIGH will indicate that AC hath is is an open collector/drain output. This pin connected to a 100pF decoupling capacitor and VIII  VIII  VIII  Signal used to indicate that main output voltate will be driven LOW when the output falls below this signal also gives an advance warning where the connected to a 100pF decoupling capacity in the connected to a 100pF decoupling capacity villation.	at to the power supply. A logic level LOW will indicate that his been lost. It is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW  Output logic level HIGH  Current that may be sourced by this pin  Current that may be sunk by this pin at low state  ge is within regulation range. The PWR_GOOD/PWOK_H side of the under-voltage threshold. In there is an impending power loss due to loss of AC input This pin is pulled high by a 1.0kohm resistor connected to citor and pulled down by a 10kohm resistor."	the AC input to the power sup de the power supply. It is reco MIN 2.0V gnal will be driven HIGH wher or system shutdown request. 3.3V inside the power supply.	pply is within the operating radius of the properties of the prope
Dutput Signals  ACOK_L  Signal used to indicate the presence of AC inputyhile a logic level HIGH will indicate that AC hath is is an open collector/drain output. This pintonnected to a 100pF decoupling capacitor and Source of	out to the power supply. A logic level LOW will indicate that as been lost. It is pulled high by a 1.0kohm resistor connected to 3.3V inside pulled down by a 100kohm resistor at the system side.  Output logic level LOW  Output logic level HIGH  Current that may be sourced by this pin  Current that may be sunk by this pin at low state  ge is within regulation range. The PWR_GOOD/PWOK_H side in there is an impending power loss due to loss of AC input This pin is pulled high by a 1.0kohm resistor connected to citor and pulled down by a 10kohm resistor."	the AC input to the power sup de the power supply. It is reco MIN 2.0V gnal will be driven HIGH wher or system shutdown request. 3.3V inside the power supply.	pply is within the operating rates ommended that this pin be  MAX 0.6V 5.0V 3.3mA 0.7mA  In the output voltage is valid and the output voltage is valid and the Timing of the this of the MAX

# **Electrical Specifications**

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Output Signals			
PS_PRESENT			
Signal used to indicate to the system that a po	wer supply is inserted in the power bay. This signal is pulled	d down to ground within the po	wer supply.
PS_INTERRUPT			
	indicate to the system that a change in power supply status red by a CLEAR_FAULT command. A 100pF decoupling capa		e triggered by faults such as OVP
		MIN	MAX
V <sub>II</sub>	Output logic level LOW		0.8V
V <sub>II</sub>	Output logic level HIGH	2.0V	5.0V
l <sub>SOURCE</sub>	Current that may be sourced by this pin		4mA
ISINE	Current that may be sunk by this pin at low state		4mA
BUS Signals			
ISHARE			
Bus signal used by the power supply for active	up to 8.0V, which corresponds to the maximum	n for n+n sharing will refer to thi	is bus voltage inorder to load
Bus signal used by the power supply for active hare.	The range of this signal for active sharing will be	n for n+n sharing will refer to thi	is bus voltage inorder to load  MAX
Bus signal used by the power supply for active hare. VOLTAGE RANGE	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum	<u> </u>	<u>-</u>
sus signal used by the power supply for active hare. VOLTAGE RANGE	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.	MIN	MAX
Bus signal used by the power supply for active hare. VOLTAGE RANGE	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit	MIN 7.65	MAX 8.35
Bus signal used by the power supply for active hare.  VOLTAGE RANGE  I SHARE	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit  Voltage at 50% load, stand-alone unit	MIN 7.65 3.65	MAX 8.35 4.35
Bus signal used by the power supply for active hare.  VOLTAGE RANGE  I SHARE	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit  Voltage at 50% load, stand-alone unit  Voltage at 0% load, stand-alone unit	MIN 7.65 3.65	MAX 8.35 4.35 0.5
Bus signal used by the power supply for active hare.  VOLTAGE RANGE  ISHARE Voltage  ISOURCE  SCL, SDA	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit  Voltage at 50% load, stand-alone unit  Voltage at 0% load, stand-alone unit	MIN 7.65 3.65 0	MAX 8.35 4.35 0.5 80mA
lus signal used by the power supply for active hare.  VOLTAGE RANGE  ISHARE  Voltage  SCL, SDA  Clock and data signals defined as per I2C requi	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit  Voltage at 50% load, stand-alone unit  Voltage at 0% load, stand-alone unit  Current that may be sourced by this pin	MIN 7.65 3.65 0	MAX 8.35 4.35 0.5 80mA
us signal used by the power supply for active hare.  VOLTAGE RANGE  ISHARE  Voltage  SCL, SDA  Clock and data signals defined as per I2C requires the system side.	The range of this signal for active sharing will be up to 8.0V, which corresponds to the maximum output current.  Voltage at 100% load, stand-alone unit  Voltage at 50% load, stand-alone unit  Voltage at 0% load, stand-alone unit  Current that may be sourced by this pin	MIN 7.65 3.65 0 a 2.2kohm resistor to 3.3V and a	MAX 8.35 4.35 0.5 80mA a 100pF decoupling capacitor at

Note: All signal noise levels are below 400 mVpk-pk from 0-100 MHz.

### I2C Addressing Table

PMBUS ADDRESSING				
A1	A0	Address		
LOW	LOW	0xB0		
LOW	HIGH	0xB2		
HIGH	LOW	0xB4		
HIGH	HIGH	0xB6		

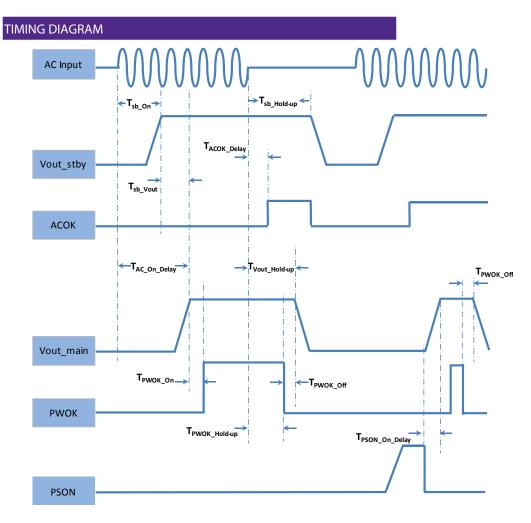
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LED INDICATORS				
A single bi-color LED is used to indicat	e the powe	er supply status.		
		Status LED		
NO AC II	NPUT TO PSU	Off		
AC PRESENT, STBY ON, MAIN	OUTPUT OFF	Blinking GREEN		
MAIN	OUTPUT ON	Solid GREEN		
OVER-VOLTAGE/UNDER-VOLT	AGE FAILURE	Blinking AMBER		
POWER SUPPLY FAILURE (OCP, OTP	, FAN FAULT)	Solid AMBER		
	- 1			
FIRMWARE REPORTING AND MONI	TORING			
OUTPUT LOADING	<u>'</u>	5 to 20%	20% to 50%	50% to 100%
INPUT VOLTAGE		+/-5%		
INPUT CURRENT		+/-0.7A fixed error +/-5%		
INPUT POWER	+	-/-10W at <125W input	<125W input +/-5%	
OUTPUT VOLTAGE		+/-4%		
OUTPUT CURRENT		0.5A fixed error	+/-5%	
TEMPERATURE		+/-5de	gC on the operating range	
FAN SPEED			Actual +/-250RPM	
PMBUS		YES		
REMOTE ON/OFF		YES		

## **Electrical Specifications**

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Timing Specifications							
	DESCRIPTION	MIN	MAX	UNIT			
Tsb_On	Delay from AC being applied to standby output being within regulation		1700	ms			
T <sub>AC_On_Delay</sub>	Delay from AC being applied to main output being within regulation		2000	ms			
T <sub>PWOK_On</sub>	Delay from output voltages within regulation limits to PWOK asserted	100	1000	ms			
T <sub>ACOK_Delay</sub>	Delay from loss of AC to deassertion of ACOK	7	14	ms			
T <sub>PWOK_Hold-up</sub>	Delay from loss of AC to deassertion of PWOK	11		ms			
T <sub>Vout_Hold-up</sub>	Delay from loss of AC to main output falling out of regulation	12		ms			
T <sub>sb_Hold-up</sub>	Delay from loss of AC to standby output falling out of regulation	400		ms			
TPWOK_Off	Delay from deassertion of PWOK to output falling out of regulation	1		ms			
T <sub>PSON</sub> _On_Delay	Delay from PSON assertion to output being within regulation		350	ms			
TPWOK_Off	Delay from deassertion of PWOK to output falling out of regulation	1		ms			
T <sub>PSON_On_Delay</sub>	Delay from PSON assertion to output being within regulation		350	ms			

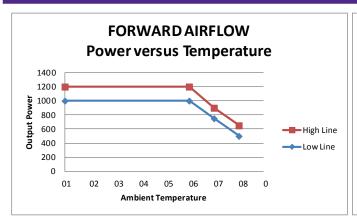


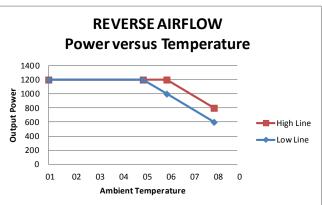
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## **Environmental Specifications**

Operating Temperatue:	-10 to 50°C, can provide derated power up to 70°C. See power derating curve
Operating Altitude:	up to 10,000 feet
Operating Relative Humidity:	10% to 90% non-condensing
Non-operating Temperature:	-40 to 85°C
Non-operating Relative Humidity:	10% to 95% non-condensing
Non-operating Altitude:	up to 50,000 feet
Vibration and Shock:	Standard oprating/non-operating random shock and vibration
ROHS Compliance:	Yes
MTBF	200,000 hours using Bell Core TR-332, issue 6 specification, Method 1 Case 3 at 25degC ambient at full load.
Operating Life	Minimum of 5 years
Reliability	All electronic component derating analysis and capacitor life calculation is done as per Emerson Network Power standards. The QAV report will be available upon request.

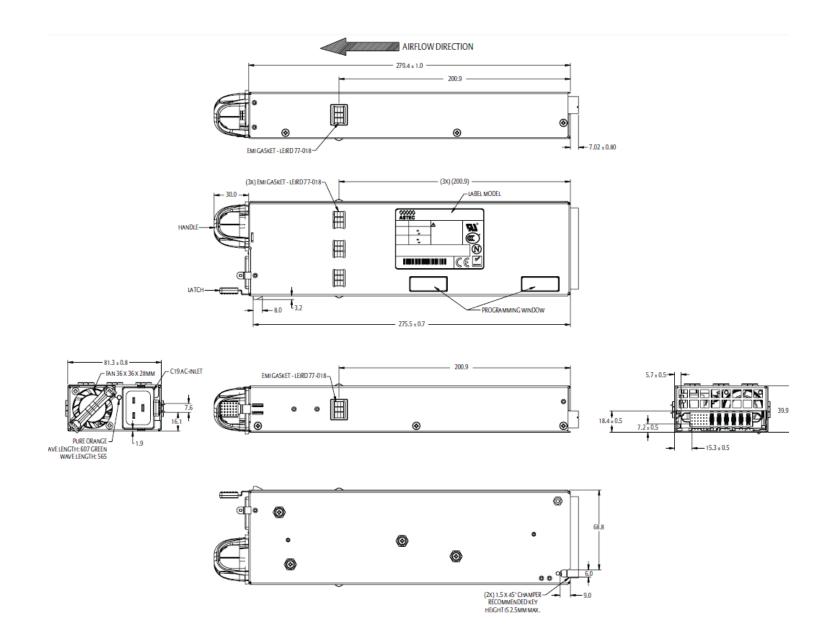
### POWER DERATING CURVE





# **Mechanical Specifications**

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## **Mechanical Specifications**

#### DC Output Connector Pinout Assignment

Male connector as viewed from the rear of the supply:

D1	D2	D3	D4	D5	D6						
C1	C2	C3	C4	C5	C6	DD1	PB2	חחח	DD 4	חחר	DD.C
B1	B2	В3	B4	B5	В6	РВІ	PBZ	PB3	PB4	PBS	PBO
A1	A2	А3	A4	A5	A6						

#### Power Supply Side

- 1. FCI Power Blade 51721 series 51721-10002406AA
- 2. Molex Power Connector SD-87667 series 87667-7002

### Mating Connector (System Side)

- FCI Power Blade

   51741-10002406CC
   Straight Pins

   FCI Power Blade

   51761-10002406AALF
   Right Angle
- 3. Any other approved equivalent

Pin Signal Name  PB 1 Main output return  PB 2 Main output return  PB 3 Main output return  PB 4 + Main output  PB 5 + Main output  PB 6 + Main output  A1 PSON_L  A2 Main output remote sense return,  VSENSE-  A3 Spare  A4 PS_PRESENT  A5 STAND-BY, +VSB  A6 STAND-BY RETURN, -VSB  B1 ACOK_H (AC Input Present)  B2 Main output remote sense, VSENSE+  B3 ISHARE  B4 PS_INHIBIT / PSKILL_LI  B5 STAND-BY  B6 STAND-BY  B7 STAND-BY  B7 STAND-BY  B8 STAND-BY  B9 STAND-BY  B1 STAND-BY  B1 ACOK_H (AC Input Present)  B2 Main output remote sense, VSENSE+  B3 ISHARE  B4 PS_INHIBIT / PSKILL_LI  B5 STAND-BY  B6 STAND-BY  B7 STAND-BY  B8 STAND-BY  B9 STAND-BY  B1 STAND-BY  B1 ACOK_H (AC Input Present)  B2 Main output remote sense, VSENSE+  B3 ISHARE  B4 PS_INHIBIT / PSKILL_LI  B5 STAND-BY  B6 STAND-BY RETURN  C1 SDA (I²C Clock Signal)  C2 SCL (I²C Clock Signal)  C3 POWER GOOD/ PWOK_H  C4 Spare  C5 STAND-BY, +VSB  C6 STAND-BY RETURN  D1 A0 (I²C Address BIT 0 Signal)  D2 A1 (I²C Address BIT 1 Signal)  D3 PS_INTERRUPT (Alarm)  D4 STAND-BY RMT SENSE, VSENSE_STBY  D5 STAND-BY, +VSB  D6 STAND-BY RETURN, -VSB	PIII ASSI	gnments
PB 2 Main output return PB 3 Main output return PB 4 + Main output PB 5 + Main output PB 6 + Main output A1 PSON_L A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY B9 STAND-BY B1 STAND-BY B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I²C Clock Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	Pin	Signal Name
PB 3 Main output return PB 4 + Main output PB 5 + Main output PB 6 + Main output A1 PSON_L A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY B9 STAND-BY B1 STAND-BY B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I²C Clock Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	PB 1	Main output return
PB 4 + Main output PB 5 + Main output PB 6 + Main output A1 PSON_L A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY B9 STAND-BY B1 STAND-BY B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I²C Clock Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	PB 2	Main output return
PB 5 + Main output PB 6 + Main output A1 PSON_L A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY B9 STAND-BY B1 ACOK_H (AC Input Present) B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I2C Clock Signal) C2 SCL (I2C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I2C Address BIT 0 Signal) D2 A1 (I2C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	PB 3	Main output return
PB 6 + Main output A1 PSON_L A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY B9 STAND-BY B1 ACOK_H (AC Input Present) B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I2C Clock Signal) C2 SCL (I2C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I2C Address BIT 0 Signal) D2 A1 (I2C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	PB 4	+ Main output
A1 PSON_L  A2 Main output remote sense return, VSENSE- A3 Spare  A4 PS_PRESENT  A5 STAND-BY, +VSB  A6 STAND-BY RETURN, -VSB  B1 ACOK_H (AC Input Present)  B2 Main output remote sense, VSENSE+ B3 ISHARE  B4 PS_INHIBIT / PSKILL_LI  B5 STAND-BY  B6 STAND-BY RETURN  C1 SDA (I²C Data Signal)  C2 SCL (I²C Clock Signal)  C3 POWER GOOD/ PWOK_H  C4 Spare  C5 STAND-BY, +VSB  C6 STAND-BY RETURN  D1 A0 (I²C Address BIT 0 Signal)  D2 A1 (I²C Address BIT 1 Signal)  D3 PS_INTERRUPT (Alarm)  D4 STAND-BY RMT SENSE, VSENSE_STBY  D5 STAND-BY, +VSB	PB 5	+ Main output
A2 Main output remote sense return, VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY B7 STAND-BY B8 STAND-BY RETURN C1 SDA (I2C Data Signal) C2 SCL (I2C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I2C Address BIT 0 Signal) D2 A1 (I2C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		·
A2 VSENSE- A3 Spare A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	A1	
A4 PS_PRESENT A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	A2	•
A5 STAND-BY, +VSB A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	A3	Spare
A6 STAND-BY RETURN, -VSB B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		·
B1 ACOK_H (AC Input Present) B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		,
B2 Main output remote sense, VSENSE+ B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY, ETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		· ·
B3 ISHARE B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	B1	ACOK_H (AC Input Present)
B4 PS_INHIBIT / PSKILL_LI B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I²C Data Signal) C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		
B5 STAND-BY B6 STAND-BY RETURN C1 SDA (I <sup>2</sup> C Data Signal) C2 SCL (I <sup>2</sup> C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		101171112
B6 STAND-BY RETURN C1 SDA (I <sup>2</sup> C Data Signal) C2 SCL (I <sup>2</sup> C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	B4	PS_INHIBIT / PSKILL_LI
C1 SDA (I <sup>2</sup> C Data Signal) C2 SCL (I <sup>2</sup> C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		
C2 SCL (I²C Clock Signal) C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I²C Address BIT 0 Signal) D2 A1 (I²C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	B6	STAND-BY RETURN
C3 POWER GOOD/ PWOK_H C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	C1	SDA (I <sup>2</sup> C Data Signal)
C4 Spare C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	C2	SCL (I <sup>2</sup> C Clock Signal)
C5 STAND-BY, +VSB C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	C3	POWER GOOD/ PWOK_H
C6 STAND-BY RETURN D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	C4	Spare
D1 A0 (I <sup>2</sup> C Address BIT 0 Signal) D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB		
D2 A1 (I <sup>2</sup> C Address BIT 1 Signal) D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	C6	
D3 PS_INTERRUPT (Alarm) D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	D1	A0 (I <sup>2</sup> C Address BIT 0 Signal)
D4 STAND-BY RMT SENSE, VSENSE_STBY D5 STAND-BY, +VSB	D2	A1 (I <sup>2</sup> C Address BIT 1 Signal)
D5 STAND-BY, +VSB	D3	PS_INTERRUPT (Alarm)
	D4	STAND-BY RMT SENSE, VSENSE_STBY
D6 STAND-BY RETURN, -VSB	D5	STAND-BY, +VSB
	D6	STAND-BY RETURN, -VSB

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