



Integrated Device Technology, Inc.

4-BIT BUS SWITCH

IDT74FST3125

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
FST3xxx – 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and SOIC

DESCRIPTION:

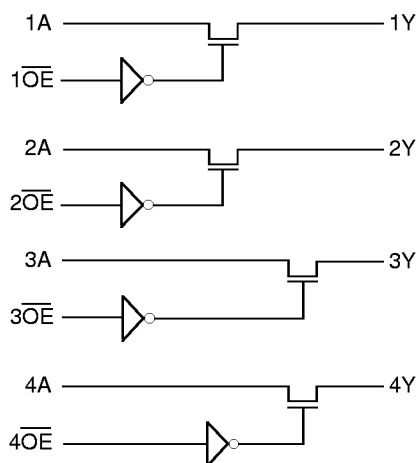
The FST3125 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source

capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

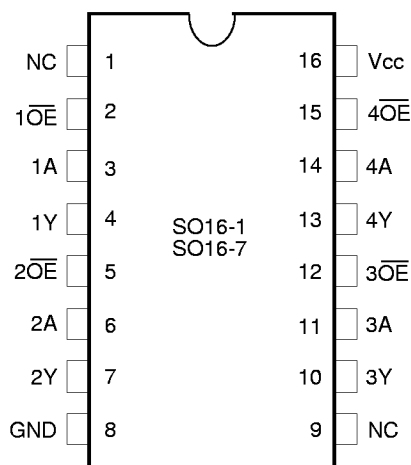
The FST3125 is a 4-bit TTL-compatible bus switch. The xOE pins provide individual enable control for each of the four bits.

FUNCTIONAL BLOCK DIAGRAM



3471 drw 01

PIN CONFIGURATION



SOIC/QSOP
TOP VIEW

3471 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
1A-4A	I/O	Bus A
1Y-4Y	I/O	Bus B
NC	—	No Connect
1OE, 4OE	I	Bus Switch Enable (Active LOW)

3471 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

AUGUST 1996

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

NOTES:

3471 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC}, Control and Switch terminals.

FUNCTION TABLE

\overline{OE}	Y	Description
H	Hi-Z	Disconnect
L	A	Connect

3471 tbl 03

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
C _{IN}	Control Input Capacitance		4	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

3471 tbl 04

- Capacitance is characterized but not tested
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max. V _I = V _{CC}	—	—	±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max. V _I = GND	—	—	±1	μA
I _{OZH}	High Impedance Output Current	V _{CC} = Max. V _O = V _{CC}	—	—	±1	μA
I _{OZL}	(3-State Output pins)	V _{CC} = Max. V _O = GND	—	—	±1	μA
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾	—	300	—	mA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
R _{ON}	Switch On Resistance ⁽⁴⁾	V _{CC} = Min. V _{IN} = 0.0V I _{ON} = 30mA	—	5	7	Ω
		V _{CC} = Min. V _{IN} = 2.4V I _{ON} = 15mA	—	10	15	Ω
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	μA
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}	—	0.1	3	μA

NOTES:

3471 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	30	40	$\mu\text{A}/$ MHz/ Switch
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling (4 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ $V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	1.2 1.5	1.6 2.4	mA

NOTES:

3471 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_i N)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$
 $\text{NT} = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_i = \text{Input Frequency}$
 $N = \text{Number of Switches Toggling at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	Max.	Unit
t_{PLH}	Data Propagation Delay	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	0.25	ns
t_{PHL}	A to Y, Y to A ^(3,4)		—	—	0.25	ns
t_{PZH}	Switch Turn on Delay		1.5	—	6.5	ns
t_{PZL}	$\overline{\text{OE}}$ to A, Y		1.5	—	6.5	ns
t_{PHZ}	Switch Turn off Delay		1.5	—	5.5	ns
t_{PLZ}	$\overline{\text{OE}}$ to A, Y ⁽³⁾	1.5	—	5.5	ns	
$ Q_C $	Charge Injection ^(5,6)	—	—	1.5	—	pC

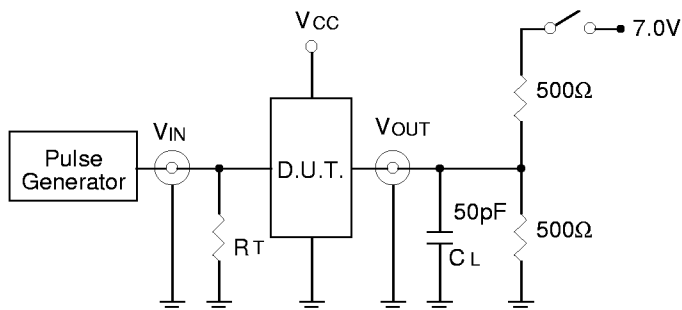
NOTES:

3471 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10M Ω scope probe, $V_{IN} = 0.0$ volts.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3471 drw 03

SWITCH POSITION

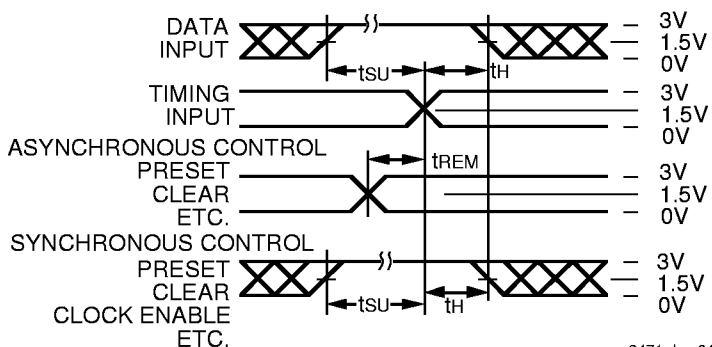
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

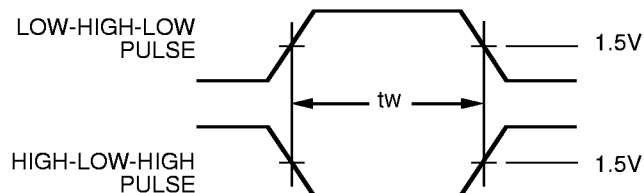
3471 Ink 08

SET-UP, HOLD AND RELEASE TIMES



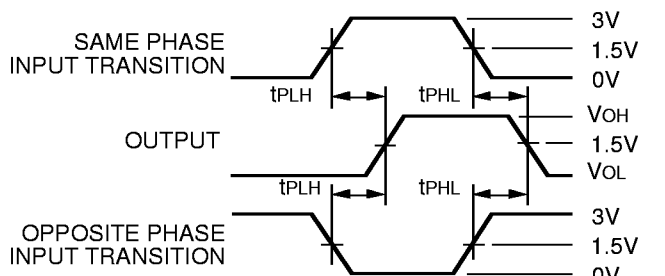
3471 drw 04

PULSE WIDTH



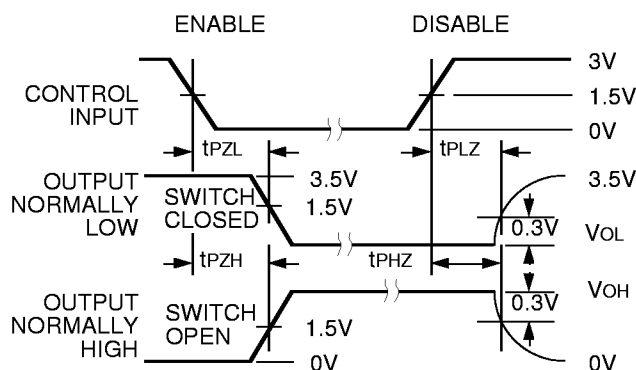
3471 drw 05

PROPAGATION DELAY



3471 drw 06

ENABLE AND DISABLE TIMES



3471 drw 07

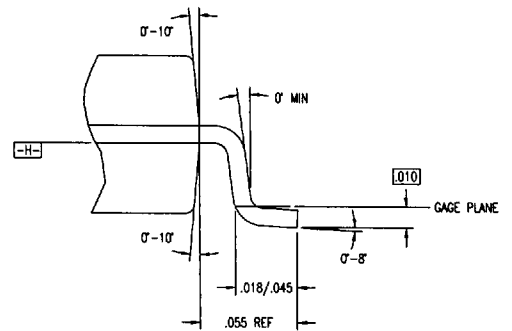
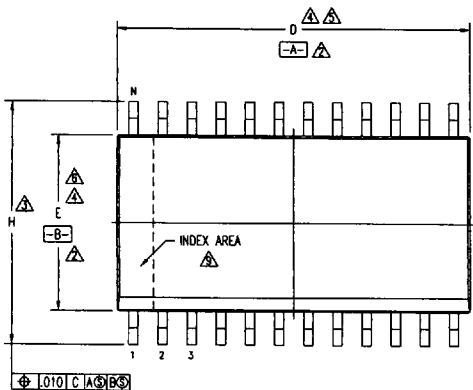
NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

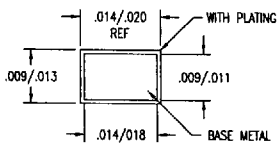
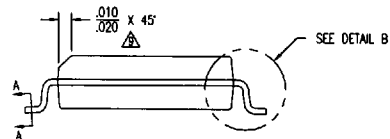
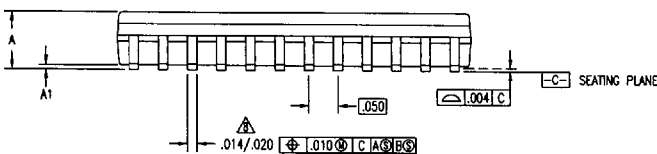
PACKAGE DIAGRAM OUTLINES

SOIC

REVISIONS				
DCH	REV	DESCRIPTION	DATE	APPROVED
27843	06	REDRAW TO JEDEC FORMAT	03/15/95	



DETAIL B



SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 492-8874 TWR: 910-338-2070	
DECIMAL	ANGULAR	±	
XXX±			
XXXX±			
XXXX±			
APPROVALS	DATE	TITLE	PS PACKAGE OUTLINE
DRWN	03/15/95		.300" BODY WIDTH SOIC
CHECKED			.050" PITCH
SIZE	DRAWING No.		REV
C	PSC-4007		06
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES


SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	S016-1				S018-1				S020-2				S024-2				S028-2			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA				AB				AC				AD				AE			
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104	
A1	.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012	
D	.403	.408	.413	4,5	.447	.454	.462	4,5	.497	.504	.511	4,5	.600	.607	.614	4,5	.700	.706	.712	4,5
E	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6
H	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3
N	16				18				20				24				28			

NOTES:

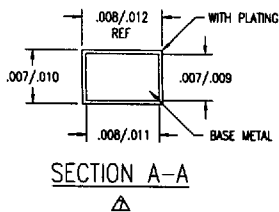
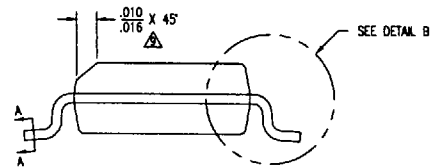
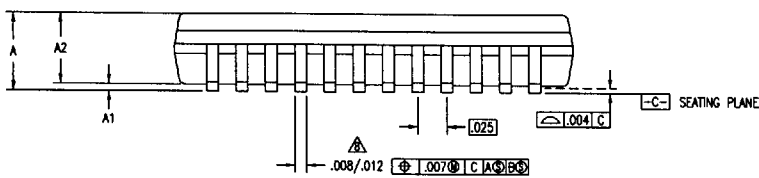
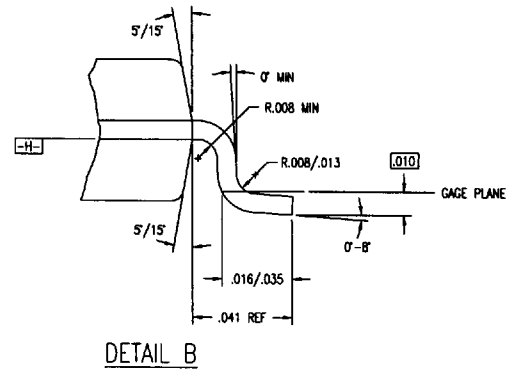
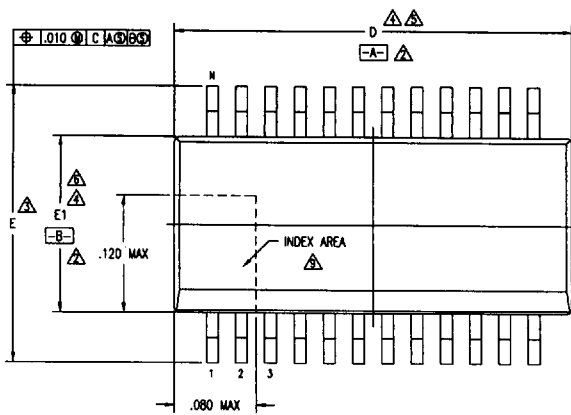
- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSION H TO BE DETERMINED AT SEATING PLANE [-C-]
- △ DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- △ DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- △ THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- 10 ALL DIMENSIONS ARE IN INCHES
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-013, VARIATION AA, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWR: 910-338-2070
DECIMAL	ANGULAR	
XX±	±	
XXXX±		
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>Ad</i>	03/15/98	PS PACKAGE OUTLINE
CHECKED		.300" BODY WIDTH SOIC
		.050" PITCH
		SIZE C DRAWING No. PSC-4007
		REV 06
DO NOT SCALE DRAWING		

4825771 0021977 67T

PACKAGE DIAGRAM OUTLINES
SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/16/93	T. WJ
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. WJ
28047	02	ADD 28 LD	08/15/95	



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DECIMAL	ANGULAR	
±	±	
DRANK	DATE	TITLE
CHECKED	12/15/93	PC PACKAGE OUTLINE .150" BODY WIDTH SSOP .025" PITCH
SIZE	DRAWING No.	REV
C	PSC-4040	02
DO NOT SCALE DRAWING		

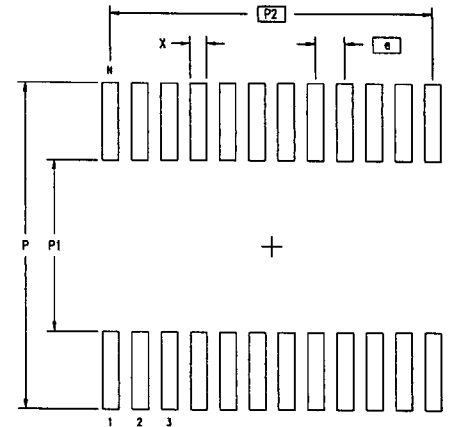
116

PACKAGE DIAGRAM OUTLINES
SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/18/93	T. VU
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	

SYMBOL	DWG # S016-7				DWG # S020-8				DWG # S024-8				DWG # S028-9			
	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.061	.064	.068		.061	.064	.068		.061	.064	.068		.061	.064	.068	
A1	.004	.006	.010		.004	.006	.010		.004	.006	.010		.004	.006	.010	
A2	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11
D	.189	.194	.196	4,5	.337	.342	.344	4,5	.337	.342	.344	4,5	.386	.390	.394	4,5
E	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3
E1	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6
N	16				20				24				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150	.142	.150
P2	.175 BSC		.225 BSC		.275 BSC		.325 BSC	
X	.010	.018	.010	.018	.010	.018	.010	.018
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
N	16		20		24		28	

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
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- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

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DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>Ad</i>	12/15/93	PC PACKAGE OUTLINE
CHECKED		.150" BODY WIDTH SSOP
		.025" PITCH
		SIZE C DRAWING No.
		PSC-4040
		REV 02
DO NOT SCALE DRAWING		

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