

## 4.0 ELECTRICAL SPECIFICATIONS

### 4.1 Absolute Maximum Ratings

Storage Temperature	.....	-65°C to +150°C
Case Temperature Under Bias	...	-40°C to +110°C
Supply Voltage		
with Respect to $V_{SS}$	.....	-0.5V to +6.5V
Voltage on Other Pins		
with Respect to $V_{SS}$	.....	-0.5V to $V_{CC} + 0.5V$

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### 4.2 Operating Conditions

Table 11. Operating Conditions (80960CA-25, -16)

Symbol	Parameter		Min	Max	Units	Notes
$V_{CC}$	Supply Voltage	80960CA-25	4.50	5.50	V	
		80960CA-16	4.50	5.50	V	
$f_{CLK2x}$	Input Clock Frequency (2-x Mode)	80960CA-25	0	50	MHz	
		80960CA-16	0	32	MHz	
$f_{CLK1x}$	Input Clock Frequency (1-x Mode)	80960CA-25	8	25	MHz	(Note 1)
		80960CA-16	8	16	MHz	
$T_C$	Case Temperature Under Bias	PGA package 80960CA-25, -16	-40	+110	°C	

#### NOTES:

- When in the 1-x input clock mode, CLKIN is an input to an internal phase-locked loop and must maintain a minimum frequency of 8 MHz for proper processor operation. However, in the 1-x mode, CLKIN may still be stopped when the processor either is in a reset condition or is reset. If CLKIN is stopped, the specified RESET low time must be provided once CLKIN restarts and has stabilized.
- Case temperatures are "instant on".

### 4.3 Recommended Connections

Power and ground connections must be made to multiple  $V_{CC}$  and  $V_{SS}$  (GND) pins. Every 80960CA-based circuit board should include power ( $V_{CC}$ ) and ground ( $V_{SS}$ ) planes for power distribution. Every  $V_{CC}$  pin must be connected to the power plane, and every  $V_{SS}$  pin must be connected to the ground plane. Pins identified as "NC" must not be connected in the system.

Liberal decoupling capacitance should be placed near the 80960CA. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages will offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt (XINT, NMI) or DMA (DREQ) input should be connected to  $V_{CC}$  through a pull-up resistor, as should BTERM if not used. Pull-up resistors should be in the range of 20 K $\Omega$  for each pin tied high. If  $\overline{READY}$  or  $\overline{HOLD}$  are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.** Refer to the *i960® CA Microprocessor User's Manual* (Order Number 270710) for more information.

## 4.4 DC Specifications

**Table 12. DC Characteristics**

 (80960CA-25, -16 under the conditions described in **Section 4.2, Operating Conditions.**)

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL}$	Input Low Voltage for all pins except $\overline{RESET}$	-0.3	+0.8	V	
$V_{IH}$	Input High Voltage for all pins except $\overline{RESET}$	2.0	$V_{CC} + 0.3$	V	
$V_{OL}$	Output Low Voltage		0.45	V	$I_{OL} = 5 \text{ mA}$
$V_{OH}$	Output High Voltage $I_{OH} = -1 \text{ mA}$ $I_{OH} = -200 \mu\text{A}$	2.4 $V_{CC} - 0.5$		V V	
$V_{ILR}$	Input Low Voltage for $\overline{RESET}$	-0.3	1.5	V	
$V_{IHR}$	Input High Voltage for $\overline{RESET}$	3.5	$V_{CC} + 0.3$	V	
$I_{LI1}$	Input Leakage Current for each pin <i>except</i> : $\overline{BTERM}$ , $\overline{ONCE}$ , $\overline{DREQ3:0}$ , $\overline{STEST}$ , $\overline{EOP3:0/TC3:0}$ , $\overline{NMI}$ , $\overline{XINT7:0}$ , $\overline{BOFF}$ , $\overline{READY}$ , $\overline{HOLD}$ , $\overline{CLKMODE}$		$\pm 15$	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{CC}^{(1)}$
$I_{LI2}$	Input Leakage Current for: $\overline{BTERM}$ , $\overline{ONCE}$ , $\overline{DREQ3:0}$ , $\overline{STEST}$ , $\overline{EOP3:0/TC3:0}$ , $\overline{NMI}$ , $\overline{XINT7:0}$ , $\overline{BOFF}$	0	-325	$\mu\text{A}$	$V_{IN} = 0.45\text{V}^{(2)}$
$I_{LI3}$	Input Leakage Current for: $\overline{READY}$ , $\overline{HOLD}$ , $\overline{CLKMODE}$	0	500	$\mu\text{A}$	$V_{IN} = 2.4\text{V}^{(3,7)}$
$I_{LO}$	Output Leakage Current		$\pm 15$	$\mu\text{A}$	$0.45 \leq V_{OUT} \leq V_{CC}$
$I_{CC}$	Supply Current (80960CA-25):  $I_{CC \text{ Max}}$ $I_{CC \text{ Typ}}$		750 600	mA mA	(Note 4) (Note 5)
$I_{CC}$	Supply Current (80960CA-16):  $I_{CC \text{ Max}}$ $I_{CC \text{ Typ}}$		550 400	mA mA	(Note 4) (Note 5)
$I_{ONCE}$	$\overline{ONCE}$ -mode Supply Current		100	mA	
$C_{IN}$	Input Capacitance for: $\overline{CLKIN}$ , $\overline{RESET}$ , $\overline{ONCE}$ , $\overline{READY}$ , $\overline{HOLD}$ , $\overline{DREQ3:0}$ , $\overline{BOFF}$ , $\overline{XINT7:0}$ , $\overline{NMI}$ , $\overline{BTERM}$ , $\overline{CLKMODE}$	0	12	pF	$F_C = 1 \text{ MHz}$
$C_{OUT}$	Output Capacitance of each output pin		12	pF	$F_C = 1 \text{ MHz}^{(6)}$
$C_{I/O}$	I/O Pin Capacitance		12	pF	$F_C = 1 \text{ MHz}$

**NOTES:**

- No pullup or pulldown.
- These pins have internal pullup resistors.
- These pins have internal pulldown resistors.
- Measured at worst case frequency,  $V_{CC}$  and temperature, with device operating and outputs loaded to the test conditions described in **Section 4.5.1, AC Test Conditions**.
- $I_{CC}$  Typical is not tested.
- Output Capacitance is the capacitive load of a floating output.
- $\overline{CLKMODE}$  pin has a pulldown resistor only when  $\overline{ONCE}$  pin is deasserted.

2

## 4.5 AC Specifications

Table 13. 80960CA AC Characteristics (25 MHz)

(80960CA-25 only, under conditions described in Section 4.2, Operating Conditions and Section 4.5.1, AC Test Conditions.)

Symbol	Parameter	Min	Max	Units	Notes	
<b>Input Clock (1, 9)</b>						
$T_F$	CLKIN Frequency	0	50	MHz		
$T_C$	CLKIN Period	In 1-x Mode ( $f_{CLK1x}$ ) In 2-x Mode ( $f_{CLK2x}$ )	40 20	125 $\infty$	ns ns	(11)
$T_{CS}$	CLKIN Period Stability	In 1-x Mode ( $f_{CLK1x}$ )		$\pm 0.1\%$	$\Delta$	(12)
$T_{CH}$	CLKIN High Time	In 1-x Mode ( $f_{CLK1x}$ ) In 2-x Mode ( $f_{CLK2x}$ )	8 8	62.5 $\infty$	ns ns	(11)
$T_{CL}$	CLKIN Low Time	In 1-x Mode ( $f_{CLK1x}$ ) In 2-x Mode ( $f_{CLK2x}$ )	8 8	62.5 $\infty$	ns ns	(11)
$T_{CR}$	CLKIN Rise Time		0	6	ns	
$T_{CF}$	CLKIN Fall Time		0	6	ns	
<b>Output Clocks (1, 8)</b>						
$T_{CP}$	CLKIN to PCLK2:1 Delay	In 1-x Mode ( $f_{CLK1x}$ ) In 2-x Mode ( $f_{CLK2x}$ )	-2 2	2 25	ns ns	(3, 12) (3)
$T$	PCLK2:1 Period	In 1-x Mode ( $f_{CLK1x}$ ) In 2-x Mode ( $f_{CLK2x}$ )		$T_C$ $2T_C$	ns ns	(12) (3)
$T_{PH}$	PCLK2:1 High Time		$(T/2) - 3$	$T/2$	ns	(12)
$T_{PL}$	PCLK2:1 Low Time		$(T/2) - 3$	$T/2$	ns	(12)
$T_{PR}$	PCLK2:1 Rise Time		1	4	ns	(3)
$T_{PF}$	PCLK2:1 Fall Time		1	4	ns	(3)
<b>Synchronous Outputs (8)</b>						
$T_{OH}$ $T_{OV}$	Output Valid Delay, Output Hold					(6, 10)
	$T_{OH1}, T_{OV1}$	A31:2	3	16	ns	
	$T_{OH2}, T_{OV2}$	BE3:0	3	18	ns	
	$T_{OH3}, T_{OV3}$	ADS	6	20	ns	
	$T_{OH4}, T_{OV4}$	W/R	3	20	ns	
	$T_{OH5}, T_{OV5}$	D/C, SUP, DMA	4	18	ns	
	$T_{OH6}, T_{OV6}$	BLAST, WAIT	5	18	ns	
	$T_{OH7}, T_{OV7}$	DEN	3	18	ns	
	$T_{OH8}, T_{OV8}$	HOLDA, BREQ	4	18	ns	
	$T_{OH9}, T_{OV9}$	LOCK	4	18	ns	
	$T_{OH10}, T_{OV10}$	DACK3:0	4	20	ns	
	$T_{OH11}, T_{OV11}$	D31:0	3	18	ns	
	$T_{OH12}, T_{OV12}$	DT/R	$T/2 + 3$	$T/2 + 16$	ns	
	$T_{OH13}, T_{OV13}$	FAIL	2	16	ns	
	$T_{OH14}, T_{OV14}$	EOP3:0/TC3:0	3	20	ns	(6, 10)
$T_{OF}$	Output Float for all outputs		3	22	ns	(6)
<b>Synchronous Inputs (1, 9, 10)</b>						
$T_{IS}$	Input Setup					
	$T_{IS1}$	D31:0	5		ns	
	$T_{IS2}$	BOFF	19		ns	
	$T_{IS3}$	BTERM/READY	9		ns	
	$T_{IS4}$	HOLD	9		ns	
$T_{IH}$	Input Hold					
	$T_{IH1}$	D31:0	5		ns	
	$T_{IH2}$	BOFF	7		ns	
	$T_{IH3}$	BTERM/READY	2		ns	
	$T_{IH4}$	HOLD	5		ns	

Table 13. 80960CA AC Characteristics (25 MHz) (Continued)

(80960CA-25 only, under conditions described in Section 4.2, Operating Conditions and Section 4.5.1, AC Test Conditions.)

Symbol	Parameter	Min	Max	Units	Notes
<b>Relative Output Timings (1, 2, 3, 8)</b>					
T <sub>AVSH1</sub>	A31:2 Valid to $\overline{ADS}$ Rising	T - 4	T + 4	ns	
T <sub>AVSH2</sub>	BE3:0, W/R, SUP, D/C, DMA, DACK3:0 Valid to $\overline{ADS}$ Rising	T - 6	T + 6	ns	
T <sub>AVEL1</sub>	A31:2 Valid to $\overline{DEN}$ Falling	T - 4	T + 4	ns	
T <sub>AVEL2</sub>	BE3:0, W/R, SUP, INST, DMA, DACK3:0 Valid to $\overline{DEN}$ Falling	T - 6	T + 6	ns	
T <sub>NLQV</sub>	WAIT Falling to Output Data Valid	± 4		ns	
T <sub>DVNH</sub>	Output Data Valid to WAIT Rising	N*T - 4	N*T + 4	ns	(4)
T <sub>NLNH</sub>	WAIT Falling to WAIT Rising	N*T ± 4		ns	(4)
T <sub>NHQX</sub>	Output Data Hold after WAIT Rising	(N + 1)*T - 8	(N + 1)*T + 6	ns	(5)
T <sub>EHTV</sub>	DT/R Hold after $\overline{DEN}$ High	T/2 - 7	∞	ns	(6)
T <sub>TVEL</sub>	DT/R Valid to $\overline{DEN}$ Falling	T/2 - 4		ns	
<b>Relative Input Timings (1, 2, 3)</b>					
T <sub>IS5</sub>	RESET Input Setup (2-x Clock Mode)	8		ns	(13)
T <sub>IH5</sub>	RESET Input Hold (2-x Clock Mode)	7		ns	(13)
T <sub>IS6</sub>	$\overline{DREQ3:0}$ Input Setup	14		ns	(7)
T <sub>IH6</sub>	$\overline{DREQ3:0}$ Input Hold	9		ns	(7)
T <sub>IS7</sub>	XINT7:0, NMI Input Setup	10		ns	(15)
T <sub>IH7</sub>	XINT7:0, NMI Input Hold	10		ns	(15)
T <sub>IS8</sub>	RESET Input Setup (1-x Clock Mode)	3		ns	(14)
T <sub>IH8</sub>	RESET Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

**NOTES:**

- See Section 4.5.2, AC Timing Waveforms for waveforms and definitions.
- See Figure 16 for capacitive derating information for output delays and hold times.
- See Figure 17 for capacitive derating information for rise and fall times.
- Where N is the number of N<sub>RAD</sub>, N<sub>RDD</sub>, N<sub>WAD</sub> or N<sub>WDD</sub> wait states that are programmed in the Bus Controller Region Table. WAIT never goes active when there are no wait states in an access.
- N = Number of wait states inserted with READY.
- Output Data and/or DT/R may be driven indefinitely following a cycle if there is no subsequent bus activity.
- Since asynchronous inputs are synchronized internally by the 80960CA, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
- These specifications are guaranteed by the processor.
- These specifications must be met by the system for proper operation of the processor.
- This timing is dependent upon the loading of PCLK2:1. Use the derating curves of Section 4.5.3, Derating Curves to adjust the timing for PCLK2:1 loading.
- In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
- When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ±0.1% between adjacent cycles.
- In 2-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 21).
- In 1-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 22).
- The interrupt pins are synchronized internally by the 80960CA. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

2

Table 14. 80960CA AC Characteristics (16 MHz)

(80960CA-16 only, under conditions described in Section 4.2, Operating Conditions and Section 4.5.1, AC Test Conditions.)

Symbol	Parameter	Min	Max	Units	Notes	
<b>Input Clock (1, 9)</b>						
T <sub>F</sub>	CLKIN Frequency	0	32	MHz		
T <sub>C</sub>	CLKIN Period	In 1-x Mode (f <sub>CLK1x</sub> )	62.5	125	ns	(11)
		In 2-x Mode (f <sub>CLK2x</sub> )	31.25	∞	ns	
T <sub>CS</sub>	CLKIN Period Stability	In 1-x Mode (f <sub>CLK1x</sub> )		±0.1%	Δ	(12)
T <sub>CH</sub>	CLKIN High Time	In 1-x Mode (f <sub>CLK1x</sub> )	10	62.5	ns	(11)
		In 2-x Mode (f <sub>CLK2x</sub> )	10	∞	ns	
T <sub>CL</sub>	CLKIN Low Time	In 1-x Mode (f <sub>CLK1x</sub> )	10	62.5	ns	(11)
		In 2-x Mode (f <sub>CLK2x</sub> )	10	∞	ns	
T <sub>CR</sub>	CLKIN Rise Time	0	6	ns		
T <sub>CF</sub>	CLKIN Fall Time	0	6	ns		
<b>Output Clocks (1, 8)</b>						
T <sub>CP</sub>	CLKIN to PCLK2:1 Delay	In 1-x Mode (f <sub>CLK1x</sub> )	-2	2	ns	(3, 12)
		In 2-x Mode (f <sub>CLK2x</sub> )	2	25	ns	(3)
T	PCLK2:1 Period	In 1-x Mode (f <sub>CLK1x</sub> )	T <sub>C</sub>		ns	(12)
		In 2-x Mode (f <sub>CLK2x</sub> )	2T <sub>C</sub>		ns	(3)
T <sub>PH</sub>	PCLK2:1 High Time	(T/2) - 4	T/2	ns	(12)	
T <sub>PL</sub>	PCLK2:1 Low Time	(T/2) - 4	T/2	ns	(12)	
T <sub>PR</sub>	PCLK2:1 Rise Time	1	4	ns	(3)	
T <sub>PF</sub>	PCLK2:1 Fall Time	1	4	ns	(3)	
<b>Synchronous Outputs (8)</b>						
T <sub>OH</sub>	Output Valid Delay, Output Hold				(6, 10)	
T <sub>OV</sub>	TOH1, TOV1	A31:2	3	18	ns	(6, 10)
	TOH2, TOV2	BE3:0	3	20	ns	
	TOH3, TOV3	ADS	6	22	ns	
	TOH4, TOV4	W/R	3	22	ns	
	TOH5, TOV5	D/C, SUP, DMA	4	20	ns	
	TOH6, TOV6	BLAST, WAIT	5	20	ns	
	TOH7, TOV7	DEN	3	20	ns	
	TOH8, TOV8	HOLDA, BREQ	4	20	ns	
	TOH9, TOV9	LOCK	4	20	ns	
	TOH10, TOV10	DACK3:0	4	22	ns	
	TOH11, TOV11	D31:0	3	20	ns	
	TOH12, TOV12	DT/R	T/2 + 3	T/2 + 18	ns	
	TOH13, TOV13	FAIL	2	18	ns	
	TOH14, TOV14	EOP3:0/TC3:0	3	22	ns	
T <sub>OF</sub>	Output Float for All Outputs	3	22	ns	(6)	
<b>Synchronous Inputs (1, 9, 10)</b>						
T <sub>IS</sub>	Input Setup	D31:0	5		ns	
		BOFF	21		ns	
		BTERM/READY	9		ns	
		HOLD	9		ns	
T <sub>IH</sub>	Input Hold	D31:0	5		ns	
		BOFF	7		ns	
		BTERM/READY	2		ns	
		HOLD	5		ns	

**Table 14. 80960CA AC Characteristics (16 MHz) (Continued)**

 (80960CA-16 only, under conditions described in **Section 4.2, Operating Conditions** and **Section 4.5.1, AC Test Conditions.**)

Symbol	Parameter	Min	Max	Units	Notes
<b>Relative Output Timings (1, 2, 3, 8)</b>					
T <sub>AVSH1</sub>	A31:2 Valid to $\overline{ADS}$ Rising	T - 4	T + 4	ns	
T <sub>AVSH2</sub>	BE3:0, W/R, SUP, D/C, DMA, DACK3:0 Valid to $\overline{ADS}$ Rising	T - 6	T + 6	ns	
T <sub>AVEL1</sub>	A31:2 Valid to $\overline{DEN}$ Falling	T - 6	T + 6	ns	
T <sub>AVEL2</sub>	BE3:0, W/R, SUP, INST, DMA, DACK3:0 Valid to $\overline{DEN}$ Falling	T - 6	T + 6	ns	
T <sub>NLQV</sub>	WAIT Falling to Output Data Valid	± 4		ns	
T <sub>DVNH</sub>	Output Data Valid to WAIT Rising	N*T - 4	N*T + 4	ns	(4)
T <sub>NLNH</sub>	WAIT Falling to WAIT Rising	N*T ± 4		ns	(4)
T <sub>NHQX</sub>	Output Data Hold after WAIT Rising	(N + 1)*T - 8	(N + 1)*T + 4	ns	(5)
T <sub>EHTV</sub>	DT/R Hold after $\overline{DEN}$ High	T/2 - 7	∞	ns	(6)
T <sub>TVEL</sub>	DT/R Valid to $\overline{DEN}$ Falling	T/2 - 4		ns	
<b>Relative Input Timings (1, 2, 3)</b>					
T <sub>IS5</sub>	RESET Input Setup (2-x Clock Mode)	10		ns	(13)
T <sub>IH5</sub>	RESET Input Hold (2-x Clock Mode)	9		ns	(13)
T <sub>IS6</sub>	DREQ3:0 Input Setup	16		ns	(7)
T <sub>IH6</sub>	DREQ3:0 Input Hold	11		ns	(7)
T <sub>IS7</sub>	XINT7:0 NMI Input Setup	10		ns	(15)
T <sub>IH7</sub>	XINT7:0 NMI Input Hold	10		ns	(15)
T <sub>IS8</sub>	RESET Input Setup (1-x Clock Mode)	3		ns	(14)
T <sub>IH8</sub>	RESET Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

**NOTES:**

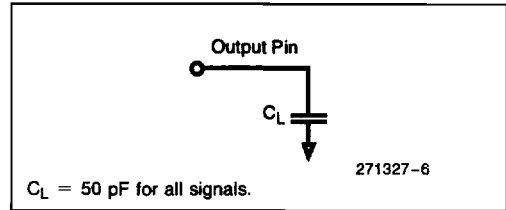
- See **Section 4.5.2, AC Timing Waveforms** for waveforms and definitions.
- See Figure 16 for capacitive derating information for output delays and hold times.
- See Figure 17 for capacitive derating information for rise and fall times.
- Where N is the number of N<sub>RD</sub>, N<sub>RD</sub>, N<sub>WD</sub> or N<sub>WD</sub> wait states that are programmed in the Bus Controller Region Table. WAIT never goes active when there are no wait states in an access.
- N = Number of wait states inserted with READY.
- Output Data and/or DT/R may be driven indefinitely following a cycle if there is no subsequent bus activity.
- Since asynchronous inputs are synchronized internally by the 80960CA, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
- These specifications are guaranteed by the processor.
- These specifications must be met by the system for proper operation of the processor.
- This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3, Derating Curves** to adjust the timing for PCLK2:1 loading.
- In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
- When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ±0.1% between adjacent cycles.
- In 2-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 21).
- In 1-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 22.)
- The interrupt pins are synchronized internally by the 80960CA. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

2

**4.5.1 AC Test Conditions**

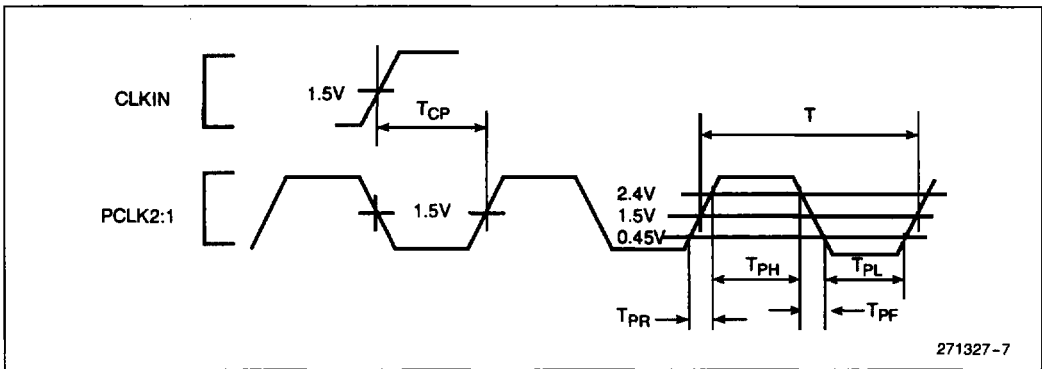
The AC Specifications in Section 4.5 are tested with the 50 pF load shown in Figure 6. Figure 15 shows how timings vary with load capacitance.

Specifications are measured at the 1.5V crossing point, unless otherwise indicated. Input waveforms are assumed to have a rise and fall time of  $\leq 2$  ns from 0.8V to 2.0V. See **Section 4.5.2, AC Timing Waveforms** for AC spec definitions, test points and illustrations.

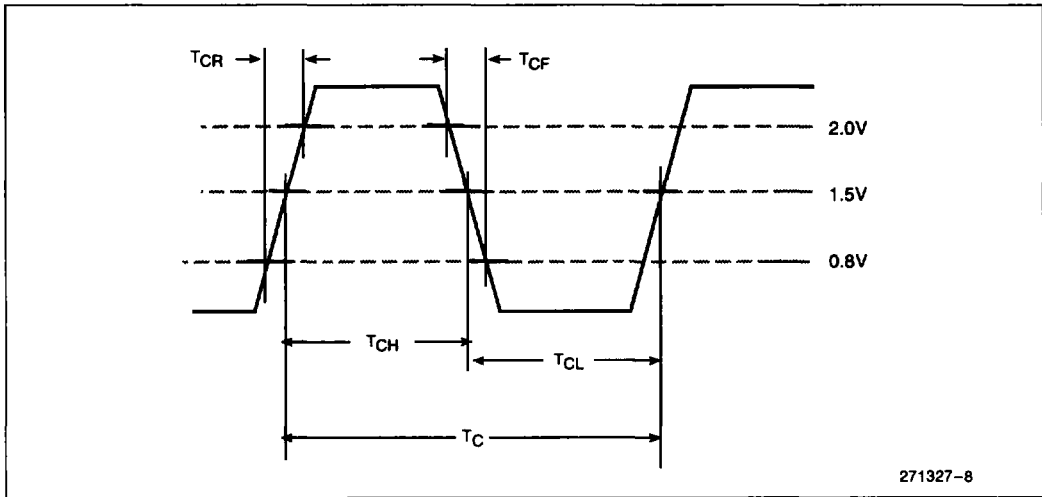


**Figure 6. AC Test Load**

**4.5.2 AC Timing Waveforms**



**Figure 7. Input and Output Clock Waveforms**



**Figure 8. CLKIN Waveform**

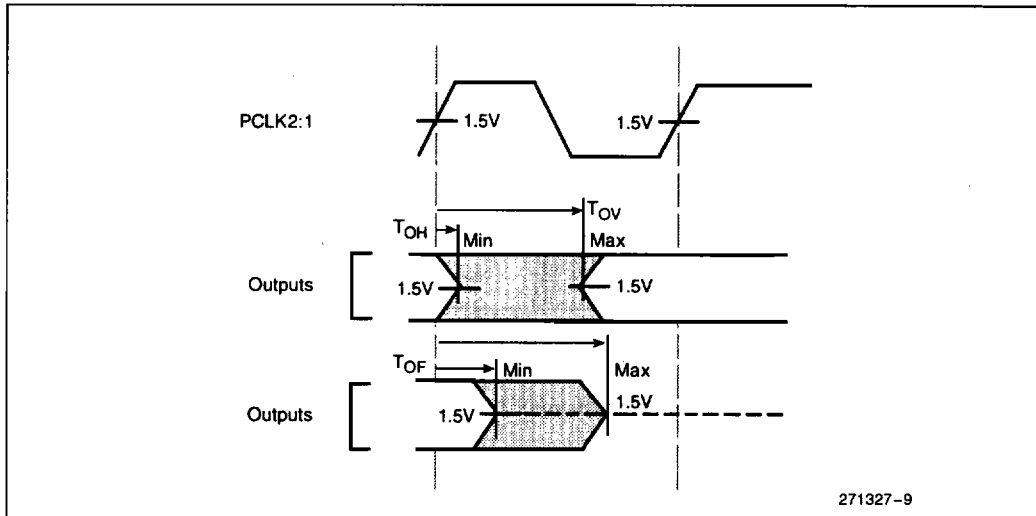


Figure 9. Output Delay and Float Waveform

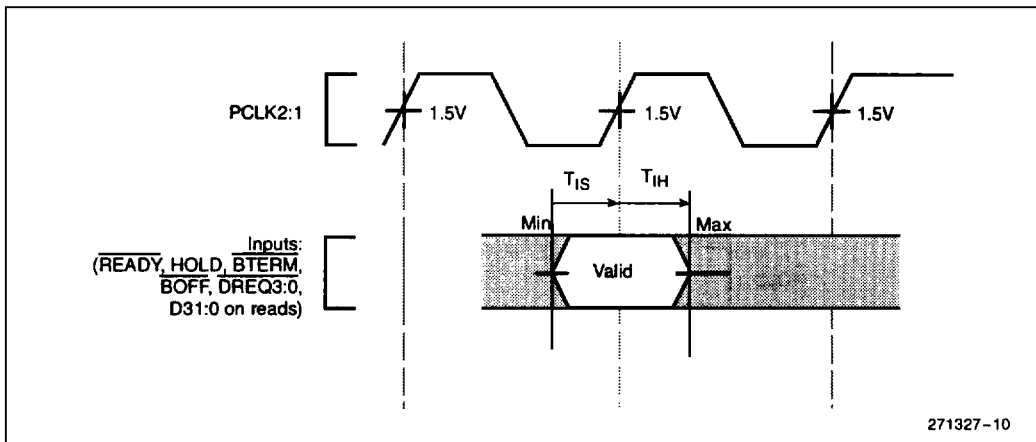


Figure 10. Input Setup and Hold Waveform

- $T_{OV}$   $T_{OH}$  OUTPUT DELAY—The maximum output delay is referred to as the Output Valid Delay ( $T_{OV}$ ). The minimum output delay is referred to as the Output Hold ( $T_{OH}$ ).
- $T_{OF}$  OUTPUT FLOAT DELAY—The output float condition occurs when the maximum output current becomes less than  $I_{LO}$  in magnitude.
- $T_{IS}$   $T_{IH}$  INPUT SETUP AND HOLD—The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

2



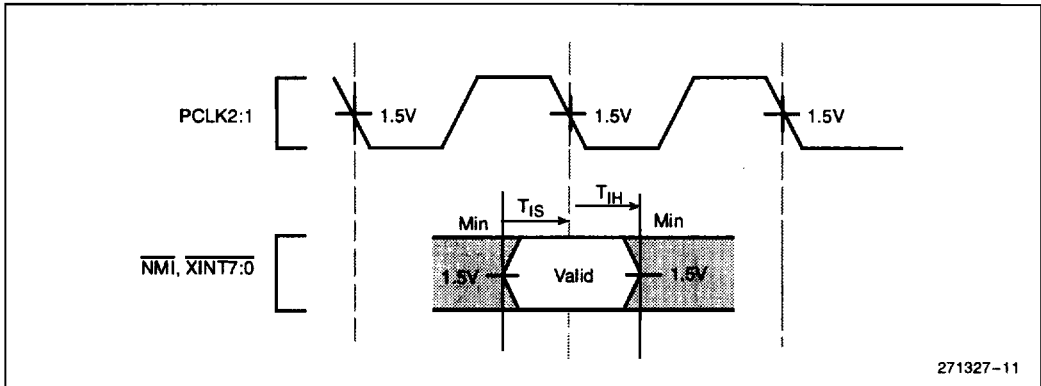


Figure 11. NMI, XINT7:0 Input Setup and Hold Waveform

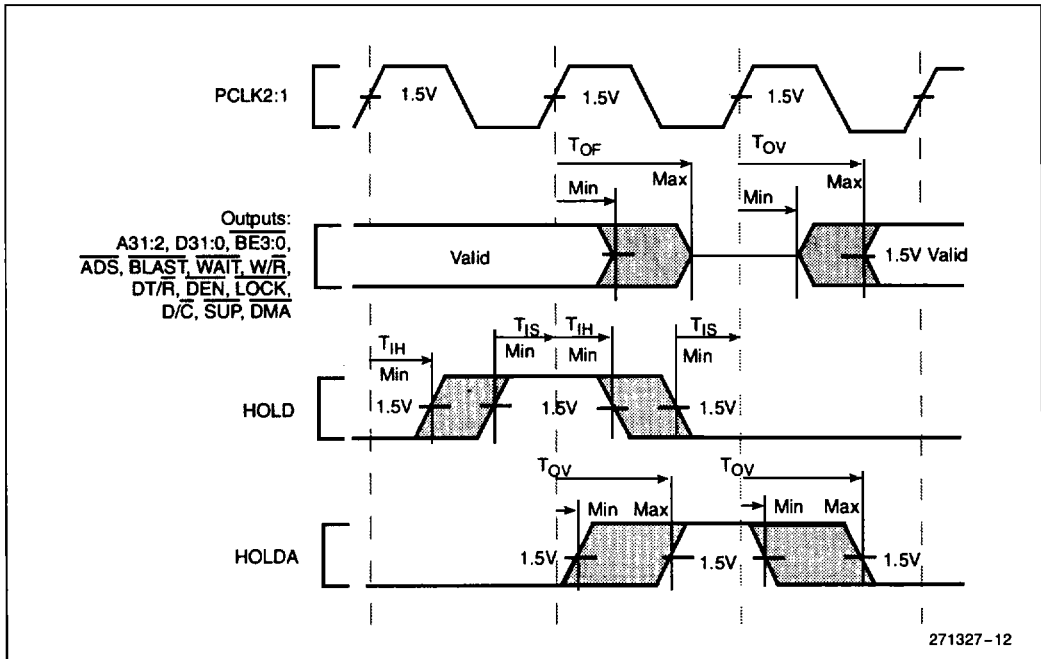


Figure 12. Hold Acknowledge Timings

- $T_{OV}$   $T_{OH}$  **OUTPUT DELAY**—The maximum output delay is referred to as the Output Valid Delay ( $T_{OV}$ ). The minimum output delay is referred to as the Output Hold ( $T_{OH}$ ).
- $T_{OF}$  **OUTPUT FLOAT DELAY**—The output float condition occurs when the maximum output current becomes less than  $I_{LO}$  in magnitude.
- $T_{IS}$   $T_{IH}$  **INPUT SETUP AND HOLD**—The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

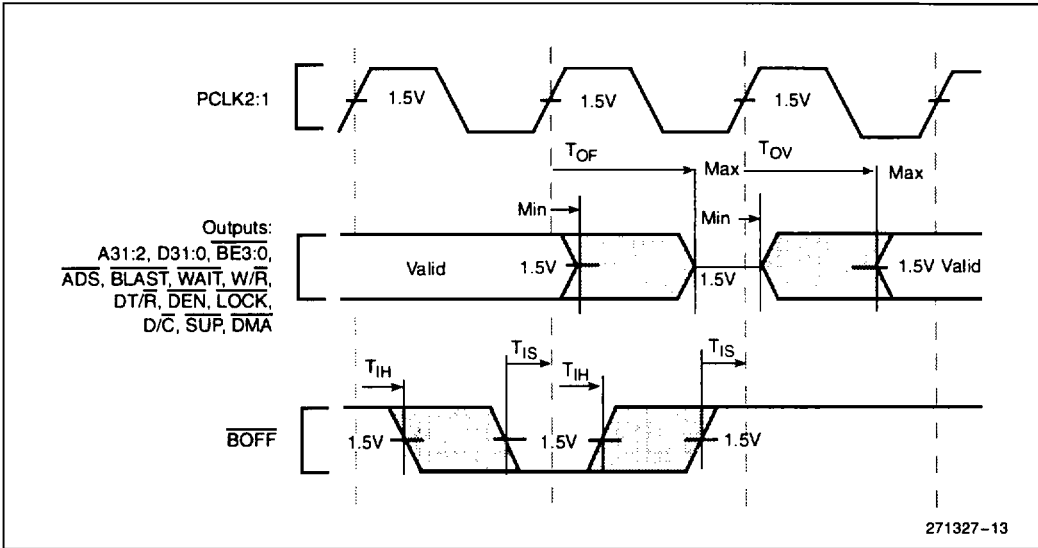
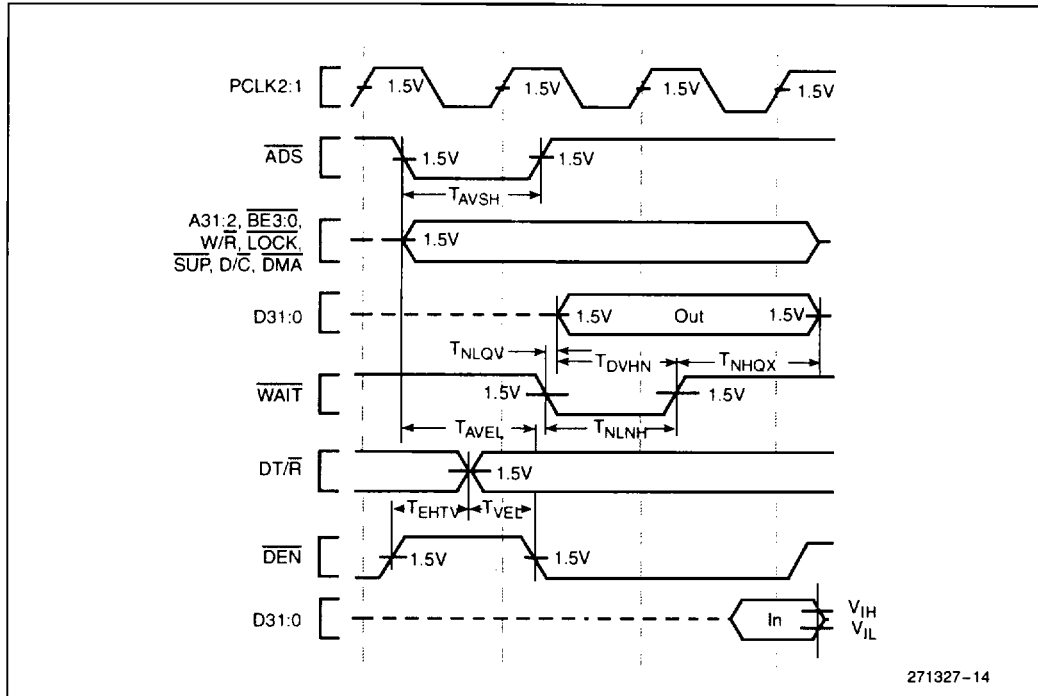


Figure 13. Bus Backoff  $\overline{BOFF}$  Timings

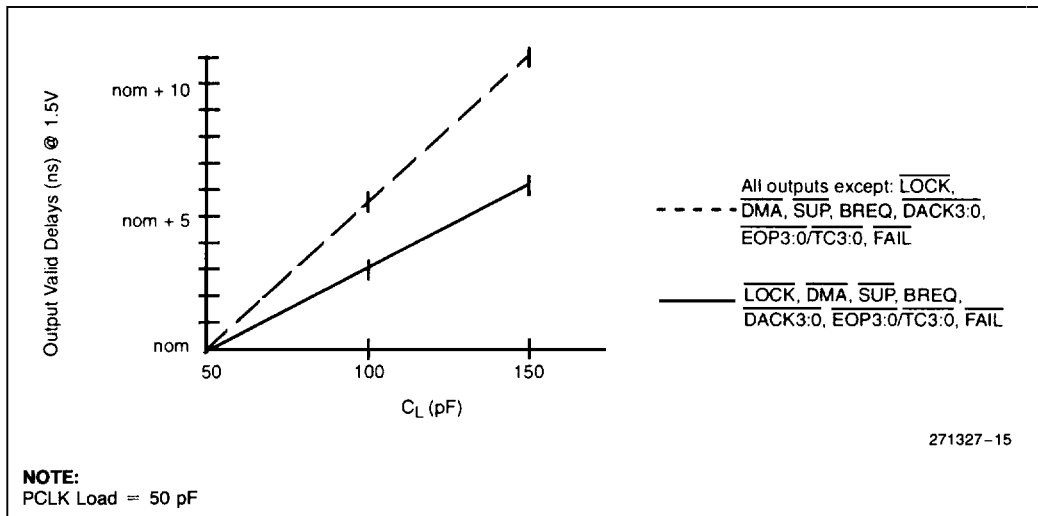
2



271327-14

Figure 14. Relative Timings Waveforms

4.5.3 Derating Curves



271327-15

**NOTE:**  
PCLK Load = 50 pF

Figure 15. Output Delay or Hold vs Load Capacitance

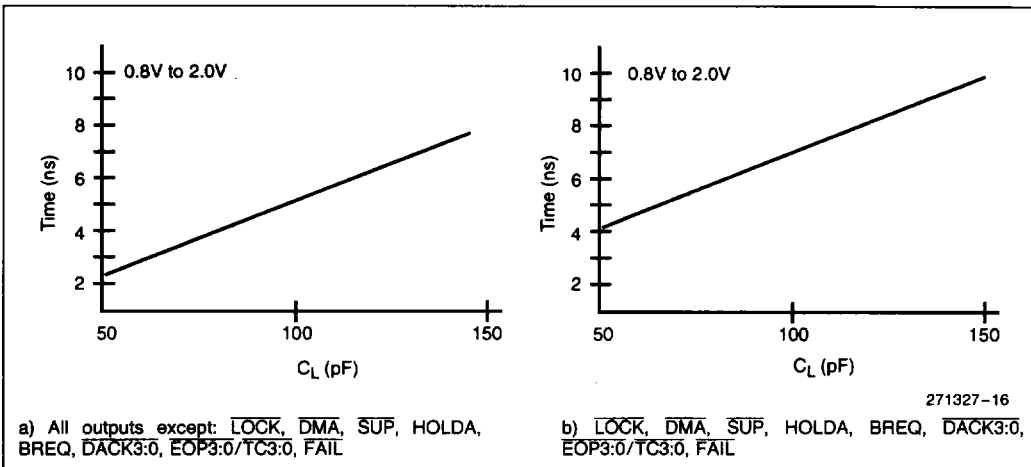


Figure 16. Rise and Fall Time Derating at Highest Operating Temperature and Minimum V<sub>CC</sub>

2

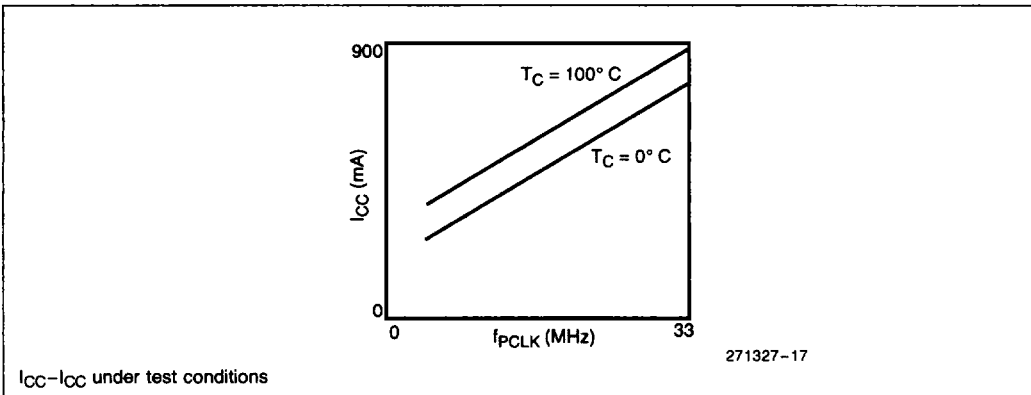


Figure 17. I<sub>CC</sub> vs Frequency and Temperature