Description

The 9DB436 is a zero delay/fanout buffer for PCI Express™ clocking. It supports PCIe Gen1–3 in zero delay mode and PCIe Gen1–4 in fanout mode. The 9DB436 is a pin-compatible upgrade to the 9DB433 and 9DB434 with a Safe-Power-Sequence (SPS) clock input.

Typical Applications

- Riser cards
- Storage
- Networking
- JBOD

Output Features

- Four 0.7V current-mode differential HCSL output pairs
- Supports zero delay buffer (ZDB) mode and fanout mode
- Selectable bandwidth for zero delay mode
- 50–110 MHz operation in PLL mode
- 5–166 MHz operation in Bypass mode

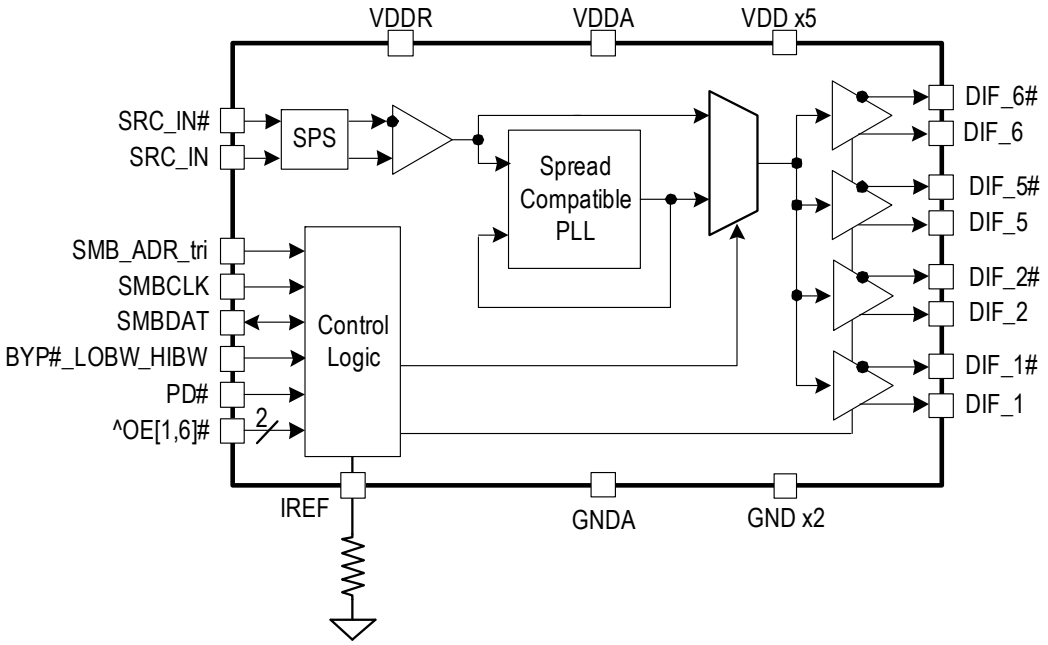
Features

- SPS internal receiver bias network keeps input clock parked when input is floating
- Supports both 85Ω and 100Ω output impedance with appropriate resistor selection
- OE# pins default to controlling outputs
- PLL or Bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible
- Outputs default to Hi-Z when disabled or when device is powered down
- SMBus interface; unused outputs can be disabled
- 3 selectable SMBus addresses

Key Specifications

- PCIe Gen3 jitter < 0.6ps rms in ZDB mode
- PCIe Gen4 additive jitter < 0.1ps rms in fanout mode
- Output cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps

Block Diagram

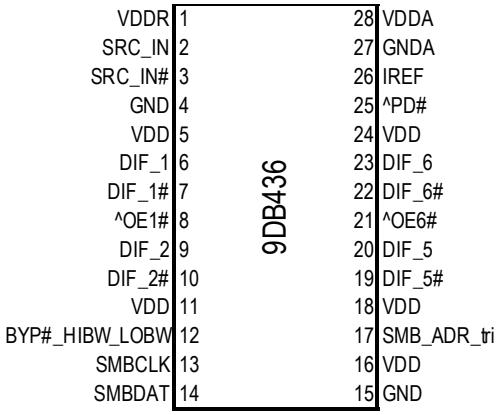


Contents

Description . . . 1
Typical Applications . . . 1
Output Features . . . 1
Features . . . 1
Key Specifications . . . 1
Block Diagram . . . 1
Pin Assignments . . . 3
Pin Descriptions . . . 3
    Power Connections . . . 4
    Operating Mode Readback . . . 4
    SMBus Address Selection and Readback . . . 5
    Tri-level Input Logic Levels . . . 5
Absolute Maximum Ratings . . . 6
Electrical Characteristics . . . 7
Test Loads and Terminations . . . 12
General SMBus Serial Interface Information . . . 13
        How to Write . . . 13
        How to Read . . . 13
Package Outline Drawings . . . 16
Marking Diagram . . . 16
Ordering Information . . . 16
Revision History . . . 17

Pin Assignments

Figure 1. Pin Assignments for 28TSSOP Package – Top View



v indicates internal pull-down resistor
^ indicates internal pull-up resistor

Pin 12 and pin 17 are latched on power-up. Ensure that the power supply to the pull-up/pull-down resistors ramps at the same time as the main supply to the chip.

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	VDDR	Power	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
2	SRC_IN	Input	HCSL SRC true input.
3	SRC_IN#	Input	HCSL SRC complementary input.
4	GND	GND	Ground pin.
5	VDD	Power	Power supply, nominally 3.3V.
6	DIF_1	Output	HCSL true clock output.
7	DIF_1#	Output	HCSL complementary clock output.
8	^OE1#	Input	Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
9	DIF_2	Output	HCSL true clock output.
10	DIF_2#	Output	HCSL complementary clock output.
11	VDD	Power	Power supply, nominally 3.3V.
12	BYP#_HIBW_ LOBW	Input	Tri-level input to select bypass mode, Hi BW PLL, or Lo BW PLL mode.
13	SMBCLK	Input	Clock pin of SMBUS circuitry.
14	SMBDAT	I/O	Data pin of SMBUS circuitry.
15	GND	GND	Ground pin.
16	VDD	Power	Power supply, nominally 3.3V.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
17	SMB_ADR_tri	Input	SMBus address select bit. This is a tri-level input that decodes 1 of 3 SMBus addresses.
18	VDD	Power	Power supply, nominally 3.3V.
19	DIF_5#	Output	HCSL complementary clock output.
20	DIF_5	Output	HCSL true clock output.
21	^OE6#	Input	Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
22	DIF_6#	Output	HCSL complementary clock output.
23	DIF_6	Output	HCSL true clock output.
24	VDD	Power	Power supply, nominally 3.3V.
25	^PD#	Input	Asynchronous active low input pin used to power down the device. Normally, the internal clocks are disabled and the VCOs and the XTAL oscillator (if any) are stopped. See the SMBus options for exact behavior. This pin has an internal pull-up resistor.
26	IREF	Output	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475Ω is the standard value for 100Ω differential impedance. Other impedances require different values.
27	GNDA	GND	Ground pin for the PLL core.
28	VDDA	Power	Power supply for PLL core.

Power Connections

Pin Number		Description
V_{DD}	GND	
1	4	SRC_IN/SRC_IN#
5,11,18, 24	4	DIF (1, 2, 5, 6)
16	15	Digital VDD/GND
28	27	Analog VDD/GND for PLL and IREF

For best results, also treat pin 1 as analog VDD.

Operating Mode Readback

BYP#_LOBW_HIBW	Mode	Byte0, bit 3	Byte 0, bit 1
Low	Bypass	0	0
Mid	PLL 100M Hi BW	1	0
High	PLL 100M Low BW	0	1

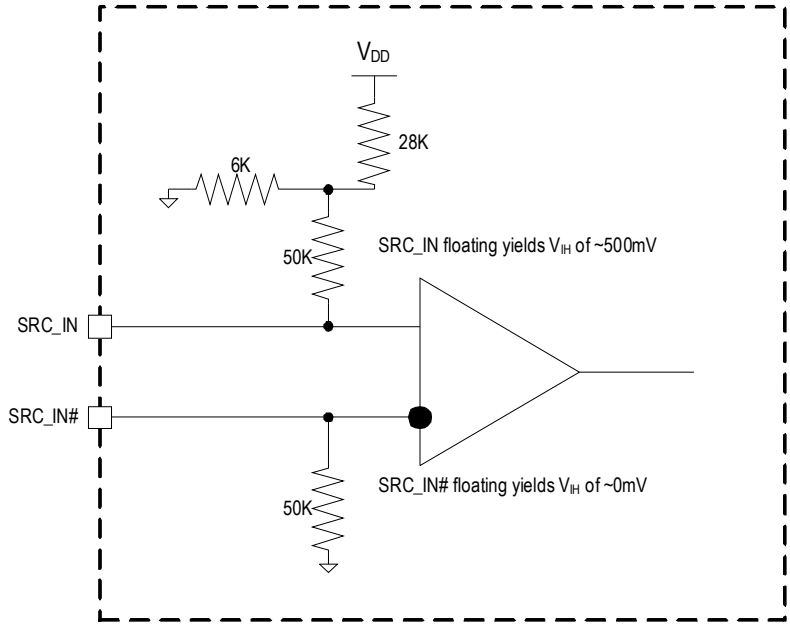
SMBus Address Selection and Readback

SMB_ADR_tri	Address
Low	DA/DB
Mid	DC/DD
High	D8/D9

Tri-level Input Logic Levels

State of Pin	Voltage
Low	< 0.8V
Mid	1.2 < Vin < 1.8V
High	Vin > 2.0V

Figure 2. Safe Power Sequence (SPS) Clock Input



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DB436. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
3.3V Core Supply Voltage	$V_{DDA/R}$				4.6	V	1,2
3.3V Core Logic Voltage	V_{DD}				4.6	V	1,2
SMBus Supply Voltage	V_{DDSMB}	SMBus pull-up resistor voltage.			5.5	V	1
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface.			V_{DD}+0.5	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics

Table 3. Input/Supply/Common Parameters

$T_A = T_{IND}$ unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Ambient Operating Temperature	T_{IND}	Industrial range.	-40		85	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs.	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs.	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5	-0.02	5	µA	1
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-100		100	µA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3V, Bypass Mode.	5		166	MHz	2
	F_{ipll}	V_{DD} = 3.3V, 100MHz PLL Mode.	50	100	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.			1	ms	1,2
Input SS Modulation Frequency for PCIe	f_{MODIN}	Allowable frequency (Triangular modulation).	30	31.5	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1	2	3	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# deassertion.		13	300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	1,2
Trise	t_R	Rise time of control inputs.			5	ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

Table 4. SMBus Parameters

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	At $I_{PULLUP.}$			0.4	V	1
SMBus Sink Current	I_{PULLUP}	At $V_{OL.}$	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V ±10%.	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Maximum V_{IL} - 0.15V) to (Minimum V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Minimum V_{IH} + 0.15V) to (Maximum V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency.			400	kHz	1,5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Table 5. DIF_IN Clock Input Parameters

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage	V_{CROSS}	Crossover voltage.	150	375	900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.6		8	V/ns	1,2
Input Leakage Current	I_{IN}	SRC_IN, V_{IN} = GND.			125	µA	
		SRC_IN#, V_{IN} = V_{DD}.	-100			µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45	50	55	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 6. DIF 0.7V Current Mode Differential Outputs

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	T_{RF}	Scope averaging on.	2	2.8	4	V/ns	1,2,3
Slew Rate Matching	ΔT_{RF}	Slew rate matching. Scope averaging on.		8	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	797	850	mV	1
Voltage Low	V_{LOW}		-150	14	150		1
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).		813	1150		1
Minimum Voltage	Vmin		-300	-1			1
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	250	378	550		1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		16	140		1,6

[1] Guaranteed by design and characterization, not 100% tested in production. I_{REF} = V_{DD}/(3 x R_R). For R_R = 475Ω (1%), IREF = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V at Zo = 50Ω (100Ω differential impedance).

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Table 7. Current Consumption

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	$I_{DD3.3OP}$	All outputs active at 100MHz, PLL Mode, C_L = full load.		78	103	mA	1
Power Down Current	$I_{DD3.3PD}$	All differential pairs driven.		28	36	mA	1
	$I_{DD3.3PDZ}$	All differential pairs tri-stated.		3	6	mA	1

[1] Guaranteed by design and characterization, not 100% tested in production.

Table 8. Output Duty Cycle, Jitter, Skew and PLL Characteristics

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
PLL Bandwidth	B_W	-3dB point in High BW Mode (industrial).	1.5	2.8	4	MHz	1
		-3dB point in High BW Mode (commercial).	2	2.8	4	MHz	1
		-3dB point in Low BW Mode.	0.7	1.1	1.4	MHz	1
PLL Jitter Peaking	t_{JPEAK}	Peak pass band gain.		1.5	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode.	45	49.2	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at100MHz.	-1	-0.4	1	%	1,4
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50% (industrial).	3500	4263	4900	ps	1
		Bypass Mode, V_T = 50% (commercial).	3500	4115	4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%.	-250	-45	250	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50% (industrial).		40	60	ps	1
		V_T = 50% (commercial).		40	50	ps	1
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	PLL Mode.		21	50	ps	1,3
		Additive jitter in Bypass Mode.		3	10	ps	1,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = V_{DD}/(3 x R_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x IREF and V_{OH} = 0.7V at Zo = 50Ω.

[3] Measured from differential waveform.

[4] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass mode.

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1.		25	35	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band. 10kHz < f < 1.5MHz		0.74	1.11	3	ps (rms)	1,2
		PCIe Gen2 High Band. 1.5MHz < f < Nyquist (50MHz)		1.95	2.36	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.51	0.60	1	ps (rms)	1,2

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures (Cont.)

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1.		5.4	8	Not Applicable	ps (p-p)	1,2,3,4
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band. 10kHz < f < 1.5MHz		0.004	0.01		ps (rms)	1,2,3,4,6
		PCIe Gen2 High Band. 1.5MHz < f < Nyquist (50MHz)		0.10	0.13		ps (rms)	1,2,3,4,6
	$t_{jphPCIeG3-CC}$	PCIe Gen3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.05	0.06		ps (rms)	1,2,3,4,6
	$t_{jphPCIeG4-CC}$	PCIe Gen4. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.05	0.06		ps (rms)	1,2,3,4,6

Table 10. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen2. (PLL BW of 16MHz, CDR = 5MHz).		0.12	0.16	Not Applicable	ps (rms)	1,4,5,6,7
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3. (PLL BW of 2–4MHz, CDR = 10MHz).		0.03	0.04		ps (rms)	1,4,5,6,7

Notes on PCIe Filtered Phase Jitter tables:

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel™-supplied Clock Jitter tool, when driven by Wenzel Associates 100MHz oscillator.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps peak-peak at 1M cycles for a BER of 1^{-12}.

[4] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRnS) PCIe clock architectures.

[5] According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. The PCIe Base Specification Rev5.0 is expected to resolve this.

[6] Additive jitter for RMS values is calculated by solving for b [$b = sqrt(c^2 - a^2)$] where “a” is rms input jitter and ‘c” is rms total jitter.

Test Loads and Terminations

Figure 3. HCSL Differential Output Test Load – Source Terminated

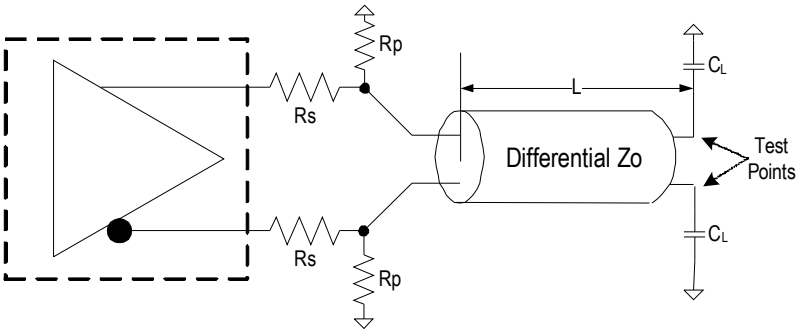


Table 11. Differential Output Termination

DIF ZO (Ω)	IREF (Ω)	RS (Ω)	RP (Ω)	L (inches)	CL (pF)
100	475	33	49.9	5	2
85	412	27	42.2 or 43.2	5	2

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			Renesas
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select Register, Read/Write Address (Selectable)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	PD_Mode	PD# drive mode	RW	Driven	Hi-Z	1
Bit 6	—	OE_Mode	OE#_Disable drive mode	RW	Driven	Hi-Z	1
Bit 5	Reserved						0
Bit 4	Reserved						X
Bit 3	—	MODE1	BYPASS#/PLL1	RW	See Operating Mode Readback table		Latched
Bit 2	Reserved						1
Bit 1	—	MODE0	BYPASS#/PLL0	RW	See Operating Mode Readback table		Latched
Bit 0	Reserved						1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						1
Bit 6	22, 23	DIF_6	Output Enable	RW	Disable	Enable	1
Bit 5	19, 20	DIF_5	Output Enable	RW	Disable	Enable	1
Bit 4	Reserved						1
Bit 3	Reserved						1
Bit 2	9, 10	DIF_2	Output Enable	RW	Disable	Enable	1
Bit 1	6, 7	DIF_1	Output Enable	RW	Disable	Enable	1
Bit 0	Reserved						1

NOTE: The SMBus Output Enable Bit must be '1' and the respective OE pin must be active for the output to run.

SMBus Table: OE Pin Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						1
Bit 6	22, 23	DIF_6	DIF_6 Stoppable with OE6#	RW	Free-run	Stoppable	1
Bit 5	19, 20	DIF_5	DIF_5 Stoppable with OE5#	RW	Free-run	Stoppable	1
Bit 4	Reserved						1
Bit 3	Reserved						1
Bit 2	9, 10	DIF_2	DIF_2 Stoppable with OE2#	RW	Free-run	Stoppable	1
Bit 1	6, 7	DIF_1	DIF_1 Stoppable with OE1#	RW	Free-run	Stoppable	1
Bit 0	Reserved						1

NOTE: To change the default to be “Stoppable”, see the 9DB434.

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						X
Bit 6	Reserved						X
Bit 5	Reserved						X
Bit 4	Reserved						X
Bit 3	Reserved						X
Bit 2	Reserved						X
Bit 1	Reserved						X
Bit 0	Reserved						X

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	RID3	REVISION ID	R	—	—	0
Bit 6	—	RID2		R	—	—	0
Bit 5	—	RID1		R	—	—	0
Bit 4	—	RID0		R	—	—	0
Bit 3	—	VID3	VENDOR ID	R	—	—	0
Bit 2	—	VID2		R	—	—	0
Bit 1	—	VID1		R	—	—	0
Bit 0	—	VID0		R	—	—	1

SMBus Table: Device ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	DID7	Device ID 7 (MSB)	RW	Device ID is 46 Hex for 9DB436		0
Bit 6	—	DID6	Device ID 6	RW			1
Bit 5	—	DID5	Device ID 5	RW			0
Bit 4	—	DID4	Device ID 4	RW			0
Bit 3	—	DID3	Device ID 3	RW			0
Bit 2	—	DID2	Device ID 2	RW			1
Bit 1	—	DID1	Device ID 1	RW			1
Bit 0	—	DID0	Device ID 0	RW			0

SMBus Table: Byte Count Register

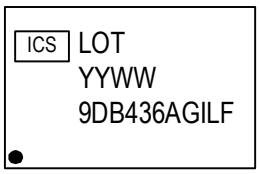
Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	BC7	Writing to this register configures how many bytes will be read back.	RW	—	—	0
Bit 6	—	BC6		RW	—	—	0
Bit 5	—	BC5		RW	—	—	0
Bit 4	—	BC4		RW	—	—	0
Bit 3	—	BC3		RW	—	—	0
Bit 2	—	BC2		RW	—	—	1
Bit 1	—	BC1		RW	—	—	1
Bit 0	—	BC0		RW	—	—	1

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/28-tssop-package-outline-drawing-44-mm-body-065mm-pitch-pgg28d1

Marking Diagram



- "LOT" denotes the lot number.
- "YYWW" is the last two digits of the year and the work week number when the part was assembled.
- Line 3: Part number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9DB436AGILF	4.4mm body, 0.65mm pitch 28-TSSOP	Tubes	-40° to +85°C
9DB436AGILFT	4.4mm body, 0.65mm pitch 28-TSSOP	Tape and Reel	-40° to +85°C

"LF" suffix to the part numbers are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator.

Revision History

Revision Date	Description of Change
November 20, 2020	Rebrand to Renesas.
October 12, 2018	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.