

AN3134 Application note

EVAL6229QR demonstration board using the L6229Q DMOS driver for a three-phase BLDC motor control application

Introduction

This application note describes the EVAL6229QR demonstration board for the L6229Q DMOS fully integrated three-phase brushless DC motor driver. The board implements a typical application that can be used as a demonstration platform for driving three-phase brushless DC motors with currents up to 1 A DC.

Thanks to the small footprint of the L6229Q (QFN 5x5 mm), the board is a very compact 30x32 mm.





AM02447v1

April 2010 Doc ID 16960 Rev 1 1/10

1 Demonstration board description

Table 1. EVAL6229QR pin description

Name	Туре	Function
VS	Power supply	Hal bridges power supply voltage
PGND	Ground	Power ground terminal.
VDD	Power supply	Hall effect sensors pull-up voltage.
H1	Sensor input	Single ended hall effect sensor input 1.
H2	Sensor input	Single ended hall effect sensor input 2.
H3	Sensor input	Single ended hall effect sensor input 3.
SGND	Ground	Signal ground terminal.
DIAG	Open-drain output	Diagnostic pin. When 'low', signals an overcurrent or overtemperature event.
TACHO	Open-drain output	Frequency-to-voltage open drain output. Every pulse from H1 pin is shaped as a fixed and adjustable length pulse.
F/R	Logic input	Selects the direction of the rotation ('H' = CW; 'L' = CCW).
EN	Logic input/output	Chip enable (active 'high'). When 'low', switches OFF all power MOSFETs of three half-bridges.
VREF	Analog input	Current controller reference voltage.
BRAKE	Logic input	Brake input pin. When 'low, switches ON all high-side power MOSFETs implementing the brake function.
OUT1	Power output	Output phase 1.
OUT2	Power output	Output phase 2.
OUT3	Power output	Output phase 3.

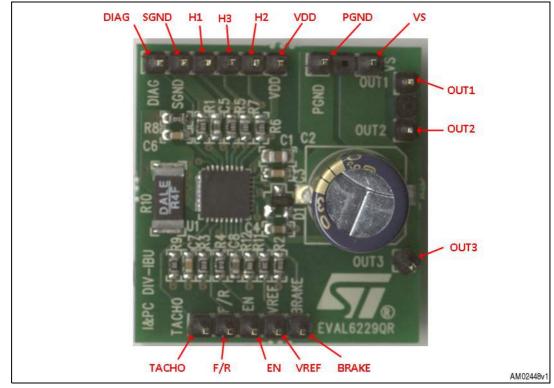


Figure 2. EVAL6229QR demonstration board pin locations

The decoding logic integrated in the device is a combinatory logic which provides the appropriate driving signals for the three-phase bridge outputs, based on the signals coming from the three hall sensors H1, H2 and H3. The hall sensors detect rotor position in a 3-phase BLDC motor.

The EN pin connected to the diagnostic output DIAG is used to implement the overcurrent and thermal protection.

To perform PWM current control, an analog reference voltage should be provided at the VREF pin. A fixed reference voltage can be easily obtained through a resistor divider from an external voltage rail and GND (possibly that which supplies the microcontroller or the rest of the application). Alternatively, a very simple way of obtaining a variable voltage without using a DAC is to low-pass filter the PWM output of a microcontroller.

Table 2 summarizes the electrical specifications of the application, *Figure 3* shows the electrical schematic, and *Table 3* provides the component list.

Table 2. EVAL6229QR: electrical specifications (recommended values)

Parameter	Value	Unit
Supply voltage range (VS)	8 to 52	Vdc
RMS output current rating (OUTx)	up to 1.4	Α
Switching frequency	up to 100	kHz
Voltage reference range (VREF)	0 to +5	٧
Input and enable voltage range	0 to +5	V
Operating temperature range	-25 to +125	°C
L6229Q thermal resistance junction-to-ambient	42	°C/W

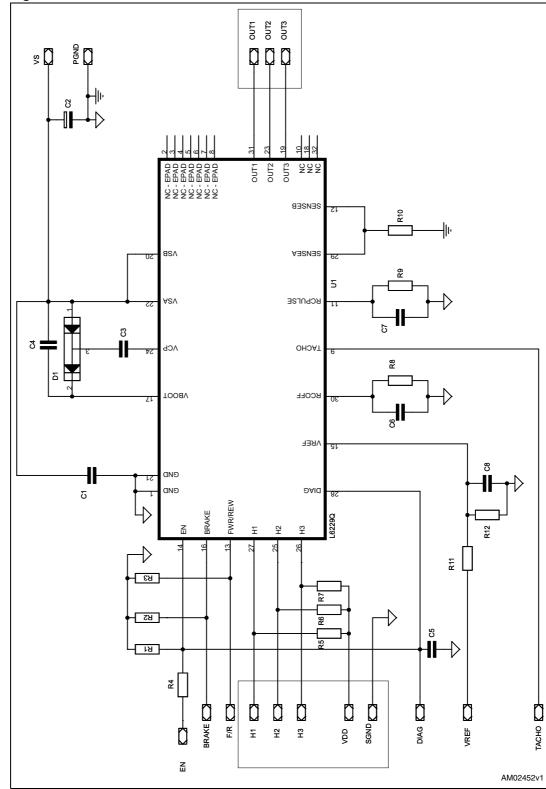


Figure 3. EVAL6229QR demonstration board schematic

Part reference	Part value	Part description	
C1	220nF/100V	Capacitor	
C2	100μF/63V	Capacitor	
C3	10nF/25V	Capacitor	
C4, C8	220nF/25V	Capacitor	
C5	5.6nF	Capacitor	
C6	820pF	Capacitor	
C7	10nF	Resistor	
D1	BAT46SW	Diodes	
R1, R2, R3, R4	100kΩ 5% 0.25W	Resistor	
R5, R6, R7	10kΩ 5% 0.25W	Resistor	
R8	100kΩ 1% 0.25W	Resistor	
R9	20kΩ 1% 0.25W	Resistor	
R10	0.4Ω 1W	Resistor	
R11	20kΩ 5% 0.25W	Resistor	
R12	2kΩ 5% 0.25W	Resistor	
U1	L6229Q	3-phase BLDC motor driver in VFQFPN5x5	

Table 3. EVAL6229QR component list

The input lines EN, BRAKE and F/R are connected to ground through a pull-down resistor which sets the default logic level to "low". An external signal can be applied to change each input status. The Hall effect inputs H1, H2 and H3 have a pull-up resistor connected to the V_{DD} voltage, which can be provided by the VDD pin.

A charge pump circuit, made up of D1, C3 and C4, generates the supply voltage for the high-side integrated MOSFETs. Due to voltage and current switching at relatively high frequency, these components are connected through short paths in order to minimize induced noise in other circuits.

R4 and C5 are used by the integrated overcurrent protection circuitry to set the protection timings (disable time $t_{DISABLE}$ is about 200 µs and delay time t_{DELAY} is about 1 µs, based on the values in *Table 3*).

R8 and C6 are used to set the off-time t_{OFF} of the PWM to about 50 μ s. When changing the RC network value, the off-time should be adjusted according to the electrical characteristics and supply voltage of the motor.

R11, R12 and C8 are low-pass filters to provide an external reference voltage through the PWM output of a microcontroller.

R9 and C7 are used to set the off-time t_{PULSE} of the TACHO pin. The TACHO output signal can be used to implement a simple frequency-to-voltage converter (speed loop control).

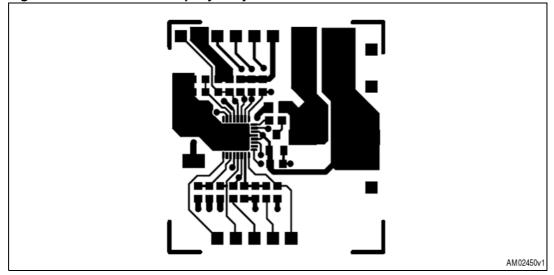
Figure 4, *Figure 5* and *Figure 6* show the component placement and the two-layer layout of the EVAL6229QR demonstration board. A GND area is used for the IC power dissipation.

32 mm

TACHO | 180 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100

Figure 4. EVAL6229QR component placement





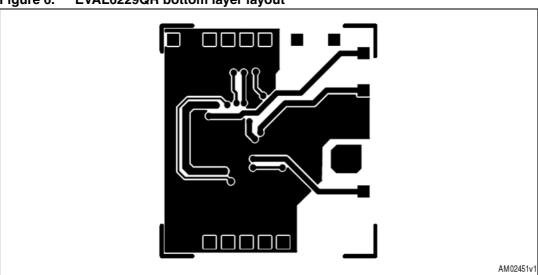


Figure 6. EVAL6229QR bottom layer layout

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AN3134 Revision history

2 Revision history

Table 4. Document revision history

Date	Revision	Changes
13-Apr-2010	1	Initial release.

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10/10 Doc ID 16960 Rev 1

