

High performance 2A ULDO linear regulator with Soft Start

Features

- 2 V to 14 V input voltage range
- 200 mΩ $r_{DS(on)}$ max
- 200 μA quiescent current at any load
- Excellent load and line regulation
- Adjustable from 1.2 V to 5 V
- 1 % voltage regulation accuracy
- Power Good output
- MLCC capacitors filter supported
- Adjustable Soft Start
- Short circuit protection
- Thermal shut down
- HSOP8 package



Description

The L6933H1.2 ultra low drop output linear regulator operates from 2 V to 14 V and is able to support output current up to 2 A. Designed with an internal 50 mΩ N-channel MOSFET, it can be used for on board DC-DC conversions saving in real estate, list of components, low noise generation and power dissipation. L6933H1.2 is available as adjustable version from 1.2 V to 5 V with a voltage regulation accuracy of 1 %.

A Soft Start function allows the device to smoothly increase the Output Voltage at the start-up, avoiding overshoot. Inhibit function is provided. The upper current limit is fixed at 2.5 A to control the current in short circuit condition within $\pm 8\%$. The current is sensed in the power MOS in order to limit the power dissipation.

The device is also provided with a thermal shut down that limits the internal temperature at 150 °C with a histeresys of 20 °C.

Applications

- Motherboards, mobile PC
- Hand-held instruments
- PCMCIA Cards
- Processors I/O
- Chipset and RAM supply

Figure 1. Typical operating circuit

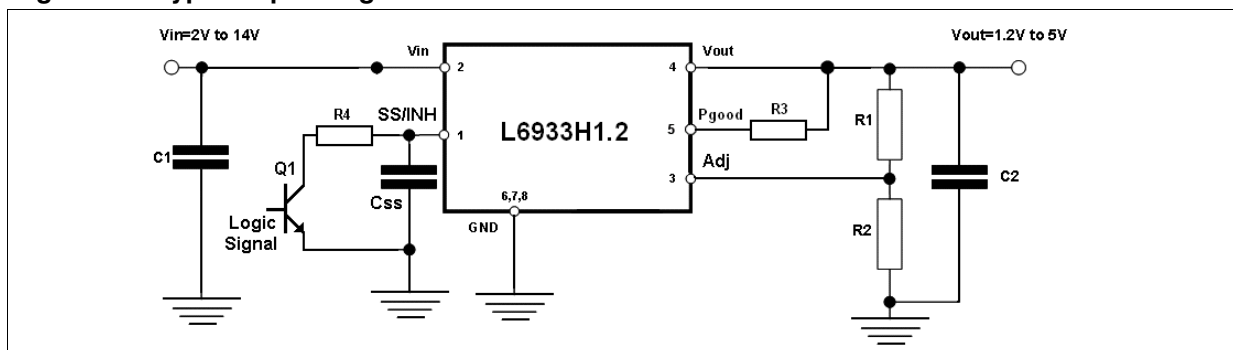


Table 1. Device summary

Order codes	Package	Packaging
L6933H1.2	HSOP8	Tube
L6933H1.2TR	HSOP8	Tape and reel

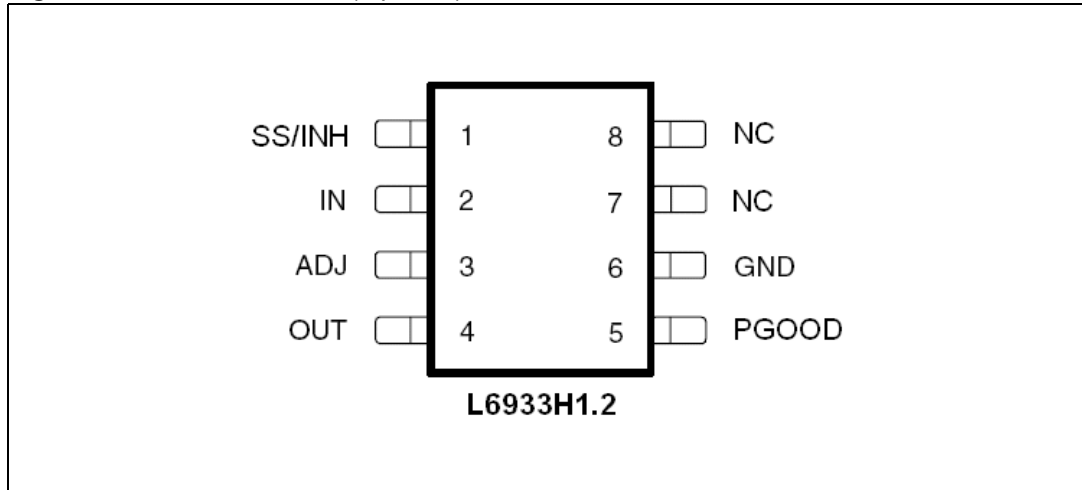
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1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 2. Pin description

Pin N°	Name	Description
SS/INH	1	The soft-start time is programmed connecting an external capacitor from this pin and GND. The internal current generator forces a current of 5 μ A through the capacitor. In steady state regulation, the voltage at this pin will be about 8 V. This pin is also used to inhibit the device: when the voltage at this pin is lower than the 0.5 V, the device is disabled.
VIN	2	Supply voltage. This pin is connected to the drain of the internal N-mos. Connect this pin to a capacitor larger than 10 μ F.
ADJ	3	Connecting this pin to a voltage divider it is possible to program the output voltage between 1.2 V and 5 V.
VOUT	4	Regulated output voltage. This pin is connected to the source of the internal N-mos. Connect this pin to a capacitor of 10 μ F.
PGOOD	5	Power good output. The pin is open drain and detects the output voltage. It is forced low if the output voltage is lower than 90 % the programmed voltage.
NC	7, 8	Not connected
GND	6	Ground pins internally connected

2 Maximum ratings

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	V_{IN} and PGood	14.5	V
	SS/INH, OUT and ADJ	-0.3 to ($V_{in} + 0.3$)	V

2.2 Thermal data

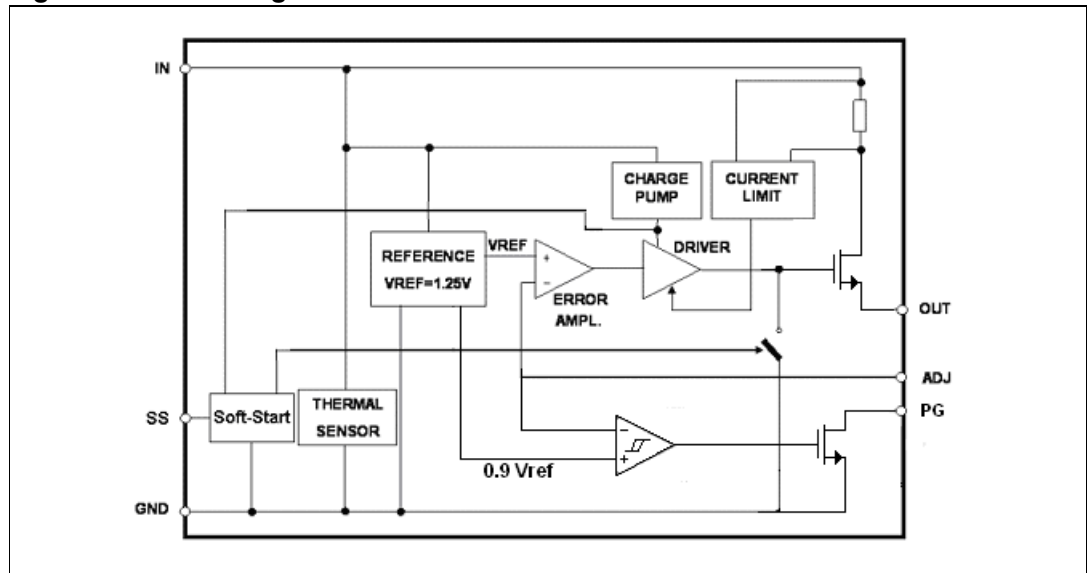
Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	34 ⁽¹⁾	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. Package mounted on board

3 Block diagram

Figure 3. Block diagram



4 Electrical characteristics

Table 5. Electrical characteristics ($T_J = 25\text{ °C}$, $V_{IN} = 5\text{ V}$ unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{IN}	Operating supply voltage		2		14	V
V_O	Output voltage	$I_O = 0.1\text{ A}$; $V_{IN} = 3.3\text{ V}$	1.188	1.2	1.212	V
	Line regulation	$V_{IN} = 2.5\text{ V} \pm 10\%$; $I_O = 10\text{ mA}$			5	mV
		$V_{IN} = 3.3\text{ V} \pm 10\%$; $I_O = 10\text{ mA}$			5	mV
		$V_{IN} = 5\text{ V} \pm 10\%$; $I_O = 10\text{ mA}$			5	mV
	Load regulation	$V_{IN} = 3.3\text{ V}$; $0.1\text{ A} < I_O < 2\text{ A}$			15	mV
$r_{DS(on)}$	Drain source ON resistance				200	m Ω
I_{OCC}	Current limiting		2.3	2.5	2.7	A
I_q	Quiescent current			0.2	0.4	mA
	Ripple rejection	$f = 120\text{ Hz}$, $I_O = 1\text{ A}$, $V_{IN} = 5\text{ V}$, $\Delta V_{IN} = 2\text{ V}_{pp}$	60	75		dB
V_{INH}	INHIBIT input threshold			0.5		V
I_{SS}	Soft start current	$V_{SS} = 0\text{ V}$		-5		μA
P_{GOOD}	P_{GOOD} threshold	V_O rise		90		% V_O
	P_{GOOD} hysteresis			10		% V_O
	P_{GOOD} saturation	$I_{P_{GOOD}} = 1\text{ mA}$		0.2	0.4	V

1. Specification referred to T from -25 °C to 125 °C .

5 Typical electrical performance

Figure 4. Output voltage vs junction temperature

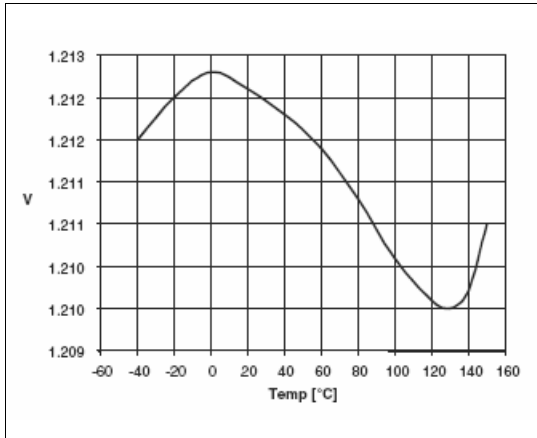
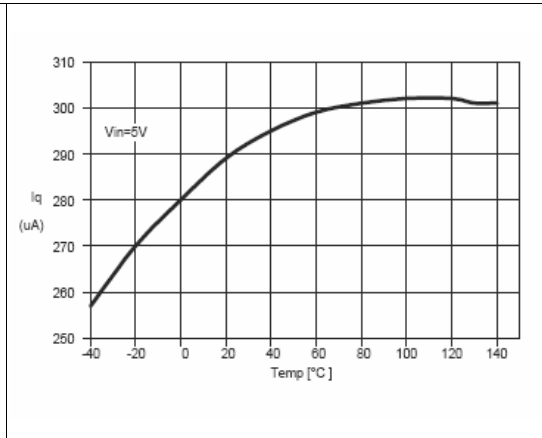


Figure 5. Quiescent current vs junction temperature



6 Soft-Start

When V_{in} is above the turn-on threshold, the device implements the Soft-Start phase: a $5 \mu A$ current is sourced from the SS pin charging the external capacitor. The voltage across SS capacitor increases until it reaches about 8 V.

The output voltage is in regulation when the SS voltage exceeds $V_{OUT} + 1 V$. The SS time results:

$$T_{SS} = \frac{C_{SS} \cdot (V_{OUT} + 1)}{I_{SS}}$$

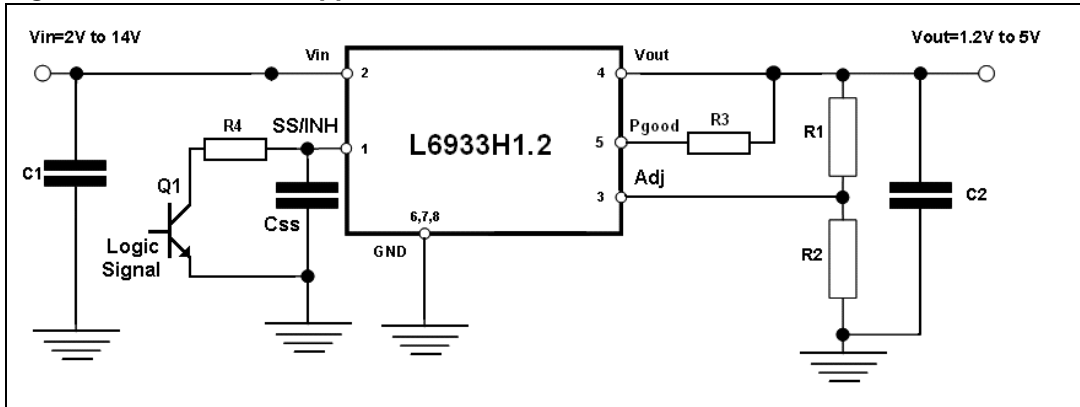
If V_{IN} is below the turn-on threshold, the SS pin is kept shorted to GND.

The SS pin can also be used as ENABLE by shorting the pin to GND through an external switch: when the voltage at this pin is lower than 0.5 V, the device is disabled.

7 Application information

7.1 Application circuit

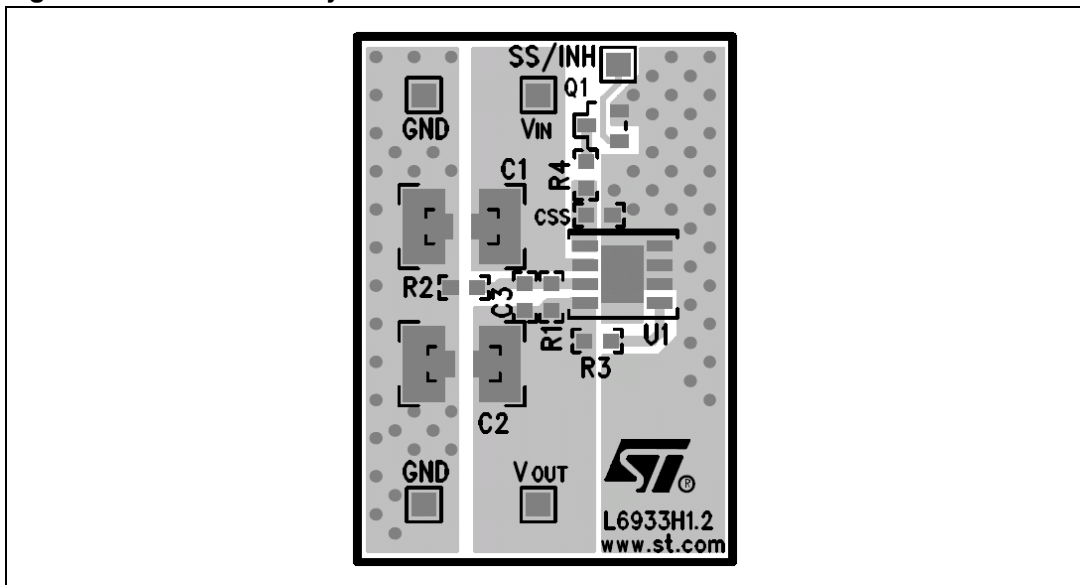
Figure 6. Demoboard application circuit



$$V_{OUT} = \frac{1.2}{R_2} \times (R_1 + R_2)$$

7.2 Demoboard layout

Figure 7. Demoboard layout



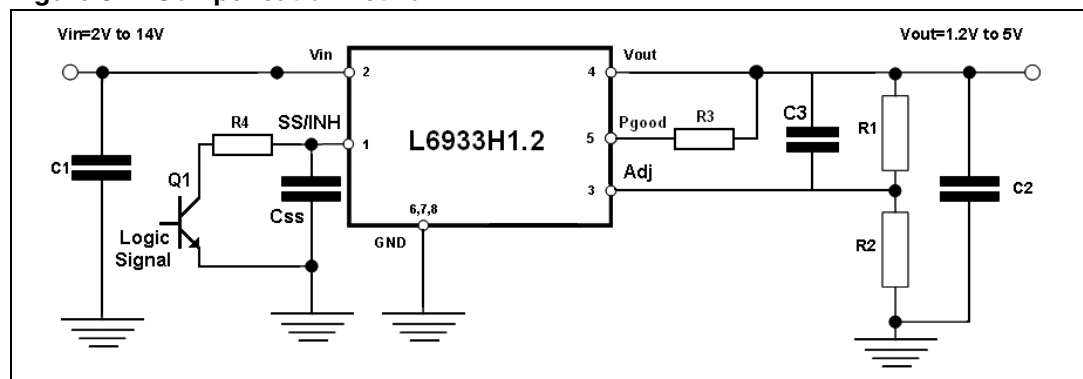
Note: SS/INH drives directly the NPN base; its current need to be properly limited.

7.3 Component part list

Table 6. Component part list *Figure 8*

Reference	Part number	Description	Manufacturer
C1	GRM32ER61C226ME20	22 μ f, 16 V	Murata
C2	GRM32ER61A106KA01	10 μ f, 10 V	Murata
C3		N.M.	
C _{SS}		10 nF, 16 V	
R1		0 Ω	
R2		N.M.	
R3		100 K Ω	
Q1		General purpose signal NPN	
R4		1 K Ω	

Figure 8. Compensation network



8 Components selection

8.1 Input capacitor

The input capacitor value depends on a lot of factors such as load transient requirements, input source (battery or DC/DC converter) and its distance from the input cap. Usually a 47 μF is enough for any application but a much lower value can be sufficient in many cases.

8.2 Output capacitor

The output capacitor choice depends basically on the load transient requirements. Tantalum, Special Polymer, POSCAP and aluminum capacitors are good and offer very low ESR values. Multilayer ceramic caps have the lowest ESR and can be used for particular applications without affecting the loop stability.

Below a list of some suggested capacitor manufacturers

Table 7. Suggested capacitor

Manufacturer	Type	Cap value (μF)	Rated voltage (V)
Murata	Ceramic	1 to 47	4 to 16
Panasonic	Ceramic	1 to 47	4 to 16
Tayo Yuden	Ceramic	1 to 47	4 to 16
TDK	Ceramic	1 to 47	4 to 16
Token	Ceramic	1 to 47	4 to 16
SANYO	Poscap	1 to 47	4 to 16
Panasonic	SP	1 to 47	4 to 16
Kemet	Tantalum	1 to 47	4 to 16

9 Package mechanical data

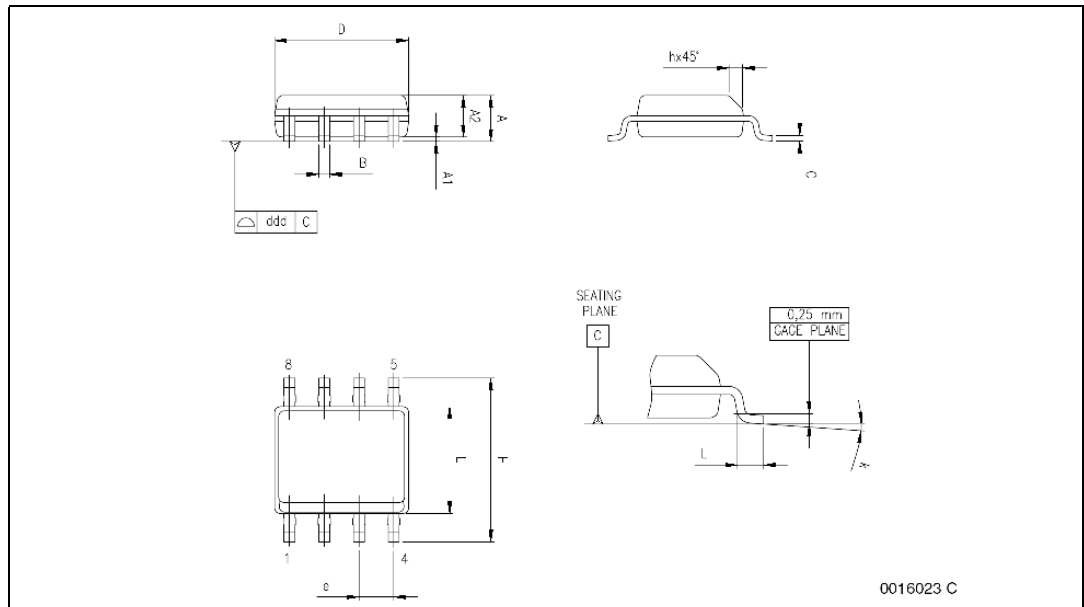
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D ⁽¹⁾	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 9. Package dimensions



10 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Mar-2006	1	First release
16-Jul-2007	2	Section 8: Components selection on page 9 updated
22-Nov-2007	3	Updated cover page.

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